

# Vending Machine Using Verilog (FPGA)

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**Abstract—** The design and implementation of a vending machine system using Verilog HDL on an FPGA board. The vending machine is equipped with multiple states including product selection, amount selection, dispensing, out-of-stock detection, refund processing, change calculation, and system reset. The project aims to demonstrate the integration of hardware description language (Verilog) with FPGA technology to create a functional vending machine prototype.

The design process involved the decomposition of the vending machine's functionality into smaller modules, each responsible for a specific task. These modules were then integrated to form the complete system. The Finite State Machine (FSM) methodology was employed to model the different states and transitions within the vending machine, ensuring sequential operation and proper functionality.

**Keywords:** Nexys A7, Product selection, Stock out, Xilinx ISE, Vivado, etc.

## I. INTRODUCTION

Based on the complaints that customers have and the vending machines out there, we decide to design a vending machine that satisfy customer's needs. Some vending machines require customers to pay in the exact amount and do not give change. To overcome this issue, we design a change dispenser that will dispense change for customers once they have bought the product. To achieve our goal, we designed a state diagram with a few 7 states, so that the vending machine will work properly, and we understand the flow of the vending machine. The vending machine is also limited to 5 products only and it will only accept: Rs1, Rs2, and Rs5. The seven-segment display is used to display the price of each item and the refund/change from his session. The vending machine algorithm was designed in Vivado, but it was simulated using Xilinx ISE Simulator. To verify whether the vending machine works properly, we ran a testbench to see whether specific inputs will result in expected outputs. Our main goal from this project is to build a vending machine that overcomes people's complaints on other vending machines.

## II. LITERATURE REVIEW

The proposed paper aligns with previous research emphasizing the use of FSM methodology and Verilog HDL for designing vending machines, ensuring efficient state management and system functionality. Studies have highlighted the significance of synthesis and implementation tools like Genus and Encounter for optimizing design

performance and meeting stringent timing and area constraints. Validation through simulation and FPGA implementation has been a common practice to verify design correctness and real-world applicability. Results from previous works have consistently demonstrated the effectiveness of FSM-based vending machine designs in providing reliable and efficient solutions for user transactions. This paper contributes to the existing body of literature by presenting a comprehensive approach to vending machine design and implementation, showcasing its feasibility and effectiveness in meeting specified requirements and performance metrics [1].

The evolution of vending machines from dispensing basic food and beverage items to offering specialized products and services, as well as the emergence of automated retail kiosks, has been well-documented. This shift towards automation and specialization has been particularly pronounced in regions like Japan, where vending machines are ubiquitous and diverse in their offerings. Similar to the transition from traditional mobile phones to smartphones, vending machines have gradually adopted smart technologies, leveraging features such as digital touch displays, internet connectivity, and advanced payment systems. The integration of sensors and cameras in smart vending machines enables data collection on customer behavior and preferences, facilitating targeted marketing and improved customer engagement. Market research indicates a growing trend towards the adoption of smart vending machines globally, driven by advancements in technology and increasing consumer demand for convenience and personalized experiences [2].

The central idea of this work is to design a vending machine that will be able to provide several items like soft drink, cake & cooldrinks to people. The machine will also deliver the change, depending on the amount of money inserted and the price of product. At the same time, we have made efforts to make the design of the Vending Machine power efficient by using power reduction techniques. In this process we have tested our design at different frequencies and analyzed the consumed power. Next, we have also calculated the power at different frequencies with different IO STANDARD like LVCMOS33, LVCMOS12, SSTL18\_I, HSTL\_I\_18. The proposed design is tested and implemented using VERILOG HDL and XILINX ISE 14.2 targeting XC3S500E FPGA. The result shows optimization of power [3].

This paper contributes to the existing literature on FPGA-based vending machine design and implementation, leveraging Verilog HDL and simulation tools like VIVADO HLS 2019.1 for verification. Previous studies have demonstrated the effectiveness of FPGA platforms such as the Zed board xc7z020clg484-1 for prototyping and testing embedded systems designs, including vending machines. Simulation results presented in this paper validate the functionality of the vending machine design under various scenarios, including sufficient and insufficient funds, and out-of-stock situations, which align with common user interactions. Additionally, synthesis results, including the utilization of logical units (LUTs) and I/O ports, provide insights into the resource requirements and efficiency of the design. By showcasing the simulation and synthesis results, this paper contributes valuable information for researchers and practitioners interested in FPGA-based vending machine development, highlighting the feasibility and performance of the proposed design [4].

The adoption of automated vending machines has surged in response to evolving lifestyles, offering a convenient means of accessing various products ranging from beverages to valuable items like gold. Traditional vending machine technologies, such as CMOS, SED, Microprocessors, and Microcontrollers, have limitations in terms of power efficiency and speed. In contrast, FPGA-based vending machines offer programmability, flexibility, and improved performance in terms of speed, response time, and power consumption. FPGA-based designs enable reprogramming without necessitating architectural changes, facilitating easier upgrades and adaptations [5].

### III. HARDWARE ARCHITECTURE

The Nexys A7, engineered by Digilent, is a dynamic FPGA development board boasting a rich hardware architecture conducive to a myriad of digital design projects. Central to its architecture lies the Xilinx Artix-7 FPGA, furnishing a bedrock of programmable logic resources. These resources encompass a spectrum of elements including programmable logic cells, configurable I/O blocks, Block RAM, DSP slices, and more, affording users unparalleled flexibility in crafting diverse digital circuits and systems. Complementing this FPGA core is DDR3 memory, furnishing ample storage for program code and data. The board also

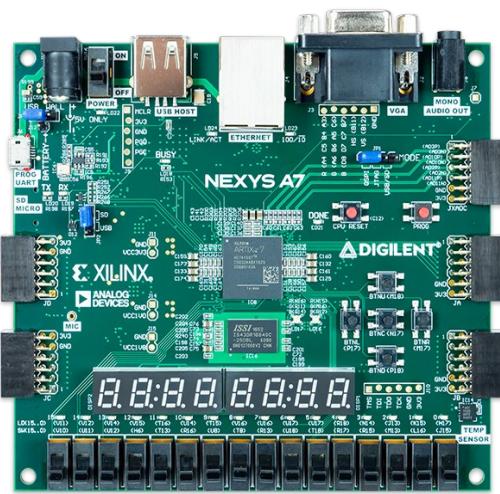


Fig. 1 NEXYS A7 EPGA

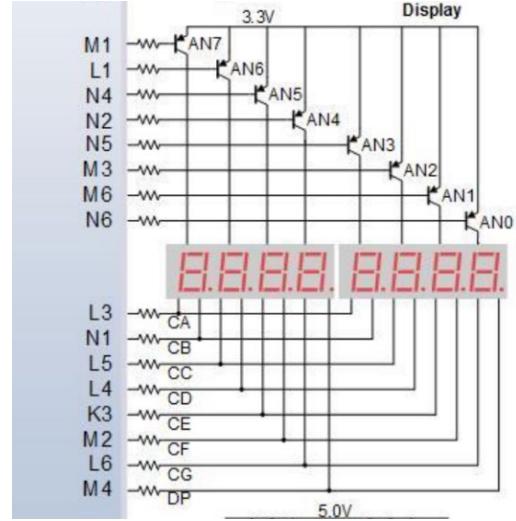


Fig. 2. Seven Seg Interfacing with Fpga

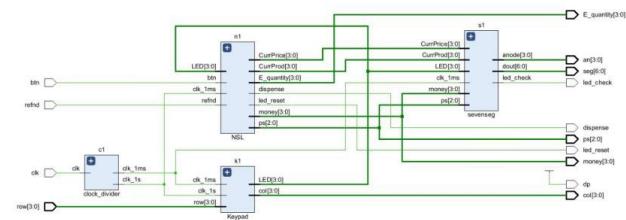


Fig. 3. RTL Schematic

brims with input/output interfaces ranging from tactile switches, push buttons, and LEDs to seven-segment displays, VGA and HDMI ports, an audio codec, USB-UART interface, and PMOD connectors. These interfaces facilitate user interaction and external device interfacing, enriching the board's versatility. Clocking resources, such as oscillators and clock input ports, ensure synchronous operation, while a robust power supply, with integrated voltage regulators, sustains the board's operations. Configuration is streamlined through a USB interface leveraging Digilent's USB-JTAG circuitry, empowering users to seamlessly program the FPGA with their designs. In sum, the Nexys A7's hardware architecture embodies a comprehensive ecosystem, empowering developers to explore and realize a spectrum of digital design aspirations.

#### IV. METHODOLOGY

If the selected item is still in stock, the vending machine will display the remaining amount of money required. However, if the item is out of stock, it will enter the "No Stock" state. Upon inserting sufficient money, the item will be dispensed, and change will be returned if necessary. If the inserted money exceeds the required amount, change will be given accordingly, but no change will be provided if the exact amount is inserted. A "Refund" option is available for customers who wish to cancel their purchase after inserting money. This ensures they can retrieve their funds if the required amount has not been reached. After dispensing an item, the vending machine must be reset before another purchase can be made.

To prevent incorrect input readings from the keypad, a clock divider is implemented. This ensures inputs are read at regular intervals, with the divider set to read inputs every half-second. This prevents issues with fast inputs or button presses, as the FPGA's native clock operates at 100 MHz, resulting in extremely short intervals between readings that could lead to inaccuracies.

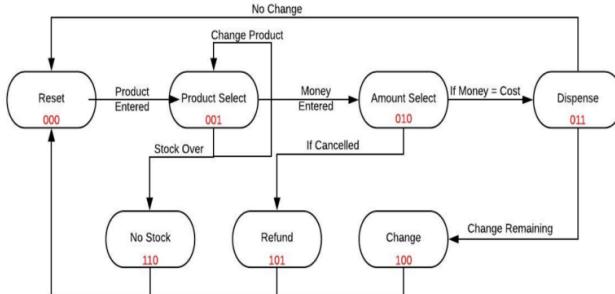


Fig. 4. Vending Machine State Diagram

### States:

1. Reset State
2. Product Selection State
3. Money Amount State
4. Dispense Item State
5. Change State
6. Refund State
7. Stock State

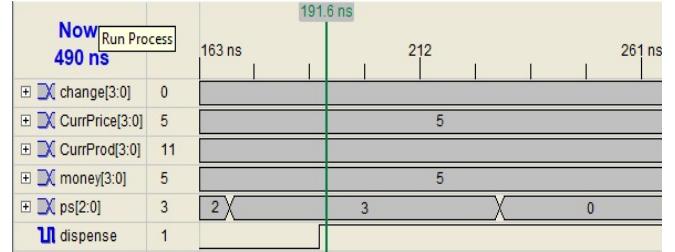
In the state diagram, State 2 presents three potential outcomes. The transition from State 2 to State 7 is automatic only if the item is unavailable; otherwise, State 2 will transition to either State 3 or remain in State 2. Similarly, in State 4, the transition to State 5 occurs solely if the inserted money exceeds the required amount; otherwise, pressing the reset button is necessary to return to the initial state. Notably, State 6 can only be reached from State 3, reflecting its nature as the refund state, activated when customers insert money. To return States 5, 6, and 7 to the reset state, pressing the reset button is required.

### V. RESULT AND DISCUSSION

#### Output Waveforms:



**Case 1:** First transition from state 0 to state 1 (selection of product)



**Case 2:** As the Ps count goes to 001 the product dispenses at next rising edge of the clock after the transition. As money matches the current price of selected product the product dispenses at its next rising edge.



**Case 3:** Dispensing product as money meets current price and dispense change. In the above waveform, the current price of product is 5rs and the money inserted is 9rs after detecting 9rd the machine will dispense the item and dispense the change of 4rs, which is visible in the change section of waveform.

#### Hardware Implementation:

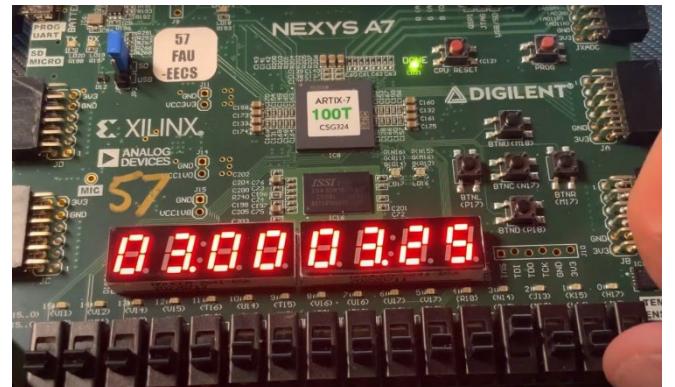


Fig. 5. Left amount is of the product and Right amount shows the money customer has inserted.

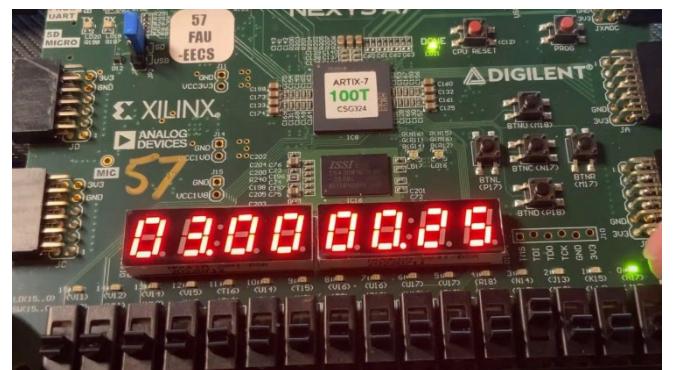


Fig. 6. Right amounts shows the Change that should be given to the customer.

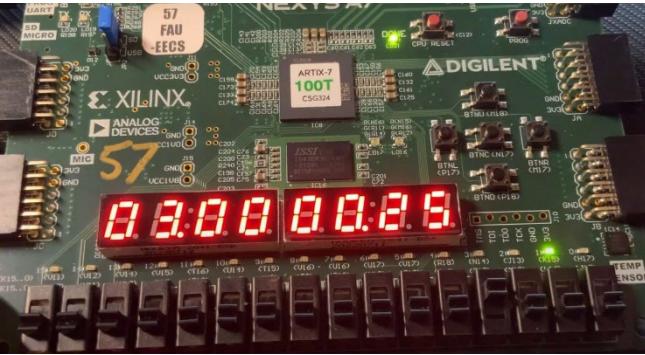


Fig. 7. The green light in right down corner indicates that this transaction is failed due to insufficient amount of money.

## VI. CONCLUSION

During the project, we employed a state machine approach to develop a vending machine. We encountered several challenges, including managing input speeds in relation to the clock speed and connecting the keypad to the FPGA. However, the primary hurdle we faced was mitigating bouncing input. Instead of implementing a conventional denouncer, we chose to create a distinct clock divider for the input. Despite these obstacles, we successfully completed the project, delivering a fully operational vending machine. It accurately dispenses change, refunds money, and notifies customers of product availability. Overall, we are satisfied with the project's outcome.

## VII. FUTURE SCOPE

Looking ahead, the vending machine project presents numerous opportunities for future expansion and improvement. One avenue for advancement lies in enhancing the user interface, potentially integrating a touchscreen display to offer intuitive interaction and detailed product information. Additionally, the integration of advanced payment systems, such as contactless payment methods or mobile payment apps, could provide users with more convenient and secure payment options. Improving inventory management through the implementation of automated tracking systems would enable real-time monitoring of product levels, facilitating timely restocking and preventing out-of-stock situations. Furthermore, the project could benefit from the utilization of data analytics to analyze user

preferences and consumption patterns, informing inventory management decisions and marketing strategies. By exploring these and other possibilities, the vending machine project can evolve into a more sophisticated and user-friendly system, delivering enhanced functionality and customer satisfaction.

## REFERENCES

- [1] Fuad, Mahamudul Hassan, Rahbaar Yeassin, KM Mehedi Hassan, Md Mahamudunnobi Sykot, and Md Faysal Nayan. "Design of a Vending Machine Using Verilog HDL and Implementation in Genus & Encounter." European Journal of Electrical Engineering and Computer Science 7, no. 6 (2023): 88-95
- [2] Qureshi, Muhammad Ali, Abdul Aziz, Hafiz Faiz Rasool, Muhammad Ibrahim, Usman Ghani, and Hasnain Abbas. "Design and Implementation of Vending Machine using Verilog HDL." In 2011 2nd International Conference on Networking and Information Technology, IPCSIT, vol. 17. 2011.
- [3] Verma, Gaurav, Ashish Papreja, Sushant Shekhar, Shikhar Maheshwari, and Sukhbani Kaur Virdi. "Low power implementation of FSM based vending machine on FPGA." In 2016 3rd International Conference on Computing for Sustainable Global Development (INDIACOM), pp. 2054-2058. IEEE, 2016.
- [4] Suthar, Mukul. "A novel implementation of FPGA based smart vending machine." In 2021 IEEE International Conference on Technology, Research, and Innovation for Betterment of Society (TRIBES), pp. 1-6. IEEE, 2021.
- [5] Mustafa, Mustafa S., Mohanad H. Nsaif Al-Mayyahi, and Nawaf H. Barnouti. "Design and implementation of vending machine embedded control system using FPGA." In Proceedings of the international conference on information and communication technology, pp. 25-30. 2019.
- [6] Anuradha, P., K. Rajkumar, Ch Navitha, and M. Jithender Reddy. "Implementation of Automatic Vending Machine Using FPGA." In International Conference on Information and Management Engineering, pp. 63-70. Singapore: Springer Nature Singapore, 2022.
- [7] Shivanand, Nayana, Meenakshi L. Rathod, and S. Chetan. "FPGA based Vending Machine For Logical Gates." In 2023 3rd International Conference on Smart Data Intelligence (ICSMDI), pp. 282-293. IEEE, 2023.
- [8] Guo, Junyi, and Yu Liu. "The design and implementation of a vending machine based on state machine, FPGA and microcontroller." In 2021 IEEE International Conference on Electrical Engineering and Mechatronics Technology (ICEEMT), pp. 525-528. IEEE, 2021.
- [9] Zhang, Jialiang. "The Design, Simulation, Verification and Implementation of Vending Machine Based on FPGA." PhD diss., The Ohio State University, 2012.
- [10] Bhonde, Poonam V., and Shweta Thakur. "Review on Design Simulation of Smart Vending Machine Using FPGA." Int. J. Res. Appl. Sci. Eng. Technol. (2018).