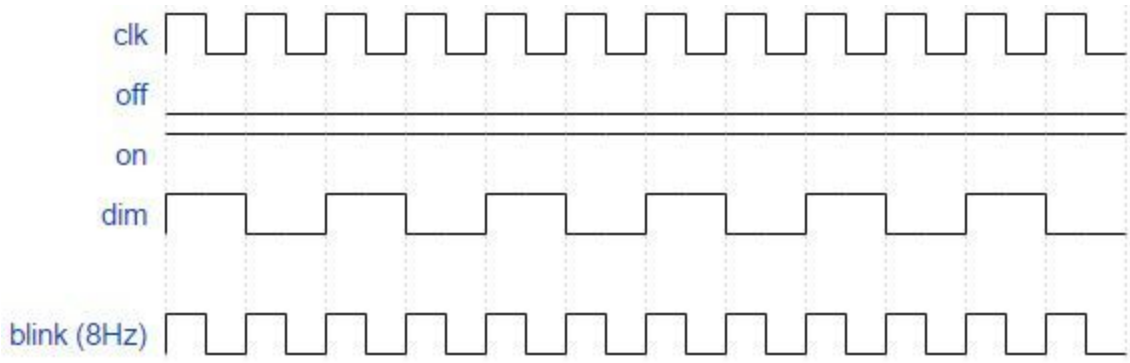
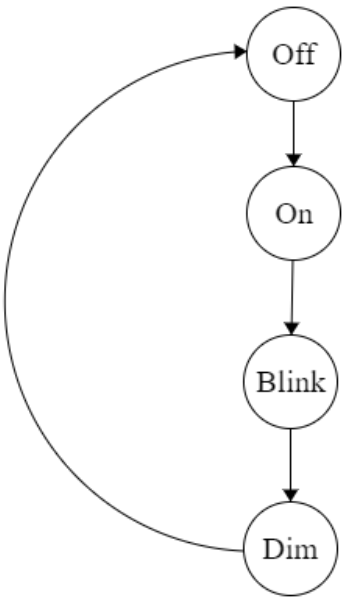
CompArch Midterm: Specification Document

Our product is a bike light designed for use in situations where a variety of lighting patterns are needed for visibility. As such, it needs to be simple to operate and with a limited subset of features. This system will have one input, a single button, and one output, the single LED that is visible on the front of the device. The device has four modes. The first mode, off, is where the LED is simply off. On, where the device is at full power and the LED is at full brightness. Blinking, where the device is blinking with a 8Hz frequency between a full power and no power state. Lastly, there is Dim, where the device will be powered on a 50% duty cycle. These states are cycled through by the button press. A single press transitions between these four states, starting at Off, then On, then Blinking, and ending with Dim, before returning to Off. Note that in the following wave diagram, that the blink train is clocked at 8Hz instead of at the normal clock's speed.



Here is the Finite State Machine diagram which represents the movements between the states. Keep in mind that each arrow represents a single button press by the system.



Subcomponent Descriptions:

1) 16 Step Up Counter

This structure is constructed out of Postive Edge Triggered D-Flip Flops with their ~Q outputs connected to their D inputs. This construction causes the D-Flip Flop to swap its outputs every time a positive edge signal is detected on the clock. This effectively cuts the frequency of the input signal in half. By chaining 16 of these together, the system counts from 0 to 2^{15} - 1, effectively counting through every number in one second due to the speed of the clock. This gives us the ability to select from that output any single bit wire to get a clock speed equal to 2^{15} / $2^{\text{wire index}}$. This is used in our main schematic in a few places, one to get an 8Hz signal for the blinking, one to get a 50% duty signal for the dim mode, and once in the input conditioner to reduce the size requirements and to achieve the required 1ms debouncing.

Inputs: A 1-bit trigger cycle to increase the count

Outputs: A 16 bit wide wire which contains the current count of the system, ranging from 0 to 2^{15} - 1 and looping back to 0.

Size: 208 GIE

2) Input Conditioner

Following on the construction from Lab 2, this input conditioner is reduced in size due to only needing the positive edge signal for our circuit. Clocked on any signal, the system will wait 2 cycles for the signal to propagate through the two D flip flops, and compares the raw input and the two flip flop outputs to each other to establish if all of

those signals are the same. That result is piped into a D flip flop with an enable, where D is set equal to the output of the last of the D flip flops used to check for signal consistency. We then compare the previous output (Q, which lags one clock signal behind) to the currently desired output (That above D) to see if we should output a positive edge (When Q = 0 and D = 1). That is fed into another D flip flop which will output a positive edge if that signal is 1 and the flip flop is not already set to 1.

Inputs: A noisy input signal and a clock signal.

Outputs: A positive edge signal and a conditioned output (Conditioned output omitted from final schematic due to it not being used)

Size: 72 GIE

3) Final system schematic

Using a 32768 Hz clock, we pipe that signal in as the trigger into our 16 state up counter, getting a series of clock signals ranging from 32768 Hz to 1Hz as described above. Using the 1024Hz signal (from our up counter, the bit at index 5), the input from the button and that clock are put into the Input conditioner to debounce errors that our specifications define as maxing out at 1 ms. That positive edge is then piped into a 4 stage Ring Counter which outputs a one hot signal of width 4, representing our Finite State Machine. Bit 0 represents off, which remains unwired. Bit 1 represents 1, which is ANDed with an input tied high at 1. Bit 2 represents Blink, which is ANDed with a 8Hz signal from our 16 state counter (at index 12). Bit 3 represents Dim, which is ANDed with the 16384Hz signal which will cause 50% duty (at index 1). These three signals are

ORed together and the result is used to drive the LED Driver circuit. The LED Driver, 4 stage Ring Counter, and clock are all defined in the lab handout.

Inputs: The button’s signal

Outputs: The LED’s lighted state

Size: 378 GIE