# Serial Artihmetic Processor

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#### Abstract

Serial arithmetic processors are a type of processor that performs operations on data one bit at a time, rather than processing multiple bits simultaneously like parallel processors. In this particular project, the design that is being constructed has specifications that would allow the user to perform a set of operations on a 4-bit operation code — OpCode. The design consits of three main modules; a data path, state generator, and a control circuit. These three modules will work in conjunction to output a 4-bit result.

#### 1 State Transition Table

The following is the truth table that will be used to construct the counter. Notice that since the counter follows an atypical counting method — Fibonacci sequence — we inleude DC (Don't cares) into our truth tables denoted by the symbol x.

Table 1: Truth table with inputs  $Q_3, Q_2, Q_1, Q_0$ , and outputs  $Q_3^+ Q_2^+ Q_1^+ Q_0^+$  representing the "next states" of the 4-digit inputs. Note that the PS stands for "Present States".

OpCode[3:0]	$MUX_{OUT}$	$x_i$	$y_i$	$c_0$	Instruction
0 0 0 0					
$0\ 0\ 0\ 1$					
0 0 1 0	$c_0$	$A_i$	$B_i$	0	add: $A + B \Rightarrow A$
0 0 1 1					
0 1 0 1					
1010					
1111					

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### **Minimal SOPs**

Lets consider d(c) to be the minterm sum of the Don't Care values mentioned earlier.

$$d(c) = \Sigma m(0, 4, 6, 7, 9, 10, 11, 12, 14, 15) \tag{1}$$

For UP = 1:

$$D_0(Q_3Q_2Q_1Q_0) = \Sigma m(2,3,8,13) + d(c)$$

$$D_1(Q_3Q_2Q_1Q_0) = \Sigma m(1,2) + d(c)$$

$$D_2(Q_3Q_2Q_1Q_0) = \Sigma m(3,8,13) + d(c)$$

$$D_3(Q_3Q_2Q_1Q_0) = \Sigma m(5, 8, 13) + d(c)$$

For 
$$UP = 0$$
:

$$D_0(Q_3Q_2Q_1Q_0) = \Sigma m(1,2,5,8) + d(c)$$

$$D_1(Q_3Q_2Q_1Q_0) = \Sigma m(2,5) + d(c)$$

$$D_2(Q_3Q_2Q_1Q_0) = \Sigma m(8) + d(c)$$

$$D_3(Q_3Q_2Q_1Q_0) = \Sigma m(13) + d(c)$$

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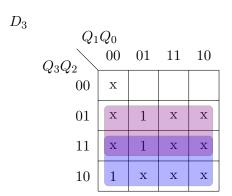
## 2 Function KMAPs

For UP = 1:

$D_0$	$Q_1$	$Q_0$			
	$Q_3Q_2$	00	01	11	10
	00	X		1	1
	01	х		x	x
	11	X	1	X	x
	10	1	Х	x	X

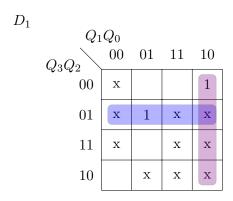
$D_1$							
	$Q_1Q_0$						
	00	00	01	11	10		
	$Q_3Q_2$						
	00	X	1		1		
	01	x		X	x		
	11	x		x	x		
	11	Λ		Λ	Λ		
	10	·	X	x	x		

$D_2$	$Q_1$	$Q_0$			
	$Q_3Q_2$	00	01	11	10
	00	x		1	
	01	х		x	x
	11	X	1	X	x
	10	1	X	X	x



For UP = 0:

$D_0$	$Q_1$	$Q_0$			
	$Q_3Q_2$	00	01	11	10
	00	X	1		1
	01	x	1	x	x
	11	x		x	x
	10	1	X	Х	x



$D_2$	$Q_1$	$Q_0$			
	$Q_3Q_2$	00	01	11	10
	00	x			
	01	x		х	х
	11	X		X	x
	10	1	Х	Х	х

$D_3$	$Q_1$	$Q_0$			
	$Q_3Q_2$	00	01	11	10
	00	x			
	01	х		x	x
	11	X	1	x	X
	10		x	x	х

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