Serial Artihmetic Processor

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Abstract

Serial arithmetic processors are a type of processor that performs operations on data one bit at a time, rather than processing multiple bits simultaneously like parallel processors. In this particular project, the design that is being constructed has specifications that would allow the user to perform a set of operations on a 4-bit operation code — OpCode. The design consits of three main modules; a data path, state generator, and a control circuit. These three modules will work in conjunction to output a 4-bit result.

1 State Transition Table

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Table 1: Truth table with inputs Q_3, Q_2, Q_1, Q_0, and outputs $Q_3^+Q_2^+Q_1^+Q_0^+$ representing the "next states" of the 4-digit inputs. Note that the PS stands for "Present States".

$OpCode[3:0]$	MUX_{OUT}	x_i	y_i	c_0	$Instruction$
0 0 0 0	c_0	A_i	0	1	dec: $A-1 \rightarrow A$
0 0 0 1	c_0	A_i	1	0	inc: $A+1 \rightarrow A$
0 0 1 0	c_0	A_i	B_i	0	add: $A+B \rightarrow A$
0 0 1 1	c_0	A_i	$\overline{B_i}$	1	sub: $A-B \rightarrow A$
0 1 0 1	c_1	A_i	1	0	and: A & $B \rightarrow A$
1 0 1 0	c_2	A_i	B_i	0	comp: $\overline{A} \rightarrow A$
1 1 1 1	c_3	A_i	$\overline{B_i}$	1	or: A — B → A

Stage Generator

Table 2: Truth table with inputs Q_3, Q_2, Q_1, Q_0, and outputs $Q_3^+Q_2^+Q_1^+Q_0^+$ representing the "next states" of the 4-digit inputs. Note that the PS stands for "Present States".

PS	$START$	s1rA s0rA	s1rB s0rB	$CSEL$	CE
T_0	0	0 0	0 0	d	0
T_0	1	1 1	d d	d	d
T_1	d	0 0	1 1	1	1
T_2	d	0 1	0 1	0	1
T_3	d	0 1	0 1	0	1
T_4	d	0 1	0 1	0	1
T_5	1	0 0	0 0	d	0
T_5	0	0 1	0 1	0	1