Lab 1: Power Management

ESE350: Embedded Systems & Microcontroller Laboratory
University of Pennsylvania

In this document, you'll fill out your responses to the questions listed in the Lab 1 Manual. Please fill out your name and link your Github repository below to begin. Be sure that your code on the repo is up-to-date before submission!

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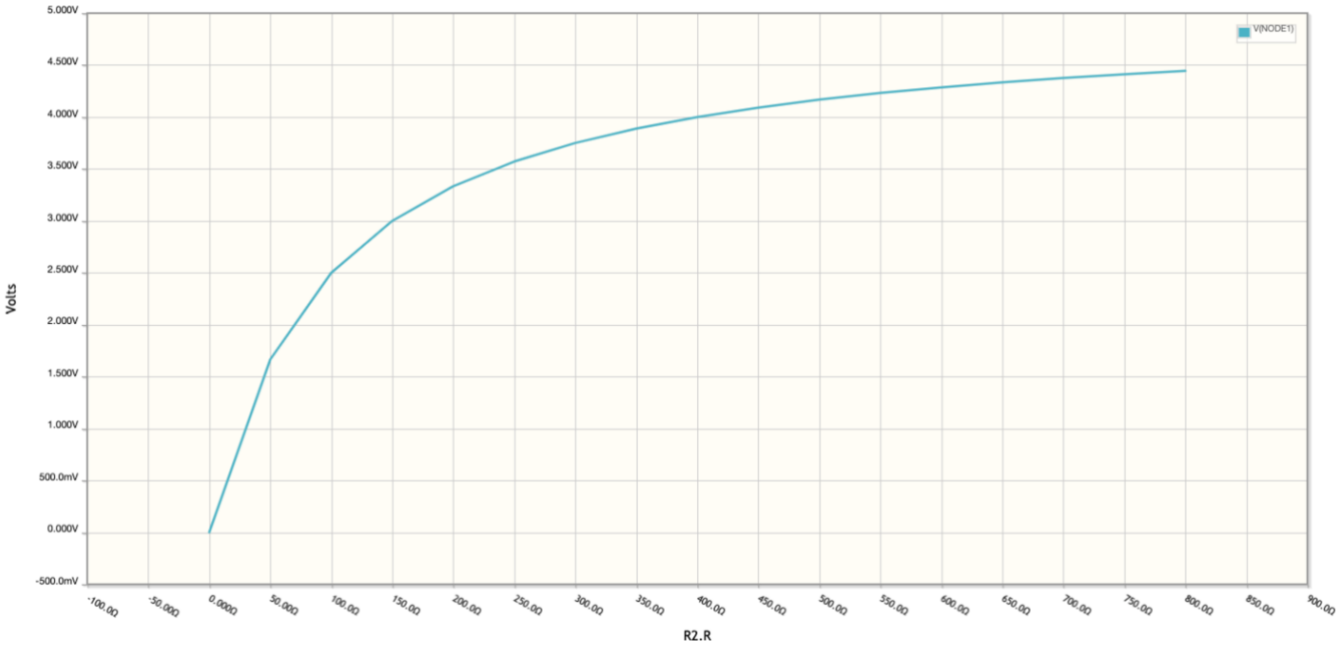
GitHub Repository: **https://github.com/LehnsherrYu/ESE519**

1. 2.5v
   According to Kirchhoff's Law:
   => $-V_1 + I R_1 + I R_2 = 0$
   => $I = \frac{V_1}{R_1+R_2}$
   Thus, the final voltage divider equations are:
   $V_{R1} = IR_1 = \frac{V_1}{R_1+R_2} R_1$
   $V_{R2} = IR_2 = \frac{V_1}{R_1+R_2} R_2$
   Using this equation, the voltage is calculated as
   $V_{Node1} = V_{R2} = \frac{5V}{200\omega} 100\omega = 2.5V$

2. 4.474v
   Using the final voltage divider equation derived in Q1:
   $V_{Node1} = V_{R2} = \frac{5V}{950\omega} 850\omega = 4.474V$

3. The image is as shown below:



Yes, this is the output expected. Because this output is consistent with the formula we have derived in Q1:

$V_{node1} = V_{R2} = IR_2 = \frac{V_1}{R_1+R_2} R_2 = \frac{5V}{100\ \omega+R_2} R_2$

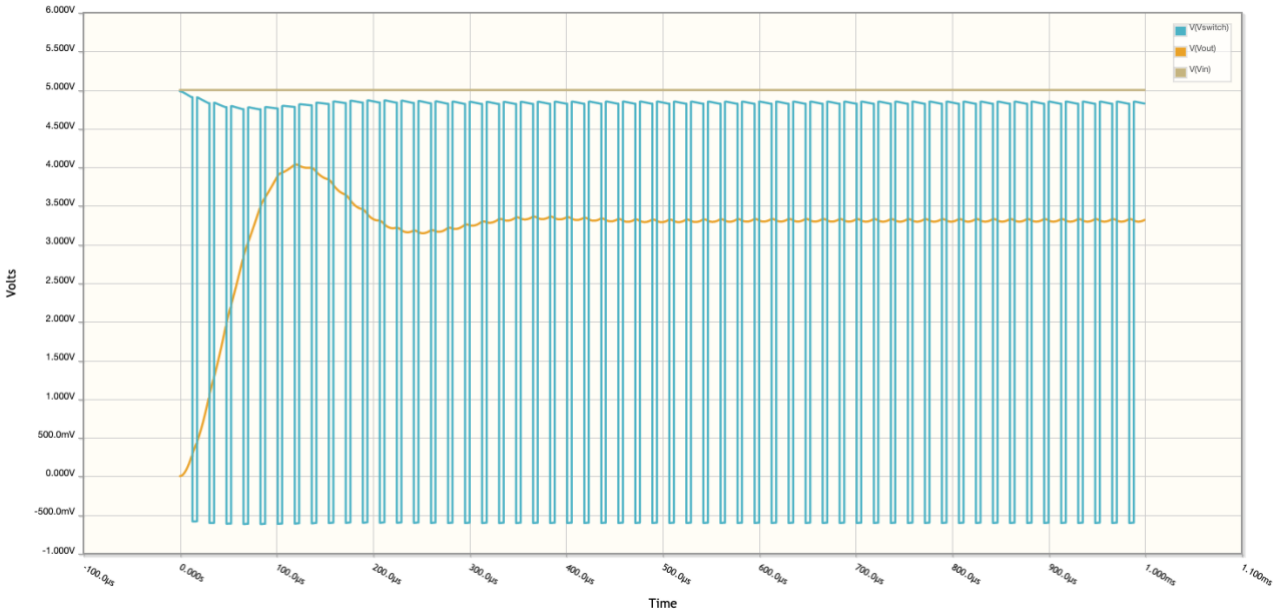
4.

Scenario1: Provide different voltage levels from a common voltage source or as a voltage reference.
Scenario2: Voltage divider can be used to reduce the input voltage. If the supply voltage is higher than what we expect, the voltage divider will be helpful.
Scenario3: The voltage divider can be used to perform the function of a simplified version of potentiometer to measure the resistance of the resistor. According to the voltage divider equation: $V_{R2} = \frac{V_1}{R_1+R_2} R_2$, if we want to measure the resistance of a resistor, we just need one power source and one resistor (the resistance is known), and we connect them in series (Just like Figure 1 in Q1). We need to measure the V_{R2} and use the formula above to calculate the resistance of that unknown resistor.
Scenario4: The circuit of voltage divider is easy to design. If there is an easy-to-design requirement to the circuit, the voltage divider can be used.
Scenario5: Circuit is cheap and simple (Requires only a few resistors).

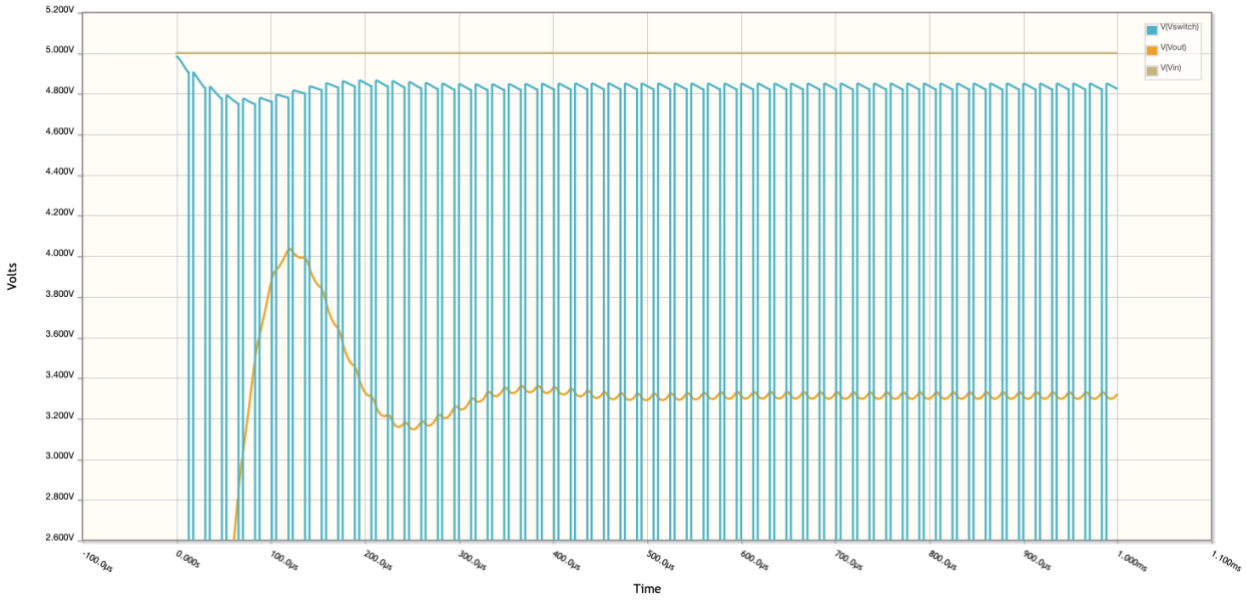
5. The duty cycle setting doesn't represent the absolute value of the time period, instead, it represent the portion of the low(OFF) time in one time period.
   As it's P-FET, according to the simulation result, the duty cycle setting for the "CLK1" part represent the low (OFF) time portion of the pulse. The MOSFET become active when the pulse is low.

6. For V_{out} to be 3.3V, duty cycle = 0.266
   For V_{out} to be 2V, duty cycle = 0.527
   The relationship between V_{out}, V_{in} and D is: $D = \frac{V_{out}}{V_{in}}$. However, as the p-channel FET is used in the lab, the formula becomes: $D = 1 - \frac{V_{out}}{V_{in}}$.
   According to the formula and after calculation: the expected duty cycle should be: (1-3.3/5) = 0.34 for V_{out} to be 3.3V (The actual value is 0.266 which is similar to 0.34).
   According to the formula and after calculation: the expected duty cycle should be: (1-2/5) = 0.6 for V_{out} to be 2V (The actual value is 0.527 which is similar to 0.6).
   In the simulation, there are loss in the switch and diode, thus the real value that has been measured is a little bit different from the one that has been calculated. However, as the experimental data is similar to the calculated data, the values do make sense.

7. The image is as shown below:



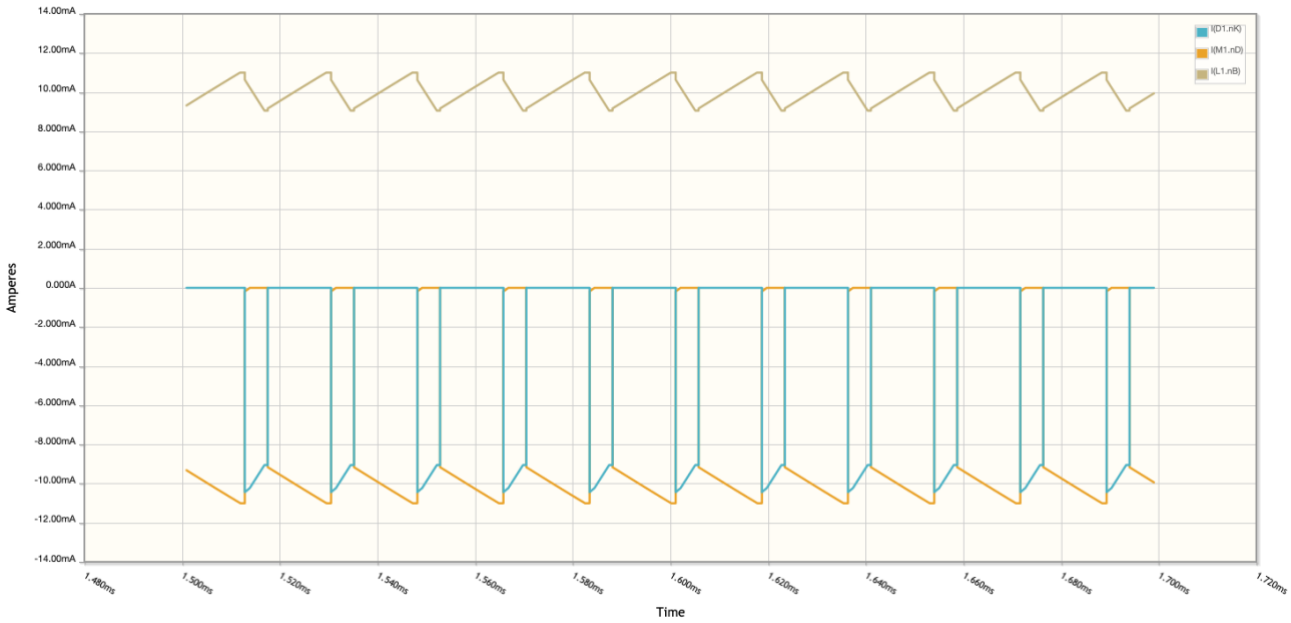
8.



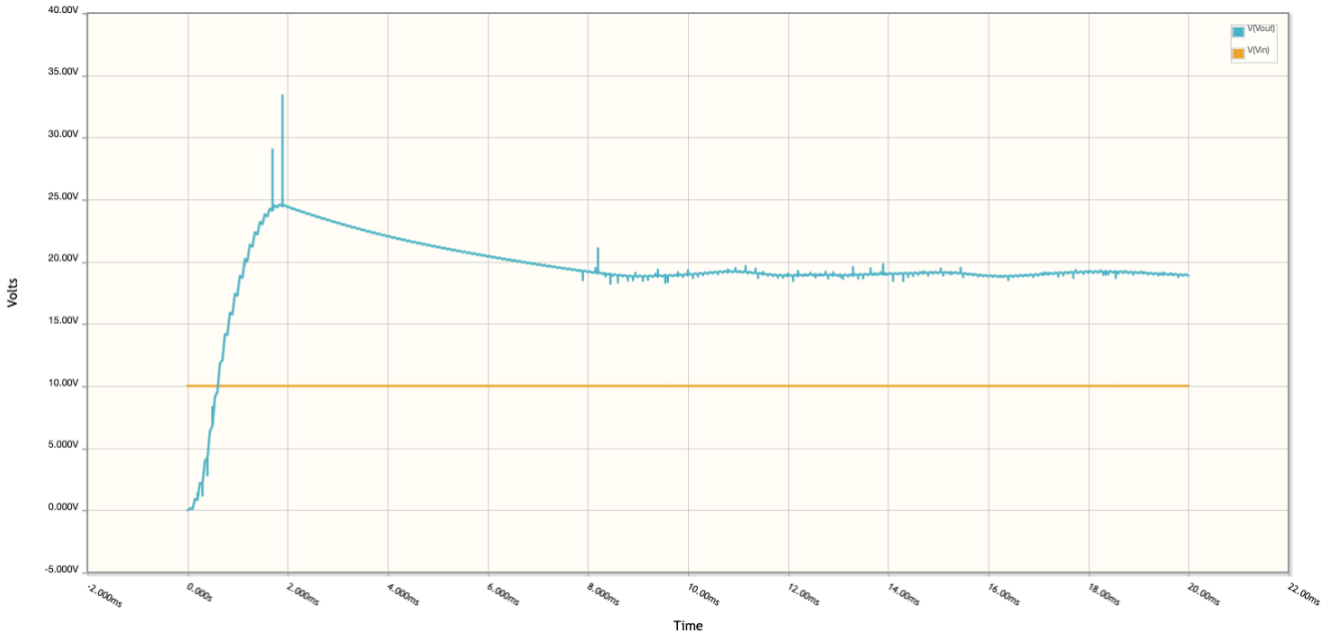
The dip at around 100us: After simulating the circuit, it will take some time for the capacitor and inductance to be fully charged and reach the steady states. This phenomenon is called transient respond.

The steady state output is not a straight horizontal line: It's due to the high frequency part of the supply which is from the clock. As the clock is continuously oscillating between high and low state, the status of the capacitor and the inductor are continuously oscillating between charged and un-charged. The buck converter has an on-state and an off-state which is oscillating in a frequency which is equal to the frequency of the clock. Thus, the value of V_{out} keeps oscillating in a small range. On the other word, it reaches a dynamic equilibrium.

9.



10. According to KCL, $I_{L1} + I_{D1} = I_{M1}$
    As can be seen from the figure, $I_{L1} + I_{D1} = I_{M1}$,which is consistent with the result of KCL, thus, the output is just what we expect.
11.

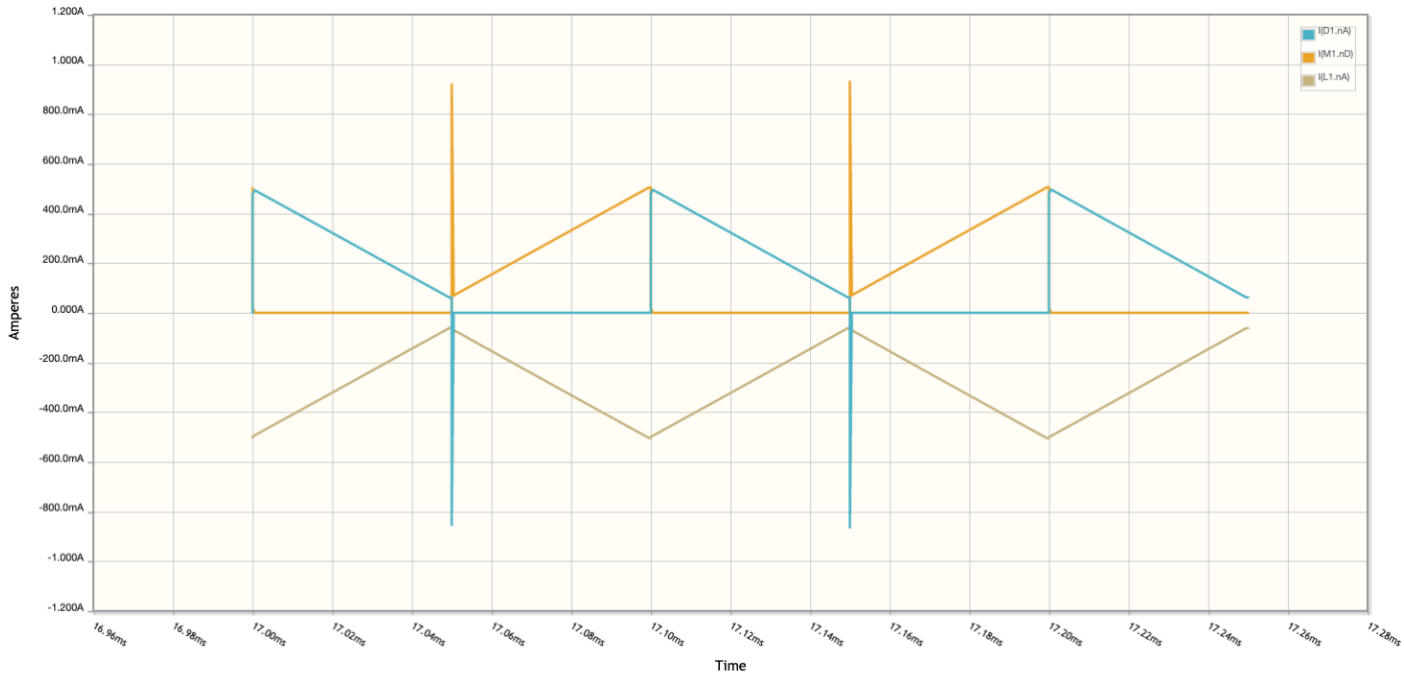


12. According to the formula of boost converter: $V_{out} = \frac{V_{in}}{1-D}$, the output voltage we calculated is V_{out} = 10v / 0.5 = 20v
    As shown in the figure, the real output is about 19v, which is quite similar to 20v. Thus, the output is just what we expect. There is a small deviation between the measured value and the calculated value because there is loss in the switch and diode.
13. Firstly, the settle down time is related to the frequency of the clock. The frequency of the clock in the boost converter(10kHz) is smaller than that of the buck

converter(56.67kHz). Thus, the settle down time for the boost converter is longer than the buck converter.

Secondly, the settle down time is also related to the magnitude of V_{out} . The V_{out} of the boost convertor is larger than the V_{out} of the buck converter, thus the time for the boost converter to settle down is longer than the buck converter.

14. The image is as shown below:



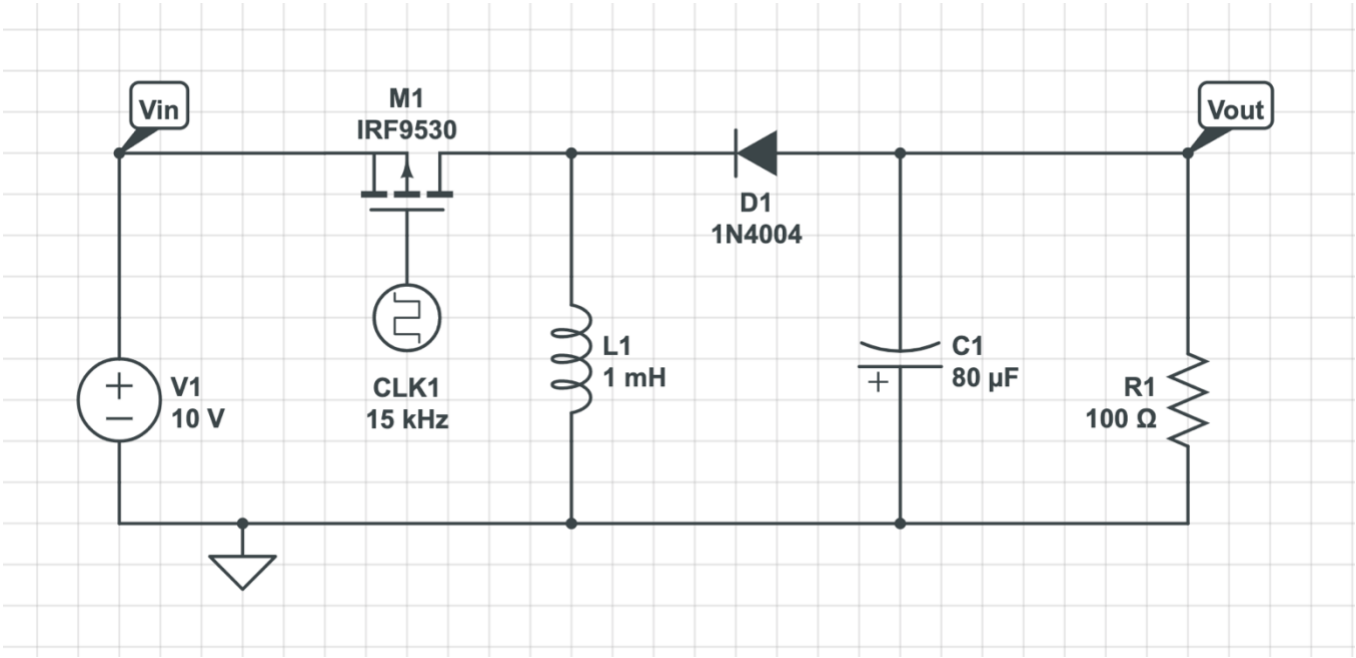
15. According to the rule of KCL, $I_{(D1,nA)} + I_{(M1,nD)} = I_{(L1,nA)}$
The experimental data we measured is consistent with what we expected.

16.

Jack	USB	Power Source?	NODE1	NODE2	NODE3
0V	5V	USB	-928.8μV	4.999V	3.3V
10V	0V	Barrel Jack	5.001V	5V	3.3V
10V	5V	Barrel Jack	5.001V	5V	3.3V
3V	5V	USB	-928.8μV	4.999V	3.3V

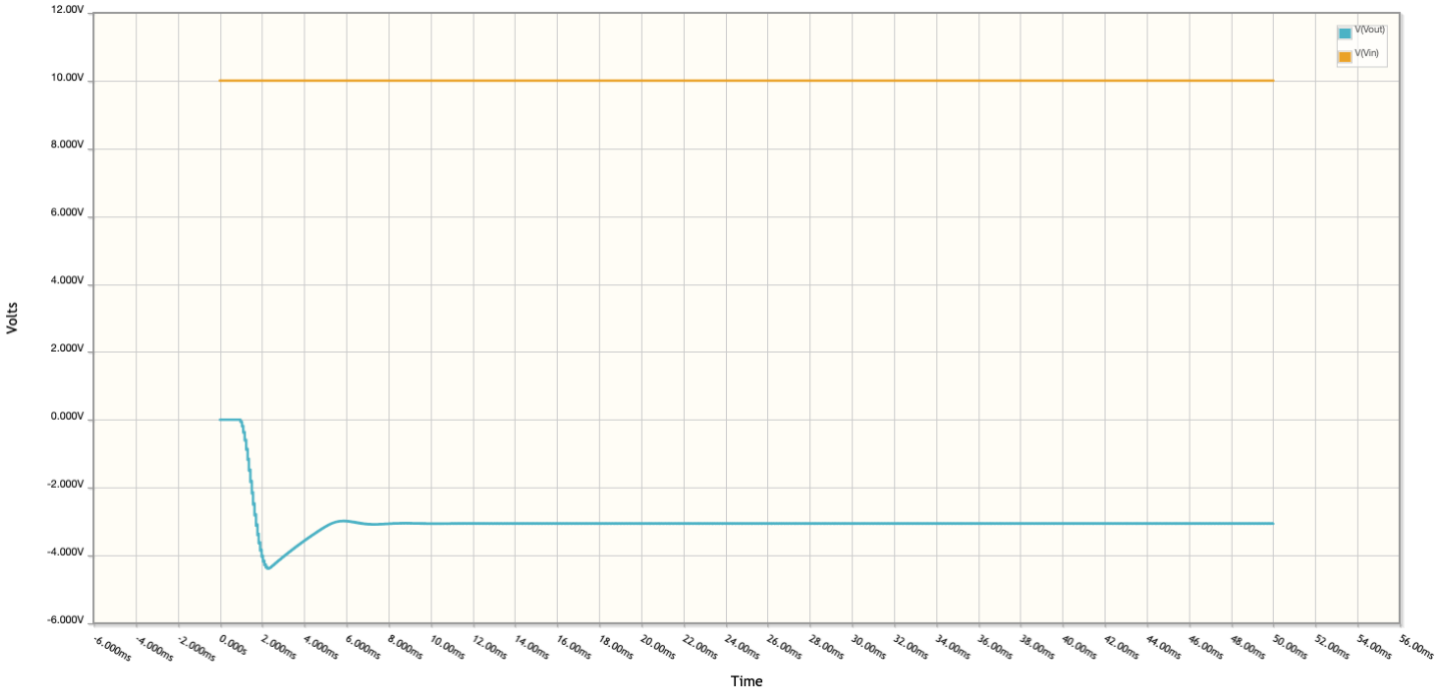
17. The inverting input is controlled by the power regulator which make it to be 3.3v. The USB has the priority to be used as the power source first. Thus, if the voltage divider is used, the Barrel Jack must larger or greater than 3.3*0.5 = 6.6V for the Barrel Jack to be used as the power source. If the voltage divider is not used, the non-Inverting input will be always larger than 3.3V. The Barrel Jack will then always be used as the power source and the circuit will be not well regulated.

18. The Buck-Boost converter is as shown below with the link:

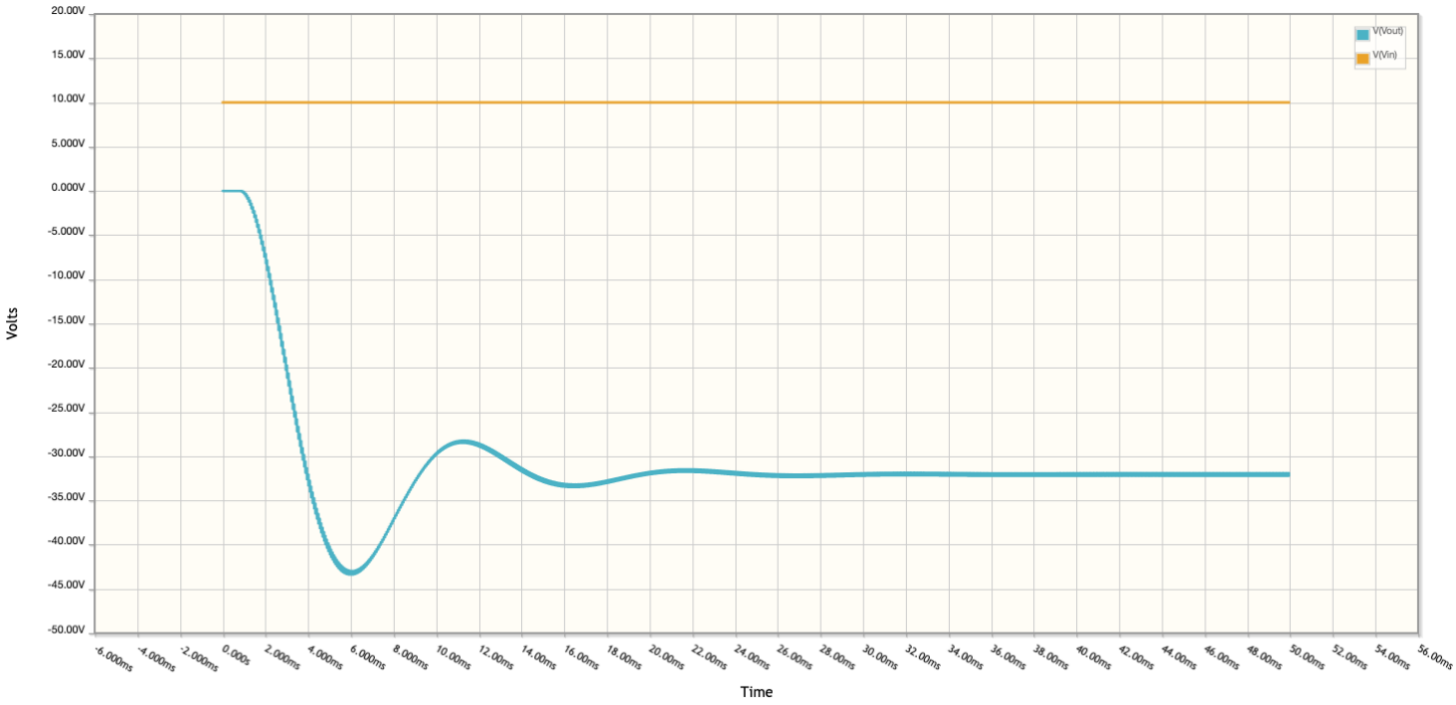


https://www.circuitlab.com/editor/#?id=54jz3d4224p7

19. The input voltage is 10 V DC and the duty cycle is 0.3(smaller than 0.5):



20. The input voltage is 10 V DC and the duty cycle is 0.8(larger than 0.5):



21. BJT and MOSFET are two different types of transistors
    Difference:
    - The MOSFET is a metal-oxide semiconductor whereas the BJT is a bipolar junction transistor
    - MOSFET is voltage controlled while BJT is current controlled (A BJT depends on the current at its base terminal whereas a MOSFET depends on the voltage at the oxide-insulated gate electrode)
    - MOSFETs are ideal for high-power applications whereas BJTs are more commonly used in low-current applications
    - A MOSFET's structure is inherently more complex than a BJT's structure
    - MOSFET is more expensive than BJT
    - The input resistance of MOSFET is higher than BJT

    Similarities:
    - Both have three terminals
    - Both are transistors

    Nowadays, MOSFET is more commonly used in analog and digital circuit than BJT. However, BJT is better in some low-current applications. Thus, while choosing from BJT and MOSFET, we need to consider many different factors including power level, drive voltage, efficiency, cost, and switching speed, etc.
    Above all, they are both irreplaceable.