Advanced Digital Design [LU]

Lab Exercise I - Metastability Measurement and Analysis

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based on an exercise by Thomas Polzer

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1 Introduction

In this task you will use a Late Transition Detector (LTD) to measure the metastability characteristic (1/MTBU vs. resolution time) of a flip flop in an FPGA and determine, based on the collected data, the metastability parameters τ and T_0. For that purpose we provide you with an (almost) working LTD based on the implementations presented in [1, 2] targeting the Terasic DE2-115 FPGA board. Before this LTD can be used, some small modifications are necessary. The template also comes with a (Python based) PC software to control the measurement process and extract the recorded data (as CSV traces).

2 Tasks

2.1 Complete the LTD implementation

The template we provide you with lacks the case separation discussed in [1, 2] (note that initially it does not work). Your first task is to add the missing features, whereat you solely need to modify the files

- `vhdl/ltd/ltd.vhd`
- `vhdl/ltd/fast_cnt_capture.vhd`

For further details refer to the comments in the code.

2.2 LTD Measurement

Perform a measurement with two differing clock duty cycles such that

- only the master can be seen
- master and slave are present

Be sure to choose a sufficiently large range of resolution times and adapt your measurement time such that a sufficient number of data points per resolution time is gathered.

2.3 MTBU Analysis

Analyze the results of both measurement runs (i.e., the two measurements with different clock duty cycle settings) from the previous task in the following way:

- Calculate τ for the master and, if applicable, the slave latch for all metastability cases (i.e., late falling/rising transition, positive/negative glitch as well as the combined count for all cases)
- Estimate T_0 (if applicable) for all cases
- Plot each case separately and visualize the parameters calculated above

Generate meaningful plots and compare the results from both measurement runs. Figures 2.1 and 2.2 show the results of some example measurements to give you a rough guideline how to present the results and what to expect from them. You are of course allowed to use any tool of your choice for analysis and visualization (Excel, Python, MATLAB, etc.).

At last investigate your results, explain the differences between the two measurement runs and argue about possible causes.

2.4 TBU Distribution Analysis

Analyze the distribution of the measured Times Between Upsets (TBU). Use box-plots to visualize the distribution of the TBU for different resolution times (example plot shown in Figure 2.3). Create separate plots for the single measurement runs and metastability cases. Compare the mean value (MTBU) with the standard deviation and the smallest/largest measured value for each resolution time. What are the implications on system reliability?

You can also create a 3D histogram (such as the one shown in Figure 2.4) to visualize the TBU distribution for different resolution times in a very compact way.

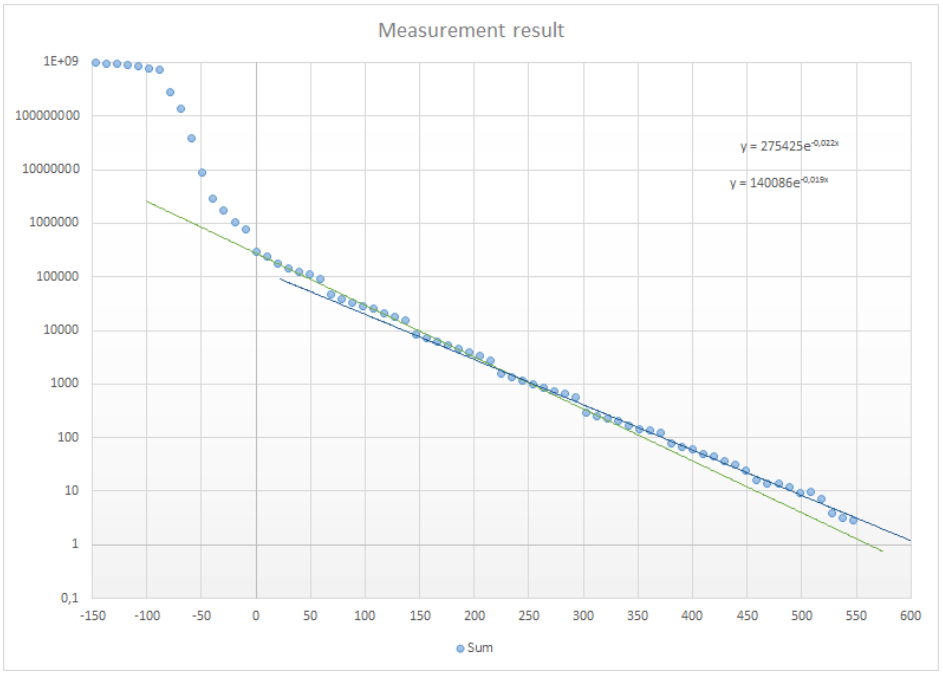

Figure 2.1: LTD example 1/MTBU vs. resolution time plot

Figure 2.2: LTD example case comparison plot

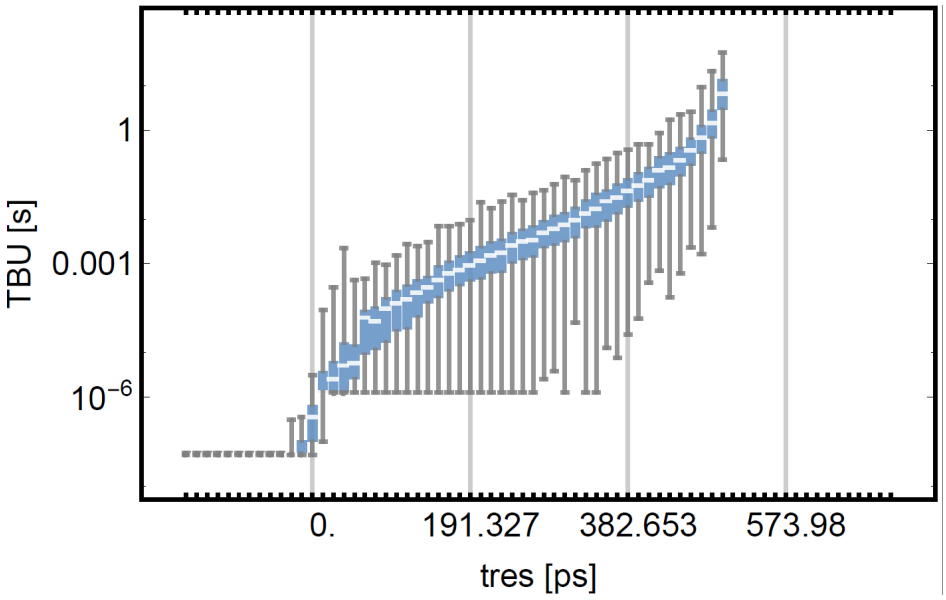

Figure 2.3: LTD Example Box Plot

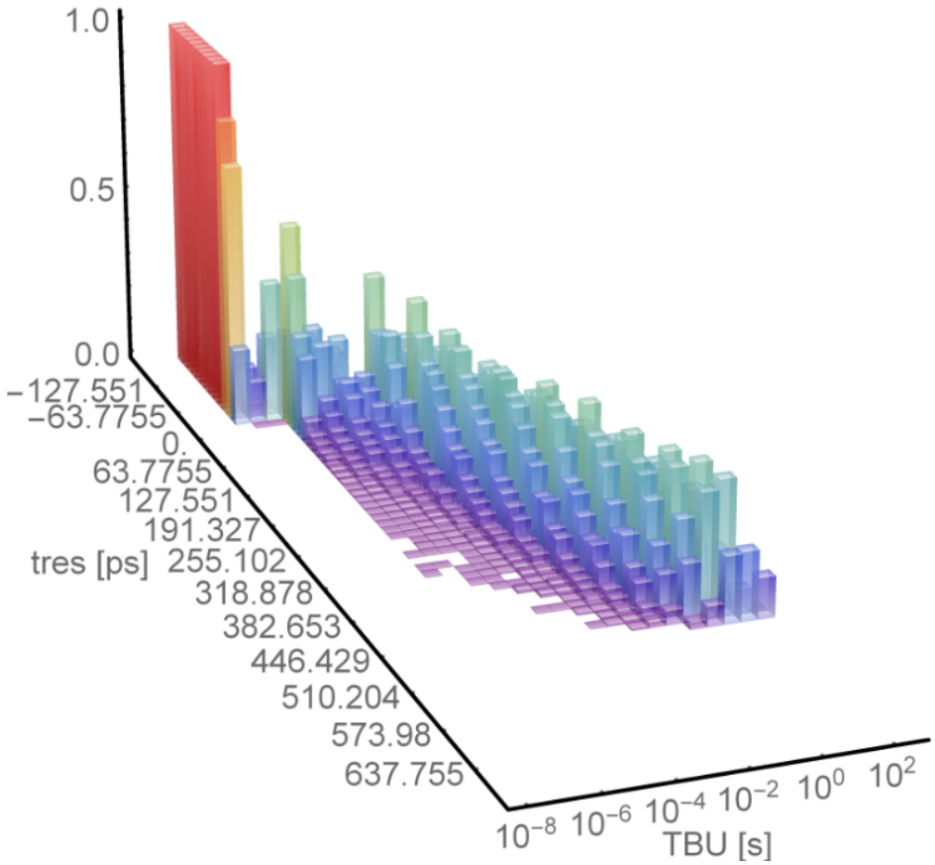

Figure 2.4: LTD Example 3D Histogram

3 Submission

Solve the tasks in Section 2 and prepare a presentation (slides) with all relevant results (modified code sections, plots, analysis) and upload it to TUWEL (deadline: Wednesday, 9 December 2020, 23:59). Further

you are supposed to schedule an appointment for an (online) exercise interview by writing an e-mail to `addlu@ecs.tuwien.ac.at`. Note that (i) you are of course allowed to use the slides during the interview and (ii) you may present multiple designs in a single interview (iii) all interviews have to be finished until end of January and (iv) your presentation will also be graded, so come well prepared.

References

[1] T. Polzer and A. Steininger. An approach for efficient metastability characterization of fpgas through the designer. In *IEEE 19th International Symposium on Asynchronous Circuits and Systems*, pages 174–182, 2013.

[2] T. Polzer and A. Steininger. Measuring the distribution of metastable upsets over time. In *2015 Euromicro Conference on Digital System Design*, pages 189–196, Aug 2015.