Wang Lei

Born on Jan. 29th, 1999
Currently living in Beijing City
A first year postgraduate student
@ UCAS, ICT

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Scientific interests

○ Multi-Level IR
○ Domain Specific Architecture
○ Compiler Optimization
○ DL Compiler

Education

Aug. 2021 - Present Master in Computer Science
University of Chinese Academy of Science Institute of Computing Technology

Aug. 2017 - Jun. 2021 Bachelor in Electronic Engineering
Nanjing Tech University
Overall GPA: 3.95 / 4.00
Ranking: 1 / 59

Currently Situation

I'm currently a first year postgraduate student @ UCAS,ICT.
My research interests lie in ML System and Optimization, looking for an internship opportunity helps me dive deeply into DL Compiler Stack.
I enjoy writing post: MLIR: A Brief Survey
I'm also a contributor of Tengine and buddy-mlir .

Awards & Honor

Competetion

First Price of 2019 National Undergraduate Electronics Design Contest
Third prize of National FPGA Competition
more competition awards.

Scholarship

2018 Chinese National Scholarship (Top 0.3%)
2019 School Principle's Scholarship (Top 0.1%)
2020 School Principle's Scholarship (Top 0.1%)
First Prize Scholarship x 3 (Top 3%)
Special Prize Scholarship x 4 (Top 3%)

Experience

Sep. 2021 - Oct. 2021. Netease Intelligent Hardware R&D Department

NPU / DLA Development intern.
NVDLA(Nvidia Deep Learning Accelerator, an opensource DLA) FPGA deployment and Software stack porting.

Oral communications

Sep. 23th, 2021. Tengine Open Talk : New Backend OpenDLA. [slides] [recording]

I made a big pull requst #1061 to integrate NVDLA with Tengine.

Last updated: March, 2022.