Lei Yang

Post-Doctoral Research Associate

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Research Interests

• **Automated Machine Learning.** Hardware/software co-exploration for neural architectures [10][11][12][13][15].

• **Embedded System.** Optimization algorithm design for high-performance and low-power computing in Network-on-Chip (NoC) based MPSoCs; Computation and communication optimization for thermo-reliable many-core systems [2][3][4][5][6][8][9][14][17][18][21][22][23][24][25][25].

• **Computing Architecture Design.** Optimized architecture design for computing and communication; Nonvolatile Memory (NVM) based many-core systems [1][7][16][19][20].

Education

Chongqing University 02/2014 – 06/2019. CHONGQING, CHINA.
• **Ph.D. in the Department of Computer Science**.
High-performance and low-power optimization algorithm design for NoC-based many-cores.

University of Pittsburgh 02/2019 – 08/2019. PITTSBURGH, U.S.
• **Visiting Scholar in the Department of Electrical and Computer Engineering Swanson School of Engineering**.
Optimization algorithm design for embedded systems.

University of California, Irvine 10/2017 – 02/2019. IRVINE, U.S.
• **Visiting Scholar in the Department of Computer Science**.
Performance and power optimization for NVM-based NoCs.

Chongqing University 09/2013 – 01/2014. CHONGQING, CHINA.
• **Master degree in Computer Science**.
Majoring on computer science and parallel computing in many-cores.

Chongqing University 09/2009 – 06/2013. CHONGQING, CHINA.
• **Bachelor degree in Computer Science**.
Majoring on computer science and network engineering.

Honors & Awards

Best Paper Nomination Award at ASP-DAC 2020	01/2020. CHINA
Best Paper Nomination Award at CODES+ISSS 2019	10/2019. USA
Best Paper Nomination Award at DAC 2019	06/2019. USA
Award of Grant at DAC 2018 PhD. Forum	06/2018. USA
Award of IEEE/CEDA Grant at ESWEEK 2017	10/2017. KOREA
Best Poster Paper Award at RTCSA 2017	08/2017. TAIWAN, CHINA
Best Paper Award at ICCD 2017	06/2017. USA
A.Richard Newton Young Fellowship Award at DAC 2017	06/2017. USA
Chinese Government Scholarship (CSC) Award	05/2017. CHINA
Most Popular Poster Award at ASP-DAC 2017 Student Research Forum	01/2017. JAPAN
Award of Student Forum Travel Grant at ASP-DAC 2017	01/2017. JAPAN
Award of Travel Grant at Future Chip 2016	12/2016. CHINA
Award of China National Scholarship	10/2016. CHINA
Best Paper Nomination Award at ASP-DAC 2016	01/2016. MACAO, CHINA
Award of 3^{rd} Prize Winner at Google Android Application Development Contest	12/2012. CHINA
Award of 2^{nd} Prize Winner at National Programming Contest for College Students	10/2012. CHINA

Proposal & Research Project

National Science Foundation (NSF)/CISE: Core Programs — SUBMITTED
Collaborative Research.
"Intermittent and Incremental Inference with Statistical Neural Network for Energy-Harvesting Powered Devices"

National Natural Science Foundation of China/(NSFC No. 6177051433) — 03/2017 – 12/2020
Research Project Writing.
"Performance and Energy Efficiency Optimization for Thermal-Reliable Many-Core Systems in the Dark Silicon Era"

National Natural Science Foundation of China/(NSFC No. 61402060) — 01/2015 – 12/2017
Main Member.
"Efficient Techniques for System-Level Soft Error Tolerance in Multiprocessor System-on-Chips"

Chongqing High-Tech Program/(No. cstc2015jcyjA40042) — 01/2016 – 12/2017
Main Member.
"Hardware-Software Collaborated Approach for the Reliability of Many-Core Systems"

Student Research Training Program/(SRTP) — 09/2011 – 06/2012
Team Leader.
A three-student group designed an barcode recognition application of commodity

Microsoft Technology Club of Chongqing University/(CQUMSTC) — 01/2011 – 12/2011
Main Member.
Organization of activities and technical training.

Teaching Experience

Teaching Certification (University of Notre Dame) FALL-2019.

- Striving for Excellence in College and University Teaching

<Embedded Systems and Applications> (TA for Prof. Weichen Liu) 2014 – 2015.

- Fully engage classes of 50 students, receiving excellent student feedback.
- Planned and conducted 4 tutorials during semester for experimental curriculums on CBT-SuperIOT platform and applications of wireless sensor networks on ZigBee.
- Marked student assignments, seeking guidance in good practice from colleagues and the University Teaching Quality Handbook.

<High-performance Parallel Computing> (TA for Prof. Edwin H. M. Sha) 2013 – 2014.

- Fully engage classes of 12 fourth-year undergraduate students, marked 10 quizzes and answered after-class questions.
- Planned and conducted 4 experimental curriculums about programming using Pthreads.
- Marked student assignments, seeking guidance in good practice from colleagues and the University Teaching Quality Handbook.

Professional Services

Technical Program Committee

· Asia and South Pacific Design Automation Conference (ASP-DAC) SIGDA SRF 2020

Journal Reviewer

· IEEE Transactions on Computers (TC)

· IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)

· IEEE Embedded System Letters (ESL)

· Journal of Circuits, Systems, and Computers (JCSC)

· Journal of IEEE Software

Conference Reviewer

· Design Automation Conference (DAC) 2018

Collaborate and mentor students

- Mengquan Li (Ph. D Candidate. $2015-$Now): Exploration of thermal reliability for photonic NoC
- Peng Chen (Ph. D Candidate. $2016-$Now): Priority-based scheduling for realtime systems
- Zheyu Yan (Ph. D Candidate. $2019-$Now): Hardware/software co-exploration for neural architectures

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Refereed Publications

I have published more than 30 research articles in refereed international conferences and premier journals. I have received one Best Paper Award in ICCD'17, and five Best Paper Nomination in ASP-DAC'20, CODES+ISSS'19, DAC'19, ASP-DAC'19 and ASP-DAC'16.
Full paper list can be found at https://dblp.uni-trier.de/pers/hd/y/Yang_0018:Lei

Three Representative Papers

1. **Lei Yang**, Zheyu Yan, Meng Li, Hyoukjun Kwon, Liangzhen Lai, Tushar Krishna, Vikas Chandra, Weiwen Jiang and Yiyu Shi, " Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *In Proc. Of Design Automation Conference* (DAC 2020). San Francisco, USA. July, 2020.
   - **Featured research: Hardware/software co-exploration for neural architectures and ASICs.**
2. **Lei Yang**, Weiwen Jiang, Weichen Liu, Edwin H. M. Sha, Yiyu Shi, Jingtong Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence", *In Proc. Of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2020). China. Jan, 2020. (**Best Paper Nomination**)
   - **Featured research: Hardware/software co-exploration for neural architectures and chips.**
3. **Lei Yang**, Weichen Liu, Nan Guan, Nikil Dutt,"Optimal Application Mapping and Scheduling for Network-on-Chips with Computation in STT-RAM based Router", *In Proc. of IEEE Transactions on Computers* (TC). August, 2018.
   - **Featured research: Hybrid router design for computation and communication efficiency.**

Selected Journal Articles

[1] **Lei Yang***, Weichen Liu, Nan Guan, Nikil Dutt, "Optimal Application Mapping and Scheduling for Network-on-Chips with Computation in STT-RAM based Router", *In Proc. of IEEE Transactions on Computers* (TC). Volume: 68, Issue: 8. pp. 1174-1189. August, 2019.

[2] Weiwen Jiang, Edwin Hsing-Mean Sha, Qingfeng Zhuge*, **Lei Yang**, Xianzhang Chen, Jingtong Hu,"On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *In Proc. of IEEE Transactions on CAD of Integrated Circuits and Systems* (TCAD). Volume: 38, Issue: 8. pp. 1515-1528. August, 2019.

[3] Weichen Liu, **Lei Yang***, Weiwen Jiang, Liang Feng, Nan Guan, Wei Zhang, Nikil Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *In Proc. of IEEE Transactions on Computers* (TC). Volume: 67, Issue: 12. pp. 1818-1834. December, 2018.

[4] Mengquan Li, Weichen Liu*, **Lei Yang**, Peng Chen, Chao Chen, "Chip Temperature Optimization for Dark Silicon Many-Core Systems", *In Proc. of IEEE Transactions on CAD of Integrated Circuits and Systems* (TCAD) 37(5): 941-953. 2018.

[5] **Lei Yang**, Weichen Liu*, Weiwen Jiang, Mengquan Li, Peng Chen, Edwin H. M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era", *In Proc. of IEEE Transactions on Parallel and Distributed Systems* (TPDS). Volume: 28, Issue:7, pp.1905-1918. July, 2017.

[6] **Lei Yang**, Weichen Liu*, Weiwen Jiang, Chao Chen, Mengquan Li, Peng Chen, Edwin H. M. Sha, "Hardware-software collaboration for dark silicon heterogeneous many-core systems", *In Proc. Of Future Generation Computer Systems* (FGCS). Volume: 68 (2017). pp.234-247. March, 2017.

[7] Weiwen Jiang, Edwin Hsing-Mean Sha, Xianzhang Chen, **Lei Yang**, Lei Zhou, Qingfeng Zhuge*, "Optimal Functional-Unit Assignment for Heterogeneous Systems Under Timing Constraint", *In Proc. of IEEE Transactions on Parallel and Distributed Systems* (TPDS). Volume: 28, Issue: 9, pp.2567-2580. 2017.

[8] **Lei Yang**, Weichen Liu*, Weiwen Jiang, Mengquan Li, Juan Yi, Edwin H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization", *In Proc. of IEEE Transactions on Very Large Scale Integration Systems* (TVLSI). Volume: 24, Issue: 10, pp.3027-3040. February, 2016.

[9] Weiwen Jiang, Qingfeng Zhuge*, Xianzhang Chen, **Lei Yang**, Juan Yi, Edwin H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum

Throughput", *In Proc. of Journal of Signal Processing Systems* (JSPS). Volume: 84, Issue: 1, pp.123-137. 2016.

Selected Conference Papers

[10] **Lei Yang**, Zheyu Yan, Meng Li, Hyoukjun Kwon, Liangzhen Lai, Tushar Krishna, Vikas Chandra, Weiwen Jiang and Yiyu Shi, " Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *In Proc. Of Design Automation Conference* (DAC 2020). San Francisco, USA. July, 2020.

[11] **Lei Yang**, Weiwen Jiang, Weichen Liu, Edwin H. M. Sha, Yiyu Shi, Jingtong Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence", *In Proc. Of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2020). China. Jan, 2020. (**Best Paper Nomination**)

[12] Weiwen Jiang, Edwin Hsing-Mean Sha, Xinyi Zhang, **Lei Yang**, Qingfeng Zhuge, Yiyu Shi, Jingtong Hu, "Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference", *In Proc. of International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2019). New York, USA. Oct, 2019. (**Best Paper Nomination**)

[13] Weiwen Jiang, Xinyi Zhang, Edwin Hsing-Mean Sha, **Lei Yang**, Qingfeng Zhuge, Yiyu Shi, Jingtong Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search", *In Proc. of ACM/IEEE Design Automation Conference* (DAC 2019). Las Vegas, USA. June, 2019. (**Best Paper Nomination**)

[14] Mengquan Li, Weichen Liu, **Lei Yang**, Peng Chen, Duo Liu, Nan Guan, "Routing in optical networkon-chip: minimizing contention with guaranteed thermal reliability", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2019). Japan. Jan, 2019. (**Best Paper Nomination**)

[15] Weiwen Jiang, E. H.-M. Sha, Qingfeng Zhuge, **Lei Yang**, Xianzhang Chen and Jingtong Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *In Proc. of International Conference on Compilers, Architecture, and Synthesis for Embedded Systems* (CASES 2018). Italy, Oct, 2018.

[16] **Lei Yang**, Weichen Liu, Peng Chen, Nan Guan, Mengquan Li, "Task Mapping on SMART NoC: Contention Matters, Not the Distance", *In Proc. of ACM/IEEE Design Automation Conference* (DAC 2017). Austin, USA. June, 2017.

[17] Weichen Liu, **Lei Yang**, Weiwen Jiang, Nan Guan, "Communication Optimization for Thermal Reliable Many-core Systems", *In Proc. of ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2017). Seoul, South Korea. Oct, 2017.

[18] **Lei Yang**, Weichen Liu, Nan Guan, Mengquan Li, Peng Chen, Edwin H. M. Sha, "Dark Silicon-Aware Hardware-Software Collaborated Design for Heterogeneous Many-Core Systems", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2017). pp.494-499. Japan. Jan, 2017.

[19] Weiwen Jiang, Edwin H. M, Qingfeng Zhuge, **Lei Yang**, Hailiang Dong, Xianzhang Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints", *In Proc. Of IEEE International Conference on Computer Design* (ICCD 2017), Boston, USA. Nov, 2017. (**Best Paper Award**)

[20] Weichen Liu, Peng Chen, **Lei Yang**, Mengquan Li, Nan Guan, "Fixed Priority Scheduling of Realtime Flows with Arbitrary Deadlines on SMART NoCs", *In Proc. of ACM/IEEE International Conference on Embedded Software* (EMSOFT 2017). Seoul, South Korea. Oct, 2017.

[21] **Lei Yang**, Weichen Liu, Weiwen Jiang, Mengquan Li, Juan Yi, Edwin H. M. Sha, "FoToNoC: A Hierarchical Management Strategy Based on Folded Torus-Like Network-on-Chip for Dark Silicon

Many-Core Systems", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2016). pp.725-730. Macau. Jan, 2016. ((**Best Paper Nomination**)

[22] **Lei Yang**, Weichen Liu, Weiwen Jiang, Wei Zhang, Mengquan Li, Juan Yi, Duo Liu, Edwin H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip based Multiprocessor System-on-Chip with Fine-Grain Communication Optimization", *In Proc. of IEEE Intl. Conferences on High Performance Computing and Communications* (HPCC 2015). pp.571-576. New York, NY. Aug, 2015.

[23] Mengquan Li, Juan Yi, Weichen Liu, Wei Zhang, **Lei Yang**, Chunhua Xiao, Edwin H. M. Sha, "An Efficient Technique for Chip Temperature Optimization of Multiprocessor Systems in the Dark Silicon Era", *In Proc. of IEEE International Conferences on High Performance Computing and Communications* (HPCC 2015). pp.688-693. New York, NY. Aug, 2015. (**Invited Paper**)

[24] **Lei Yang**, Weichen Liu, Weiwen Jiang, Juan Yi, Duo Liu, Qingfeng Zhuge, "Contention-Aware Task and Communication Co-Scheduling for Network-on-Chip based Multiprocessor System-on-Chip", *In Proc. of IEEE International Conference on Embedded and Real-Time Computing Systems and Applications* (RTCSA 2014). Chongqing, China. August, 2014.

[25] Weiwen Jiang, Qingfeng Zhuge, Juan Yi, **Lei Yang**, Edwin Hsing-Mean Sha, "On self-timed ring for consistent mapping and maximum throughput", *In Proc. of IEEE 20th International Conference on Embedded and Real-Time Computing Systems and Applications* (RTCSA 2014). Chongqing, China, August 20-22, 2014.

Book Chapter

[25] **Lei Yang**, Weichen Liu, Weiwen Jiang, Mengquan Li, Jie Wang, "Isolation of Physical and Logical Views of Dark-Silicon Many-Core Systems for Reliability and Performance Co-Optimization", *Embedded System Technology*, Springer, 2016.