Lei (Lydia) Yang

Assistant Professor, University of New Mexico

Address: 498 Terrace St NE, Albuquerque, NM 87106

Email: leiyang@unm.edu
Tel: +1 (949)302-7908
Skype: leiyang0416

Homepage: http://www.ece.unm.edu/faculty-staff/electrical-and-computer/lei-yang.html

Employment

University of New Mexico 08/2020 – Now. Albuquerque, U.S.
- **Assistant Professor in the Department of Electrical and Computer Engineering**.

Focus on the system-level optimization of applied machine learning.

University of Notre Dame 10/2019 – 08/2020. Notre Dame, U.S.
- **Postdoctoral Researcher in the Department of Computer Science and Engineering**.
- **PI: Prof. Yiyu Shi**

Focus on the co-exploration of neural architectures and hardware design.

University of Pittsburgh 02/2019 – 08/2019. Pittsburgh, U.S.
- **Research Scholar in the Department of Electrical and Computer Engineering**.
- **PI: Prof. Jingtong Hu**

Optimization algorithm design for embedded systems.

Education

University of California, Irvine 10/2017 – 02/2019. Irvine, U.S.
- **Joint Ph.D. program in Donald Bren School of Information and Computer Sciences**.
- **Advisor: Prof. Nikil Dutt**

Performance and power optimization for NVM-based NoCs.

Chongqing University 02/2014 – 06/2019. Chongqing, China.
- **Ph.D. degree in the Department of Computer Science**.
- **Advisor: Prof. Weichen Liu**.

High-performance and low-power optimization algorithm design for NoC-based many-cores.

Chongqing University 09/2009 – 06/2013. Chongqing, China.
- **Bachelor degree in Computer Science**.

Majoring on computer science and network engineering.

Research Interests

- **System-Level Optimization for Applied Machine Learning.** Design and optimization of machine learning models for specific embedded systems, including fair medical AI, collaborative drug discovery, and subsurface estimation [14][15][17].

• **Automated Machine Learning.** Hardware and software co-exploration for neural network architectures [1][2][3][13][18][19] [20][21][23].

• **Embedded System.** Optimization algorithm design for high-performance and low-power computing in Network-on-Chip (NoC) based MPSoCs; Computation and communication optimization for thermo-reliable many-core systems [5][6][7][8][9][11][12][22][25][26][29][30][31][35][33].

• **Computing Architecture Design.** Optimized architecture design for high-performance computing and communication; Nonvolatile Memory (NVM) based many-core systems [4][10][24][27][28].

Honors & Awards

Best Paper Award at IEEE TCAD 2021	10/2021. USA
First place at the 31^{st} ACM SIGDA University Demonstration	10/2021. USA
Best Paper Nomination Award at ASP-DAC 2020	01/2020. CHINA
Best Paper Nomination Award at CODES+ISSS 2019	10/2019. USA
Best Paper Nomination Award at DAC 2019	06/2019. USA
Best Paper Nomination Award at ASP-DAC 2019	01/2019. JAPAN
Award of Grant at DAC 2018 PhD. Forum	06/2018. USA
Award of IEEE/CEDA Grant at ESWEEK 2017	10/2017. KOREA
Best Poster Paper Award at RTCSA 2017	08/2017. CHINA
Best Paper Award at ICCD 2017	06/2017. USA
A.Richard Newton Young Fellowship Award at DAC 2017	06/2017. USA
Chinese Government Scholarship (CSC) Award	05/2017. CHINA
Most Popular Poster Award at ASP-DAC 2017 Student Research Forum	01/2017. JAPAN
Award of Student Forum Travel Grant at ASP-DAC 2017	01/2017. JAPAN
Award of Travel Grant at Future Chip 2016	12/2016. CHINA
Award of China National Scholarship	10/2016. CHINA
Best Paper Nomination Award at ASP-DAC 2016	01/2016. CHINA

Proposal & Research Project

National Science and Education Center (NSEC) at Los Alamos — AWARDED
Role: PI.
Amount: $80K for the first year, and possible for a second year of funding.
"Intelligent Quantum Sensing with Quantum Neural Networks"

National Institutes of Health (NIH) — PENDING
Role: Co-I.
"Achieve Fair AI-Assisted Mobile Dermatology Diagnosis through Unsupervised Federated Learning"

National Science Foundation (NSF)/FAI — PENDING
Role: PI.
"FAI: Addressing the Fairness Issues in AI-Assisted Healthcare Mobile Apps through Unsupervised Federated Learning"

Johnson & Johnson WiSTEM^{2}D PENDING

Role: PI.

"Towards a Collaborative and Privacy-Preserving Learning Framework for Molecule Drug Discovery"

National Science Foundation (NSF)/EPSCoR Track-2 PENDING

Role: Co-PI.

"Machine Learning-based Modeling Experimental Approach for Advanced Manufacturing"

Intelligent Additive Manufacturing Cluster in New Mexico (I AM CiNM) PENDING

Role: Member/Research Proposal Writing.

"Intelligent Additive Manufacturing (I-AM): Building optimized, coordinated, secure, resilient systems, and preparing future workforce"

Teaching Experience

<Advanced Computer Architecture> (Univ. of New Mexico, ECE 538) 2021 FALL

- Instructor.

<Design of Computers> (Univ. of New Mexico, ECE 438) 2021 SPRING

- Instructor.

<Advanced Computer Architecture> (Univ. of New Mexico, ECE 538) 2020 FALL

- Instructor.

<Machine Learning for Embedded Systems> (Univ. of Notre Dame, CSE60685) 2020 SPRING

- Teaching Assistant.

Teaching Certification (Univ. of Notre Dame) 2019 FALL

- Striving for Excellence in College and University Teaching

<Embedded Systems and Applications> (Chongqing University) 2015 FALL

- Teaching Assistant.

<High-performance Parallel Computing> (Chongqing University) 2013 FALL

- Teaching Assistant.

Professional Services

Chair or Organizer

· Organizer and Session Chair - 2021 DAC Early Career Workshop

· Registration Chair - International Conference on Computer Design (ICCD) 2021

· Workshop Organizer - Workshop on Energy-Efficient Machine Learning (E2ML) 2021

· Session Chair - Design Automation Conference (DAC) 2021

· Session Chair - ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC 2021)

· Session Chair - IEEE International System-on-Chip Conference (SOCC 2020)

Technical Program Committee

· Design Automation Conference (DAC) 2022

· International Conference on Application-specific Systems, Architectures and Processors (ASAP) 2021

· International Conference On Computer Aided Design (ICCAD) 2021

· IEEE Computer Society Annual Symposium on VLSI (ISLVLSI) 2021

· Design Automation Conference (DAC) 2021

· ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) 2021
· ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC) SRF 2020,2021
· ACM/SIGAPP Symposium On Applied Computing (SAC) 2020
· IEEE Computer Society Annual Symposium on VLSI (ISLVLSI) 2020
· IEEE International System-on-Chip Conference (SOCC) 2020
· International Workshop on Memory and Storage Computing (MSC 2020)

Journal Reviewer

· IEEE Transactions on Computers (TC)
· IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
· ACM Transactions on Cyber-Physical Systems (TCPS)
· ACM Journal on Emerging Technologies in Computing Systems (JETC)
· IEEE Embedded System Letters (ESL)
· Journal of Systems Architecture (JSA)
· IEEE Transactions on Embedded Computing Systems (TETC)
· ACM Transactions on Design Automation of Electronic Systems (TODAES)
· ACM Transactions on Embedded Computing Systems (TECS)
· IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT)
· Mathematical Problems in Engineering
· IET Cyber-Physical Systems: Theory Applications
· Journal of Circuits, Systems, and Computers (JCSC)
· IEEE Computational Intelligence Magazine (CIM)
· Journal of Network and Computer Applications (JNCA)
· Journal of IEEE Software

Mentor of Students

- **Daniel Manu** (Ph. D Candidate at the University of New Mexico) $08/2020-$Now
  Co-exploration of GNNs and hardware design
- **Junhuan Yang** (Ph. D Candidate at the University of New Mexico) $09/2021-$Now
  System-Level Optimization for Applied Machine Learning
- **Petro Mushidi Tshakwanda** (Graduate Student at the University of New Mexico) $09/2021-$Now
  Machine leaning for IoT devices
- **Chaeeun Park** (Undergraduate Student at the University of New Mexico) $09/2021-$Now
  System-Level Optimization for Applied Machine Learning
- **Lucas Zhou** (Undergraduate Student at the University of New Mexico) $08/2020 - 08/2021$
  Co-exploration of GNNs and hardware design

Publications

I have published more than 40 research articles in refereed international conferences and premier journals. I have received Best Paper Awards in IEEE TCAD'21 and ICCD'17, together with 5 Best Paper Nominations in ASP-DAC'20, CODES+ISSS'19, DAC'19, ASP-DAC'19 and ASP-DAC'16. Full paper list can be found at https://dblp.uni-trier.de/pers/hd/y/Yang_0018:Lei

Selected Journal Articles

[1] Weiwen Jiang, **Lei Yang**, S. Dasgupta, Jingtong Hu, and Yiyu Shi , "Standing on the Shoulders of Giants: Hard- ware and Neural Architecture Co-Search with Hot Start", Accepted by International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS) 2020, also appears at IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). (acceptance rate 94/375=25.1%)

[2] Weiwen Jiang, Qiuwen Lou, Zeyu Yan, **Lei Yang**, Jingtong Hu, Xiaobo Hu, and Yiyu Shi, , "Device-Circuit-Architecture Co- Exploration for Computing-in-Memory Neural Accelerators", *In Proc. of IEEE Transactions on Computers* (TC). Apr, 2020.

[3] Weiwen Jiang, **Lei Yang**, E. H.-M Sha, QF Zhuge, Shouzhen Gu, S.Dasgupta, Yiyu Shi and Jingtong Hu , "Hardware/Software Co-Exploration of Neural Architectures", *In Proc. of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD). Mar, 2020. (**Best Paper Award**)

[4] **Lei Yang**, Weichen Liu, Nan Guan, Nikil Dutt, "Optimal Application Mapping and Scheduling for Network-on-Chips with Computation in STT-RAM based Router", *In Proc. of IEEE Transactions on Computers* (TC). Volume: 68, Issue: 8. pp. 1174-1189. August, 2019.

[5] Weiwen Jiang, Edwin Hsing-Mean Sha, Qingfeng Zhuge*, **Lei Yang**, Xianzhang Chen, Jingtong Hu,"On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *In Proc. of IEEE Transactions on CAD of Integrated Circuits and Systems* (TCAD). Volume: 38, Issue: 8. pp. 1515-1528. August, 2019.

[6] Weichen Liu, **Lei Yang**, Weiwen Jiang, Liang Feng, Nan Guan, Wei Zhang, Nikil Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *In Proc. of IEEE Transactions on Computers* (TC). Volume: 67, Issue: 12. pp. 1818-1834. December, 2018.

[7] Mengquan Li, Weichen Liu, **Lei Yang**, Peng Chen, Chao Chen, "Chip Temperature Optimization for Dark Silicon Many-Core Systems", *In Proc. of IEEE Transactions on CAD of Integrated Circuits and Systems* (TCAD) 37(5): 941-953. 2018.

[8] **Lei Yang**, Weichen Liu*, Weiwen Jiang, Mengquan Li, Peng Chen, Edwin H. M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era", *In Proc. of IEEE Transactions on Parallel and Distributed Systems* (TPDS). Volume: 28, Issue:7, pp.1905-1918. July, 2017.

[9] **Lei Yang**, Weichen Liu, Weiwen Jiang, Chao Chen, Mengquan Li, Peng Chen, Edwin H. M. Sha, "Hardware-software collaboration for dark silicon heterogeneous many-core systems", *In Proc. Of Future Generation Computer Systems* (FGCS). Volume: 68 (2017). pp.234-247. March, 2017.

[10] Weiwen Jiang, Edwin Hsing-Mean Sha, Xianzhang Chen, **Lei Yang**, Lei Zhou, Qingfeng Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems Under Timing Constraint", *In Proc. of IEEE Transactions on Parallel and Distributed Systems* (TPDS). Volume: 28, Issue: 9, pp.2567-2580. 2017.

[11] **Lei Yang**, Weichen Liu, Weiwen Jiang, Mengquan Li, Juan Yi, Edwin H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization", *In Proc. of IEEE Transactions on Very Large Scale Integration Systems* (TVLSI). Volume: 24, Issue: 10, pp.3027-3040. February, 2016.

[12] Weiwen Jiang, Qingfeng Zhuge, Xianzhang Chen, **Lei Yang**, Juan Yi, Edwin H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum Throughput", *In Proc. of Journal of Signal Processing Systems* (JSPS). Volume: 84, Issue: 1, pp.123-137. 2016.

Selected Conference Papers

[13] Yuhong Song, Edwin Hsing-Mean Sha, Qingfeng Zhuge, Rui Xu, Yongzhuo Zhang, Bingzhe Li and **Lei Yang**, "BSC: Block-based Stochastic Computing to Enable Accurate and Efficient TinyML", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2022). Jan, 2022. Virtual Conference. (Accepted)

[14] Daniel Manu, Yi Sheng, Junhuan Yang, Jieren Deng, Tong Geng, Ang Li, Caiwen Ding, Weiwen Jiang and **Lei Yang**, "FL-DISCO: Federated Generative Adversarial Network for Graph-based Molecule Drug Discovery", *In Proc. Of* 2021 International Conference On Computer Aided Design (ICCAD 2021). Nov, 2021. (Accepted)

[15] Yawen Wu, Dewen Zeng, Zhepang Wang, Yi Sheng, **Lei Yang**, Alaina J James, Yiyu Shi and Jingtong Hu, "Federated Contrastive Learning for Dermatological Disease Diagnosis via On-device Learning", *In Proc. Of* 2021 International Conference On Computer Aided Design (ICCAD 2021). Nov, 2021. (Accepted)

[16] Zhiding Liang, Zhepeng Wang, Junhuan Yang, **Lei Yang**, Jinjun Xiong, Yiyu Shi and Weiwen Jiang, "Can Noise on Qubits Be Learned in Quantum Neural Network? A Case Study on QuantumFlow", *In Proc. Of* 2021 International Conference On Computer Aided Design (ICCAD 2021). Nov, 2021. (Accepted)

[17] Daniel Manu, Shaoyi Huang, Caiwen Ding and **Lei Yang**, "Co-Exploration of Graph Neural Network and Network-on-Chip Design Using AutoML", *In Proc. Of Great Lakes Symposium on VLSI 2021* (GLSVLSI 2021). June, 2021. New York, NY, USA.

[18] **Lei Yang**, Zheyu Yan, Meng Li, Hyoukjun Kwon, Liangzhen Lai, Tushar Krishna, Vikas Chandra, Weiwen Jiang and Yiyu Shi, " Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *In Proc. Of Design Automation Conference* (DAC 2020). San Francisco, USA. July, 2020. (acceptance rate 228/992=23.0%)

[19] **Lei Yang**, Weiwen Jiang, Weichen Liu, Edwin H. M. Sha, Yiyu Shi, Jingtong Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence", *In Proc. Of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2020). China. Jan, 2020. (**Best Paper Nomination**) (12 out of 263 submissions)

[20] Weiwen Jiang, Edwin Hsing-Mean Sha, Xinyi Zhang, **Lei Yang**, Qingfeng Zhuge, Yiyu Shi, Jingtong Hu, "Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference", *In Proc. of International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2019). New York, USA. Oct, 2019. (**Best Paper Nomination**) (3 out of 74 submissions)

[21] Weiwen Jiang, Xinyi Zhang, Edwin Hsing-Mean Sha, **Lei Yang**, Qingfeng Zhuge, Yiyu Shi, Jingtong Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search", *In Proc. of ACM/IEEE Design Automation Conference* (DAC 2019). Las Vegas, USA. June, 2019. (**Best Paper Nomination**) (5 out of 815 submissions)

[22] Mengquan Li, Weichen Liu, **Lei Yang**, Peng Chen, Duo Liu, Nan Guan, "Routing in optical networkon-chip: minimizing contention with guaranteed thermal reliability", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2019). Japan. Jan, 2019. (**Best Paper Nomination**)

[23] Weiwen Jiang, E. H.-M. Sha, Qingfeng Zhuge, **Lei Yang**, Xianzhang Chen and Jingtong Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *In Proc. of International*

Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2018). Italy, Oct, 2018.

[24] **Lei Yang**, Weichen Liu, Peng Chen, Nan Guan, Mengquan Li, "Task Mapping on SMART NoC: Contention Matters, Not the Distance", *In Proc. of ACM/IEEE Design Automation Conference* (DAC 2017). Austin, USA. June, 2017.

[25] Weichen Liu, **Lei Yang**, Weiwen Jiang, Nan Guan, "Communication Optimization for Thermal Reliable Many-core Systems", *In Proc. of ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis* (CODES+ISSS 2017). Seoul, South Korea. Oct, 2017.

[26] **Lei Yang**, Weichen Liu, Nan Guan, Mengquan Li, Peng Chen, Edwin H. M. Sha, "Dark Silicon-Aware Hardware-Software Collaborated Design for Heterogeneous Many-Core Systems", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2017). pp.494-499. Japan. Jan, 2017.

[27] Weiwen Jiang, Edwin H. M, Qingfeng Zhuge, **Lei Yang**, Hailiang Dong, Xianzhang Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints", *In Proc. Of IEEE International Conference on Computer Design* (ICCD 2017), Boston, USA. Nov, 2017. (**Best Paper Award**)

[28] Weichen Liu, Peng Chen, **Lei Yang**, Mengquan Li, Nan Guan, "Fixed Priority Scheduling of Realtime Flows with Arbitrary Deadlines on SMART NoCs", *In Proc. of ACM/IEEE International Conference on Embedded Software* (EMSOFT 2017). Seoul, South Korea. Oct, 2017.

[29] **Lei Yang**, Weichen Liu, Weiwen Jiang, Mengquan Li, Juan Yi, Edwin H. M. Sha, "FoToNoC: A Hierarchical Management Strategy Based on Folded Torus-Like Network-on-Chip for Dark Silicon Many-Core Systems", *In Proc. of ACM/IEEE Asia and South Pacific Design Automation Conference* (ASP-DAC 2016). pp.725-730. Macau. Jan, 2016. (**Best Paper Nomination**)

[30] **Lei Yang**, Weichen Liu, Weiwen Jiang, Wei Zhang, Mengquan Li, Juan Yi, Duo Liu, Edwin H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip based Multiprocessor System-on-Chip with Fine-Grain Communication Optimization", *In Proc. of IEEE Intl. Conferences on High Performance Computing and Communications* (HPCC 2015). pp.571-576. New York, NY. Aug, 2015.

[31] Mengquan Li, Juan Yi, Weichen Liu, Wei Zhang, **Lei Yang**, Chunhua Xiao, Edwin H. M. Sha, "An Efficient Technique for Chip Temperature Optimization of Multiprocessor Systems in the Dark Silicon Era", *In Proc. of IEEE International Conferences on High Performance Computing and Communications* (HPCC 2015). pp.688-693. New York, NY. Aug, 2015. (**Invited Paper**)

[32] **Lei Yang**, Weichen Liu, Weiwen Jiang, Wei Zhang, Mengquan Li, Juan Yi, Duo Liu, Edwin H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip based Multiprocessor System-on-Chip with Fine-Grain Communication Optimization", *In Proc. of IEEE Intl. Conferences on High Performance Computing and Communications* (HPCC 2015). pp.571-576. New York, NY. Aug, 2015.

[33] **Lei Yang**, Weichen Liu, Weiwen Jiang, Juan Yi, Duo Liu, Qingfeng Zhuge, "Contention-Aware Task and Communication Co-Scheduling for Network-on-Chip based Multiprocessor System-on-Chip", *In Proc. of IEEE International Conference on Embedded and Real-Time Computing Systems and Applications* (RTCSA 2014). Chongqing, China. August, 2014.

[34] **Lei Yang**, Weichen Liu, Weiwen Jiang, Juan Yi, Duo Liu, Qingfeng Zhuge, "Contention-Aware Task and Communication Co-Scheduling for Network-on-Chip based Multiprocessor System-on-Chip", *In Proc. of IEEE International Conference on Embedded and Real-Time Computing Systems and Applications* (RTCSA 2014). Chongqing, China. August, 2014.

Book Chapter

[35] **Lei Yang**, Weichen Liu, Weiwen Jiang, Mengquan Li, Jie Wang, "Isolation of Physical and Logical Views of Dark-Silicon Many-Core Systems for Reliability and Performance Co-Optimization", *Embedded System Technology*, Springer, 2016.