ECE342: Lab Submission Instruction

File Transfer, Sanity Check, Submit and Checking Marks

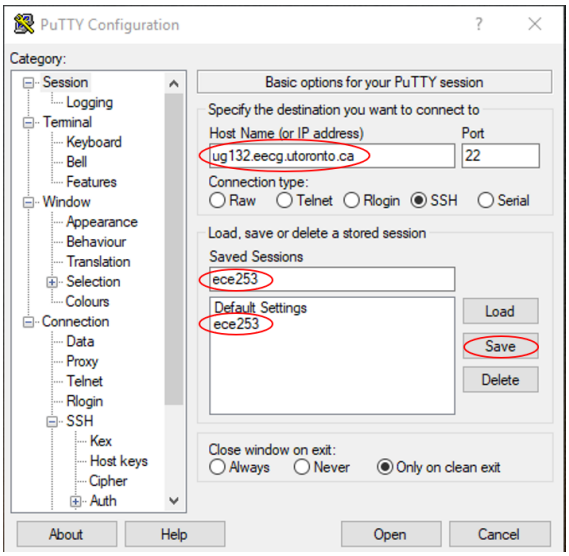
The goal of this document is to provide step-by-step instructions on how to submit the lab assignments for automarking in ECE342[1].

Prerequisite 1: UG Machine Login

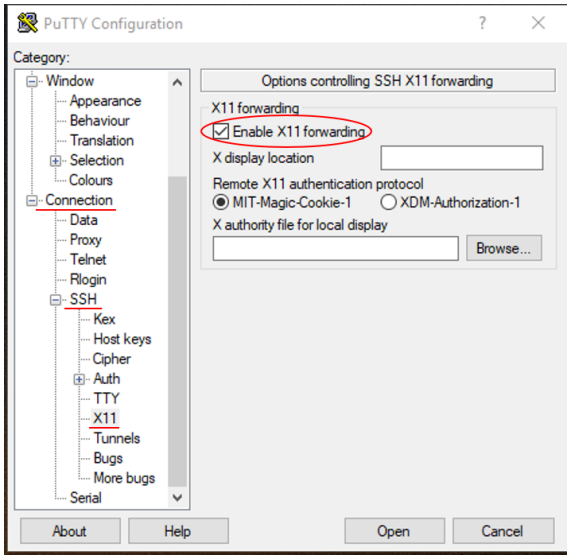
The UG machines are Linux-based machines located in the ECE Workstations Labs. The address of these machines range from `ug132.eecg.utoronto.ca - ug180.eecg.utoronto.ca`. You should make sure that you can log into your ECE account on these machines. You can use SSH to access the UG machines remotely.

Note: If this is the first time you are logging into these machines, your username is your UTORID and your default password is your student number. Once you log in (after following the instructions below), make sure to secure your account by changing your password with the `passwd` command.

For Windows users: You can install PuTTY, which is a an SSH client. The first time you open up PuTTY, you will have to configure your connection to a UG machine. Pick a machine from the range of `ug132 - ug180` and enter the address in the Host Name field (Figure 1a). You can save the configuration by giving it a name and pressing **Save**, and it should appear in your list of Saved Sessions. Double click on the saved session or click **Open** to initiate a connection. You may get a warning message saying the server's host key is not cached in the registry, click Yes. You can now enter your username and password to log into your account on this machine.



(a) PuTTY configuration.



(b) X11 forwarding.

Figure 1: PuTTY set up to connect to UG machines.

Optional: forward graphics. You may also want to install Xming if you want to remotely run graphical applications (e.g. ModelSim) remotely. You can update your PuTTY configuration to support graphical applications by doing the following (Figure 1b):

1. left click on your saved session and click `Load`

[1] This document is based on instructions created for ECE253 by Julie Hsiao.

2. go to `Connection` → `SSH` → `X11` and click `Enable X11 forwarding`
3. go back to `Session` and click `Save`

Make sure you have Xming running in the background and you can now open a connection on PuTTY that supports graphical applications.

For Mac users: Open the **Terminal** app and type: `ssh username@ug132.eecg.utoronto.ca`. Make sure to replace `username` with your actual username and change `ug132` to any machines between the range of `ug132 - ug180`. You may get a warning message saying the remote host identification has changed, type `yes`. You should now be able to enter you password and log into your account on the UG machine.

Optional: forward graphics. You may want to install XQuartz if you want to run graphical applications (e.g. ModelSim) remotely. To be able to run graphical applications remotely, you want to enable X11 forwarding when you connect to the UG machines. You can do this by adding the `-X` option when you connect: `ssh -X username@ug132.eecg.utoronto.ca`.

How to Submit Labs

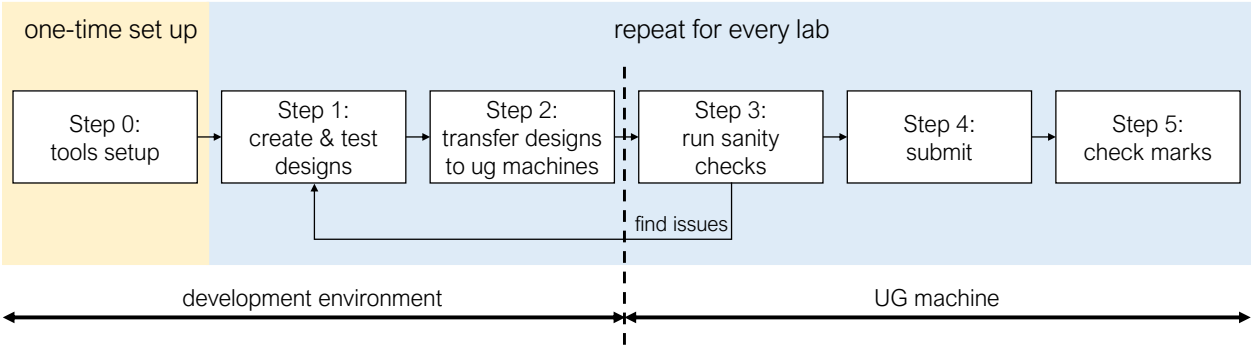


Figure 2: Process in completing each lab assignment.

Figure 2 shows a flow chart of the design cycle for completing each lab assignment. Here, the development environment refers to where you write, compile and simulate your design using ModelSim. The UG machine is where you need to send the designs to in order to submit your lab assignments. This document describes **Steps 2 to 5** in this design process. By the end of this document, you should know how to:

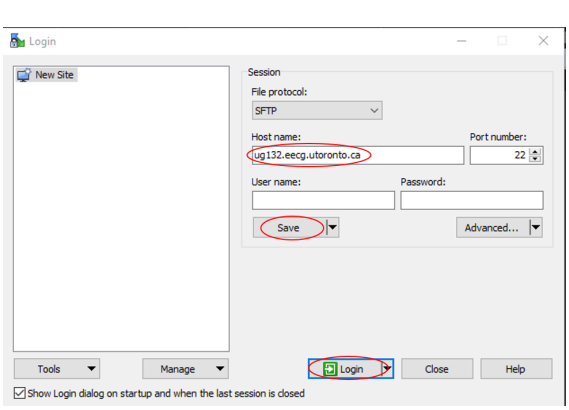
- transfer files between the UG machines and your development environment
- run a format check on your design
- submit your design for each lab
- check what files you have submitted for each lab
- check what tests you've passed/failed after receiving your grade

1 Transfer Designs to UG Machine

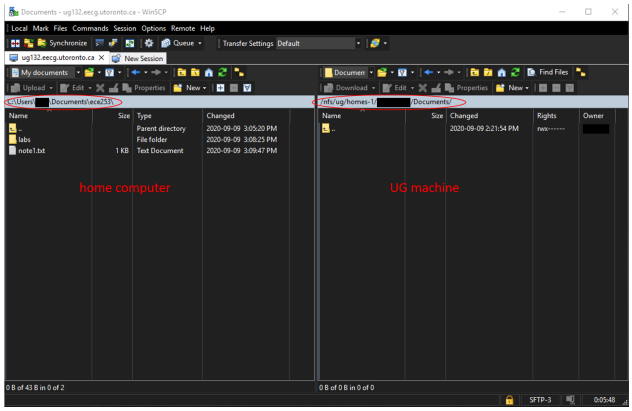
At this point in the design process, you should have completed and tested your designs and are ready to submit. In this document, we will use examples where you are submitting Verilog files. Depending on the lab, you may be required to submit files of different formats. The same submission procedure applies. If your development environment is on the UG machines themselves, you can ignore this and proceed to the next step.

For Windows users: You can install WinSCP, which is a an SCP/SFTP client. The first time you open up WinSCP, you will have to configure your connection to a UG machine. Pick a machine from the range of `ug132 - ug180` and enter the address in the **Host name** field (Figure 3a). You can save the configuration

so you don't have to type in the address every time by pressing **Save**. Click **Login** and you should be able to see the file system on the UG machines on the right panel, while the left panel is your home machine (Figure 3b). You should now be able to drag and drop files between the two panels to transfer files between your home computer and the UG machine.



(a) WinSCP configuration.



(b) WinSCP interface.

Figure 3: WinSCP set up to transfer files to and from UG machines.

For Mac users: You can use the `scp` command in the terminal to transfer files to and from the UG machines. The `scp` command is in the form: `scp /path/to/source/file /path/to/destination`. If any of the source or destination path is on a remote machine, the path should be prepended with `username@remote.machine.address:` (note the `:` at the end). For example, to transfer a file called `lab0.v` from the Documents directory on your Mac to the home directory on the UG machine, do the following:

1. Open the **Terminal** app
2. Navigate to the location of the file you want to transfer: `cd Documents`
3. Issue SCP command: `scp lab0.v teststudent@ug132.eecg.utoronto.ca:~`

Similarly, if you want to transfer a file called lab1.v from the UG machine's home directory back to your Mac, you can type: `scp teststudent@ug132.eecg.utoronto.ca:~/lab1.v ~/Documents`. Make sure you replace the `username` with your actual username and replace `ug132` with any of the machines between `ug132 - ug180`.

2 Run Sanity Check

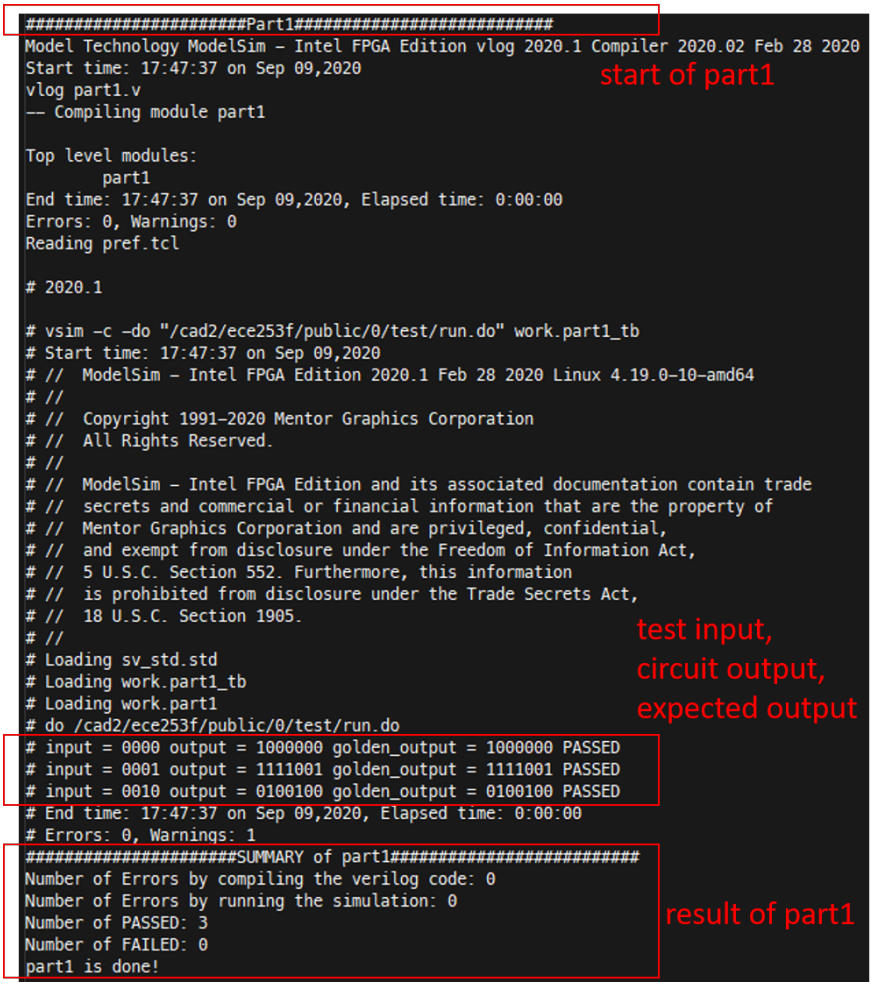
In this course, we provide you with a simple tester for each lab to make sure your design can be marked by the automarker. These testers serve as a sanity check to help you determine if all naming conventions have been followed. **Important: passing the sanity check does not mean you pass all test cases for the lab!** You need to come up with your own test cases (in Step 1 of Figure 2) to make sure your design works correctly under all inputs. The testers for each lab will be released as the semester goes on and will have the form: `/cad2/ece342s/public/<lab#>/tester`.

By this step, your Verilog design should have been transferred to the UG machine, and you are ready to run a sanity test on your design. Do the following to run the tester:

1. Connect to the UG machine via terminal (see Prerequisite 1: UG Machine Login if you forgot how to do this).
2. Navigate to the directory containing your designs.
3. Run the tester for that specific lab (e.g. `/cad2/ece342s/public/1/tester` for testing lab 1).

The tester may take some time to run, and you should see the terminal print out information on whether each part of your lab passed the sanity check. An example of what the output looks like is in Figure 4. As

a reminder, your files should be named `part1.sv`, `part2.sv`, etc. The automarker will not be able to mark your code if they are named incorrectly.




```
####################Part1#########################
Model Technology ModelSim - Intel FPGA Edition vlog 2020.1 Compiler 2020.02 Feb 28 2020
Start time: 17:47:37 on Sep 09,2020
vlog part1.v
-- Compiling module part1

Top level modules:
        part1
End time: 17:47:37 on Sep 09,2020, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
Reading pref.tcl

# 2020.1

# vsim -c -do "/cad2/ece253f/public/0/test/run.do" work.part1_tb
# Start time: 17:47:37 on Sep 09,2020
# //  ModelSim - Intel FPGA Edition 2020.1 Feb 28 2020 Linux 4.19.0-10-amd64
# //
# //  Copyright 1991-2020 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  ModelSim - Intel FPGA Edition and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading sv_std.std
# Loading work.part1_tb
# Loading work.part1
# do /cad2/ece253f/public/0/test/run.do
# input = 0000 output = 1000000 golden_output = 1000000 PASSED
# input = 0001 output = 1111001 golden_output = 1111001 PASSED
# input = 0010 output = 0100100 golden_output = 0100100 PASSED
# End time: 17:47:37 on Sep 09,2020, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
####################SUMMARY of part1#########################
Number of Errors by compiling the verilog code: 0
Number of Errors by running the simulation: 0
Number of PASSED: 3
Number of FAILED: 0
part1 is done!
```

Figure 4: Example of the tester output.

3 Submit

Once you have confirmed with the tester that your files can be marked by the automarker, you are ready to submit them. Naviage to the directory containing your files if you are not already there. The submit command follows this format:

`submitece342s <lab#> <part1 file name> [optional name to additional parts]`

This command allows you to submit one or more files for a specific lab. For example, the command to submit parts 1, 2 and 3 for lab 1 is: `submitece342s 1 part1.v part2.v part3.v` For each lab, submission will open when the lab is released. You can submit files at any time before the deadline, and you may re-submit files as many times as you want before the deadline. Only the most recent submitted file will be used for marking. Submission will close after the deadline and you will see an error message if you try to use the submit command for that lab.

You can list the files you've submitted for each lab by using the following:

`submitece342s -l <lab#>`

For example, after submitting parts 1 to 3 for lab 1, `submitece342s -l 1` will print `part1.v part2.v part3.v`. It is a good idea to use this command and double check that all the files you want to submit for a lab are submitted successfully.

4 Check Marks

After your lab has been graded, we will release a marker script that you can use to see where you lost marks. The marker operates very similar to the tester:

1. Connect to the UG machine via terminal.
2. Navigate to the directory containing your designs.
3. Run the marker for that specific lab (e.g. `/cad2/ece342s/public/1/marker` for testing lab 1).

The marker may take some time to run, and it outputs the result to the terminal.