CS1026 Hilary Term Lab 1

Aim: Design a circuit which acts as a logical XOR gate, using only NAND gates.

A good way to achieve gate minimisation is to use Boolean algebra on the desired function. The equation of an XOR gate is:

$$F = X'Y + Y'X$$

Which, substituting the two minterms for A and B and using De Morgan's theorem:

$$F = A + B$$

$$\Rightarrow F = (A' \cdot B')'$$

The above is the minimised equation, X'Y and Y'X NANDed(AND').

To verify, a truth table is used:

XY	$((X'Y)' \cdot (Y'X)')'$
00	0
01	1
10	1
11	0

With the knowledge that a NOT gate can be made by simply connecting the one input into both input ports of the NAND (see diagram), the gate minimised circuit diagram can now easily be drawn: