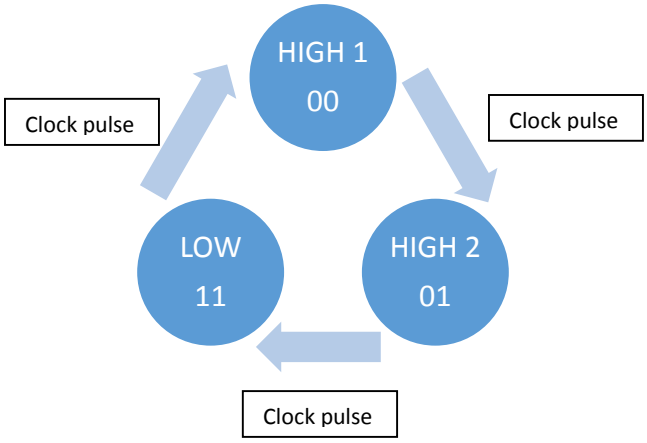
CS1026 Hilary Term Lab 7

Aim: To design a synchronous sequential circuit whose output is the system clock frequency divided by 3 (ie: the period is 3 times greater), using JK flip-flops.

(Note: we will assume a duty cycle of two thirds).

The first step in the procedure is to design a finite-state machine diagram, representing the behaviour of the circuit under a clock cycle.

The circuit will have an *output* which can take *2 values*: HIGH or LOW. However the circuit itself must have *3 states,* to which it changes on every rising edge of the clock cycle. The diagram below should clarify the need for 3 states:



One period of the clock cycle is equivalent to the time between pulses, therefore the above algorithm takes three times as long to cycle than the clock, so implementing this finite state machine will produce a circuit which outputs a signal of frequency CLK-freq/3.

The next step is to determine the Present State/Next State table of the machine.

Since there are 11_2 possible states, we need to use 2 flip flops (one for each bit).

The table is drawn below, where Q1, and Q2 are the states of the flip flops, the binary value Q1 Q2 represents the current state of the circuit, the JK values are the inputs to the respective flip flops, and Z is the circuit output:

Q1	Q2	$Q1^+$	$Q2^+$	J1	K1	J2	K2	Z
0	0	0	1	0	-	1	-	1
0	1	1	1	1	-	-	0	1
1	1	0	0	-	1	-	1	0
1	0	-	-	-	-	-	-	-

There are certain values we don't care about, which are marked as - . For example, when Q1 transitions from 0 to 1, it doesn't matter what value K1 takes, so long as J1 is 1 (because when the J input is 1, the JK flip flop either toggles (k = 1) or sets (k = 0), both of which result in Q = 1).

We don't care about the state 10 at all, as it is not a valid state in the machine.

Now that we have the present state next state table figured out, we can use it as a Karnaugh map to group our minterms (JK variables) together to obtain simplified Boolean expressions for the operation of the circuit at each clock pulse.

Q1	Q2	$Q1^+$	$Q2^+$	J1	K1	J2	K2	Z
0	0	0	1	0	-	1	-	1
0	1	1	1	1	-	-	0	1
1	1	0	0	-	1	-	1	0
1	0	-	-	-	-	-	-	-

This grouping gives us the following equations:

$$J1 = Q2$$

$$K1 = 1$$

$$J2 = 1$$

$$K2 = Q1$$

$$Z = Q1'$$

With the characteristic equations now determined, we can draw the circuit: