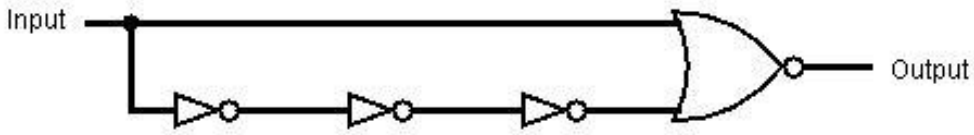
CS1026 Hilary Term Lab 6

1. Design a negatively edge triggered D flip-flop.

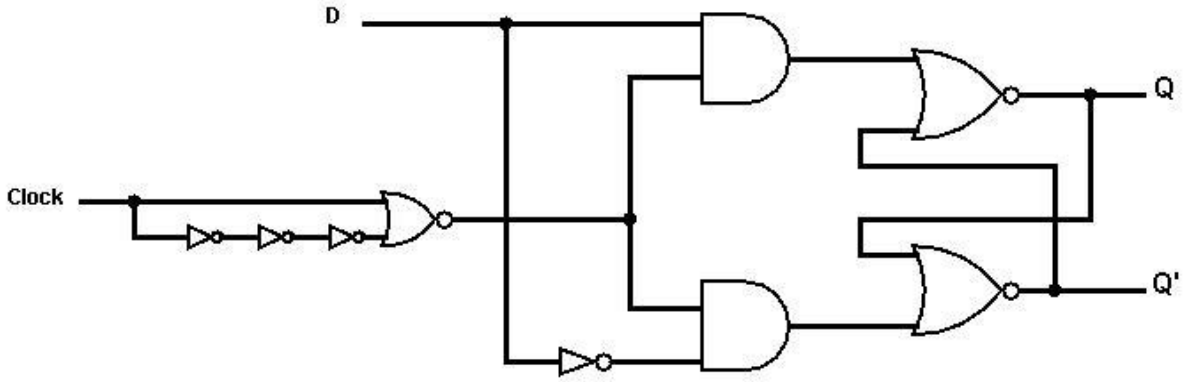
A D *"delay"* flip-flop is a bistable multivibrator, for which the value of the input D determines whether a *set* or *reset* operation is performed. However the ouput is only updated when a second input, the *Enable*, is high.

A negatively edge triggered D flip-flop uses a modified version of a clock signal as the Enable input, such that the enable is only high when said clock signal is transitioning from high to low.

This can be achieved by designing a circuit which will emit a short pulse only when its input is decreasing. We can implement this using the inherent delay of electronic components (transistors) in the following circuit:



The output is high only for the short period of time it takes for the effects of a high-low change to travel through the series of NOT gates. Attaching this to a periodic clock signal will give a pulse on the negative edge, and so we can design the required circuit:

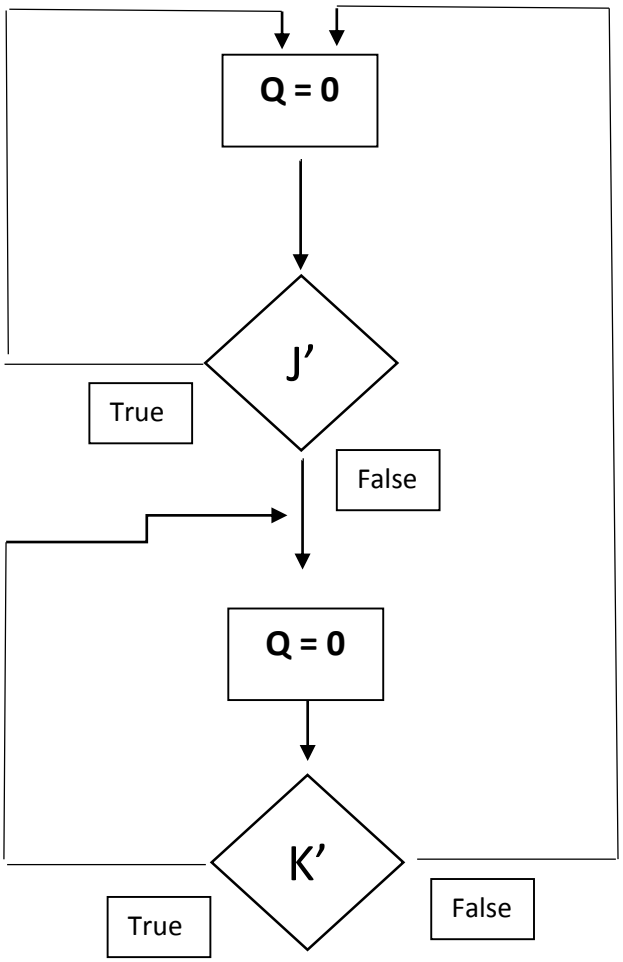


2. Give the PS/NS table for a JK flip-flop

J	K	Q	Q^+	Operation
0	0	0	*0*	*Hold*
0	0	1	*1*	*Hold*
0	1	0	*0*	*Reset*
0	1	1	*0*	*Reset*
1	0	0	*1*	*Set*
1	0	1	1	Set
1	1	0	1	Toggle
1	1	1	0	toggle

The JK flip-flop is practically an SR flip-flop modified so that there is no race condition (ie: when JK = 11 the circuit has a defined output).

3. Give the Algorithmic State Machine for the JK flip-flop.



J' = J'K' + J'K

ie: the output remains low while operation is hold, reset or not toggle. This becomes the **first condition** of the algorithm.

Otherwise, Q must be 1. The next state is then determined by:

K' = J'K' JK'

Ie: the output remains high while operation is hold, set or not toggle. This is the **second condition** of the algorithm.

With the two states and the two conditions of the circuit represented, the ASM is complete.