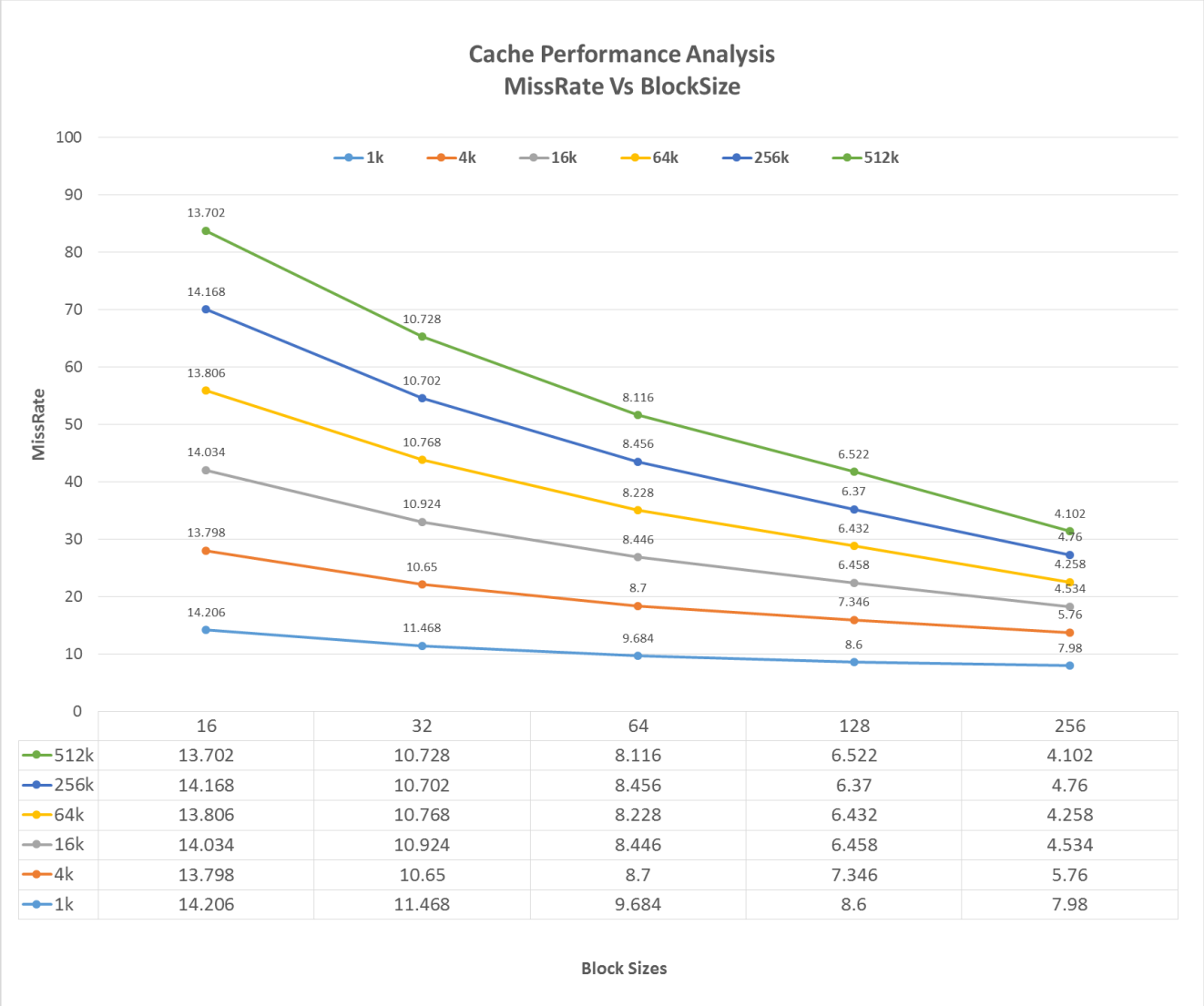
Cache Performance Analysis

CACHE PERFORMANCE ANALYSIS ON DIFFERENT BLOCK SIZES

Configuration 1a: Miss rate Vs Block size



	16	32	64	128	256
512k	13.702	10.728	8.116	6.522	4.102
256k	14.168	10.702	8.456	6.37	4.76
64k	13.806	10.768	8.228	6.432	4.258
16k	14.034	10.924	8.446	6.458	4.534
4k	13.798	10.65	8.7	7.346	5.76
1k	14.206	11.468	9.684	8.6	7.98

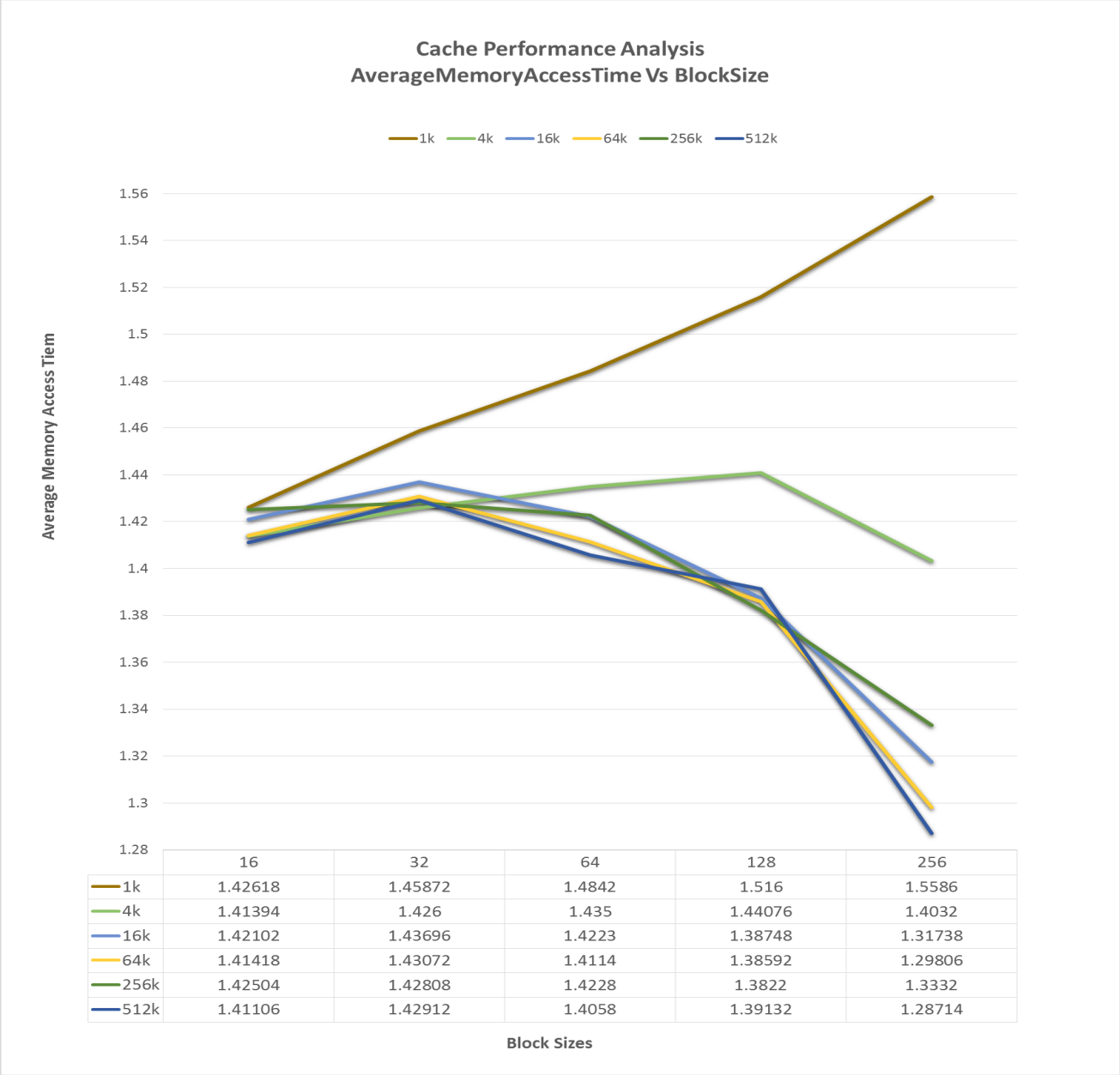
Figure 1 : Miss_Rate Vs Block_Size

In Figure 1 we present the variation in miss rates with increase in the block size for various cache sizes. For the above mentioned scenario associativity is assumed to be 1 way.

Observation:
As expected, the miss rate follows a convex pattern for all the applications with increasing block size. Smaller block size has higher miss rate. Large blocks have a lesser miss rate.

Conclusion:
1. To reduce the number of miss we should use larger block size.
2. Larger block size reduces number of compulsory misses.
3. Larger blocks take advantage of spatial locality.

Configuration 1b: Average Memory Access Time Vs Block size



	16	32	64	128	256
1k	1.42618	1.45872	1.4842	1.516	1.5586
4k	1.41394	1.426	1.435	1.44076	1.4032
16k	1.42102	1.43696	1.4223	1.38748	1.31738
64k	1.41418	1.43072	1.4114	1.38592	1.29806
256k	1.42504	1.42808	1.4228	1.3822	1.3332
512k	1.41106	1.42912	1.4058	1.39132	1.28714

Fig 2 : Average_Memory_Access_Time Vs Block_Size

In Figure 2 we present the variation in Average memory access time with increase in the block size for various cache sizes. For the above mentioned scenario associativity is assumed to be 1 way.

Observation:

1. With the increase in block size the memory access time increase for smaller cache.

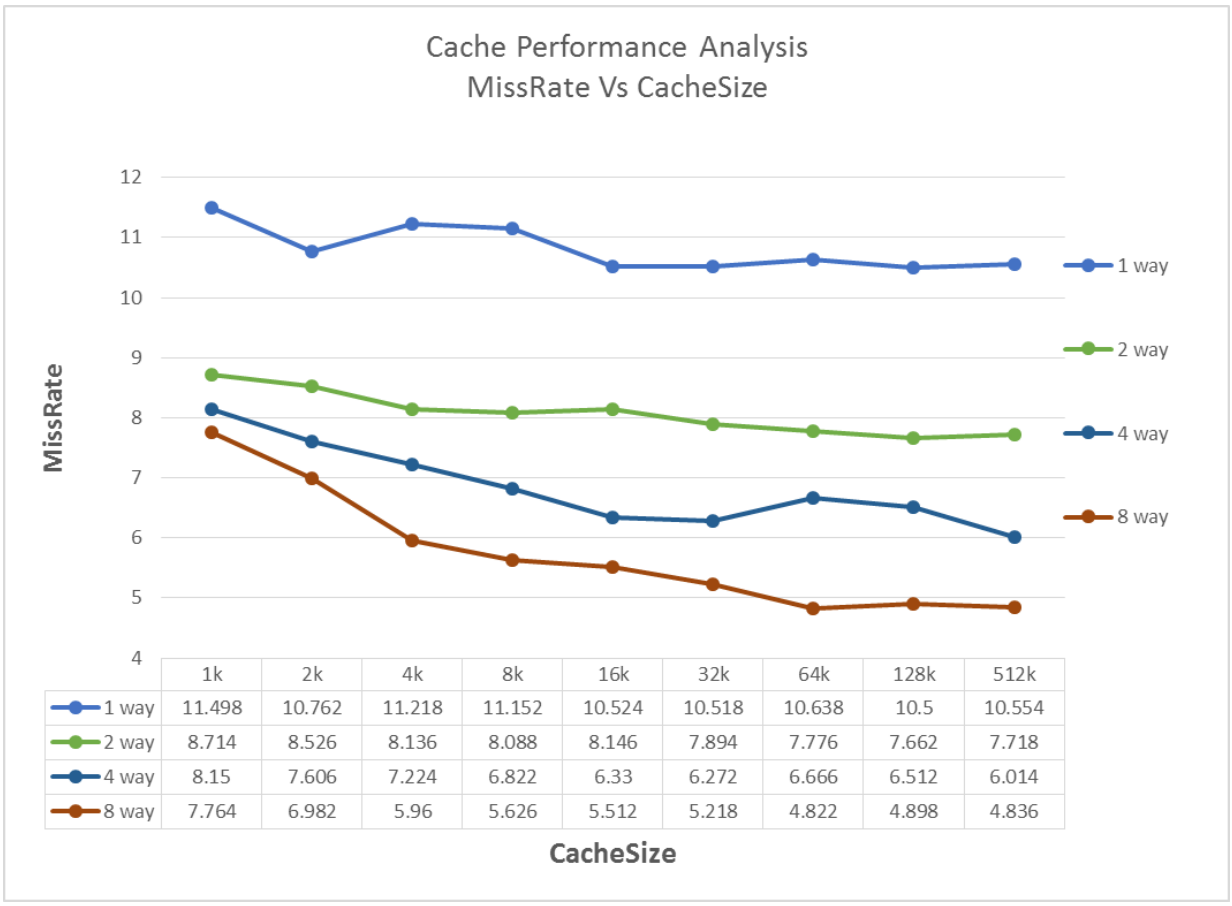
2. With the increase in block size the memory access time initially increases and after a threshold it starts to decrease for larger cache.

Conclusion:

1. Larger block size with smaller cache increase miss penalty.
    - Larger block size means that fewer blocks will be in cache this increases capacity misses and conflict misses.
2. To reduce average memory access time:
    - We should try to reduce miss rate.
    - Make cache bigger.

CACHE PERFORMANCE ANALYSIS ON DIFFERENT SET ASSOCIATIVITY

Configuration 2a: Miss Rate Vs Cache size



	1k	2k	4k	8k	16k	32k	64k	128k	512k
1 way	11.498	10.762	11.218	11.152	10.524	10.518	10.638	10.5	10.554
2 way	8.714	8.526	8.136	8.088	8.146	7.894	7.776	7.662	7.718
4 way	8.15	7.606	7.224	6.822	6.33	6.272	6.666	6.512	6.014
8 way	7.764	6.982	5.96	5.626	5.512	5.218	4.822	4.898	4.836

Fig 3 : Miss_Rate Vs Cache_Size

In Figure 3 we present the variation in Miss Rate with increase in the cache size for various set associativity. For the above mentioned scenario block size is assumed to be 32.

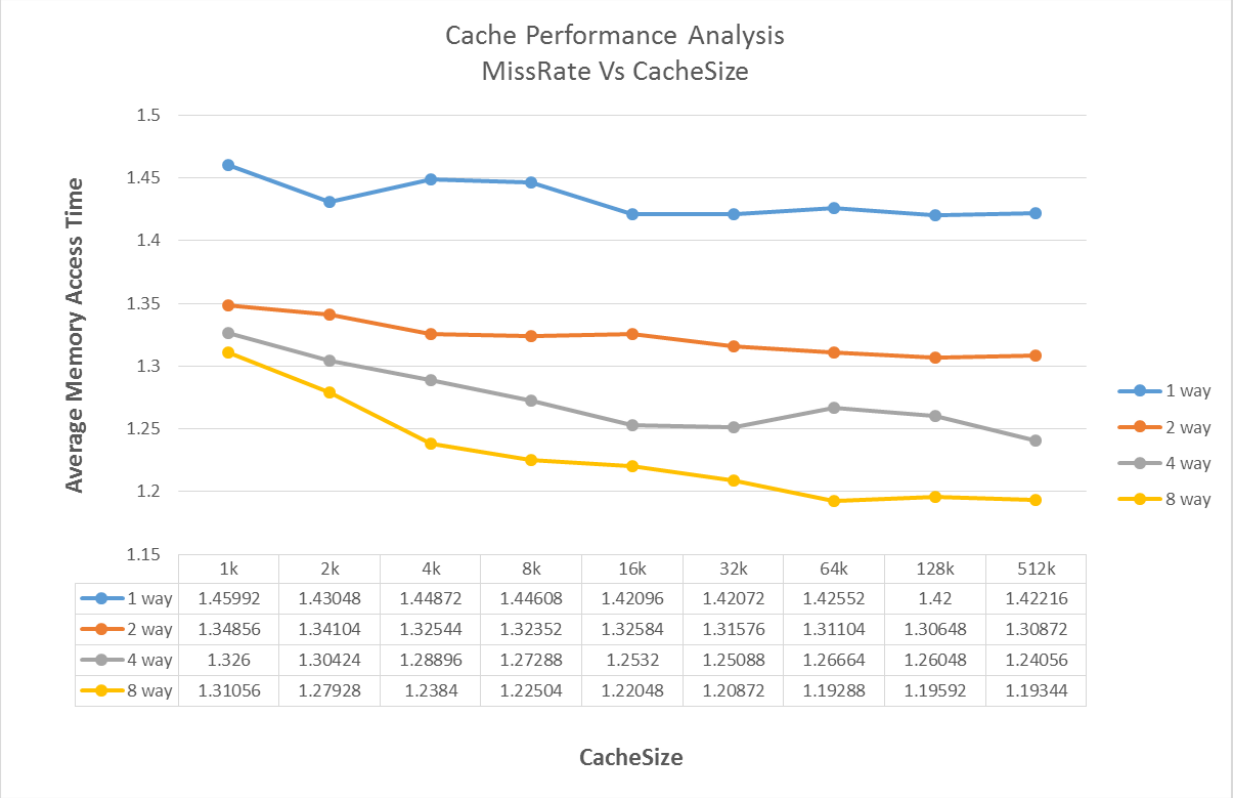
Observation:

1. 1k cache has almost the same miss rate as 512k cache for given associativity.

Conclusion:

1. Associativity is directly related to conflict misses. To reduce miss rate, associativity should be increased.

Configuration 2b: Average Memory Access Time Vs Cache size



	1k	2k	4k	8k	16k	32k	64k	128k	512k
1 way	1.45992	1.43048	1.44872	1.44608	1.42096	1.42072	1.42552	1.42	1.42216
2 way	1.34856	1.34104	1.32544	1.32352	1.32584	1.31576	1.31104	1.30648	1.30872
4 way	1.326	1.30424	1.28896	1.27288	1.2532	1.25088	1.26664	1.26048	1.24056
8 way	1.31056	1.27928	1.2384	1.22504	1.22048	1.20872	1.19288	1.19592	1.19344

Fig 4 : Average_Memory_Access_Time Vs Cache_Size

In Figure 4 we present the variation in Average memory access time with increase in the cache size for various set associativity. For the above mentioned scenario block size is assumed to be 32.

Observation:

1. With the increase in cache size the memory access time decreases slowly.
2. Increased associativity increase the probability that contiguous data is moved into the cache on a miss.
3. Increased number of associativity decrease the probability that a specific line is evicted.

Conclusion:

To reduce average memory access time:

1. We should try to reduce miss rate.
2. Make cache bigger.