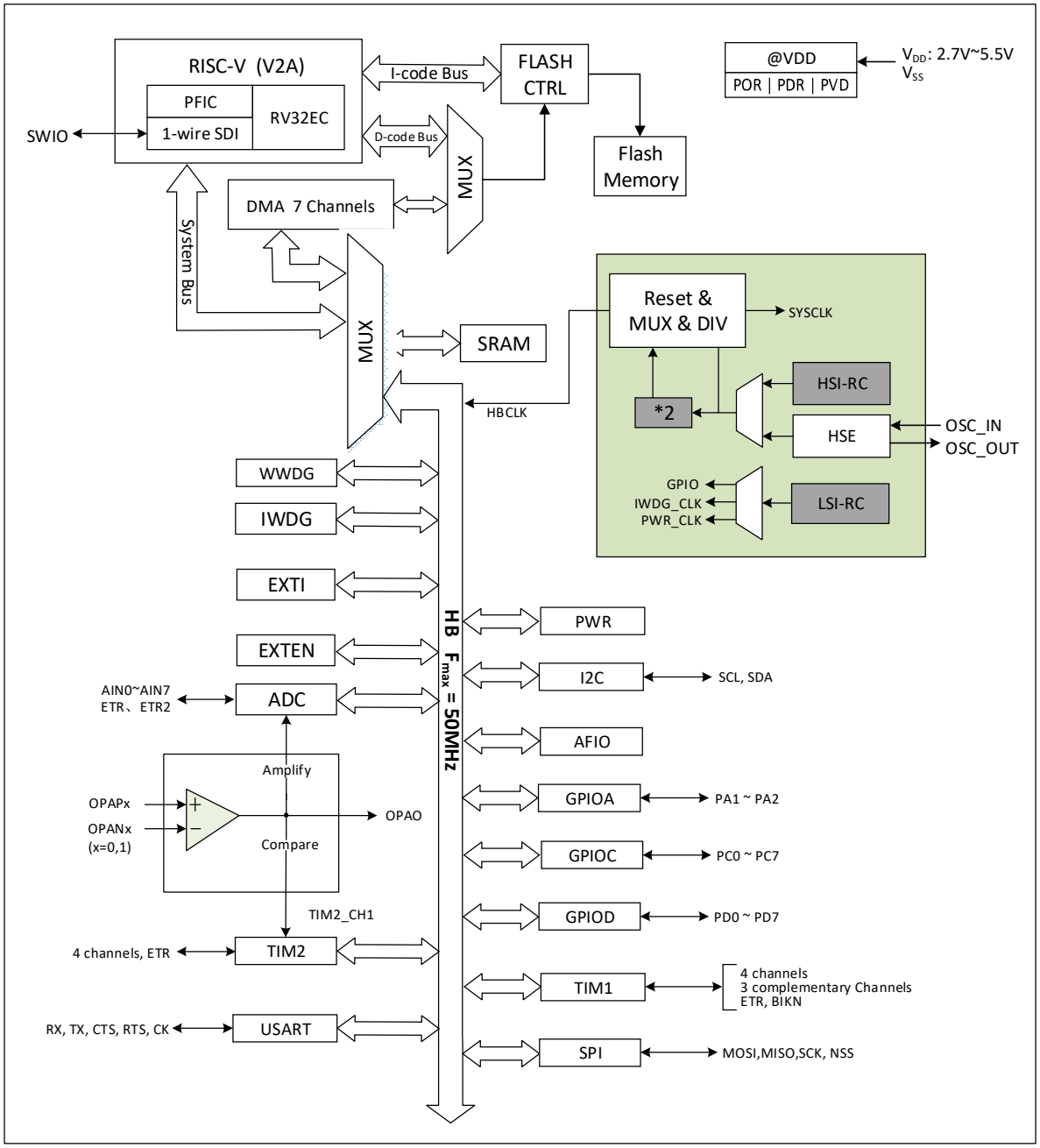
Chapter 1 Memory and Bus Architecture

1.1 Bus Architecture

The CH32V003 series is designed based on the RISC-V instruction set, and its architecture interacts the core, arbitration unit, DMA module, SRAM storage and other parts through multiple buses. The design integrates a general-purpose DMA controller to reduce the CPU load and improve access efficiency, as well as data protection mechanisms, automatic clock switching protection mechanisms and other measures to increase system stability. The system block diagram is shown in Figure 1-1.

Figure 1-1 CH32V003 system block diagram



The system is equipped with: General-purpose DMA controller to reduce the CPU burden and improve efficiency; clock tree hierarchy management to reduce the total power consumption of peripherals, as well as data protection mechanisms, clock security system protection mechanisms and other measures to increase system stability.

- The instruction bus (I-Code) connects the core to the FLASH instruction interface and prefetching is done

on this bus.

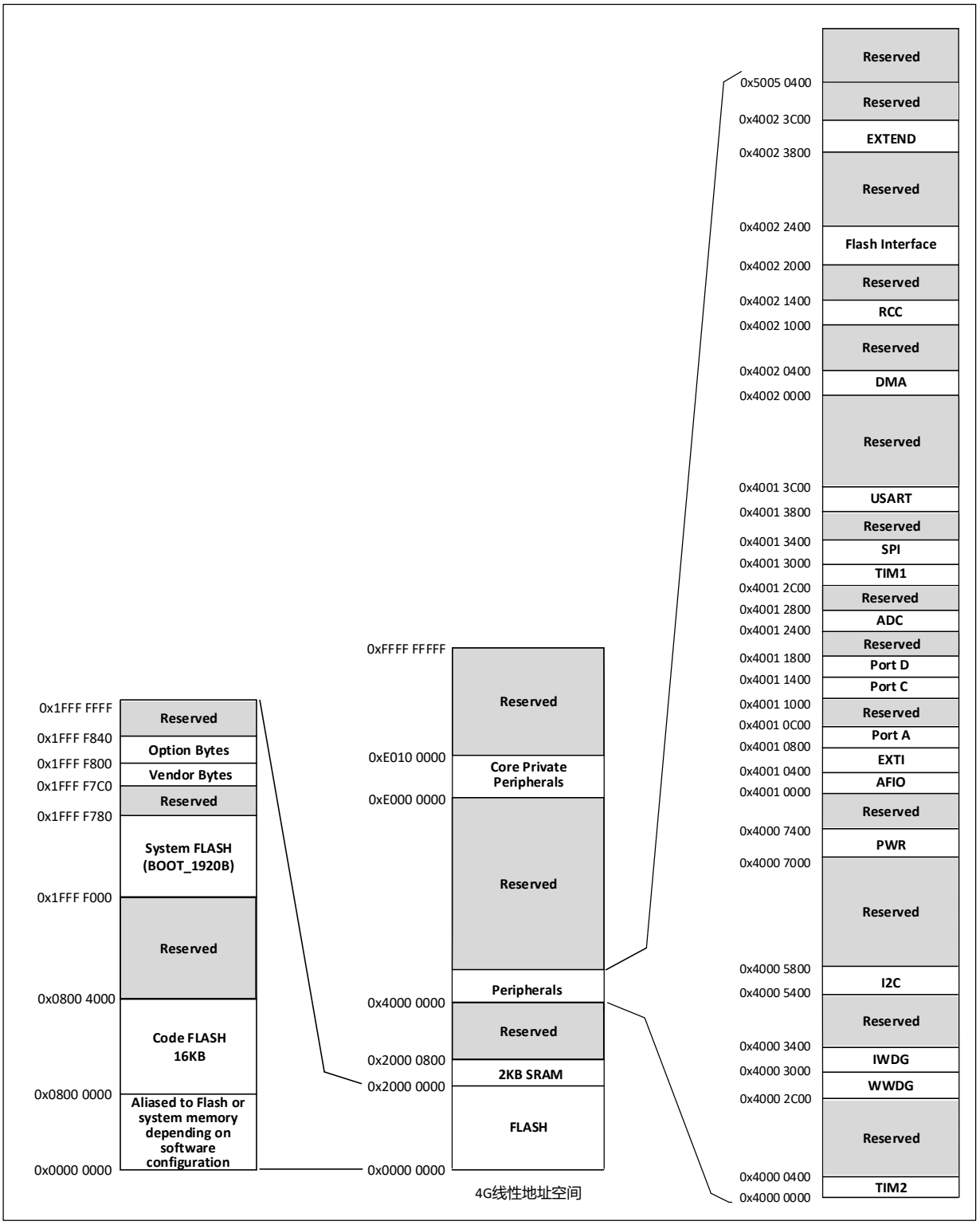
- The data bus (D-Code) connects the core to the FLASH data interface for constant loading and debugging.
- The system bus connects the core to the bus matrix and is used to coordinate accesses to the core, DMA, SRAM and peripherals.
- The DMA bus is responsible for the DMA of the HB master interface connected to the bus matrix, which is accessed by FLASH data, SRAM and peripherals.
- The bus matrix is responsible for the access coordination between the system bus, data bus, DMA bus, SRAM and HB bridge.

1.2 Memory Image

The CH32V003 family contains program memory, data memory, core registers, peripheral registers, and more, all addressed in a 4GB linear space.

System storage stores data in small-end format, i.e., low bytes are stored at the low address and high bytes are stored at the high address.

Figure 1-2 Storage image



1.2.1 Memory Allocation

Built-in 2KB SRAM, starting address 0x20000000, supports byte, half-word (2 bytes), and full-word (4 bytes) access.
Built-in 16KB program Flash memory (CodeFlash) for storing user applications.
Built-in 1920B System memory (bootloader) for storing the system bootloader (factory-cured bootloader).
Built-in 64B space for vendor configuration word storage, factory-cured and unmodifiable by users.
Built-in 64B space for user-option bytes storage.