Chapter 11 General-purpose Timer (GPTM)

The general-purpose timer module contains a 16-bit auto-reloadable timer, TIM2, for measuring pulse width or generating pulses of a specific frequency, PWM waves, etc. It can be used in automation control, power supply, etc.

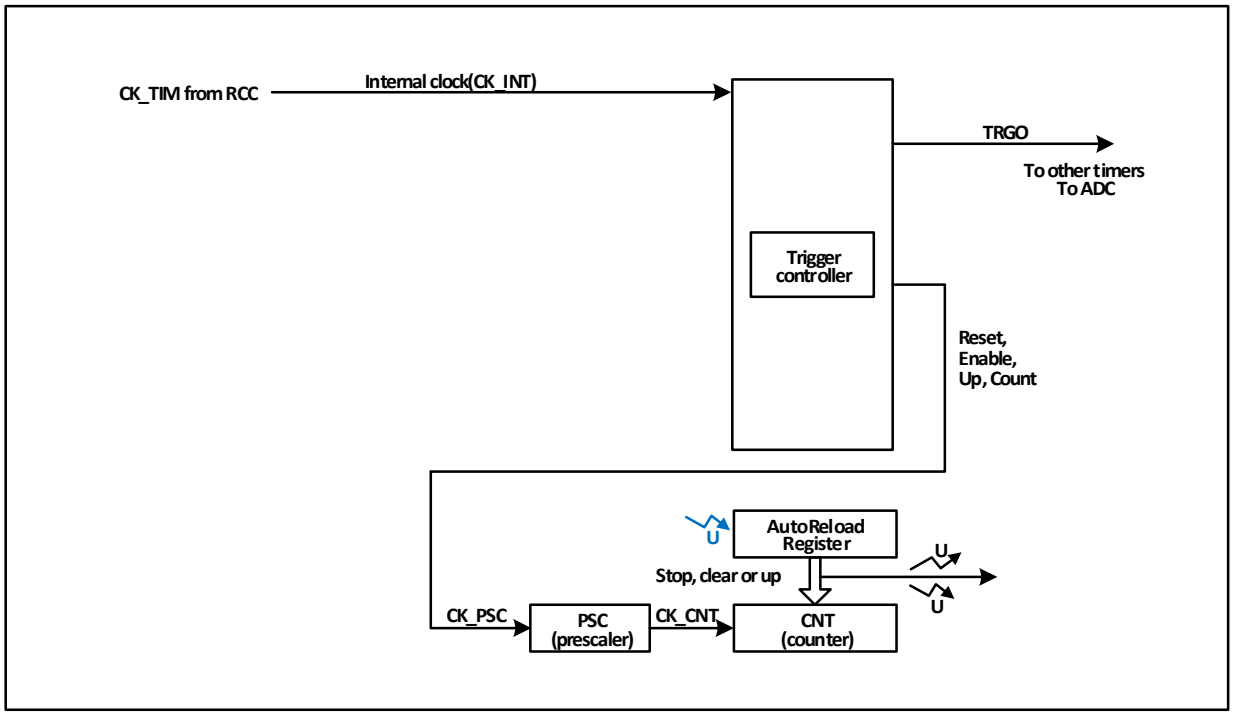
11.1 Main Features

The main features of the general-purpose timer include.

- 16-bit auto-reload counter, supports incremental counting mode, decremental counting mode and incremental and decremental counting mode
- 16-bit prescaler with dynamically adjustable crossover factor from 1 to 65536
- Support four independent comparison capture channels
- Each comparison capture channel supports multiple operating modes, such as: input capture, output comparison, PWM generation, and single pulse output
- Support external signal control timer
- Support DMA in multiple modes
- Support incremental coding, cascading and synchronization between timers

11.2 Principle and Structure

Figure 11-1 Block diagram of the structure of the general-purpose timer



11.2.1 Overview

As shown in Figure 11-1, the structure of the general-purpose timer can be roughly divided into three parts, namely the input clock part, the core counter part and the compare capture channel part.

The clock for the general-purpose timer can come from the HB bus clock (CK_INT), from the external clock input pin (TIMx_ETR), from other timers with clock output (ITRx), and from the input of the compare capture channel (TIMx_CHx). These input clock signals become CK_PSC clocks after various set filtering and

dividing operations, etc., and are output to the core counter section. In addition, these complex clock sources can also be output as TRGO to other peripherals such as timers and ADCs.

The core of the general-purpose timer is a 16-bit counter (CNT). cK_PSC is divided by a prescaler (PSC) to become cK_CNT and then finally fed to the CNT, which supports incremental counting mode, decremental counting mode, and incremental and decremental counting mode, and has an auto-reload register (ATRLR) to reload the initialization value for the CNT at the end of each counting cycle.

The general-purpose timer has four sets of compare capture channels, each of which can input pulses from exclusive pins or output waveforms to pins, i.e., the compare capture channels support both input and output modes. The input of each channel of the compare capture register supports filtering, dividing, edge detection, and other operations, and supports mutual triggering between channels, and can also provide clock for the core counter CNT. Each comparison capture channel has a set of comparison capture registers (CHxCVR) that support comparison with the main counter (CNT) to output pulses.

11.2.2 Difference between General-purpose Timer and Advanced-control Timer

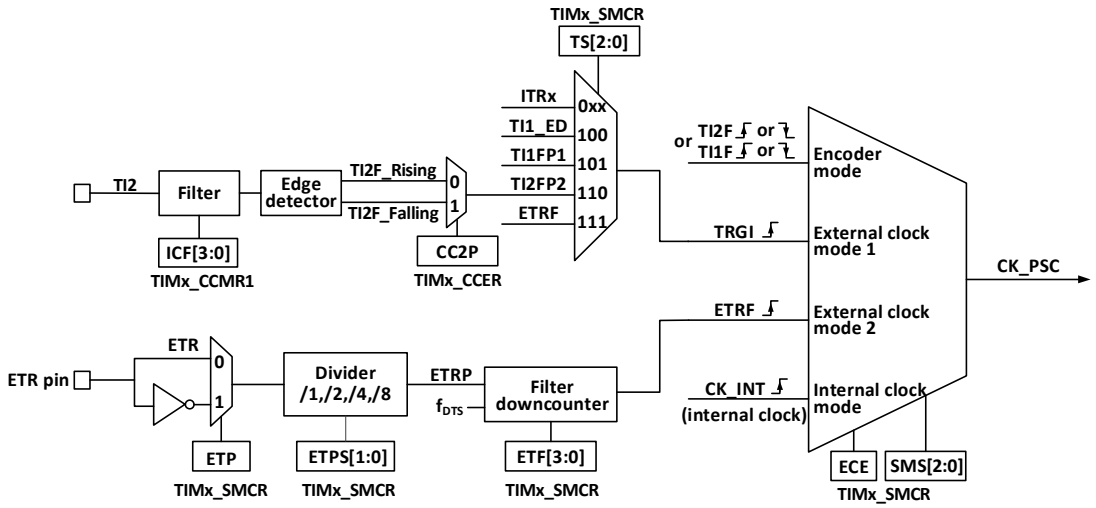
Compared to advanced-control timers, general purpose timers lack the following features.

1) The general-purpose timer lacks a repeat count register for counting the count cycles of the core counter.
2) The comparison capture channel of the general-purpose timer lacks deadband generation and has no complementary output.
3) The general-purpose timer does not have a brake signal mechanism.

11.2.3 Clock Input

This section discusses the source of CK_PSC. The clock source portion of the overall block diagram of the general-purpose timer is captured here.

Figure 11-2 General-Purpose Timer CK_PSC Source Block Diagram



The optional input clocks can be divided into 4 categories.

1) Route of the external clock pin (ETR) input: ETR → ETRP → ETRF.
2) Internal HB clock input route: CK_INT.
3) Route from the comparison capture channel pin (TIMx_CHx): TIMx_CHx → TIx → TIxFPx, this route is also used in encoder mode.
4) Input from other internal timers: ITRx.

The actual operation can be divided into 3 categories by determining the choice of input pulse for the SMS of the CK_PSC source.

1) Selection of the internal clock source (CK_INT).
2) External clock source mode 1.

3) External clock source mode 2.
4) Encoder mode.

All 4 clock source sources mentioned above can be selected by these 4 operations.

11.2.3.1 Internal Clock Source (CK_INT)

If the general-purpose timer is started when the SMS field is held at 000b, then it is the internal clock source (CK_INT) that is selected as the clock. At this point CK_INT is CK_PSC.

11.2.3.2 External Clock Source Mode 1

When the SMS domain is set to 111b, external clock source mode 1 is enabled. When external clock source 1 is enabled, TRGI is selected as the source for CK_PSC. it is worth noting that the user also needs to select the source for TRGI by configuring the TS domain. the TS domain can select the following types of pulses as clock sources.

1) Internal trigger (ITRx, x is 0,1,2,3).
2) Comparison of the signal after capturing channel 1 through the edge detector (TI1F_ED).
3) Comparison of signals TI1FP1, TI2FP2 of the capture channel.
4) The signal ETRF from the external clock pin input.

11.2.3.3 External Clock Source Mode 2

Use external trigger mode 2 to count on every rising or falling edge of the external clock pin input. When the ECE position is set, the external clock source mode 2 is used. when using the external clock source mode 2, ETRF is selected as CK_PSC. the ETR pin becomes ETRP after passing through the optional inverter (ETP), divider (ETPS), and then ETRF after passing through the filter (ETF).

With the ECE position bit and the SMS set to 111b, then it is equivalent to the TS selecting ETRF as the input.

11.2.3.4 Encoder Mode

Setting the SMS to 001b, 010b, 011b will enable the encoder mode. Enabling encoder mode allows you to select a specific level in TI1FP1 and TI2FP2 to signal the output with another jump edge as the signal. This mode is used when an external encoder is used. Refer to Section 11.3.7 for specific functions.

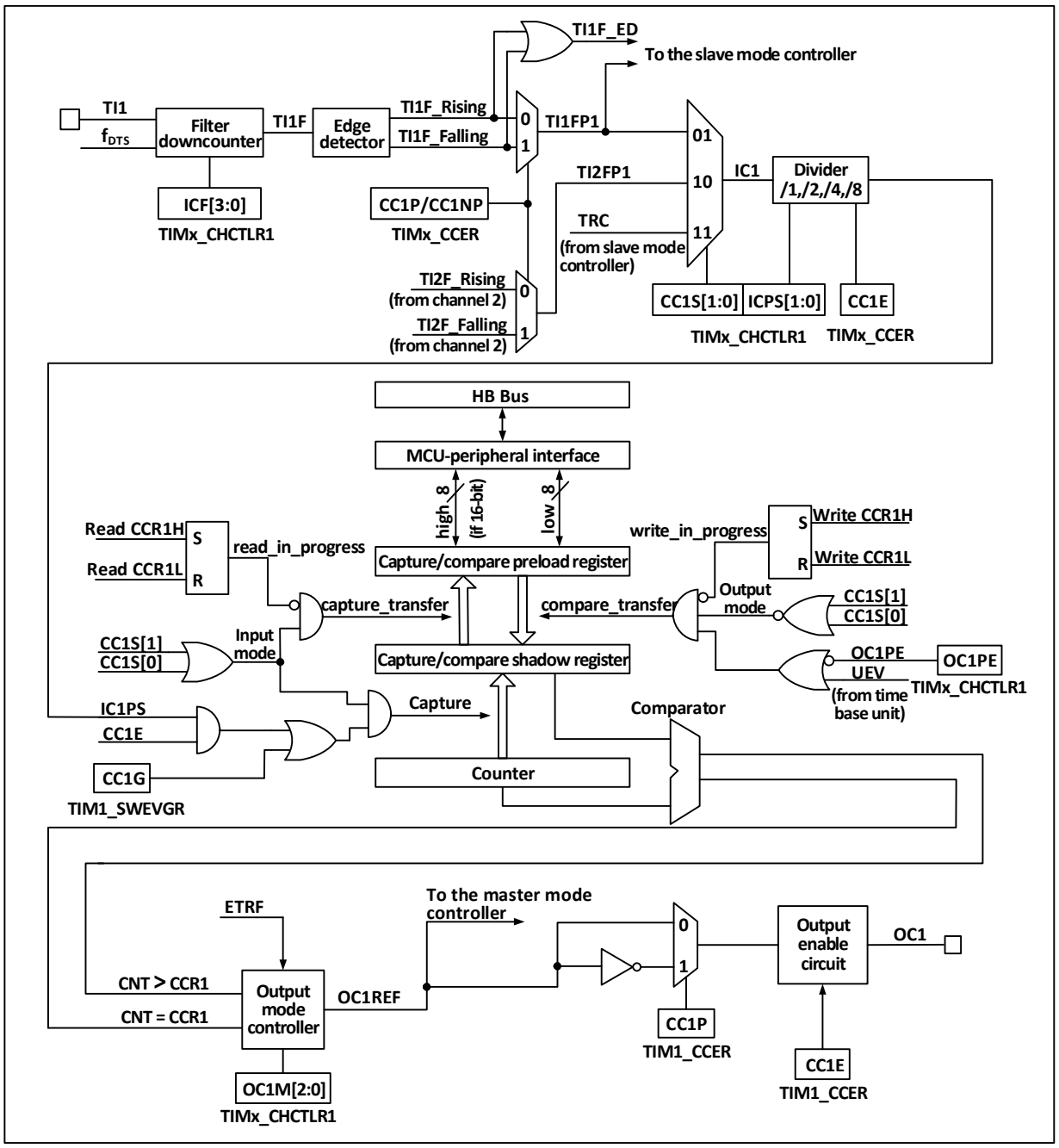
11.2.4 Counters and Peripherals

CK_PSC is input to the prescaler (PSC) for dividing. the PSC is 16-bit and the actual dividing factor is equal to the value of R16_TIMx_PSC + 1. CK_PSC goes through the PSC and becomes CK_INT. changing the value of R16_TIM1_PSC does not take effect in real time, but is updated to the PSC after an update event. the update event includes a UG bit clear and reset.

11.2.5 Compare/capture Channels

The core of the compare/capture channel, which is the core of the timer to achieve complex functions, is the compare/capture register, supplemented by digital filtering, frequency division and inter-channel multiplexing in the peripheral input section, and comparator and output control in the output section. The structure block diagram of the compare/capture channel is shown in Figure 11-3.

Figure 11-3 Block diagram of the structure of the comparison capture channel



The signal is input from the channel x pin and optionally made as TIx (the source of TI1 can be more than CH1, see block diagram 10-1 of the timer), TI1 is passed through the filter (ICF[3:0]) to generate TI1F, and then divided into TI1F_Rising and TI1F_Falling through the edge detector, these two signals are selected (CC1P) to generate TI1FP1, TI1FP1 and TI2FP1 from channel 2 are sent together to CC1S to select to become IC1, which is sent to the comparison capture register after ICPS dividing.

The compare capture register consists of a preload register and a shadow register, and the read/write process operates only on the preload register. In capture mode, the capture occurs on the shadow register and is then copied to the preload register; in compare mode, the contents of the preload register are copied to the shadow register, and then the contents of the shadow register are compared to the core counter (CNT).

11.3 Functionality and Implementation

The complex functions of a general-purpose timer are implemented by manipulating the timer's compare capture channel, clock input circuitry, and counter and peripheral components. The clock input to the timer can be derived from multiple clock sources including the input to the compare capture channel. The operation

of the compare capture host channel and clock source selection directly determines its function. The compare capture channel is bidirectional and can operate in both input and output modes.

11.3.1 Input Capture Mode

The input capture mode is one of the basic functions of the timer. The principle of input capture mode is that when a determined edge on the ICxPS signal is detected, a capture event is generated and the current value of the counter is latched into the compare capture register (R16_TIMx_CHCTLRx). The CCxIF (in R16_TIMx_INTFR) is set when a capture event occurs, and the corresponding interrupt or DMA is generated if enabled. If the CCxIF is already set when a capture event occurs, the CCxOF bit is set. the CCxIF can be cleared by software, or by hardware by reading the compare capture register. CCxOF is cleared by software.

An example of channel 1 to illustrate the steps to use the input capture mode is as follows.

1) Configure the CCxS domain to select the source of the ICx signal. For example, set it to 10b and select TI1FP1 as the source of IC1, not using the default setting, the CCxS domain defaults to making the comparison capture module the output channel.
2) Configure the ICxF domain to set the digital filter for the TI signal. The digital filter will sample the signal at a determined frequency, a determined number of times, and then output a hop. This sampling frequency and number of times is determined by ICxF.
3) Configure the CCxP bit to set the polarity of the TIxFPx. For example, keeping the CC1P bit low and selecting rising edge jumps.
4) Configure the ICxPS domain to set the ICx signal to be the crossover factor between ICxPS. For example, keeping ICxPS at 00b, without crossover.
5) Configure the CCxE bit to allow capturing the value of the core counter (CNT) into the compare capture register. Set the CC1E bit.
6) Configure the CCxIE and CCxDE bits as needed to determine whether to allow enable interrupts or DMA.

This completes the comparison capture channel configuration.

When a captured pulse is input to TI1, the value of the core counter (CNT) is recorded in the compare capture register, CC1IF is set, and the CCIOF bit is set when CC1IF has been set before. If the CC1IE bit is set, then an interrupt is generated; if CC1DE is set, a DMA request is generated. An input capture event can be generated by software by way of writing the event generation register (R16_TIMx_SWEVGR).

11.3.2 Compare Output Mode

The compare output mode is one of the basic functions of the timer. The principle of the compare output mode is to output a specific change or waveform when the value of the core counter (CNT) agrees with the value of the compare capture register. the OCxM field (in R16_TIMx_CHCTLRx) and the CCxP bit (in R16_TIMx_CCER) determine whether the output is a definite high or low level or a level flip. The CCxIF bit is also set when a compare coherent event is generated. If the CCxIE bit is pre-set, an interrupt will be generated; if the CCxDE bit is pre-set, a DMA request will be generated.

To configure to compare output modes, proceed as follows.

1) Configuring the clock source and auto-reload value of the core counter (CNT).
2) Set the count value to be compared to the comparison capture register (R16_TIMx_CHxCVR).
3) Set the CCxIE bit if an interrupt needs to be generated.
4) Keep OCxPE at 0 to disable the preload register for the compare capture register.
5) Setting the output mode, setting the OCxM field and the CCxP bit.
6) Enable the output, setting the CCxE bit.
7) Setting the CEN bit to start the timer.

11.3.3 Forced Output Mode

The output pattern of the timer's compare capture channel can be forced by software to output a determined level without relying on comparison of the compare capture register's shadow register with the core counter.

This is done by setting OCxM to 100b, which forces OCxREF to low, or by setting OCxM to 101b, which

forces OCxREF to high.

Note that by forcing OCxM to 100b or 101b, the comparison process between the internal main counter and the compare capture register is still going on, the corresponding flags are still set, and interrupts and DMA requests are still being generated.

11.3.4 PWM Input Mode

The PWM input mode is used to measure the duty cycle and frequency of PWM and is a special case of the input capture mode. The operation is the same as input capture mode except for the following differences: PWM occupies two compare capture channels and the input polarity of the two channels is set to opposite, one of the signals is set as trigger input and SMS is set to reset mode.

For example, to measure the period and frequency of the PWM wave input from TI1, the following operations are required.

1) Set TI1 (TI1FP1) to be the input of IC1 signal. Set CC1S to 01b.
2) Set TI1FP1 to rising edge active. Holding CC1P at 0.
3) Set TI1 (TI1FP2) as the input of IC2 signal. Set CC2S to 10b.
4) Select TI1FP2 to set to falling edge active. Set CC2P to 1.
5) Select TI1FP1 as the source of the clock source. set TS to 101b.
6) Set the SMS to reset mode, i.e. 100b.
7) Enables input capture. cc1e and cc2e are set.

11.3.5 PWM Output Mode

PWM output mode is one of the basic functions of the timer. PWM output mode is most commonly used to determine the PWM frequency using the reload value and the duty cycle using the capture comparison register. Set 110b or 111b in the OCxM field to use PWM mode 1 or mode 2, set the OCxPE bit to enable the preload register, and finally set the ARPE bit to enable the automatic reload of the preload register. The value of the preload register can only be sent to the shadow register when an update event occurs, so the UG bit needs to be set to initialize all registers before the core counter starts counting. In PWM mode, the core counter and the compare capture register are always comparing, and depending on the CMS bit, the timer is able to output edge-aligned or center-aligned PWM signals.

- Edge alignment

When using edge alignment, the core counter is incremented or decremented, and in the PWM mode 1 scenario, OCxREF rises to high when the core counter value is greater than the compare capture register; when the core counter value is less than the compare captureregister (for example, when the core counter grows to the value of R16_TIMx_ATRLR and reverts to full 0), OCxREF falls to low.

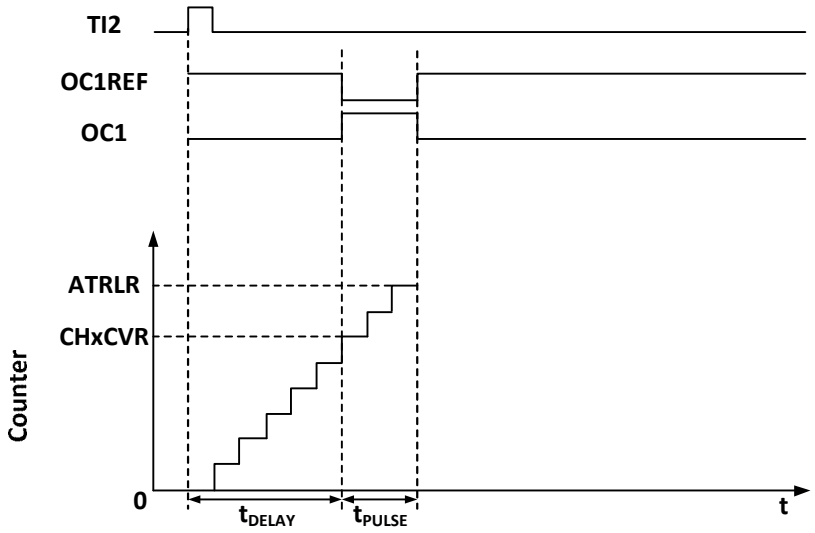
- Central alignment

When using the central alignment modes, the core counter runs in alternating incremental and decremental count modes, and OCxREF performs rising and falling jumps when the values of the core counter and the compare capture register match. However, the comparison flags are set at different times in the three central alignment modes. When using the central alignment modes, it is best to generate a software update flag (set the UG bit) before starting the core counter.

11.3.6 Single Pulse Mode

The single pulse mode can respond to a specific event by generating a pulse after a delay, with programmable delay and pulse width. Setting the OPM bit stops the core counter when the next update event UEV is generated (counter flips to 0).

Figure 11-4 Event generation and impulse response



As shown in Figure 11-4, a positive pulse of length Tpulse needs to be generated on OC1 after a delay Tdelay at the beginning of a rising edge detected on the TI2 input pin.

1) Set TI2 to trigger. Setting the CC2S field to 01b to map TI2FP2 to TI2; setting the CC2P bit to 0b to set TI2FP2 as rising edge detection; setting the TS field to 110b to set TI2FP2 as trigger source; setting the SMS field to 110b to set TI2FP2 to be used to start the counter.
2) Tdelay is defined by the Compare Capture Register and Tpulse is determined by the value of the Auto Reload Value Register and the Compare Capture Register.

11.3.7 Encoder Mode

The encoder mode is a typical application of the timer and can be used to access the biphasic output of the encoder. The counting direction of the core counter is synchronized with the direction of the encoder's rotation axis, and each pulse output from the encoderwill add or subtract one from the core counter. To use the encoder, set the SMS field to 001b (count only on TI2 edge), 010b (count only on TI1 edge) or 011b (count on both TI1 and TI2 edges), connect the encoder to the input of the comparison capture channels 1 and 2, and set a reload value counter value, which can be set to a larger value. When in encoder mode, the internal compare capture register, prescaler, repeat count register, etc. of the timer are working normally. The following table shows the relationship between the counting direction and the encoder signal.

Table 11-1 Relationship between counting direction and encoder signal of timer encoder mode

Counting effective edges	The level of relative signals	TI1FP1 signal edge		TI2FP2 signal edge	
		Rising edge	Falling edge	Rising edge	Falling edge
Counting at TI1 edge only	High	Downward counting	Upward counting	No count	
	Low	Upward counting	Downward counting		
Counting at TI2 edge only	High	No count		Upward counting	Downward counting
	Low			Downward counting	Upward counting
Double edge counting at TI1 and TI2	High	Downward counting	Upward counting	Upward counting	Downward counting
	Low	Upward counting	Downward counting	Downward counting	Upward counting

11.3.8 Timer Synchronization Mode

Timers are capable of outputting clock pulses (TRGO) and also receiving inputs from other timers (ITRx). The source of ITRx (TRGO from other timers) is different for different timers. The timer internal trigger connections are shown in Table 11-2.

Table 11-2 GTPM internal trigger connection

From timer	ITR0(TS=000)	ITR1(TS=001)	ITR2(TS=010)	ITR3(TS=011)
TIM2	TIM1			
TIM1		TIM2		

11.3.9 Debug Mode

When the system enters the debug mode, the timer can be controlled to continue running or stop according to the setting of DBG module.

11.4 Register Description

Table 11-3 TIM2-related registers list

Name	Offset address	Description	Reset value
R16_TIM2_CTLR1	0x40000000	TIM2 control register1	0x0000
R16_TIM2_CTLR2	0x40000004	TIM2 control register2	0x0000
R16_TIM2_SMCFGR	0x40000008	TIM2 Slave mode control register	0x0000
R16_TIM2_DMAINTENR	0x4000000C	TIM2 DMA/interrupt enable register	0x0000
R16_TIM2_INTFR	0x40000010	TIM2 interrupt status register	0x0000
R16_TIM2_SWEVGR	0x40000014	TIM2 event generation register	0x0000
R16_TIM2_CHCTLR1	0x40000018	TIM2 compare/capture control register1	0x0000
R16_TIM2_CHCTLR2	0x4000001C	TIM2 compare/capture control register2	0x0000
R16_TIM2_CCER	0x40000020	TIM2 compare/capture enable register	0x0000
R16_TIM2_CNT	0x40000024	TIM2 counter	0x0000
R16_TIM2_PSC	0x40000028	TIM2 count clock prescaler	0x0000
R16_TIM2_ATRLR	0x4000002C	TIM2 auto-reload register	0xFFFF
R32_TIM2_CH1CVR	0x40000034	TIM2 compare/capture register1	0x00000000
R32_TIM2_CH2CVR	0x40000038	TIM2 compare/capture register2	0x00000000
R32_TIM2_CH3CVR	0x4000003C	TIM2 compare/capture register3	0x00000000
R32_TIM2_CH4CVR	0x40000040	TIM2 compare/capture register4	0x00000000
R16_TIM2_DMACFGR	0x40000048	TIM2 DMA control register	0x0000
R16_TIM2_DMAADR	0x4000004C	TIM2 DMA address register in continuous mode	0x0000

11.4.1 Control Register 1 (TIM2_CTLR1)

Offset address: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPLVL	CAPOV	Reserved				CKD[1:0]		ARPE	CMS[1:0]		DIR	OPM	URS	UDIS	CEN

Bit	Name	Access	Description	Reset value
15	CAPLVL	RW	In double-edge capture mode, the capture level indication is enabled. 0: Turn off the indication function 1: Enables the indication function. *Note: When enabled, [16] of CHxCVR indicates the*	0

			level corresponding to the capture value.	
14	CAPOV	RW	Capture value mode configuration. 0: The capture value is the actual counter value 1: The CHxCVR value is 0xFFFF when a counter overflow is generated before capture.	0
[13:10]	Reserved	RO	Reserved	0
[9:8]	CKD[1:0]	RW	These 2 bits define the division ratio between the timer clock (CK_INT) frequency, the sampling clock used by the digital filter. 00: Tdts=Tck_int; 01: Tdts= 2xTck_int; 10: Tdts= 4xTck_int; 11：Reserved.	0
7	ARPE	RW	Auto-reload preload enable bit. 1: Enables the Auto-reload value register (ATRLR). 0: Auto-reload value register (ATRLR) is disabled.	0
[6:5]	CMS[1:0]	RW	Central alignment mode selection. 00: Edge-aligned mode. The counter counts up or down based on the direction bit (DIR). 01: Central alignment mode 1. The counter counts up and down alternately. The output compare interrupt flag bit of the channel configured as output (CCxS=00 in the CHCTLRx register) is set only when the counter counts down. 10: Central alignment mode 2. The counter counts up and down alternately. The output compare interrupt flag bit of the channel configured as output (CCxS=00 in the CHCTLRx register) is set only when the counter counts up. 11: Central alignment mode 3. The counter counts up and down alternately. The output compare interrupt flag bit of the channel configured as output (CCxS=00 in the CHCTLRx register) is set when the counter counts both up and down. *Note: When the counter is enabled (CEN=1), the transition from edge-aligned mode to center-aligned mode is not allowed.*	0
4	DIR	RW	Counting direction. 0: the counter's counting mode is incremental. 1: The counting mode of the counter is decimal counting. *Note: This bit is not valid when the counter is configured in central alignment mode or encoder mode.*	0
3	OPM	RW	Single pulse mode. 1: The counter stops (clearing the CEN bit) when the next update event occurs. 0: The counter does not stop when the next update event occurs.	0
2	URS	RW	Update request source, by which the software selects the source of the UEV event. 1: if an update interrupt or DMA request is enabled, only an update interrupt or DMA request is generated if the counter overflows/underflows. 0: If an update interrupt or DMA request is enabled, the update interrupt or DMA request is generated by any of the following events. -Counter overflow/underflow -Setting the UG position -Updates generated from the mode controller	0

1	UDIS	RW	Disable updates, the software allows/disables the generation of UEV events via this bit. 1: UEV is disabled. no update event is generated and the registers (ATRLR, PSC, CHCTLRx) maintain their values. If the UG bitis set or a hardware reset is issued from the mode controller, the counter and prescaler are reinitialized. 0: UEV is allowed. update (UEV) events are generated by any of the following events: - Counter overflow/underflow -Setting the UG position -Updates generated from the mode controller registers with caches are loaded with their preloaded values.	0
0	CEN	RW	Enable the counter (Counter enable). 1: Enables the counter. 0: Disable the counter. *Note: The external clock, gated mode and encoder mode will not work until the CEN bit is set in software. Trigger mode can automatically set the CEN bit in hardware.*	0

11.4.2 Control Register 2 (TIM2_CTLR2)

Offset address: 0x04

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TI1S	MMS[2:0]			CCDS	Reserved		

Bit	Name	Access	Description	Reset value
[15:8]	Reserved	RO	Reserved	0
7	TI1S	RW	TI1 selection. 1: TIMx_CH1, TIMx_CH2 and TIMx_CH3 pins connected to TI1 input after heterodyning. 0: TIMx_CH1 pin is connected directly to TI1 input.	0
[6:4]	MMS[2:0]	RW	Master mode selection: These 3 bits are used to select the synchronization information (TRGO) sent to the slave timer in master mode. The possible combinations are as follows. 000: The Reset-UG bit is used as a trigger output (TRGO). If the reset is generated by a trigger input (from a mode controller in reset mode), there is a delay in the signal on TRGO relative to the actual reset. 001: Enable - The counter enable signal CNT_EN is used as a trigger output (TRGO). Sometimes it is necessary to start multiple timers at the same time or to control the enable from timers over a period of time. The counter enable signal is generated by the logical or of the trigger input signal in CEN control bit and gated mode. When the counter enable signal is controlled by a trigger input, there is a delay on TRGO unless master/slave mode is selected (see the description of the MSM bit in the TIMx_SMCFGR register). 010: The update event is selected as a trigger input (TRGO). For example, the clock of a master timer may be used as a prescaler for a slave timer. 011: comparison pulse that triggers the output to send a positive pulse (TRGO) when a capture or a successful comparison occurs, when the CC1IF flag is to be set	0

			(even if itis already high). 100: The OC1REF signal is used as a trigger output (TRGO. 101: The OC2REF signal is used as a trigger output (TRGO). 110: The OC3REF signal is used as a trigger output (TRGO). 111: The OC4REF signal is used as a trigger output (TRGO).	
3	CCDS	RW	1: Sending a DMA request for CHxCVR when an update event occurs. 0: Generate a DMA request for CHxCVR when CHxCVR occurs.	0
[2:0]	Reserved	RO	Reserved	0

11.4.3 Slave Mode Control Register (TIM2_SMCFGR)

Offset address: 0x08

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETP	ECE	ETPS[1:0]		ETF[3:0]				MSM	TS[2:0]			Reserved	SMS[2:0]		

Bit	Name	Access	Description	Reset value
15	ETP	RO	ETR trigger polarity selection, this bit selects whether to input ETR directly or to input the inverse of ETR. 1: Invert ETR, active low or falling edge. 0: ETR, active high or rising edge.	0
14	ECE	RW	External clock mode 2 enabled selection. 1: Enables external clock mode 2. 0: Disable external clock mode 2. *Note 1: Slave mode can be used simultaneously with external clock mode 2: reset mode, gated mode and trigger mode; however, TRGI cannot be connected to ETRF in this case (TS bit cannot be 111b).* *Note 2: When both external clock mode 1 and external clock mode 2 are enabled, the external clock input is ETRF.*	0
[13:12]	ETPS[1:0]	RW	The external trigger signal (ETRP) is divided into frequencies, and the maximum frequency of this signal cannot exceed 1/4 of the TIMxCLK frequency, which can be downconverted by this domain. 00: Prescaler off. 01: ETRP frequency divided by 2. 10: ETRP frequency divided by 4. 11: ETRP frequency divided by 8.	0
[11:8]	ETF[3:0]	RW	Externally triggered filtering, in fact, the digital filter is an event counter that uses a certain sampling frequency to generate a jump in the output after N events are recorded. 0000: no filter, sampled in Fdts. 0001: sampling frequency Fsampling=Fck_int,N=2. 0010: sampling frequency Fsampling=Fck_int, N=4. 0011: Sampling frequency Fsampling=Fck_int, N=8. 0100: sampling frequency Fsampling = Fdts/2, N = 6. 0101: sampling frequency Fsampling = Fdts/2, N = 8. 0110: sampling frequency Fsampling = Fdts/4, N = 6. 0111: sampling frequency Fsampling = Fdts/4, N = 8. 1000: sampling frequency Fsampling = Fdts/8, N = 6.	0

			1001: sampling frequency Fsampling = Fdts/8, N = 8. 1010: sampling frequency Fsampling = Fdts/16, N = 5. 1011: sampling frequency Fsampling = Fdts/16, N = 6. 1100: sampling frequency Fsampling = Fdts/16, N = 8. 1101: sampling frequency Fsampling = Fdts/32, N = 5. 1110: sampling frequency Fsampling = Fdts/32, N = 6. 1111: Sampling frequency Fsampling=Fdts/32, N=8.	
7	MSM	RW	Master/slave mode selection. 1: The event on the trigger input (TRGI) isdelayed to allow perfect synchronization between the current timer (via TRGO) and its slave timer. This is useful when the synchronization of several timers to a single external event is required. 0: Does not function.	0
[6:4]	TS[2:0]	RW	Trigger select field, these 3 bits select the trigger input source used to synchronize the counter. 000: Internal trigger 0 (ITR0). 001: Internal trigger 1 (ITR1). 010: Internal trigger 2 (ITR2). 011: Internal trigger 3 (ITR3). 100: Edge detector of TI1 (TI1F_ED). 101: Filtered timer input 1 (TI1FP1). 110: Filtered timer input 2 (TI2FP2). 111: External trigger input (ETRF). The above only changes when SMS is 0.	0
3	Reserved	RO	Reserved	0
[2:0]	SMS[2:0]	RW	Input mode selection field. Selects the clock and trigger mode of the core counter. 000: driven by the internal clock CK_INT. 001: encoder mode 1, where the core counter increments or decrements the count at the edge of TI2FP2 depending on the level of TI1FP1. 010: encoder mode 2, where the core counter increments or decrements the count at the edge of TI1FP1, depending on the level of TI2FP2. 011: encoder mode 3, where the core counter increments and decrements the count on the edges of TI1FP1 and TI2FP2 depending on the input level of another signal; 100: reset mode, where the rising edge of the trigger input (TRGI) will initialize the counter and generate a signal to update the registers. 101: Gated mode, when the trigger input (TRGI) is high, the counter clock is turned on; at the trigger input becomes low, the counter is stopped, and the counter starts and stops are controlled. 110: Trigger mode, where the counter is started on the rising edge of the trigger input TRGI and only the start of the counter is controlled. 111: External clock mode 1, rising edge of the selected trigger input (TRGI) drives the counter.	0

11.4.4 TIM2 DMA/Interrupt Enable Register (TIM2_DMAINTENR)

Offset address: 0x0C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	TDE	Reserved	CC4DE	CC3DE	CC2DE	CC1DE	UDE	Reserved	TIE	Reserved	CC4IE	CC3IE	CC2IE	CC1IE	UIE

Bit	Name	Access	Description	Reset value
15	Reserved	RO	Reserved	0
14	TDE	RW	Trigger the DMA request enable bit. 1: Allowing DMA requests to be triggered. 0: Triggering of DMA requests is prohibited.	0
13	Reserved	RO	Reserved	0
12	CC4DE	RW	Compare the DMA request enable bit of capture channel 4. 1: Allows comparison of DMA requests for capture channel 4. 0: Disable comparison of DMA requests for capture channel 4.	0
11	CC3DE	RW	Compare the DMA request enable bit of capture channel 3. 1: Allows comparison of DMA requests for capture channel 3. 0: Disable comparison of DMA requests for capture channel 3.	0
10	CC2DE	RW	Compare the DMA request enable bit of capture channel 2. 1: allows comparison of DMA requests for capture channel 2. 0: Disable comparison of DMA requests for capture channel 2.	0
9	CC1DE	RW	Compare the DMA request enable bit of capture channel 1. 1: allows comparison of DMA requests for capture channel 1. 0: Disable comparison of DMA requests for capture channel 1.	0
8	UDE	RW	Updated DMA request enable bit. 1: DMA requests that allow updates. 0: DMA requests for updates are disabled.	0
7	Reserved	RO	Reserved	0
6	TIE	RW	Trigger the interrupt enable bit. 1: Enables triggering of interrupts. 0: Trigger interrupt is disabled.	0
5	Reserved	RO	Reserved	0
4	CC4IE	RW	Compare capture channel 4 interrupt enable bit. 1: Allows comparison of capture channel 4 interrupts. 0: Disable compare capture channel 4 interrupt.	0
3	CC3IE	RW	Compare capture channel 3 interrupt enable bit. 1: Allows comparison of capture channel 3 interrupts. 0: Disable compare capture channel 3 interrupt.	0
2	CC2IE	RW	Compare capture channel 2 interrupt enable bit. 1: allows comparison of capture channel 2 interrupts. 0: Disable compare capture channel 2 interrupt.	0
1	CC1IE	RW	Compare capture channel 1 interrupt enable bit. 1: allows comparison of capture channel 1 interrupts. 0: Disable compare capture channel 1 interrupt.	0
0	UIE	RW	Update the interrupt enable bit. 1: Allowing updates to be interrupted. 0: Disable update interruption.	0

11.4.5 Interrupt Status Register (TIM2_INTFR)

Offset address: 0x10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			CC4OF	CC3OF	CC2OF	CC1OF	Reserved		TIF	Reserved	CC4IF	CC3IF	CC2IF	CC1IF	UIF

Bit	Name	Access	Description	Reset value
[15:13]	Reserved	RO	Reserved	0
12	CC4OF	RW0	Compare capture channel 4 to repeat capture flag bits.	0
11	CC3OF	RW0	Compare capture channel 3 to repeat capture flag bits.	0
10	CC2OF	RW0	Compare capture channel 2 to repeat capture flag bits.	0
9	CC1OF	RW0	The compare capture channel 1 repeat capture flag bit is used only when the compare capture channel is configured for input capture mode. This flag is set by hardware and a software write of 0 clears this bit. 1: the value of the counter is captured into the capture comparison register when the status of CC1IF has been set. 0: No duplicate captures are generated.	0
[8:7]	Reserved	RO	Reserved	0
6	TIF	RW0	Trigger interrupt flag bit, when a trigger event occurs by hardware to this location bit, by software to clear. Trigger events include the detection of a valid edge at the TRGI input from a mode other than gated, or any edge in gated mode. 1: Trigger event generation. 0: No trigger event is generated.	0
5	Reserved	RO	Reserved	0
4	CC4IF	RW0	Compare capture channel 4 interrupt flag bits.	0
3	CC3IF	RW0	Compare capture channel 3 interrupt flag bits.	0
2	CC2IF	RW0	Compare capture channel 2 interrupt flag bits.	0
1	CC1IF	RW0	Compare capture channel 1 interrupt flag bits. If the compare capture channel is configured in output mode, this bit is set by hardware when the counter value matches the compare value, except in centrosymmetric mode. This bit is cleared by software. 1: The value of the core counter matches the value of compare capture register 1; 0: No match occurs. If compare capture channel 1 is configured in input mode, this bit is set by hardware when a capture event occurs and it is cleared by software or by reading the compare capture register. 1: the counter value has been captured compare capture register 1. 0: No input capture is generated.	0
0	UIF	RW0	Update interrupt flag bit, this bit is set by hardware when an update event is generated and cleared by software. 1: Update interrupt generation. 0: No update event is generated. The following scenarios generate update events. If UDIS = 0, when the repeat counter value overflows or underflows. If URS = 0, UDIS = 0, when the UG bit is set, or when the counter core counter is reinitialized by software. If URS = 0, UDIS = 0, when the counter CNT is	0

			reinitialized by a trigger event.	

11.4.6 TIM2 Event Generation Register (TIM2_SWEVGR)

Offset address: 0x14

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved									TG	Reserved	CC4G	CC3G	CC2G	CC1G	UG

Bit	Name	Access	Description	Reset value
[15:7]	Reserved	RO	Reserved	0
6	TG	WO	The trigger event generation bit, which is set by software and cleared by hardware, is used to generate a trigger event. 1: Generate a trigger event, TIF is set, and the corresponding interrupts and DMAs are generated if enabled. 0: No action.	0
5	Reserved	RO	Reserved	0
4	CC4G	WO	Compare capture event generation bit 4. Generate Compare Capture Event 4.	0
3	CC3G	WO	Compare capture event generation bit 3. Generate Compare Capture Event 3.	0
2	CC2G	WO	Compare capture event generation bit 2. Generate Compare Capture Event 2.	0
1	CC1G	WO	Compare capture event generation bit 1. Generate Compare Capture Event 1. This bit is set by software and cleared by hardware. It is used to generate a compare capture event. 1: Generate a compare capture event on compare capture channel 1. If compare capture channel 1 is configured as output: set the CC1IF bit. Generate the corresponding interrupts and DMAs if they are enabled. If compare capture channel 1 is configured as input: the current core counter value is captured to compare capture register 1; set the CC1IF bit and generate the corresponding interrupts and DMAs if they are enabled. If CC1IF is already set, set the CC1OF bit. 0: No action.	0
0	UG	WO	Update event generation bit to generate an update event. This bit is set by software and is automatically cleared by hardware. 1: Initialize the counter and generate an update event. 0: No action. *Note: The prescaler counter is also cleared to zero, but the prescaler factor remains unchanged. The core counter is cleared if in centrosymmetric mode or incremental counting mode; if in decremental counting mode, the core counter takes the value of the reload value register.*	0

11.4.7 Compare/Capture Control Register 1 (TIM2_CHCTLR1)

Offset address: 0x18

The channel can be used in input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxS bit. The other bits of this register serve different purposes in input and output modes. OCxx describes the function of the channel in output mode and ICxx describes the function of

the channel in input mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC2CE	OC2M[2:0]			OC2PE	OC2FE	CC2S[1:0]		OC1CE	OC1M[2:0]			OC1PE	OC1FE	CC1S[1:0]	
IC2F[3:0]				IC2PSC[1:0]				IC1F[3:0]				IC1PSC[1:0]			

Comparison mode (pin direction is output).

Bit	Name	Access	Description	Reset value
15	OC2CE	RW	Compare capture channel 2 clear enable bit. 1: Clear the OC2REF bit zero once the ETRF input is detected high. 0: OC2REF is not affected by the ETRF input.	0
[14:12]	OC2M[2:0]	RW	Compare the Capture Channel 2 mode setting field. The 3 bits define the action of the output reference signal OC2REF, which determines the values of OC2, OC2N. OC2REF is active high, while the active levels of OC2 and OC2N depend on the CC2P, CC2NP bits. 000: Freeze. Comparison of the value of the capture register with the value of the comparison between the core counters does not work for OC2REF. 001: force to set to valid level. Forcing OC1REF high when the core counter has the same value as the comparison capture register 1. 010: Force to set to invalid level. Forcing OC2REF low when the value of the core counter is the same as the comparison capture register 1. 011: Flip. Flips the level of OC2REF when the core counter is the same as the value of compare capture register 1. 100: Forced to invalid level. Forces OC2REF to low. 101: Force to valid level. Force OC2REF to high. 110: PWM mode 1: When counting up, channel 2 is invalid level once the core counter is greater than the value of the compare capture register, otherwise it is valid level; when counting down, channel 2 is valid level once the core counter is greater than the value of the compare capture register, otherwise it is invalid level. 111: PWM mode 2: When counting up, channel 2 is valid level once the core counter is greater than the value of the compare capture register, otherwise it is invalid level; when counting down, channel 2 is invalid level once the core counter is greater than the value of the compare capture register, otherwise it is valid level (OC2REF=1). *Note: This bit cannot be modified once the LOCK level is set to 3 and CC2S=00b. In PWM mode 1 or PWM mode 2, the OC2REF level is changed only when the comparison result is changed or when switching from freeze mode to PWM mode in the output comparison mode.*	0
11	OC2PE	RW	Compare Capture Register 2 preload enable bit. 1: Enable the preload function of the compare capture register 2, the read and write operations operate only on the preload register, and the preload value of the compare capture register 2 is loaded into the current shadow register when the update event comes. 0: Disable the preload function of compare capture register 2. The compare capture register 2 can be	0

			written at any time, and the newly written value takes effect immediately. *Note: Once the LOCK level is set to 3 and CC2S=00, this bit cannot be modified. PWM mode can be used only in single pulse mode (OPM=1) without confirming the pre-load register, otherwise its action is not determined.*	
10	OC2FE	RW	Compare Capture Channel 2 fast enable bit, this bit is used to speed up the response of the compare capture channel output to trigger input events. 1: The active edge of the input to the flipflop acts as if a comparison match has occurred. Therefore, the OC is set to the comparison level independent of the comparison result. The delay between the valid edge of the sample trigger and the output of the compare capture channel 2 is reduced to 3 clock cycles. 0: Based on the value of the counter and compare capture register 1, compare capture channel 2 operates normally, even if the flip-flop is open. The minimum delay to activate the compare capture channel 2 output is 5 clock cycles when the input of the flipflop has a valid edge. OC2FE only works when the channel is configured to PWM1 or PWM2 mode.	0
[9:8]	CC2S[1:0]	RW	Compare capture channel 2 input selection fields. 00: comparison capture channel 2 is configured as an output. 01: comparison capture channel 2 is configured as an input and IC2 is mapped on TI2. 10: comparison capture channel 2 is configured as an input and IC2 is mapped onTI1. 11: Compare Capture Channel 2 is configured as an input and IC2 is mapped on TRC. This mode works only when the internal trigger input is selected (by the TS bit). *Note: Compare Capture Channel 2 is writable only when the channel is off (when CC2E is zero).*	0
7	OC1CE	RW	Compare capture channel 1 clear enable bit.	0
[6:4]	OC1M[2:0]	RW	Compare capture channel 1 mode setting field.	0
3	OC1PE	RW	Compare capture register 1 preload enable bit.	0
2	OC1FE	RW	Compare capture channel 1 fast enable bit.	0
[1:0]	CC1S[1:0]	RW	Compare capture channel 1 input selection fields.	0

Capture mode (pin direction is input).

Bit	Name	Access	Description	Reset value
[15:12]	IC2F[3:0]	RW	The input capture filter 2 configuration field, these bits set the sampling frequency of the TI1 input and the digital filter length. The digital filter consists of an event counter, which records N events and then generates a jump in the output. 0000: no filter, sampled at fDTS. 1000: sampling frequency Fsampling = Fdts/8, N = 6. 0001: sampling frequency Fsampling=Fck_int, N=2. 1001: sampling frequency Fsampling = Fdts/8, N = 8. 0010: sampling frequency Fsampling=Fck_int, N=4. 1010: sampling frequency Fsampling = Fdts/16, N = 5. 0011: sampling frequency Fsampling=f=Fck_int, N=8. 1011: sampling frequency Fsampling = Fdts/16, N = 6.	0

			0100: sampling frequency Fsampling = Fdts/2, N = 6. 1100: sampling frequency Fsampling = Fdts/16, N = 8. 0101: sampling frequency Fsampling = Fdts/2, N = 8. 1101: sampling frequency Fsampling = Fdts/32, N = 5. 0110: sampling frequency Fsampling = Fdts/4, N = 6. 1110: sampling frequency Fsampling = Fdts/32, N = 6. 0111: sampling frequency Fsampling = Fdts/4, N = 8. 1111: Sampling frequency Fsampling=Fdts/32, N=8.	
[11:10]	IC2PSC[1:0]	RW	Compare capture channel 2 prescaler configuration field, these 2 bits define the prescaler coefficient for compare capture channel 2. Once CC1E = 0, the prescaler is reset. 00: without prescaler, one capture is triggered for each edge detected on the capture input. 01: capture triggered every 2 events. 10: capture triggered every 4 events. 11: Capture is triggered every 8 events.	0
[9:8]	CC2S[1:0]	RW	Compare the capture channel 2 input selection field, these 2 bits define the direction of the channel (input/output), and the selection of the input pin. 00: Comparative capture channel 1 channel is configured as an output. 01: Comparison capture channel 1 channel is configured as an input and IC1 is mapped on TI1. 10: Comparison capture channel 1 channel is configured as an input and IC1 is mapped on TI2. 11: The compare capture channel 1 channel is configured as an input and IC1 is mapped on TRC. This mode works only when the internal trigger input is selected (by the TS bit). *Note: CC1S is writable only when the channel is off (CC1E is 0).*	0
[7:4]	IC1F[3:0]	RW	Input capture filter 1 configuration field.	0
[3:2]	IC1PSC[1:0]	RW	Compare the capture channel 1 prescaler configuration field.	0
[1:0]	CC1S[1:0]	RW	Compare capture channel 1 input selection fields.	0

11.4.8 Compare/Capture Control Register 2 (TIM2_CHCTLR2)

Offset address: 0x1C

The channel can be used in input (capture mode) or output (compare mode), and the direction of the channel is defined by the corresponding CCxS bit. The other bits of this register serve different purposes in input and output modes. OCxx describes the function of the channel in output mode and ICxx describes the function of the channel in input mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC4CE	OC4M[2:0]			OC4PE	OC4FE	CC4S[1:0]		OC3CE	OC3M[2:0]			OC3PE	OC3FE	CC3S[1:0]	
IC4F[3:0]				IC4PSC[1:0]				IC3F[3:0]				IC3PSC[1:0]			

Comparison mode (pin direction is output).

Bit	Name	Access	Description	Reset value
15	OC4CE	RW	Compare capture channel 4 clear enable bit.	0
[14:12]	OC4M[2:0]	RW	Compare the capture channel 4 mode setting field.	0
11	OC4PE	RW	Compare Capture Register 4 preload enable bit.	0
10	OC4FE	RW	Compare capture channel 4 fast enable bit.	0
[9:8]	CC4S[1:0]	RW	Compare capture channel 4 input selection fields.	0

7	OC3CE	RW	Compare capture channel 3 clear enable bit.	0
[6:4]	OC3M[2:0]	RW	Compare the capture channel 3 mode setting field.	0
3	OC3PE	RW	Compare Capture Register 3 preload enable bit.	0
2	OC3FE	RW	Compare capture channel 3 fast enable bit.	0
[1:0]	CC3S[1:0]	RW	Compare capture channel 3 input selection fields.	0

Capture mode (pin direction is input).

Bit	Name	Access	Description	Reset value
[15:12]	IC4F[3:0]	RW	Input capture filter 4 configuration field.	0
[11:10]	IC4PSC[1:0]	RW	Compare the capture channel 4 prescaler configuration field.	0
[9:8]	CC4S[1:0]	RW	Compare capture channel 4 input selection fields.	0
[7:4]	IC3F[3:0]	RW	Input capture filter 3 configuration field.	0
[3:2]	IC3PSC[1:0]	RW	Compare the capture channel 3 prescaler configuration field.	0
[1:0]	CC3S[1:0]	RW	Compare capture channel 3 input selection fields.	0

11.4.9 Compare/Capture Enable Register (TIM2_CCER)

Offset address: 0x20

15 14	13	12	11 10	9	8	7 6	5	4	3 2	1	0
Reserved	CC4P	CC4E	Reserved	CC3P	CC3E	Reserved	CC2P	CC2E	Reserved	CC1P	CC1E

Bit	Name	Access	Description	Reset value
[15:14]	Reserved	RO	Reserved	0
13	CC4P	RW	Compare the capture channel 4 output polarity setting bit.	0
12	CC4E	RW	Compare capture channel 4 output enable bit.	0
[11:10]	Reserved	RO	Reserved	0
9	CC3P	RW	Compare the capture channel 3 output polarity setting bit.	0
8	CC3E	RW	Compare capture channel 3 output enable bit.	0
[7:6]	Reserved	RO	Reserved	0
5	CC2P	RW	Compare the capture channel 2 output polarity setting bit.	0
4	CC2E	RW	Compare capture channel 2 output enable bit.	0
[3:2]	Reserved	RO	Reserved	0
1	CC1P	RW	Compare the capture channel 1 output polarity setting bit. CC1 channel configured as output: 1: OC1 active low. 0: OC1 active high. CC1 channel configured as input: This bit selects whether IC1 or the inverted signal of IC1 is used as the trigger or capture signal. 1: Inverted: capture occurs on the falling edge of IC1; when used as an external trigger, IC1 is inverted. 0: Non-inverted: capture occurs on the rising edge of IC1; when used as an external trigger, IC1 is not inverted. *Note: Once the LOCK level (LOCK bit in TIMx_BDTR register) is set to 3 or 2, this bit cannot be modified.*	0
0	CC1E	RW	Compare capture channel 1 output enable bit. The CC1 channel is configured as output:	0

			1: ON. the OC1 signal is output to the corresponding output pin, and its output level depends on the values of the MOE, OSSI, OSSR, OIS1, OIS1N, and CC1NE bits. 0: off. OC1 disables output, so the output level of OC1 depends on the values of the MOE, OSSI, OSSR, OIS1, OIS1N, and CC1NE bits. The CC1 channel is configured as an input: This bit determines whether the counter value can be captured into the TIMx_CCR1 register. 1: capture enable. 0: capture disable.	

11.4.10 Counter for General-purpose Timer (TIM2_CNT)

Offset address: 0x24

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT[15:0]															

Bit	Name	Access	Description	Reset value
[15:0]	CNT[15:0]	RW	The real-time value of the timer's counter.	0

11.4.11 Counting Clock Prescaler (TIM2_PSC)

Offset address: 0x28

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSC[15:0]															

Bit	Name	Access	Description	Reset value
[15:0]	PSC[15:0]	RW	The dividing factor of the prescaler of the timer; the clock frequency of the counter is equal to the input frequency of the divider/(PSC+1).	0

11.4.12 Auto-reload Value Register (TIM2_ATRLR)

Offset address: 0x28

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATRLR[15:0]															

Bit	Name	Access	Description	Reset value
[15:0]	ATRLR[15:0]	RW	The value of ATRLR[15:0] will be loaded into the counter, read section 10.2.4 for when ATRLR acts and updates; the counter stops when ATRLR is empty.	0xFFFF

11.4.13 Compare/capture Register 1 (TIM2_CH1CVR)

Offset address: 0x34

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															LEVEL1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CH1CVR[15:0]

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
16	LEVEL1	RO	The level indication bit corresponding to the captured value	0
[15:0]	CH1CVR[15:0]	RW	The value compare/capture register channel 1.	0

11.4.14 Compare/capture Register 2 (TIM2_CH2CVR)

Offset address: 0x38

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															LEVEL2
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH2CVR[15:0]															

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
16	LEVEL2	RO	The level indication bit corresponding to the captured value	0
[15:0]	CH2CVR[15:0]	RW	The value compare/capture register channel 2.	0

11.4.15 Compare/capture Register 3 (TIM2_CH3CVR)

Offset address: 0x3C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															LEVEL3
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH3CVR[15:0]															

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
16	LEVEL3	RO	The level indication bit corresponding to the captured value	0
[15:0]	CH3CVR[15:0]	RW	The value compare/capture register channel 3.	0

11.4.16 Compare/capture Register 4 (TIM2_CH4CVR)

Offset address: 0x40

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															LEVEL4
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH4CVR[15:0]															

Bit	Name	Access	Description	Reset value
[31:17]	Reserved	RO	Reserved	0
16	LEVEL4	RO	The level indication bit corresponding to the captured value	0
[15:0]	CH4CVR[15:0]	RW	The value compare/capture register channel 4.	0

11.4.17 DMA Control Register (TIM2_DMACFGR)

Offset address: 0x48

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			DBL[4:0]					Reserved			DBA[4:0]				

Bit	Name	Access	Description	Reset value
[15:13]	Reserved	RO	Reserved	0
[12:8]	DBL[4:0]	RW	The length of the DMA continuous transmission, the actual value of which is the value of this field + 1.	0
[7:5]	Reserved	RO	Reserved	0
[4:0]	DBA[4:0]	RW	These bits define the offset of the DMA in continuous mode from the address where control register 1 is located.	0

11.4.18 DMA Address Register for Continuous Mode (TIM2_DMAADR)

Offset address: 0x4C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMAADR[15:0]															

Bit	Name	Access	Description	Reset value
[15:0]	DMAADR[15:0]	RW	The address of the DMA in continuous mode.	0