Chapter 12 Universal Synchronous Asynchronous Receiver Transmitter (USART)

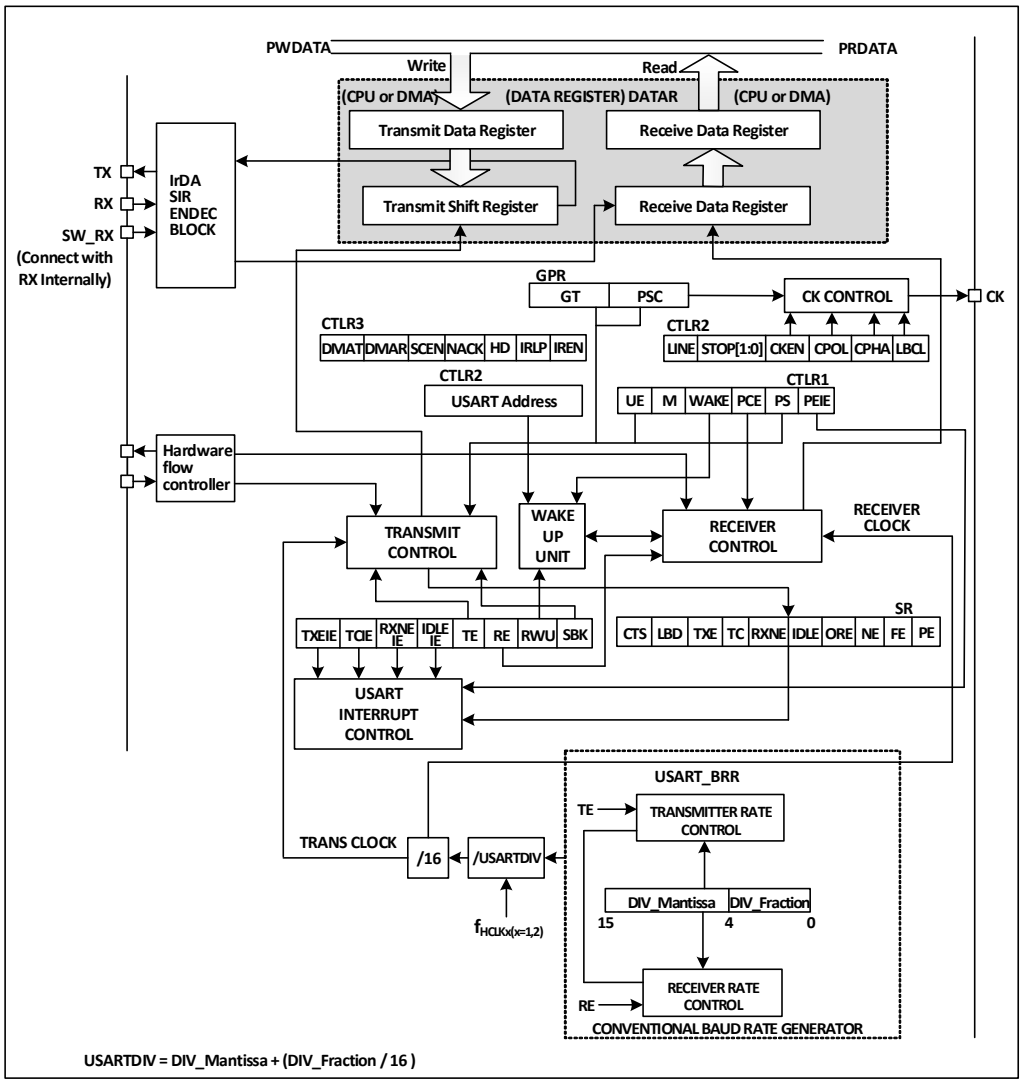
The module contains one Universal Synchronous Asynchronous Transceiver USART1.

12.1 Main Features

- Full-duplex or half-duplex synchronous or asynchronous communication
- NRZ data format
- Fractional baud rate generator, up to 3Mbps
- Programmable data length
- Configurable stop bits
- Support LIN, IrDA encoders, smart cards
- DMA support
- Multiple interrupt sources

12.2 Overview

Figure 12-1 Block diagram of a general-purpose synchronous/asynchronous transceiver



When TE (transmit enable bit) is set, the data in the transmit shift register is output on the TX pin and the clock

is output on the CK pin. When transmitting, the first bit shifted out is the least significant bit and each data frame starts with a low start bit, then the transmitter sends an 8- or 9-bit data word depending on the setting on the M (word length) bit, and finally a configurable number of stop bits. If equipped with a parity check bit, the last bit of the data word is the check bit. After the TE is set an idle frame is sent, which is 10 or 11 bits high and contains the stop bit. The disconnect frame is 10 or 11 bits low followed by the stop bit.

12.3 Baud Rate Generator

The baud rate of the transceiver = HCLK/(16*USARTDIV), HCLK is the clock of HB. The value of USARTDIV is determined by the two fields DIV_M and DIV_F in USART_BRR, which is calculated by the formula The formula is as follows.

USARTDIV = DIV_M+(DIV_F/16)

It is important to note that the bit rate generated by the baud rate generator may not always generate exactly the baud rate required by the user, and there may be deviations. In addition to taking as close a value as possible, a way to reduce the deviation is to increase the HB clock. For example, if you set the baud rate to 115200bps, the value of USARTDIV is set to 39.0625, which will give you a baud rate of exactly 115200bps at the highest frequency, but if you need a baud rate of 921600bps, the calculated USARTDIV is 4.88, but the closest value filled in USART_BRR is actually only 4.875. 4.875, the actual baud rate is 923076bps, which is 0.16% error. When the serial waveform sent by the sender is transmitted to the receiver, the baud rate of the receiver and the sender is subject to some error. The error mainly comes from three aspects: the actual baud rate of the receiver and the sender is not the same; the receiver and the sender's clock has errors; the waveform in the line generated by the change. Peripheral module receiver is a certain receiving tolerance, when the sum of the above three aspects of the total deviation is less than the module's tolerance limit, the total deviation does not affect the transmission and reception. The tolerance limitof the module is affected by whether to use fractional baud rate and M-bit (data field word length), using fractional baud rate and using 9-bit data field length will reduce the tolerance limit, but not less than 3%.

12.4 Synchronous Mode

Synchronous mode allows the system to output a clock signal when using the USART module. When synchronous mode is enabled to send data externally, the CK pin will output the clock externally at the same time.

The way to turn on the synchronous mode is to the CLKEN position bit in control register 2 (R16_USARTx_CTLR2), but also need to turn off the LIN mode, smart card mode, infrared mode and half duplex mode, i.e. ensure that the SCEN, HDSEL and IREN bits are in reset, these three in control register 3 (R16_USARTx_CTLR3).

The key point of using synchronous mode is the clock output control. There are several points to note.

a) The USART module synchronization mode works only in the main mode, i.e. the CK pin outputs only the clock and does not receive inputs.
   Outputs a clock signal only when data is output on the TX pin.
   The LBCL bit determines whether the clock is output when the last data bit is sent, the CPOL bit determines the polarity of the clock, and the CPHA determines the phase of the clock. These three bits are in control register 2 (R16_USARTx_CTLR2), which needs to be set when TE and RE are not enabled, see Figure 12-2 for the differences.
   The receiver will only sample at the output clock in synchronous mode, requiring a certain amount of signal build time and hold time from the device, as shown in Figure 12-3.

Figure 12-2 USART clock timing example (M=0)

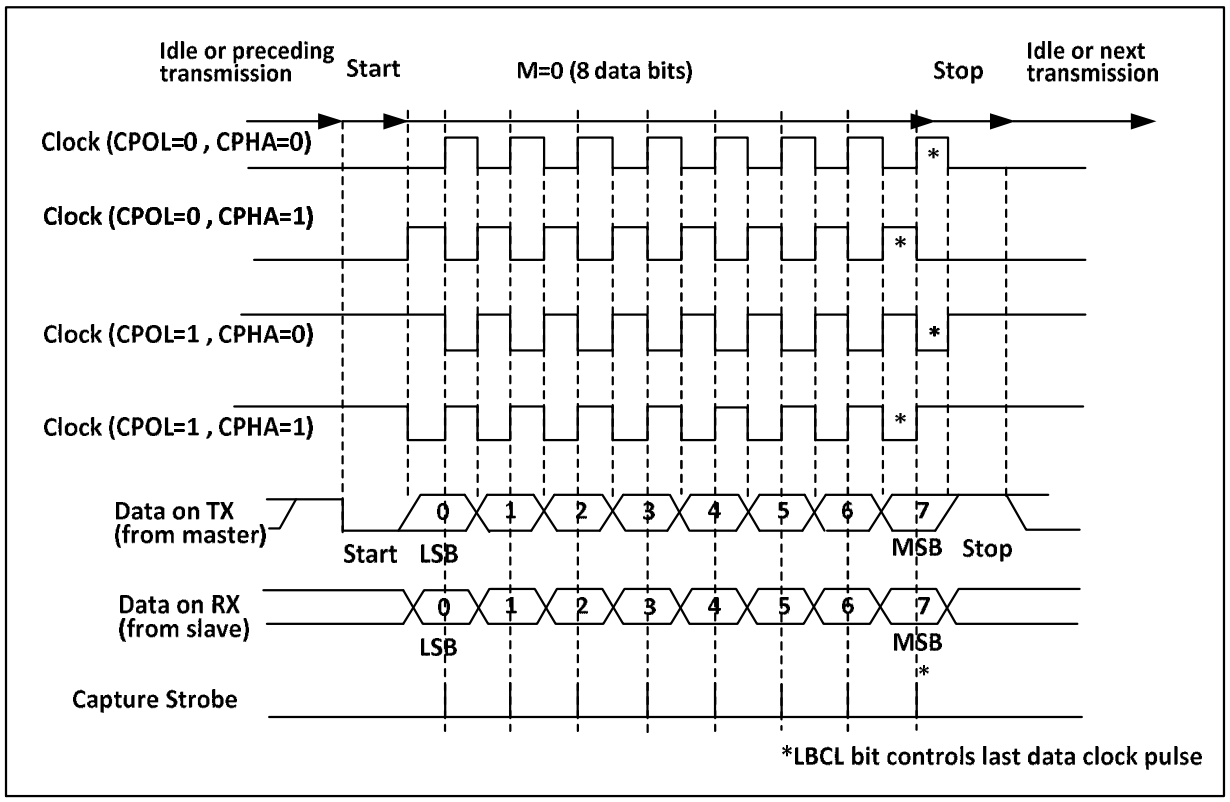
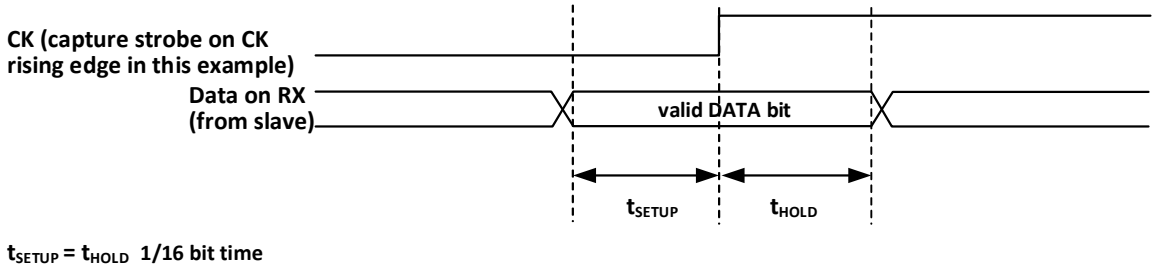


Figure 12-3 Data Sample Hold Time



12.5 1-wire Half-duplex Mode

Half-duplex mode supports the use of a single pin (TX pin only) for receive and transmit, with the TX and RX pins connected internally on the chip.

The way to turn on the half-duplex mode is to set the HDSEL position bit in control register 3 (R16_USARTx_CTLR3), but it is also necessary to turn off the LIN mode, smart card mode, IR mode and synchronous mode, i.e. to ensure that the SCEN, CLKEN and IREN bits are in reset, which are in control registers 2 and 3 (R16_USARTx_CTLR2 and R16_USARTx_CTLR3).

After setting to half duplex mode, you need to set the IO port of TX to open-drain output high mode. With TE set, the data will be sent out as soon as it is written to the data register. Special attention should be paid to the fact that the half-duplex mode may cause bus conflicts when multiple devices use a single bus to send and receive, which needs to be avoided by the user with software itself.

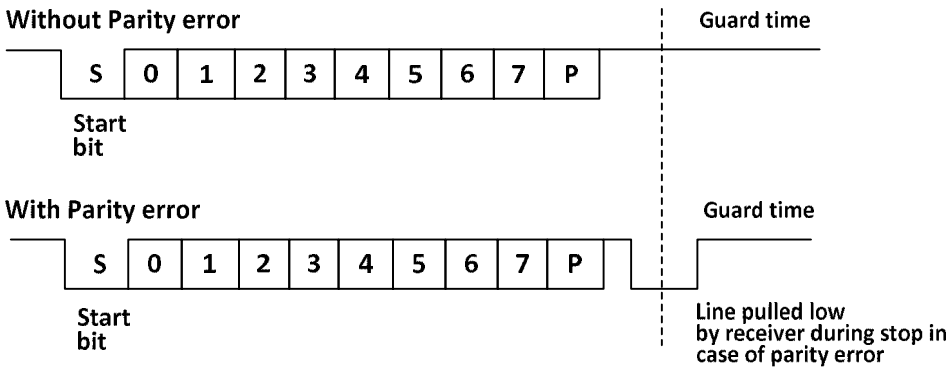
12.6 Smart Card

Smart card mode supports ISO7816-3 protocol access to smart card controllers.

The smart card mode is turned on by setting the SCEN position bit in control register 3

(R16_USARTx_CTLR3), but it is also necessary to turn off LIN mode, half duplex mode and IR mode, i.e. to ensure that the LINEN, HDSEL and IREN bits are in reset, but CLKEN can be turned on to output the clock, these bits are in control registers 2 and 3 (R16_USARTx_CTLR2 and R16_USARTx_CTLR3).
To support smart card mode, USART should be set to 8 bits of data plus 1 bit of parity, and its stop bit is recommended to be configured to 1.5 bits for both transmit and receive. Smart card mode is a 1-wire half-duplex protocol that uses the TX line for data communication and should be configured as an open-drain output plus a pull. When the receiver receives a frame of data and detects a parity error, it sends a NACK signal, i.e., it actively pulls the TX down by one cycle during the stop bit, and the sender detects the NACK signal, which generates a frame error whereby the application can retransmit. Figure 17-4 shows the waveforms on the TX pin in the correct case and in the case of a parity error. the TC flag (transmit complete flag) of the USART can delay the GT (protection time) generation by one clock, and the receiver will not recognize the NACK signal it sets as the start bit.

Figure 12-4 (Un)Occurrence of parity error diagram



In smart card mode, the waveform output from the CK pin when enabled has nothing to do with communication; it simply clocks the smart card with the value of the AHB clock followed by a five-bit settable clock division (twice the value of the PSC, up to 62 divisions).

12.7 IrDA

The USART module supports control of IrDA infrared transceivers for physical layer communication. The LINEN, STOP, CLKEN, SCEN and HDSEL bits must be cleared to use IrDA. NRZ (non-return to zero) coding is used between the USART module and the SIR physical layer (infrared transceiver) and is supported up to 115200 bps rates.
IrDA is a half-duplex protocol, if UASRT is sending data to SIR physical layer, then IrDA decoder will ignore the newly sent IR signal, if USART is receiving data from SIR, then SIR will not accept the signal from USART. the level logic of USART to SIR and SIRto USART is different. In SIR receive logic, the high level is 1 and the low level is 0, but in SIR send logic, the high level is 0 and the low level is 1.

12.8 DMA

The USART module supports DMA function, which can be used to achieve fast and continuous sending and receiving. When DMA is enabled, the DMA writes data from the set memory space to the transmit buffer when TXE is set. When using DMA to receive, each time RXNE is set, DMA transfers the data in the receive buffer to a specific memory space.

12.9 Interruptions

The USART module supports a variety of interrupt sources, including transmit data register empty (TXE),

CTS, transmit complete (TC), receive data ready (RXNE), dataoverflow (ORE), line idle (IDLE), parity error (PE), disconnect flag (LBD), noise (NE), overflow for multi-buffered communication (ORT), and frame error (FE), among others.

Table 12-1 Relationship between interrupts and corresponding enable bits

Interrupt source	Enable bit
Transmit data register empty (TXE)	TXEIE
Allowed to send (CTS)	CTSIE
Transmission complete（TC）	TCIE
Received data ready to be read（RXNE）	RXNEIE
Overrun error detected（ORE）	
Idle line detected（IDLE）	IDLEIE
Parity error（PE）	PEIE
Break flag（LBD）	LBDIE
Noise flag（NE）	EIE
Overflow of multi-buffered communication (ORE)	
Frame error for multibuffered communication (FE)	

12.10 Register Description

Table 12-2 USART-related registers list

Name	Offset address	Description	Reset value
R32_USART_STATR	0x40013800	UASRT status register	0x000000C0
R32_USART_DATAR	0x40013804	UASRT data register	0x000000XX
R32_USART_BRR	0x40013808	UASRT baud rate register	0x00000000
R32_USART_CTLR1	0x4001380C	UASRT control register 1	0x00000000
R32_USART_CTLR2	0x40013810	UASRT control register 2	0x00000000
R32_USART_CTLR3	0x40013814	UASRT control register 3	0x00000000
R32_USART_GPR	0x40013818	UASRT protection time and prescaler register	0x00000000

12.10.1 USART Status Register (USART_STATR)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NE	FE	PE

Bit	Name	Access	Description	Reset value
[31:10]	Reserved	RO	Reserved	0
9	CTS	RW0	CTS state change flag. If the CTSE bit is set, this bit will be set high by hardware when the nCTS output state changes. It is cleared to zero by software. If the CTSIE bit is already set, an interrupt will be generated. 1: the presence of changes on the nCTS state line. 0: No change on the nCTS state line.	0
8	LBD	RW0	LIN Break detection flag. This bit is set by hardware when a LIN Break is detected. It is cleared by software.	0

			If LBDIE is already set, an interrupt will be generated. 1: LIN Break detected. 0: No detection of pending LIN Break.	
7	TXE	RO	Send data register empty flag. This bit is set by hardware when the data in the TDR register is transferred to the shift register by hardware. If TXEIE is already set, an interrupt will be generated to perform a write operation to the data register and this bit will be reset. 1: the data has been transferred to the shift register. 0: The data has not been transferred to the shift register.	1
6	TC	RW0	Send completion flag. When a frame containing data is sent and TXE is set, the hardware will set this bit, and if TCIE is set, an interrupt will be generated, and the software will clear this bit by reading it and then writing to the data register. It is also possible to write 0 directly to clear this bit. 1: Sending completed. 0: Sending is not yet complete.	1
5	RXNE	RW0	Read data register non-empty flag, this bit is set by hardware when data in the shift register is transferred to the data register. If RXNEIE is already set, a corresponding interrupt is also generated. A read operation of the data register clears this bit. It is also possible to clear the bit by writing a 0 directly. 1: Data received and able to be read out. 0: The data has not been received.	0
4	IDLE	RO	Bus idle flag. When the bus is idle, this bit will be set by hardware. If IDLEIE is already set, the corresponding interrupt will be generated. The operation of reading the status register and then reading the data register will clear this bit. 1: The bus is idle. 0: No bus idle is detected. *Note: This bit will not be set again until RXNE is set.*	0
3	ORE	RO	Overload error flag. This bit will be set when there is data in the receive shift register that needs to be transferred to the data register, but there is still data in the receive field of the data register that has not been read out. If RXNEIE is set, the corresponding interrupt will also be generated. 1: Occurrence of an overload error. 0: No overload error. *Note: In case of an overload error, the value of the data register is not lost, but the value of the shift register is overwritten. If the EIEable bit is set, the ORE flag position bit generates an interrupt in multi-buffer communication mode.*	0
2	NE	RO	Noise error flag. It is set by hardware when the noise error flag is detected. The operation of reading the status register and then reading the data register resets this bit. 1: Noise detected. 0: No noise is detected. *Note: This bit does not generate an interrupt. If the EIE bit is set, the FE flag position*	0

			bit generates an interrupt in multi-buffer communication mode.	
1	FE	RO	Frame error flag. This bit will be set by hardware when a synchronization error, excessive noise or disconnect character is detected. Reading this bit and then reading the data register operation will reset this bit. 1: Frame error detected. 0: No frame error detected. *Note: This bit will not generate an interrupt. If the EIE bit is set, the FE flag position bit will generate an interrupt in multi-buffer communication mode.*	0
0	PE	RO	Checksum error flag. In receive mode, hardware sets this bit if a parity check error is generated. A read of this bit and then a read of the data register operation resets this bit. Before clearing this bit, software must wait for the RXNE flag bit to be set. If the PEIE has been set previously, then this bit being set generates a corresponding interrupt. 1: A parity error. 0: No inspection error.	0

12.10.2 USART Data Register (USART_DATAR)

Offset address: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							DR[8:0]								

Bit	Name	Access	Description	Reset value
[31:9]	Reserved	RO	Reserved	0
[8:0]	DR[8:0]	RW	Data register. This register is actually the receive data register (RDR) and send register (TDR) two registers composed of DR read and write operation start is read receive register (RDR) and write send register (TDR) respectively.	X

12.10.3 USART Baud Rate Register (USART_BRR)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV_Mantissa[11:0]												DIV_Fraction[3:0]			

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
[15:4]	DIV_ Mantissa[11:0]	RW	These 12 bits define the integer part of the dividing factor of the frequency divider.	0
[3:0]	DIV_ Fraction[3:0]	RW	These 4 bits define the fractional part of the dividing factor of the frequency divider.	0

12.10.4 USART Control Register 1 (USART_CTLR1)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		UE	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	RWU	SBK

Bit	Name	Access	Description	Reset value
[31:14]	Reserved	RO	Reserved	0
13	UE	RW	USART enable bit. When this bit is set, both the USART divider and the output stop working after the current byte transfer is completed.	0
12	M	RW	Word long bit. 1: 9 data bits; 0: 8 data bits.	0
11	WAKE	RW	Wake-up bit. This bit determines the method of waking up the USART. 1: Address marker; 0: Bus idle.	0
10	PCE	RW	The parity bit is enabled. For the receiver, it is the parity check of the data; for the sender, it is the insertion of the parity bit. Once this bit is set, the parity bit enable will take effect only after the current byte transmission is completed.	0
9	PS	RW	Parity selection. 0 means even parity, 1 means odd parity. When this bit is set, the parity bit enable will take effect only after the current byte transmission is completed.	0
8	PEIE	RW	Parity check interrupt enable bit. This bit indicates that parity check error interrupts are allowed.	0
7	TXEIE	RW	TXE interrupt enable. This bit indicates that a TXE interrupt is allowed to be generated.	0
6	TCIE	RW	Transmit completion interrupt enable. This bit indicates that the transmit completion interrupt is allowed to be generated.	0
5	RXNEIE	RW	RXNE interrupt enable. This bit indicates that a RXNE interrupt is allowed to be generated.	0
4	IDLEIE	RW	IDLE interrupt enable. This bit allows IDLE interrupt to be generated.	0
3	TE	RW	Transmitter enable. Setting this bit will enable the transmitter.	0
2	RE	RW	Receiver enable. Setting this bit enables the receiver, which starts detecting the start bit on the RX pin.	0
1	RWU	RW	Receiver wakeup. This bit determines whether to place the USART in silent mode. 1: The receiver is in silent mode. 0: The receiver is in normal operation mode. *Note 1: Before setting the RWU bit, the USART needs to receive a data byte first, otherwise it cannot be woken up by bus idle in silent mode.* *Note 2: When configured as address mark wake-up, the RWU bit cannot be modified by software when RXNE is set.*	0
0	SBK	RW	Send break bit. Set this bit to send break character. It is reset by hardware on the stop bit of the break frame.	0

			1: Send; 0: Do not send.	

12.10.5 USART Control Register 2 (USART_CTLR2)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	LINEN	STOP[1:0]		CLKEN	CPOL	CPHA	LBCL	Reserved	LBDIE	LBDL	Reserved	ADD[3:0]			

Bit	Name	Access	Description	Reset value
[31:15]	Reserved	RO	Reserved	0
14	LINEN	RW	LIN mode enable, set to enable LIN mode. The LIN mode enables the capability to send LIN Synch Breaks using the SBK bit in the USART_CR1 register, and to detect LIN Sync breaks.	0
[13:12]	STOP[1:0]	RW	STOP bits. These bits are used for programming the stop bits. 00: 1 Stop bit 01: 0.5 Stop bit 10: 2 Stop bits 11: 1.5 Stop bit	0
11	CLKEN	RW	Clock enable. This bit allows the user to enable the CK pin. 0: CK pin disabled 1: CK pin enabled	0
10	CPOL	RW	Clock polarity This bit allows the user to select the polarity of the clock output on the CK pin in synchronous mode. It works in conjunction with the CPHA bit to produce the desired clock/data relationship 0: Steady low value on CK pin outside transmission window. 1: Steady high value on CK pin outside transmission window. *Note: This bit cannot be modified after enabling transmit.*	0
9	CPHA	RW	Clock phase This bit allows the user to select the phase of the clock output on the CK pin in synchronous mode. It works in conjunction with the CPOL bit to produce the desired clock/data relationship 0: The first clock transition is the first data capture edge. 1: The second clock transition is the first data capture edge. *Note: This bit cannot be modified after enabling transmit.*	0
8	LBCL	RW	Last bit clock pulse This bit allows the user to select whether the clock pulse associated with the last data bit transmitted (MSB) has to be output on the CK pin in synchronous mode. 0: The clock pulse of the last data bit is not output to the CK pin	0

			1: The clock pulse of the last data bit is output to the CK pin *Note: This bit cannot be modified after enabling transmit.*	
7	Reserved	RW	Reserved	0
6	LBDIE	RW	LIN Break detection interrupt enable, this position bit enables interrupts caused by LBD.	0
5	LBDL	RW	LIN Break detection length, this bit is used to select whether the Break character detection is 11 bits or 10 bits. 1: 11-bit Break character detection. 0: 10-bit Break character detection.	0
4	Reserved	RW	Reserved	0
[3:0]	ADD[3:0]	RW	Address of the USART node, this bit-field gives the address of the USART node. This is used in multiprocessor communication during mute mode, for wake up with address mark detection.	0

12.10.6 USART Control Register 3 (USART_CTLR3)

Offset address: 0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					CTSIE	CTSE	RTSE	DMAT	DMAR	SCEN	NACK	HDSEL	IRLP	IREN	EIE

Bit	Name	Access	Description	Reset value
[31:11]	Reserved	RO	Reserved	0
10	CTSIE	RW	CTS interrupt enable bit, when this bit is set, an interrupt will be generated when CTS is set.	0
9	CTSE	RW	CTS enable bit, setting this bit will enable CTS flow control.	0
8	RTSE	RW	RTS enable bit, setting this bit will enable RTS flow control.	0
7	DMAT	RW	DMA transmit enable bit. This bit 1 uses DMA when transmitting.	0
6	DMAR	RW	DMA receive enable bit. This position 1 uses DMA on receive.	0
5	SCEN	RW	Smartcard mode enable bit, set to 1 to enable smart card mode.	0
4	NACK	RW	Smartcard NACK enable bit, set this bit to send NACK in case of check error.	0
3	HDSEL	RW	Half-duplex selection bit, set this bit to select half-duplex mode.	0
2	IRLP	RW	IrDA low-power bit, set this bit to enable low-power mode when IrDA is selected.	0
1	IREN	RW	IrDA enable bit, set this bit to enable infrared mode.	0
0	EIE	RW	Error interrupt enable bit, when set, generates an interrupt if FE, ORE or NE is set provided that DMAR is set.	0

12.10.7 USART Guard Time and Prescaler Register (USART_GPR)

Offset address: 0x18

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GT[7:0]								PSC[7:0]							

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
[15:8]	GT[7:0]	RW	Guard time value. This bit-field gives the Guard time value in terms of number of baud clocks. This is used in Smartcard mode. The Transmission Complete flag is set after this guard time value.	0
[7:0]	PSC[7:0]	RW	Prescaler value field. In IrDA Low-power mode, the source clock is divided by this value (all 8 bits valid), with a value of 0 indicating retention. In normal IrDA mode, this bit can only be set to 1. In smartcard mode, the source clock is divided by twice this value (valid in the lower 5 bits) to clock the smart card, with a value of 0 indicating retention.	0