

CH32V003 Datasheet

V1.4

Overview

CH32V003 series is an industrial-grade general-purpose microcontroller designed based on QingKe RISC-V2A core, which supports 48MHz system main frequency in the product function. The series features wide voltage, single-wire serial debug interface, low-power consumption and ultra-small package. It provides commonly used peripheral functions, built-in 1 group of DMA controller, 1 group of 10-bit analog-to-digital conversion ADC, 1 group of op-amp comparator, multiple timers, standard communication interfaces such as USART, I2C, SPI, etc. The rated operating voltage of the product is 3.3V or 5V, and the operating temperature range is -40°C~85°C industrial- grade.

Features

Core

- QingKe 32-bit RISC-V core, RV32EC instruction set
- Fast programmable interrupt controller + hardware interrupt stack
- Support 2-level interrupt nesting
- Support system main frequency 48MHz

Memory

- 2KB volatile data storage area SRAM
- 16KB program memory CodeFlash
- 1920B BootLoader
- 64B non-volatile system configuration memory
- 64B user-defined memory

Power management and low-power consumption

- System power supply V_{DD} : 3.3V or 5V
- Low-power mode: Sleep, Standby

Clock & Reset

- Built-in factory-trimmed 24MHz RC oscillator
- Built-in 128KHz RC oscillator
- High-speed external 4~25MHz oscillator
- Power on/down reset, programmable voltage detector

• 1 group of 1-channel general-purpose DMA controller

- 7 channels, support ring buffer
- Support TIMx/ADC /USART/I2C/SPI

• 1 group of OPA and comparator: connected with ADC and TIM2

• 1 group of 10-bit ADC

- Analog input range: 0~V_{DD}
- 8 external signals + 2 internal signals
- Support external delayed triggering

Multiple timers

- 1 16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
- 1 16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
- 2 watchdog timers (independent watchdog and window watchdog)
- SysTick: 32-bit counter

Communication interfaces

- 1 USART interfaces
- 1 I2C interfaces
- 1 SPI interfaces

GPIO port

- 3 groups of GPIO ports, 18 I/O ports
- Mapping 1 external interrupt
- Security features: 64-bit unique ID
- Debug mode: 1-wire serial debug interface (SDI)
- Package: SOP, TSSOP or QFN

Model	Flash memory	SRAM	Pin	General- purpose I/O	Advanced- control timer		Watchdog	System clock source	Channe		I2C	USART	Package Form
CH32V003F4P6	16K	2K	20	18	1	1	2	3	8	1	1	1	TSSOP20
CH32V003F4U6													QFN20
CH32V003A4M6	16K	2K	16	14	1	1	2	3	6		1	1	SOP16
CH32V003J4M6	16K	2K	8	6	1	1	2	3	6	_	1	1	SOP8