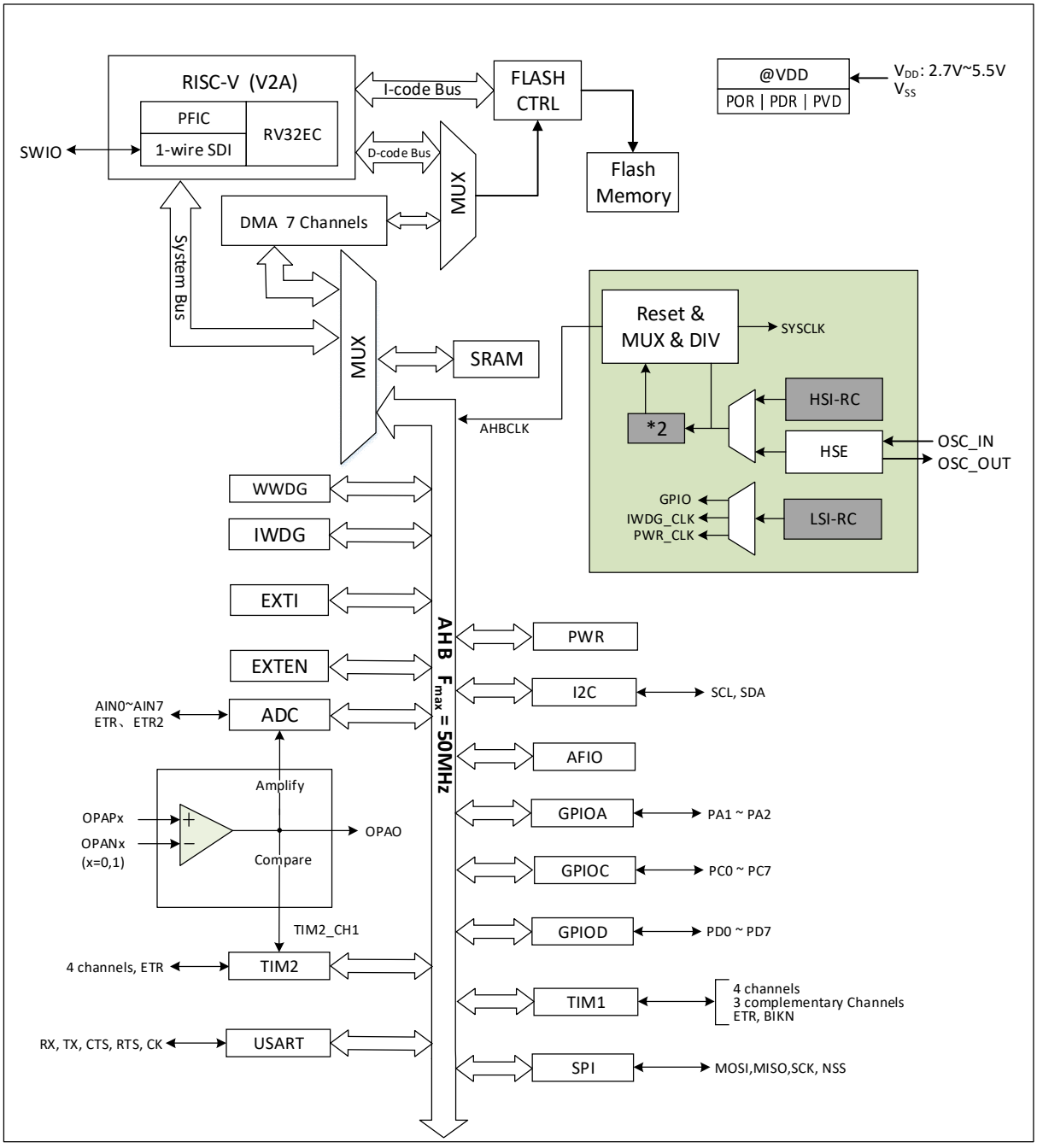
Chapter 1 Specification

1.1 System architecture

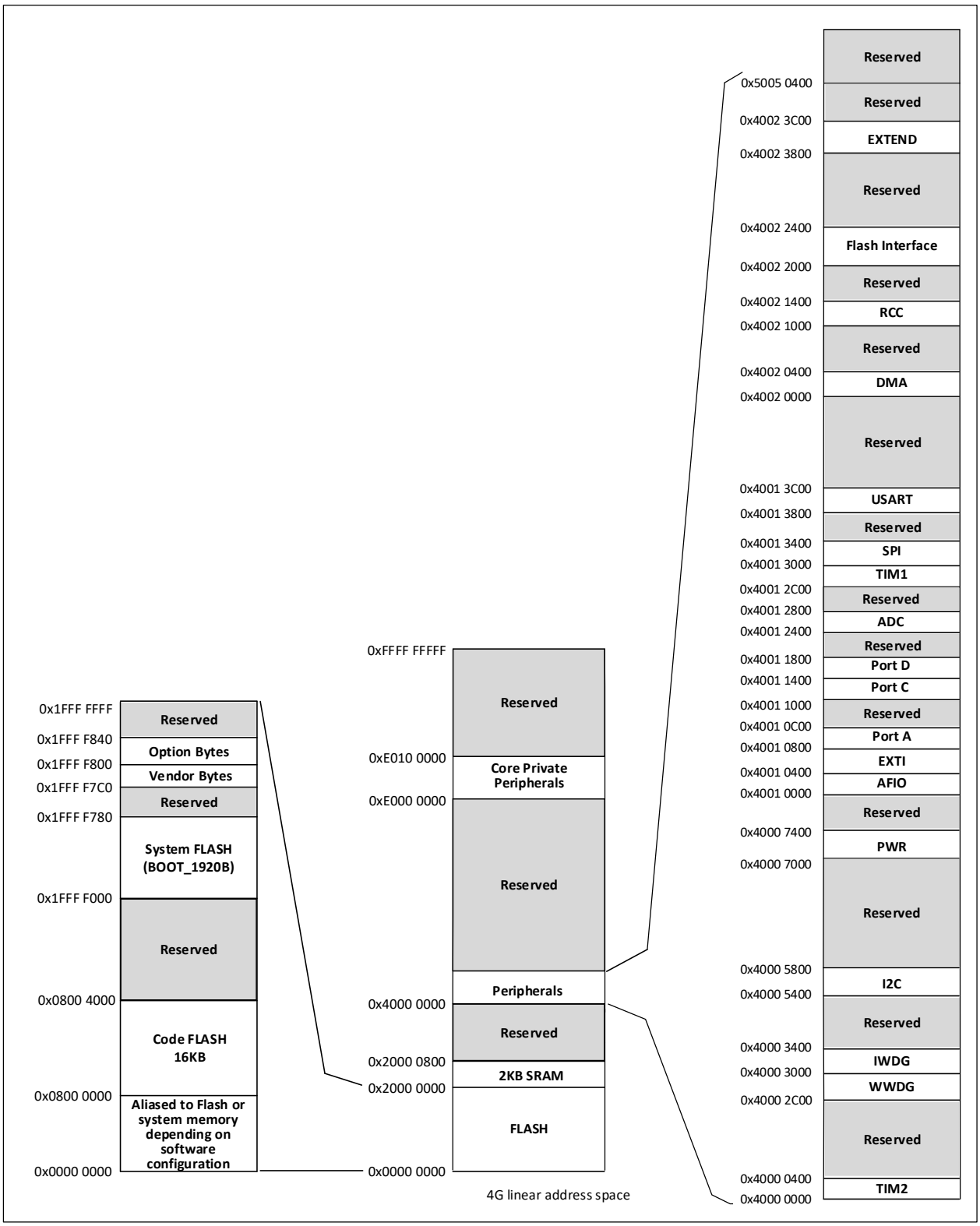
The microcontroller is based on the RISC-V instruction set of QingKe V2A design, and its architecture includes the core, arbitration unit, DMA module, SRAM storage and other parts of the interaction through multiple groups of buses. The design integrates a general-purpose DMA controller to reduce CPU load and improve access efficiency, and also has data protection mechanisms and automatic clock switching protection to increase system stability. The following diagram shows the overall architecture of the product.

Figure 1-1 System block diagram



1.2 Memory map

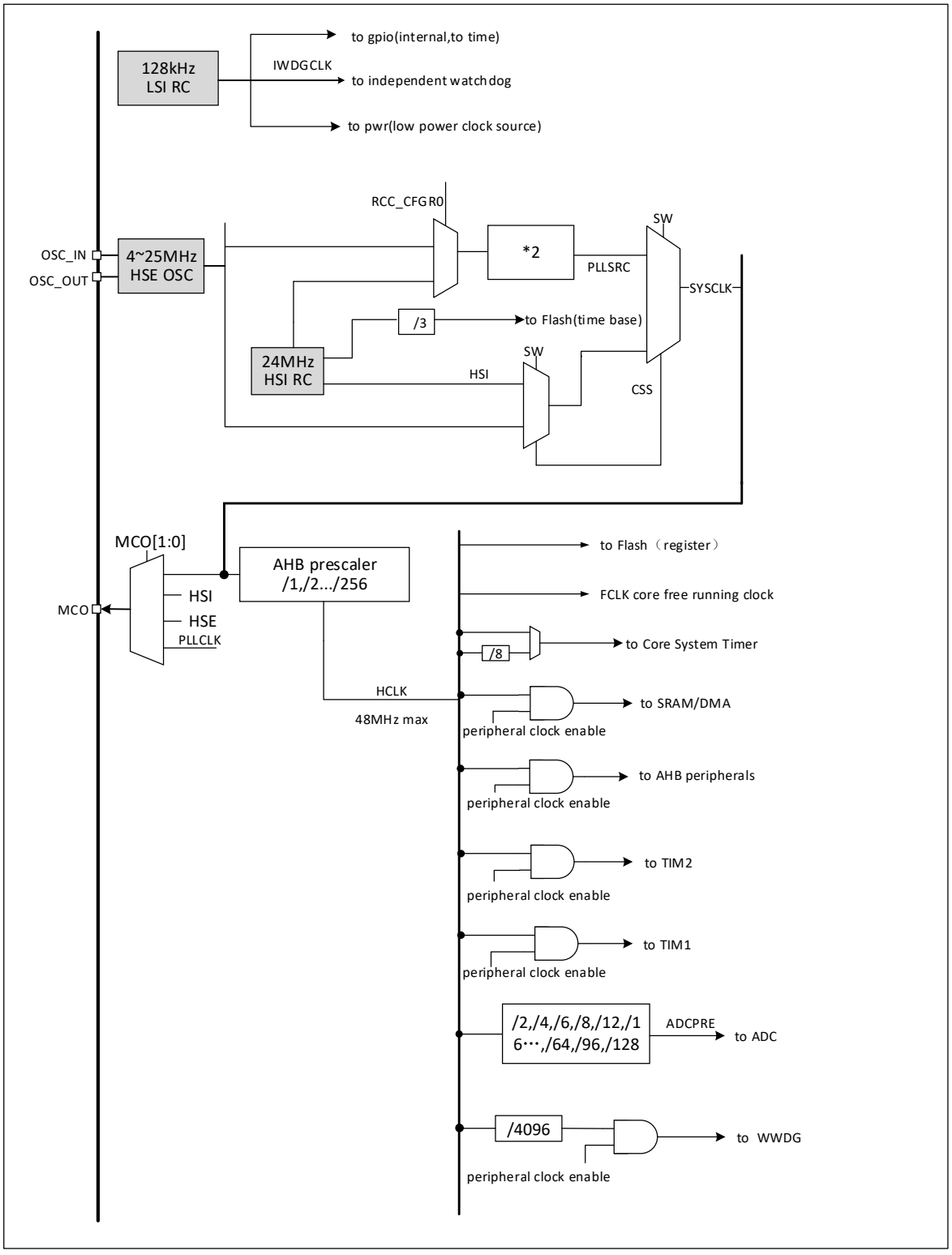
Figure 1-2 Memory address map



1.3 Clock tree

Three groups of clock sources are introduced into the system: internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI), external high-frequency oscillator (HSE), and external low-frequency oscillator (LSE). Among them, the low-frequency clock source provides the clock reference for RTC and independent watchdog. The high-frequency clock source is directly or indirectly output as system clock (SYSCLK) via 2X frequency. The system clock is then provided by each prescaler to provide the AHB domain in peripheral control clock and sampling or output clock. Some modules need to be directly provided by the PLL clock.

Figure 1-3 Clock tree block diagram



1.4 Functional description

1.4.1 RISC-V2A processor

The RISC-V2A supports the EC subset of the RISC-V instruction set. The processor is managed internally in a modular fashion and contains units such as a fast programmable interrupt controller (PFIC), extended instruction support, and more. The bus is connected to an external unit module to enable interaction between the external function module and the core. RV32EC instruction set, small-end data mode.

The processor with its minimal instruction set, multiple operating modes, and modular custom expansion can be flexibly applied to different scenarios of microcontroller design, such as small area low-power embedded scenarios.

- Support machine mode
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- 1-wire serial debug interface (SDI)
- Custom extended commands

1.4.2 On-chip memory and boot mode

Built-in 2K bytes SRAM area for data storage, data loss after power down.

Built-in 16K bytes of program flash memory storage (Code FLASH) for user applications and constant data storage.

Built-in 1920 bytes of system storage (System FLASH) for system bootloader storage (factory-cured bootloader)

64 bytes are used for the system non-volatile configuration information storage area and 64 bytes are used for the user select word storage area.

Support Boot and user code jumping to each other.

1.4.3 Power supply scheme

V_{DD} = 2.7～5.5V: Power supply for some I/O pins and internal voltage regulator (V_{DD} performance gradually deteriorates if less than 2.9V when using ADC).

1.4.4 Power supply monitor

This product integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in working condition to ensure that the system is in supply. It works when the power exceeds 2.7V; when V_{DD} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without using an external reset circuit.

In addition, the system is equipped with a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage of V_{DD} power supply with the set threshold V_{PVD}.Turn on the corresponding edge interrupt of PVD, and you can receive interrupt notification when V_{DD} drops to the PVD threshold or rises to the PVD threshold. Refer to Chapter 4 for the values of $V_{POR/PDR}$ and V_{PVD}.

1.4.5 Voltage regulator

After reset, the regulator is automatically turned on, and there are 3 operation modes according to the application mode.

- ON mode: Normal operation, providing stable core power.
- Low-power mode: When the CPU enters Stop mode, system automatically enters Standby mode.

1.4.6 Low-power mode

The system supports 2 low-power modes, which can be selected for low-power consumption, short start-up time and multiple wake-up events to achieve the best balance.

- Sleep mode

In Sleep mode, only the CPU clock is stopped, but all peripheral clocks are powered normally and the peripherals are in a working state. This mode is the shallowest low-power mode, but it is the fastest mode to wake up the system.
Exit condition: any interrupt or wake-up event.

- Standby mode

The PDDS and SLEEPDEEP bits are set, and the WFI/WFE instruction is executed to enter. The power supply of the kernel part is turned off, and the RC oscillator of HSI and the HSE crystal oscillator are also turned off, and the lowest power consumption can be achieved in this mode.
Exit conditions: any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset, where EXTI signal includes one of 18 external I/O ports, output of PVD, AWU auto-wakeup.

1.4.7 Fast Programmable Interrupt Controller (PFIC)

The product's built-in Fast Programmable Interrupt Controller (PFIC) supports up to 255 interrupt vectors, providing flexible interrupt management capabilities with minimal interrupt latency. The current product manages 4 core private interrupts and 23 peripheral interrupt management, with other interrupt sources reserved. the registers of PFIC are all accessible in machine privileged mode.

- 2 individually maskable interrupts
- Provide a non-maskable interrupt NMI
- Hardware interrupt stack (HPE) support without instruction overhead
- Provide 2-way meter-free interrupt (VTF)
- Vector table supports address or command mode
- Support 2-level interrupt nesting
- Support break tail link function

1.4.8 External interrupt/event controller (EXTI)

The external interrupt/event controller contains a total of 8 edge detectors for generating interrupt/event requests. Each interrupt line can be independently configured with its trigger event (rising or falling edge or double edge) and can be individually masked; the pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal AHB. 18 general purpose I/O ports are optionally connected to the same external interrupt source.

1.4.9 General-purpose DMA controller

The system has built-in 1 group of general-purpose DMA controllers, manages 8 channels in total, and flexibly handles high-speed data transmission from memory to memory, peripherals to memory, and memory to peripherals, and supports ring buffer mode. Each channel has a dedicated hardware DMA request logic to support one or more peripherals' access requests to the memory. The access priority, transfer length, source address and destination address of the transfer can be configured.

The main peripherals used by DMA include: general-purpose/advanced-control/basic timers TIMx, DAC,

USART, I2C and SPI.

Note: DMA and CPU access the system SRAM after arbitration by the arbiter.

1.4.10 Clock and boot

The system clock source HSI is turned on by default. After the clock is not configured or reset, the internal 24MHz RC oscillator is used as the default CPU clock, and then an external 4~25MHz clock or PLL clock can be additionally selected. When the clock security mode is turned on, if the HSE is used as the system clock (directly or indirectly), the system clock will automatically switch to the internal RC oscillator when the external clock is detected to be invalid, and the HSE and PLL will be automatically turned off at the same time; in low-power consumption mode, the system will automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt.

1.4.11 Analog-to-digital converter (ADC)

The product is embedded with a 10-bit analog/digital converter (ADC) that shares up to eight external channels and two internal channel samples, with programmable channel sampling times for single, continuous, sweep or intermittent conversion. Provides analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring channel signal voltages. Supports external event-triggered transitions with trigger sources including internal signals from the on-chip timer and external pins. Support for using DMA operation. Supports external trigger delay function. When this function is enabled, the controller delays the trigger signal according to the configured delay time when an external trigger edge is generated, and the ADC conversion is triggered as soon as the delay time is reached.

1.4.12 Timer and watchdog

The timers in the system include an advanced-control timer, a general-purpose timer, two watchdog timers and system time base timer.

- Advanced-control timer

The advanced-control timer is a 16-bit auto-loading up/down counter with a 16-bit programmable prescaler. In addition to the complete general-purpose timer function, it can be regarded as a three-phase PWM generator distributed to 6 channels, with a complementary PWM output function with dead zone insertion, allowing the timer to be updated after a specified number of counter cycles to repeat counting cycle, braking function, etc. Many functions of the advanced-control timer are the same as the general timer, and the internal structure is also the same. Therefore, the advanced-control timer can cooperate with other TIM timers through the timer link function to provide synchronization or event link functions.

- General-purpose timer

The general-purpose timer is a 16-bit or 32-bit auto-loading up/down counter with a programmable 16-bit prescaler and 4 independent channels. Each channel supports input capture, output comparison, and PWM generation and single pulse mode output. It can also work with advanced-control timers through the timer link function to provide synchronization or event link functions. In Debug mode, the counter can be frozen while the PWM outputs are disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism. These timers can also process signals from incremental encoders, as well as digital outputs from 1 to 3 Hall sensors.

- Independent watchdog

The independent watchdog is a configurable 12-bit down counter that supports 7 frequency division factors. The clock is provided by an internal independent 128 KHz RC oscillator (LSI); because the LSI is independent of the main clock, it can run in Stop and Standby modes. IWDG is outside the main program and can work completely independently. Therefore, it is used to reset the entire system when a problem occurs, or as a free timer to provide timeout management for the application. It can be configured as software or hardware to start the watchdog through the option byte. In Debug mode, the counter can be frozen.

- Window Watchdog

The window watchdog is a 7-bit down counter and can be set to free-running. It can be used to reset the entire system when a problem occurs. It is driven by the main clock and has an early warning interrupt function; in Debug mode, the counter can be frozen.

- SysTick Timer

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be used exclusively in real-time operating systems to provide a "heartbeat" rhythm for the system, or as a standard 32-bit counter. It has an automatic reload function and a programmable clock source.

1.4.13 Communication interface

1.4.13.1 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The product provides 1 group of Universal Synchronous/Asynchronous Receiver Transmitters (USART). It supports full-duplex asynchronous communication, synchronous one-way communication and half-duplex single-wire communication. It also supports LIN (Local Interconnect Network), compatible with ISO7816 smart card protocol and IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation. It also allows multi-processor communication. It uses a fractional baud rate generator system and supports DMA operation continuous communication.

1.4.13.2 Serial Peripheral Interface (SPI)

1 serial peripherals interface (SPI) provide master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8 or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

1.4.14.3 I2C bus

1 I2C bus interface, able to work in multi-master mode or slave mode, complete with all I2C bus specific timing, protocols, arbitration, etc., supporting both standard and fast communication speeds.
The I2C interface provides 7-bit or 10-bit addressing and supports dual slave address addressing in 7-bit slave mode. A hardware CRC generator/checker is built-in.

1.4.14 General-purpose input and output (GPIO)

The system provides 3 groups of GPIO ports with a total of 18 GPIO pins. Each pin can be configured by software as output (push-pull or open-drain), input (with or without pull-up or pull-down) or multiplexed peripheral function port. Most GPIO pins are shared with digital or analog multiplexed peripherals. Except for ports with analog input functions, all GPIO pins have high current passing capabilities. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.

The I/O pins in the system is provided by V_{DD}. Changing the V_{DD} power supply will change the high value of the I/O pin output level to adapt to the external communication interface level. Please refer to the pin description for specific pins.

1.4.15 Operational amplifier/comparator (OPA)

The product has a built-in set of op-amps/comparators, with internal selection associated to the ADC and TIM2 (CH1) peripherals, whose inputs and outputs can be selected by changing the configuration for multiple channels. Support for external analog small signals are amplified and fed into the ADC to achieve small signal ADC conversion, can also complete the signal comparator function, the comparison results from the GPIO output or directly into the TIMx input channel.

1.4.16 1-wire serial debug interface (SDI)

The core comes with a 1-wire serial debug interface, SWIO pin (Single Wire Input Output). The default debug interface pin function is turned on after system power on or reset.