Chapter 9 Analog-to-digital Converter (ADC)

The ADC module contains a 10-bit successive approximation type analog-to-digital converter with up to 24MHz input clock. It supports 8 external channels and 2 internal signal source sampling sources. Single conversion and continuous conversion of channels, automatic scan mode between channels, intermittent mode, external trigger mode, double sampling, trigger delay, etc. can be accomplished. The channel voltage can be monitored to see if it is within the threshold range by using the analog watchdog function.

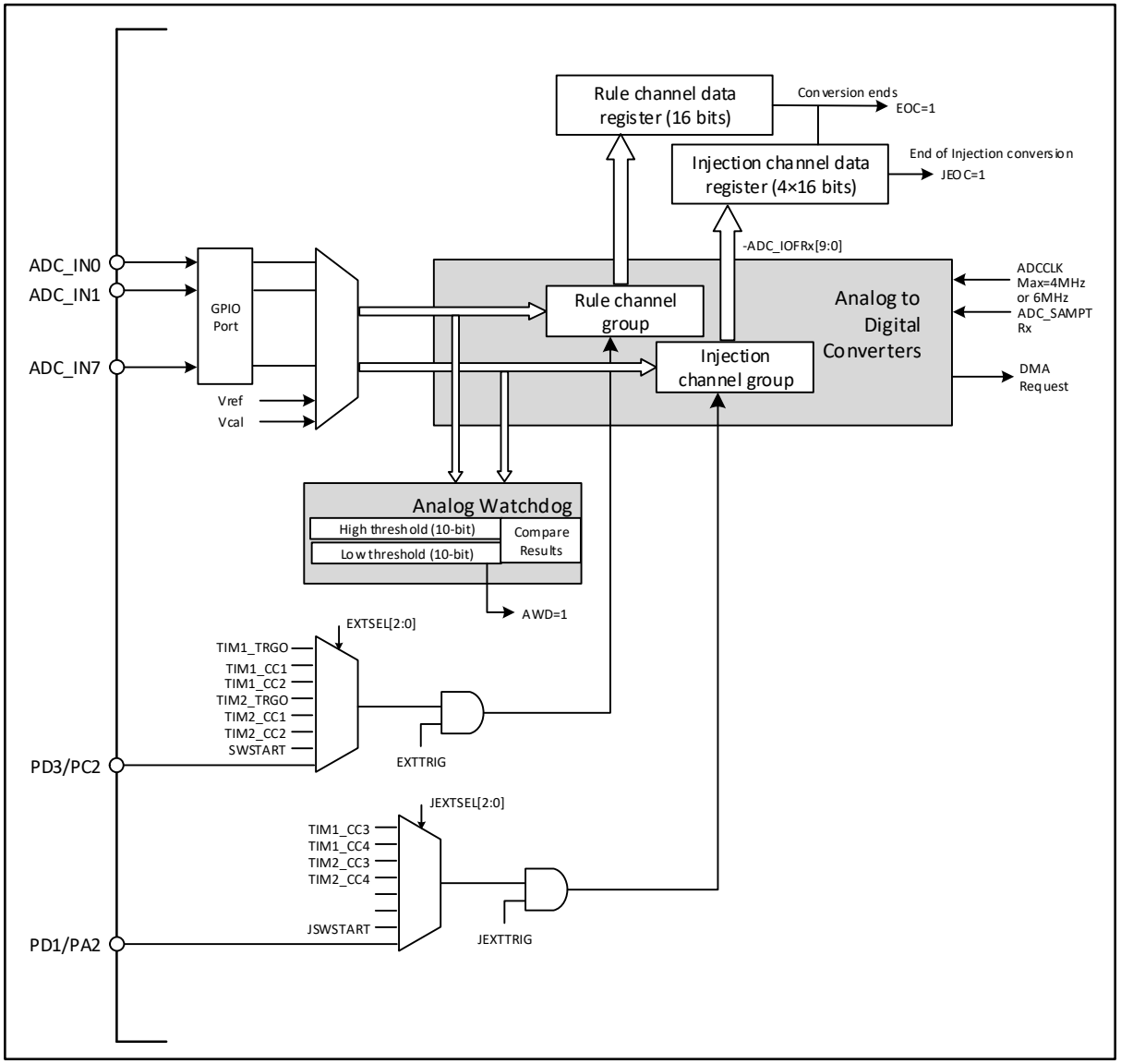
9.1 Main Features

- 10-bit resolution
- Supports 8 external channels and 2 internal signal sources for sampling
- Multiple sampling conversion methods for multiple channels: single, continuous, scan, trigger, intermittent, etc.
- Data alignment modes: left-aligned, right-aligned
- Sampling time can be programmed separately by channel
- Both rule conversion and injection conversion support external triggering
- Analog watchdog to monitor channel voltage, self-calibration function
- ADC channel input range: $0 \leqslant V_{IN} \leqslant V_{DDA}$
- Trigger delay

9.2 Functional Description

9.2.1 Module Structure

Figure 9-1 ADC module block diagram



9.2.2 ADC Configuration

1) Module power-up

An ADON bit of 1 in the ADC_CTLR2 register indicates that the ADC module is powered up. When the ADC module enters the power-up state (ADON=1) from the power-down mode (ADON=0), a delay period t_{STAB} is required for the module stabilization time. After that, the ADON bit is written to 1 again and is used as the start signal for software to start the ADC conversion. By clearing the ADON bit to 0, the current conversion can be terminated and the ADC module placed in power-down mode, a state in which the ADC consumes almost no power.

2) Sampling clock

The register operation of the module is based on the HBCLK (HB bus) clock, and the clock reference of its conversion unit, ADCCLK, is configured by the ADCPRE field of the RCC_CFGR0 register to divide the frequency. Refer to datasheet *CH32V003DS0* for detailed information.

3) Channel configuration

The ADC module provides 10 channel sampling sources, including 8 external channels and 2 internal channels. They can be configured into two types of conversion groups: regular groups and injection groups. to achieve a group conversion consisting of a series of conversions in any order on any number of channels.
Conversion group.

- Rule group: consists of up to 16 conversions. The rule channels and their conversion order are set in the ADC_RSQRx register. The total number of conversions in the rule group should be written to L[3:0] in the ADC_RSQR1 register.
- Injection group: consists of up to 4 conversions. The injection channels and the order of their conversions are set in the ADC_ISQR register. The total number of conversions in the injection group should be written in JL[1:0] of the ADC_ISQR register.

Note: If the ADC_RSQRx or ADC_ISQR registers are changed during conversion, the current conversion is terminated and a new start signal is sent to the ADC to convert the newly selected group.

2 internal channels.

- Vref internal reference voltage: connected to ADC_IN8 channel.
- Vcal internal calibration voltage: connected to ADC_IN9 channel, 2 steps selectable.

4) Calibration

The ADC has a built-in self-calibration mode. A calibration session significantly reduces accuracy errors due to variations in the internal capacitor banks. During calibration, an error correction code is calculated on each capacitor, which is used to eliminate the errors generated on each capacitor in subsequent conversions.
Initialize the calibration register by writing RSTCAL position 1 of ADC_CTLR2 register and wait for RSTCAL hardware to clear 0 to indicate the completion of initialization. Set the CAL bit to start the calibration function. Once the calibration is finished, the hardware will automatically clear the CAL bit and store the calibration code into ADC_RDATAR. After that, the normal conversion function can be started. It is recommended to perform an ADC calibration when the ADC module is powered up.
Note: Before starting the calibration, you must ensure that the ADC module is in the power-up state (ADON=1) for more than at least two ADC clock cycles.

5) Programmable sampling time

The ADC uses several ADCCLK cycles to sample the input voltage. The number of sampling cycles for a channel can be changed using the SMPx[2:0] bits in the ADC_SAMPTR1 and ADC_SAMPTR2 registers. Each channel can be sampled separately using a different time.
The total conversion time is calculated as follows.

$$T_{CONV} = \text{sampling time} + 11T_{ADCCLK}$$

The ADC's rule channel conversion supports the DMA function. The value of the rule channel conversion is stored in a data-only register, ADC_RDATAR. To prevent the data in ADC_RDATAR register from being fetched in time when multiple rule channels are converted in succession, the DMA function of ADC can be enabled. The hardware will generate a DMA request at the end of the conversion of a rule channel (EOC set) and transfer the converted data from the ADC_RDATAR register to the user-specified destination address.
After the channel configuration of the DMA controller module is completed, write DMA position 1 of the ADC_CTLR2 register to enable the DMA function of the ADC.
Note: Injection group conversion does not support DMA function.

6) Data alignment

The ALIGN bit in the ADC_CTLR2 register selects the alignment of the ADC converted data storage. 10-bit data supports left-aligned and right-aligned modes.
The data register ADC_RDATAR of the rule group channel holds the actual converted 10-bit digital value; while the data register ADC_IDATARx of the injection group channel is the actual converted data minus the value written after the offset defined in the ADC_IOFRx register, there will be positive and negative cases, so

there are sign bits (SIGNB).

Table 9-1 Data left alignment

Rule group data register

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0	0

Inject group data register

SIGNB	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0	0

Table 9-2 Data right alignment

Rule group data register

0	0	0	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Inject group data register

SIGNB	SIGNB	SIGNB	SIGNB	SIGNB	SIGNB	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

9.2.3 External Trigger Source

The ADC conversion start event can be triggered by an external event. If the EXTTRIG or JEXTTRIG bits of the ADC_CTLR2 register are set, the conversion of a rule group or injection group channel can be triggered by an external event, respectively. In this case, the configuration of EXTSEL[2:0] and JEXTSEL[2:0] bits determines the external event source for the rule group and injection group.

Note: When an external trigger signal is selected for ADC rule or injection conversion, only its rising edge can start the conversion.

Table 9-3 External trigger sources for rule group channels

EXTSEL[2:0]	Trigger source	Type
000	TRGO event of timer 1	Internal signal from on-chip timer
001	CC1 event of timer 1	
010	CC2 event of timer 1	
011	TRGO event of timer 2	
100	CC1 event of timer 2	
101	CC2 event of timer 2	
110	PD3/PC2 events	From external pins
111	SWSTART software trigger	Software control bits

Table 9-4 External trigger sources for injection group channels

JEXTSEL[2:0]	Trigger source	Type
000	CC3 event of timer 1	Internal signal from on-chip timer
001	CC4 event of timer 1	
010	CC3 event of timer 2	
011	CC4 event of timer 2	
100	-	
101	-	
110	PD1/PA2	From external pins
111	JSWSTART software trigger	Software control bits

9.2.4 Conversion Mode

Table 9-5 Conversion mode combinations

ADC_CTLR1 and ADC_CTLR2 register control bits					ADC conversion mode
CONT	SCAN	RDISCEN/IDISCEN	JAUTO	Start event	
0	0	0	0	ADON position 1	Single single-channel mode: A rule channel performs a single conversion.
				External trigger method	Single single-channel mode: A single conversion is performed on one of the rule channels or injection channels.

	1	0	0	ADON position 1 or external trigger method	Single scan mode: performs a single conversion of all selected rule group channels (ADC_RSQRx) or all injection group channels (ADC_ISQR) one by one in sequence. Trigger injection method: When the rule group channel conversion process can be inserted into the injection group channel all conversion, and then continue the rule group channel conversion afterwards; but the rule group channel conversion will not be inserted when converting the injection group channel.
			1	ADON position 1 or external trigger method	Single scan mode: performs a single conversion of all selected rule group channels (ADC_RSQRx) or all injection group channels (ADC_ISQR) one by one in sequence. Automatic injection method: After the rule group channel is converted, the injection group channel is automatically converted.
	0	1 (RDISCEN and IDISCEN cannot be 1 at the same time)	0	External trigger method	Single intermittent mode: Each time an event is started, a short sequence (DISCNUM[2:0] defined number) of channel number transitions is executed and cannot be restarted until all selected channel transitions are completed. *Note: The IDISCEN and RDISCEN control bits are selected for the rule group and injection group respectively, and the intermittent mode cannot be configured for the rule group and injection group at the same time.*
			1	-	Disable this mode.
	1	1	X	-	No such mode.
1	0	0	0	ADON position 1 or external trigger method	Continuous single channel/scan mode: repeat a new round of transitions at the end of each round until CONT clears 0 to terminate.
	1	0	0		
			1		

Note: The external trigger events for rule groups and injection groups are different, and the 'ACON' bit can only initiate rule group channel conversion, so the initiation events for rule group and injection group channel conversion are independent.

1) Single single-channel conversion mode

In this mode, only one conversion is executed for the current 1 channel. This mode performs conversion for the channel that is sorted 1st in the rule group or injection group, where it is initiated by setting ADON position 1 of the ADC_CTLR2 register (for rule channels only) or can be initiated by external trigger (for rule channels or injection channels). Once the conversion of the selected channel is completed it will.

If the conversion is for a rule group channel, the conversion data is stored in the 16-bit ADC_RDATAR register, the EOC flag is set, and an ADC interrupt is triggered if the EOCIE bit is set.

If the conversion is for an injection group channel, the conversion data is stored in the 16-bit ADC_IDATAR1 register, the EOC and JEOC flags are set, and an ADC interrupt is triggered if the JEOCIE or EOCIE bit is set.

2) Single scan mode conversion

The ADC scan mode is entered by setting the SCAN bit of the ADC_CTLR1 register to 1. This mode is used

to scan a group of analog channels and perform a single conversion for all channels selected by ADC_RSQRx register (for regular channels) or ADC_ISQR (for injection channels) one by one, and the next channel in the same group is converted automatically when the current channel conversion is finished.
In the scan mode, there is a subdivision into triggered injection mode and automatic injection mode depending on the status of the JAUTO bit.

- Trigger injection

JAUTO bit is 0. When the trigger event of injection group channel conversion occurs during the scanning of rule group channels, the current conversion is reset and the sequence of injection channels is performed in a single scan, and the last interrupted rule group channel conversion is resumed after all selected injection group channel scanning conversions are completed.
If a rule channel start event occurs while the injection group channel sequence is currently being scanned, the injection group conversion is not interrupted, but the rule sequence conversion is executed again after the injection sequence conversion is completed.
Note: When using triggered injection conversions, you must ensure that the interval between triggered events is longer than the injection sequence. For example, if the overall time to complete the conversion of the injection sequence takes 28 ADCCLK, then the minimum value of the event interval to trigger the injection channel is 29 ADCCLK.

- Auto-injection

The JAUTO bit is set to 1, and conversion of the selected channel of the injection group is performed automatically after scanning all the channels selected by the rule group for conversion. This approach can be used to convert up to 20 conversion sequences in the ADC_RSQRx and ADC_ISQR registers.
In this mode, external triggering of the injection channel must be disabled (IEXTTRIG JEXTTRIG=0).
Note: For ADC clock prescaler factor (ADCPRE[1:0]) of 4 to 8, 1 ADCCLK interval is automatically inserted when switching from rule conversion to injection sequence or from injection conversion to rule sequence; when ADC clock prescaler factor is 2, there is a delay of 2 ADCCLK intervals.

3) Single intermittent mode conversion

The intermittent mode of the rule group or injection group is entered by setting the RDISCEN or IDISCEN bit of the ADC_CTLR1 register to 1. This mode differs from scanning a complete set of channels in scan mode, but divides a set of channels into multiple short sequences, and each external trigger event will perform a short sequence of scan transitions.
The length of the short sequence n (n<=8) is defined in DISCNUM[2:0] of ADC_CTLR1 register, when RDISCEN is 1, it is the interrupted mode of the rule group, and the total length to be converted is defined in L[3:0] of ADC_RSQR1 register; when IDISCEN is 1, it is the interrupted mode of the injection group, and the total length to be converted is defined in JL[1:0] of ADC_ISQR register. It is not possible to set both the rule group and the injection group to intermittent mode.
Example of rule group intermittent mode.

RDISCEN=1, DISCNUM[2:0]=3, L[3:0]=8, channels to be converted = 1, 3, 2, 5, 8, 4, 10, 6
The 1st external trigger: conversion sequence is: 1, 3, 2
The 2nd external trigger: conversion sequence is: 5, 8, 4
The 3rd external trigger: conversion sequence is: 10, 6, while generating EOC events
The 4th external trigger: conversion sequence is: 1, 3, 2

Examples of intermittent patterns injected into groups.

IDISCEN=1, DISCNUM[2:0]=1, JL[1:0]=3, channel to be converted=1, 3, 2
The 1st external trigger: conversion sequence is: 1
The 2nd external trigger: the conversion sequence is: 3
The 3rd external trigger: conversion sequence is: 2, generating both EOC and JEOC events
The 4th external trigger: conversion sequence is: 1

Note: 1. When converting a rule group or injection group in intermittent mode, the conversion sequence does not automatically start from the beginning when it ends. When all subgroups have been converted, the next trigger event starts the conversion of the first subgroup.

2. You cannot use auto-injection (JAUTO=1) and intermittent mode at the same time.

3. You cannot set intermittent mode for both rule groups and injection groups, and intermittent mode can only be used for a group of conversions.

4) Continuous conversion

In the continuous conversion mode, another conversion is started as soon as the previous ADC conversion is completed. The conversion will not stop on the last channel of the selection group, but will continue conversion from the first channel of the selection group again. The startup events in this mode include external trigger events and the ADON bit is set to 1. After setting the startup, the CONT bit needs to be set to 1.

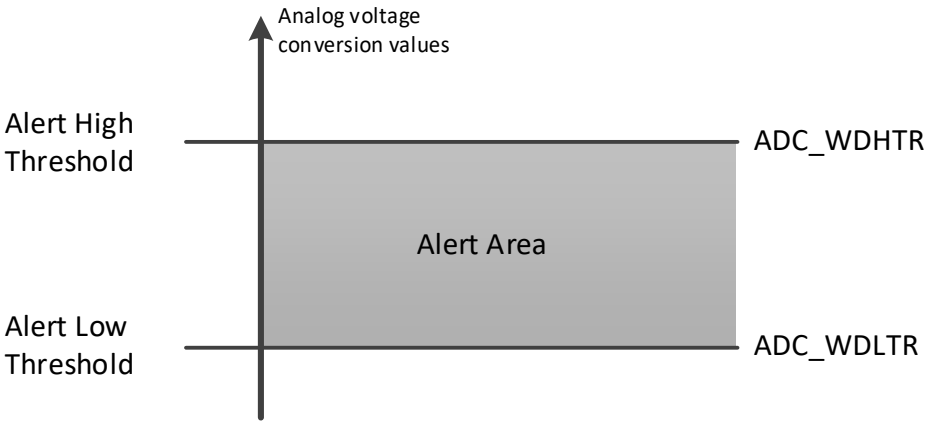
If a regular channel is converted, the conversion data is stored in the ADC_RDATAR register, the conversion end flag EOC is set, and if EOCIE is set, an interrupt is generated.

If an injection channel is converted, the conversion data is stored in the ADC_IDATARx register, the injection conversion end flag JEOC is set, and if JEOCIE is set, an interrupt is generated.

9.2.5 Analog Watchdog

The AWD analog watchdog status bit is set if the analog voltage being converted by the ADC is below the low threshold or above the high threshold. The threshold settings are located in the lowest 10 valid bits of the ADC_WDHTR and ADC_WDLTR registers. The AWDIE bit of the ADC_CTLR1 register is set to allow the corresponding interrupt to be generated.

Figure 9-4 Analog watchdog threshold area



Configure the AWDSGL, AWDEN, JAWDEN and AWDCH[4:0] bits of the ADC_CTLR1 register to select the channel for analog watchdog alerting, as related in the following table.

Table 9-6 Analog Watchdog channel selection

Simulation of watchdog alert channel	ADC_CTLR1 register control bit			
	AWDSGL	AWDEN	JAWDEN	AWDCH[4:0]
No vigilance	Ignore	0	0	Ignore
All injection channels	0	0	1	Ignore
All rule channels	0	1	0	Ignore
All injection and rule channels	0	1	1	Ignore
Single injection channel	1	0	1	Determine the channel number
Single rule channel	1	1	0	Determine the channel number
Single injection and rule channel	1	1	1	Determine the channel number

9.3 Register Description

Table 9-7 ADC-related registers list

Name	Access address	Description	Reset value
R32_ADC_STATR	0x40012400	ADC status register	0x00000000
R32_ADC_CTLR1	0x40012404	ADC control register 1	0x02000000
R32_ADC_CTLR2	0x40012408	ADC control register 2	0x00000000
R32_ADC_SAMPTR1	0x4001240C	ADC sample time register 1	0x00000000
R32_ADC_SAMPTR2	0x40012410	ADC sample time register 2	0x00000000
R32_ADC_IOFR1	0x40012414	ADC injected channel data offset register 1	0x00000000
R32_ADC_IOFR2	0x40012418	ADC injected channel data offset register 2	0x00000000
R32_ADC_IOFR3	0x4001241C	ADC injected channel data offset register 3	0x00000000
R32_ADC_IOFR4	0x40012420	ADC injected channel data offset register 4	0x00000000
R32_ADC_WDHTR	0x40012424	ADC watchdog high threshold register	0x000003FF
R32_ADC_WDLTR	0x40012428	ADC watchdog low threshold register	0x00000000
R32_ADC_RSQR1	0x4001242C	ADC regular sequence register 1	0x00000000
R32_ADC_RSQR2	0x40012430	ADC regular sequence register 2	0x00000000
R32_ADC_RSQR3	0x40012434	ADC regular sequence register 3	0x00000000
R32_ADC_ISQR	0x40012438	ADC injected sequence register	0x00000000
R32_ADC_IDATAR1	0x4001243C	ADC injected data register 1	0x00000000
R32_ADC_IDATAR2	0x40012440	ADC injected data register 2	0x00000000
R32_ADC_IDATAR3	0x40012444	ADC injected data register 3	0x00000000
R32_ADC_IDATAR4	0x40012448	ADC injected data register 4	0x00000000
R32_ADC_RDATAR	0x4001244C	ADC regular data register	0x00000000
R32_ADC_DLYR	0x40012450	ADC delayed data register	0x00000000

9.3.1 ADC Status Register (ADC_STATR)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											STRT	JSTRT	JEOC	EOC	AWD

Bit	Name	Access	Description	Reset value
[31:5]	Reserved	RO	Reserved	0
4	STRT	RW0	Rule channel transition start state. 1: Rule channel conversion has started. 0: Rule channel conversion is not started. This bit is set to 1 by hardware and cleared to 0 by software (write 1 is not valid).	0
3	JSTRT	RW0	Injection channel conversion start state. 1: Injection channel conversion has started. 0: Injection channel conversion has not started. This bit is set to 1 by hardware and cleared to 0 by software (write 1 is not valid).	0
2	JEOC	RW0	Injection into the end state of the channel group conversion. 1: Conversion complete. 0: The conversion is not completed. This bit is set to 1 by hardware (all injected channels are converted) and cleared to 0 by software (write 1 is invalid).	0
1	EOC	RW0	Conversion end state. 1: Conversion complete.	0

			0: The conversion is not completed. This bit is set to 1 by hardware (end of rule or injection channel group conversion), cleared by software to 0 (write 1 is invalid) or when reading ADC_RDATAR.	
0	AWD	RW0	Analog watchdog flag bit. 1: Occurrence of simulated watchdog events. 0: No simulated watchdog event occurred. This bit is set to 1 by hardware (conversion value is out of range of ADC_WDHTR and ADC_WDLTR registers) and cleared to 0 by software (write 1 is not valid).	0

9.3.2 ADC Control Register 1 (ADC_CTLR1)

Offset address: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					CALVOL[1:0]		Reserved	AWDEN	JAWDEN	Reserved					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISCNUM[2:0]			JDISCEN	DISCEN	JAUTO	AWDSGL	SCAN	JEOCIE	AWDIE	EOCIE	AWDCH[4:0]				

Bit	Name	Access	Description	Reset value
[31:27]	Reserved	RO	Reserved	0
[26:25]	CALVOL[1:0]	RW	Calibration voltage selection 01: Calibration voltage 2/4 AVDD 10: Calibration voltage 3/4 AVDD Other: Invalid	01b
24	Reserved	RO	Reserved	0
23	AWDEN	RW	Analog watchdog function enable bit on the rule channel. 1: Enable the analog watchdog on the rule channel. 0: Disable the analog watchdog on the rule channel.	0
22	JAWDEN	RW	Analog watchdog function enable bit on the injection channel. 1: Enable the analog watchdog on the injection channel. 0: Disable the analog watchdog on the injection channel.	0
[21:16]	Reserved	RO	Reserved	0
[15:13]	DISCNUM[2:0]	RW	Number of rule channels to be converted after external triggering in intermittent mode. 000: 1 channel. ... 111: 8 channels.	0
12	JDISCEN	RW	Inject the intermittent mode enable bit on the channel. 1: Enable intermittent mode on the injection channel. 0: Disable intermittent mode on the injection channel.	0
11	DISCEN	RW	Intermittent mode enable bit on rule channel. 1: Enables intermittent mode on the rule channel. 0: Disable intermittent mode on the rule channel.	0
10	JAUTO	RW	After the opening of the rule channel is completed, the injection channel group enable bit is automatically switched. 1: Enable automatic injection channel group switching. 0: Disable automatic injection channel group conversion. *Note: This mode requires disabling the external trigger function of the injection channel.*	0
9	AWDSGL	RW	In scan mode, use the analog watchdog enable bit on a	0

			single channel. 1: Use an analog watchdog on a single channel (AWDCH[4:0] selection). 0: Use analog watchdog on all channels.	
8	SCAN	RW	Scan mode enable bit. 1: Enable scan mode (continuous conversion of all channels selected by ADC_IOFRx and ADC_RSQRx). 0: Disable scan mode.	0
7	JEOCIE	RW	Inject the channel group end-of-conversion interrupt enable bit. 1: Enable the injection of the channel group conversion completion interrupt (IEOC JEOC flag). 0: Disable the injection channel group conversion completion interrupt.	0
6	AWDIE	RW	Analog watchdog interrupt enable bit. 1: Enable the analog watchdog interrupt. 0: Disable the analog watchdog interrupt. *NOTE: In scan mode, this interrupt will abort the scan if it occurs.*	0
5	EOCIE	RW	End of conversion (rule or injection channel group) interrupt enable bit. 1: Enable the end-of-conversion interrupt (EOC flag). 0: Disable the end-of-conversion interrupt.	0
[4:0]	AWDCH[4:0]	RW	Analog watchdog channel selection bits. 00000: Analog input channel 0. 00001: Analog input channel 1. ... 01111: Analog input channel 15.	0

9.3.3 ADC Control Register 2 (ADC_CTLR2)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									SWSTART	JSWSTART	EXTTRIG	EXTSEL[2:0]			Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JEXTTRIG	JEXTSEL[2:0]			ALIGN	Reserved		DMA	Reserved				RSTCAL	CAL	CONT	ADON

Bit	Name	Access	Description	Reset value
[31:23]	Reserved	RO	Reserved	0
22	SWSTART	RW	To start a rule channel conversion, you need to set the software trigger to. 1: Initiate rule channel conversion. 0: Reset state. This bit is set by software and cleared to 0 by hardware when conversion starts.	0
21	JSWSTART	RW	To initiate an injection channel transition, set the software to trigger: 1: initiates an injection channel transition; 0: reset state. This bit is set by software and is cleared to 0 by hardware or 0 by software when the conversion starts.	0
20	EXTTRIG	RW	External trigger transition mode enable for the rule channel.	0

			1: Use of external events to initiate conversions. 0: Turn off the external event activation function.	
[19:17]	EXTSEL[2:0]	RW	External trigger event selection for initiating rule channel conversion. 000: TRGO event for timer 1. 001: CC1 event of timer 1. 010: CC2 event of timer 1. 011: TRGO event of timer 2. 100: CC1 event of timer 2. 101: CC2 event of timer 2. 110: PD3/PC2 events. 111: SWSTART software trigger.	0
16	Reserved	RO	Reserved	0
15	JEXTTRIG	RW	External trigger transition mode enable for the injected channel. 1: Use of external events to initiate conversions. 0: Turn off the external event activation function.	0
[14:12]	JEXTSEL[2:0]	RW	External trigger event selection for initiating injection channel conversion. 000: CC3 event of timer 1; 001: CC4 event of timer 1; 010: CC3 event of timer 2; 011: CC4 event of timer 2; 100: Reserved; 101: Reserved; 110: PD1/PA2; 111: JSWSTART software trigger.	0
11	ALIGN	RW	Data alignment. 1: left-aligned; 0: right-aligned.	0
[10:9]	Reserved	RO	Reserved	0
8	DMA	RW	Direct Memory Access (DMA) mode enable. 1: Enable DMA mode. 0: Disable DMA mode.	0
[7:4]	Reserved	RO	Reserved	0
3	RSTCAL	RW	Reset calibration, this bit is set by software and cleared by hardware after the reset is completed. 1: Initialization of the calibration registers. 0: Calibration register is initialized. *Note: If RSTCAL is set while conversion is in progress, additional cycles are required to clear the calibration register.*	0
2	CAL	RW	A/D calibration, this bit is set by software and cleared to 0 by hardware at the end of calibration. 1: Start of calibration. 0: Calibration is complete.	0
1	CONT	RW	Continuous conversion enable. 1: Continuous conversion mode. 0: Single conversion mode. If this bit is set, the conversion will continue until the bit is cleared.	0
0	ADON	RW	On/off A/D converter When this bit is 0, writing 1 will wake up the ADC from power-down mode; when this bit is 1, writing 1 will start the conversion. 1: Turn on the ADC and start the conversion. 0: Turn off ADC conversion/calibration and enter power-down mode. *Note: A conversion is initiated when only ADON is changed in the register, and no new conversion is initiated*	0

			if there are any other bits sent for change.	

9.3.4 ADC Sample Time Configuration Register 1 (ADC_SAMPTR1)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved														SMP15[2:1]	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP15[0]		SMP14[2:0]			SMP13[2:0]			SMP12[2:0]			SMP11[2:0]			SMP10[2:0]	

Bit	Name	Access	Description	Reset value
[31:18]	Reserved	RO	Reserved	0
[17:0]	SMPx[2:0]	RW	SMPx[2:0]: sample time configuration for channel x. 000: 3 cycles; 001: 9 cycles. 010: 15 cycles; 011: 30 cycles. 100: 43 cycles; 101:57 cycles. 110: 73 cycles; 111: 241 cycles. These bits are used to independently select the sample time for each channel, and the channel configuration value must remain constant during the sample cycle.	0

9.3.5 ADC Sample Time Configuration Register 2 (ADC_SAMPTR2)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SMP9[2:0]			SMP8[2:0]			SMP7[2:0]			SMP6[2:0]			SMP5[2:1]	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMP5[0]		SMP4[2:0]			SMP3[2:0]			SMP2[2:0]			SMP1[2:0]			SMP0[2:0]	

Bit	Name	Access	Description	Reset value
[31:30]	Reserved	RO	Reserved	0
[29:0]	SMPx[2:0]	RW	SMPx[2:0]: sample time configuration for channel x. 000: 3 cycles; 001: 9 cycles. 010: 15 cycles; 011: 30 cycles. 100: 43 cycles; 101:57 cycles. 110: 73 cycles; 111: 241 cycles. These bits are used to independently select the sample time for each channel, and the channel configuration value must remain constant during the sample cycle.	

9.3.6 ADC Injected Channel Data Offset Register x (ADC_IOFRx) (x=1/2/3/4)

Offset address: 0x14 + (x-1)*4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						JOFFSETx[11:0]									

Bit	Name	Access	Description	Reset value

[31:10]	Reserved	RO	Reserved	0
[9:0]	JOFFSETx[11:0]	RW	The data offset value of the injected channel x. When converting the injected channels, this value defines the value used to subtract from the original conversion data. The result of the conversion can be read out in the ADC_IDATARx register.	0

9.3.7 ADC Watchdog High Threshold Register (ADC_WDHTR)

Offset address: 0x24

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						HT[9:0]									

Bit	Name	Access	Description	Reset value
[31:10]	Reserved	RO	Reserved	0
[9:0]	HT[9:0]	RW	Analog watchdog high threshold setting value.	3FFh

Note: You can change the values of WDHTR and WDLTR during the conversion process, but they will take effect at the next conversion.

9.3.8 ADC Watchdog Low Threshold Register (ADC_WDLTR)

Offset address: 0x28

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						LT[9:0]									

Bit	Name	Access	Description	Reset value
[31:10]	Reserved	RO	Reserved	0
[9:0]	LT[9:0]	RW	Analog watchdog low threshold setting value.	0

Note: You can change the values of WDHTR and WDLTR during the conversion process, but they will take effect at the next conversion.

9.3.9 ADC Regular Sequence Register 1(ADC_RSQR1)

Offset address: 0x2C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								L[3:0]				SQ16[4:1]			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ16[0]	SQ15[4:0]					SQ14[4:0]						SQ13[4:0]			

Bit	Name	Access	Description	Reset value
[31:24]	Reserved	RO	Reserved	0
[23:20]	L[3:0]	RW	Number of channels to be converted in a regular channel conversion sequence. 0000-1111: 1-16 conversions.	0
[19:15]	SQ16[4:0]	RW	The number of the 16th conversion channel in the rule sequence (0-9).	0
[14:10]	SQ15[4:0]	RW	The number of the 15th conversion channel in the rule sequence (0-9).	0
[9:5]	SQ14[4:0]	RW	The number of the 14th conversion channel in the rule sequence (0-9).	0
[4:0]	SQ13[4:0]	RW	The number of the 13th conversion channel in the rule sequence (0-9).	0

9.3.10 ADC Regular Sequence Register 2(ADC_RSQR2)

Offset address: 0x30

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ12[4:0]					SQ11[4:0]					SQ10[4:1]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ10[0]		SQ9[4:0]					SQ8[4:0]					SQ7[4:0]			

Bit	Name	Access	Description	Reset value
[31:30]	Reserved	RO	Reserved	0
[29:25]	SQ12[4:0]	RW	The number of the 12th conversion channel in the rule sequence (0-9).	0
[24:20]	SQ11[4:0]	RW	The number of the 11th conversion channel in the rule sequence (0-9).	0
[19:15]	SQ10[4:0]	RW	The number of the 10th conversion channel in the rule sequence (0-9).	0
[14:10]	SQ9[4:0]	RW	The number of the 9th conversion channel in the rule sequence (0-9).	0
[9:5]	SQ8[4:0]	RW	The number of the 8th conversion channel in the rule sequence (0-9).	0
[4:0]	SQ7[4:0]	RW	The number of the 7th conversion channel in the rule sequence (0-9).	0

9.3.11 ADC Regular Sequence Register 3(ADC_RSQR3)

Offset address: 0x34

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		SQ6[4:0]					SQ5[4:0]					SQ4[4:1]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SQ4[0]		SQ3[4:0]					SQ2[4:0]					SQ1[4:0]			

Bit	Name	Access	Description	Reset value
[31:30]	Reserved	RO	Reserved	0
[29:25]	SQ6[4:0]	RW	The number of the 6th conversion channel in the rule sequence (0-9).	0
[24:20]	SQ5[4:0]	RW	The number of the 5th conversion channel in the rule sequence (0-9).	0

[19:15]	SQ4[4:0]	RW	The number of the 4th conversion channel in the rule sequence (0-9).	0
[14:10]	SQ3[4:0]	RW	The number of the 3th conversion channel in the rule sequence (0-9).	0
[9:5]	SQ2[4:0]	RW	The number of the 2th conversion channel in the rule sequence (0-9).	0
[4:0]	SQ1[4:0]	RW	The number of the 1th conversion channel in the rule sequence (0-9).	0

9.3.12 ADC Injected Sequence Register (ADC_ISQR)

Offset address: 0x38

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										JL[1:0]		JSQ4[4:1]			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JSQ4[0]	JSQ3[4:0]					JSQ2[4:0]				JSQ1[4:0]					

Bit	Name	Access	Description	Reset value
[31:22]	Reserved	RO	Reserved	0
[21:20]	JL[1:0]	RW	Inject the number of channels to be converted in the channel conversion sequence. 00-11: 1-4 conversions.	0
[19:15]	JSQ4[4:0]	RW	The number of the 4th conversion channel in the injection sequence (0-9). *Note: The software writes and assigns the channel number (0-9) as the 4th in the sequence to be converted.*	0
[14:10]	JSQ3[4:0]	RW	The number of the 3th conversion channel in the injection sequence (0-9).	0
[9:5]	JSQ2[4:0]	RW	The number of the 2th conversion channel in the injection sequence (0-9).	0
[4:0]	JSQ1[4:0]	RW	The number of the 1th conversion channel in the injection sequence (0-9).	0

Note: Unlike the regular conversion sequence, if the length of JL[1:0] is less than 4, the sequence order of conversion starts from (4 - JL).

For example, when JL[1:0]=3 (4 injected transitions in the sequencer), the ADC will convert channels in the following order: JSQ1[4:0], JSQ2[4:0], JSQ3[4:0], and JSQ4[4:0];

When JL[1:0]=2 (3 injected transitions in the sequencer), the ADC will convert the channels in the following order: JSQ2[4:0], JSQ3[4:0] and JSQ4[4:0];

When JL[1:0]=1 (2 injected conversions in the sequencer), the ADC converts the channels in the following order: first JSQ3[4:0], then JSQ4[4:0];

When JL[1:0] = 0 (1 injection conversion in the sequencer), the ADC will convert only the JSQ4[4:0] channels.

If ADCx_ISQR[21:0]=10 00111 00011 00111 00010, the ADC will convert channels in the following order: JSQ2[4:0], JSQ3[4:0], and JSQ4[4:0], indicating that the scan conversions are performed in the following channel order: 7, 3, 7.

9.3.13 ADC Injected Data Register (ADC_IDATARx) (x=1/2/3/4)

Offset address: 0x3C + (x-1)*4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

JDATA[15:0]

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
[15:0]	JDATA[15:0]	RO	Injection of channel conversion data (data left- aligned or right-aligned).	0

9.3.14 ADC Regular Data Register (ADC_RDATAR)

Offset address: 0x4C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA[15:0]															

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
[15:0]	DATA[15:0]	RO	Rule channel conversion data (data left-aligned or right-aligned)	0

9.3.15 ADC Delayed Data Register (ADC_DLYR)

Offset address: 0x50

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						DLYSRC	DLYVLU[8:0]								

Bit	Name	Access	Description	Reset value
[31:10]	Reserved	RO	Reserved	0
9	DLYSRC	RW	External trigger source delay selection 0: Rule channel external trigger delay 1: Injection channel external trigger delay	0
[8:0]	DLYVLU[8:0]	RW	External trigger delay data, delay time configuration, unit: ADC clock cycle	0