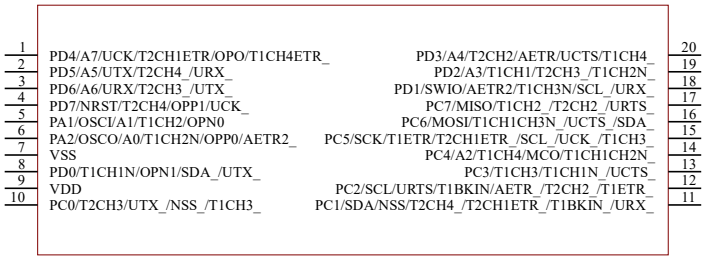
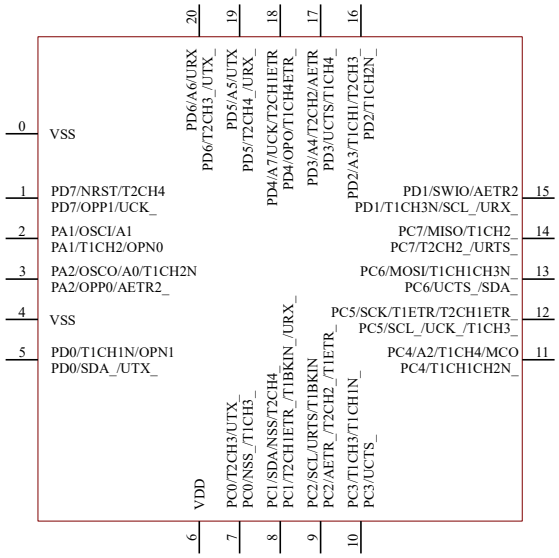
Chapter 2 Pinouts and Pin Definition

2.1 Pinouts

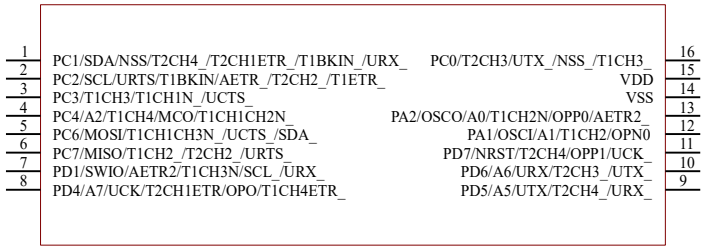
CH32V003F4P6



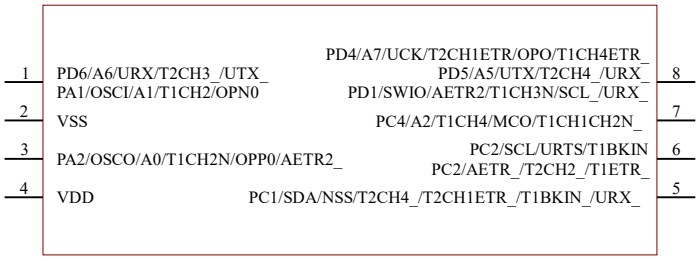
CH32V003F4U6



CH32V003A4M6



CH32V003J4M6



Note: The multiplexed functions in the pin diagram are abbreviated.

Example: A: ADC, A7 (ADC_IN7)

T: TIME, T2CH4 (TIM2_CH4)

U: USART, URX (USART_RX)

OP: OPA, OPO (OPA_OUT), OPP1 (OPA_P1)

OSCI (OSCIN)

OSCO (OSCOUT)

SDA (I2C_SDA)

SCL (I2C_SCL)

SCK (SPI_SCK)

NSS (SPI_NSS)

MOSI (SPI_MOSI)

MISO (SPI_MISO)

AETR(ADC_ETR)

2.2 Pin description

Table 2-1 Pin definitions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Pin No.				Pin name	Pin type	Main function (after reset)	Default alternate function	Remapping function
SOP16	TSSOP20	QFN20	SOP8					
-	-	0	-	VSS	P	VSS	-	-
8	1	18	8	PD4	I/O/A	PD4	UCK/T2CH1ETR(1)/A7/ OPO	TIETR_2/T1CH4_3
9	2	19	8	PD5	I/O/A	PD5	UTX/A5	T2CH4_3/URX_2
10	3	20	1	PD6	I/O/A	PD6	URX/A6	T2CH3_3/UTX_2
11	4	1	-	PD7	I/O/A	PD7	NRST/T2CH4/OPP1	UCK_1/UCK_2/T2CH4_2
12	5	2	1	PA1	I/O/A	PA1	T1CH2/A1/OPN0	OSCI/T1CH2_2
13	6	3	3	PA2	I/O/A	PA2	TICH2N/A0/OPP0	OSCO/AETR2_1/TICH2N_2
14	7	4	2	VSS	P	VSS	-	-
-	8	5	-	PD0	I/O/A	PD0	TICH1N/OPN1	SDA_1/UTX_1/TICH1N_2
15	9	6	4	VDD	P	VDD	-	-

16	10	7	-	PC0	I/O	PC0	T2CH3	NSS_1/UTX_3/T2CH3_2 /T1CH3_1
1	11	8	5	PC1	I/O/FT	PC1	SDA/NSS	T1BKIN_1/T2CH4_1 T2CH1ETR(1)_2/URX_3 /T2CH1ETR(1)_3/T1BKIN_3
2	12	9	6	PC2	I/O/FT	PC2	SCL/URTS/T1BKIN	AETR_1/T2CH2_1 /T1ETR_3/URTS_1 /T1BKIN_2
3	13	10	-	PC3	I/O	PC3	T1CH3	T1CH1N_1/UCTS_1 /T1CH3_2/T1CH1N_3
4	14	11	7	PC4	I/O/A	PC4	T1CH4/MCO/A2	T1CH2N_1/T1CH4_2 /T1CH1_3
-	15	12	-	PC5	I/O/FT	PC5	SCK/T1ETR	T2CH1ETR(1)_1/SCL_2 /SCL_3/UCK_3/T1ETR_1 /T1CH3_3/SCK_1
5	16	13	-	PC6	I/O/FT	PC6	MOSI	T1CH1_1/UCTS_2/SDA_2 /SDA_3/UCTS_3/T1CH3N_ 3 /MOSI_1
6	17	14	-	PC7	I/O	PC7	MISO	T1CH2_1/URTS_2 /T2CH2_3/URTS_3 /T1CH2_3/MISO_1
7	18	15	8	PD1	I/O/A	PD1	SWIO/T1CH3N/AETR2	SCL_1/URX_1/T1CH3N_1 /T1CH3N_2
-	19	16	-	PD2	I/O/A	PD2	T1CH1/A3	T2CH3_1/T1CH2N_3 /T1CH1_2
-	20	17	-	PD3	I/O/A	PD3	A4/T2CH2/AETR/UCTS	T2CH2_2/T1CH4_1

Note: 1. TIM2_CH1, TIM2_ETR;

2. The value after the underline of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example: T1CH4_3 indicates that the corresponding bit of the AFIO register is configured as 11b;

3. Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input.

O = CMOS level tri-state output.

P = power supply.

FT = 5V tolerant.

A = Analog signal input or output.

2.3 Pin alternate functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-2 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI	SWIO	OPA
PA1	A1	T1CH2/T1CH2_2			OSCI				OPN0
PA2	A0/AETR2_1	T1CH2N/T1CH2N_2			OSCO				OPP0
PC0		T1CH3_1	T2CH3/T2CH3_2	UTX_3			NSS_1		
PC1		T1BKIN_1/T1BKIN_3	T2CH4_1/T2CH1ETR(1)_2 /T2CH1ETR(1)_3	URX_3		SDA	NSS		
PC2	AETR_1	T1BKIN/T1ETR_3 /T1BKIN_2	T2CH2_1	URTS/URTS_1		SCL			
PC3		T1CH3/T1CH1N_1 T1CH3_2/T1CH1N_3		UCTS_1					
PC4	A2	T1CH4/T1CH2N_1 /T1CH4_2/T1CH1_3			MCO				
PC5		T1ETR/T1CH3_3 /T1ETR_1	T2CH1ETR(1)_1	UCK_3		SCL_2/SCL_3	SCK/SCK_1		
PC6		T1CH1_1/T1CH3N_3		UCTS_2/UCTS_3		SDA_2/SDA_3	MOSI/MOSI_1		
PC7		T1CH2_1/T1CH2_3	T2CH2_3	URTS_2/URTS_3			MISO/MISO_1		
PD0		T1CH1N/T1CH1N_2		UTX_1		SDA_1			OPN1
PD1	AETR2	T1CH3N/T1CH3N_1 /T1CH3N_2		URX_1		SCL_1		SWIO	
PD2	A3	T1CH1/T1CH2N_3 /T1CH1_2	T2CH3_1						
PD3	A4/AETR	T1CH4_1	T2CH2/T2CH2_2	UCTS					
PD4	A7	T1ETR_2/T1CH4_3	T2CH1ETR(1)	UCK					OPO
PD5	A5		T2CH4_3	UTX/URX_2					
PD6	A6		T2CH3_3	URX/UTX_2					
PD7			T2CH4/T2CH4_2	UCK_1/UCK_2	NRST				OPP1

Note: TIM2_CH1、TIM2_ETR.