CH32V003 Reference Manual

V1.7

https://www.wch-ic.com

Overview

CH32V003 series are industrial-grade general-purpose microcontrollers designed based on 32-bit RISC-V instruction set and architecture. It adopts QingKe V2A core, RV32EC instruction set, and supports 2 levels of interrupt nesting. The series are mounted with rich peripheral interfaces and function modules. Its internal organizational structure meets the low-cost and low-power embedded application scenarios.

This manual provides detailed information on the use of the CH32V003 series for the user's application development, and is applicable to products with different memory capacities, functional resources, and packages in the series; any differences will be specially explained in the corresponding functional chapters.

Please refer to the Datasheet *CH32V003DS0* for the device characteristics of this product.

For information about the core, please refer to the *QingKeV2_Processor_Manual*.

RISC-V core version overview

Features / Core versions	Instruction set	Hardware stack levels	Interrupt nesting levels	Fast interrupt channels	Flow line	Vector table model	Extensions instruction	Debug interface
QingKe V2A	RV32EC	2	2	2	2	Address or command	Support	1-wire

Abbreviated description of the bit attribute in the register:

Register bit properties	Property description
RF	Read-only property that reads a fixed value.
RO	Read-only attribute, changed by hardware.
RZ	Read-only property, auto bit clear 0 after read operation.
WO	Write only attribute (not readable, read value uncertain)
WA	Write-only attribute, writable in Safe mode.
WZ	Write only attribute, auto bit clear 0 after write operation.
RW	Readable and writable.
RWA	Readable, writable in Safe mode.
RW1	Readable, write 1 is valid, write 0 is invalid.
RW0	Readable, write 0 valid, write 1 invalid.
RW1T	Readable, write 0 invalid, write 1 flipped.