Chapter 3 Electrical Characteristics

3.1 Test conditions

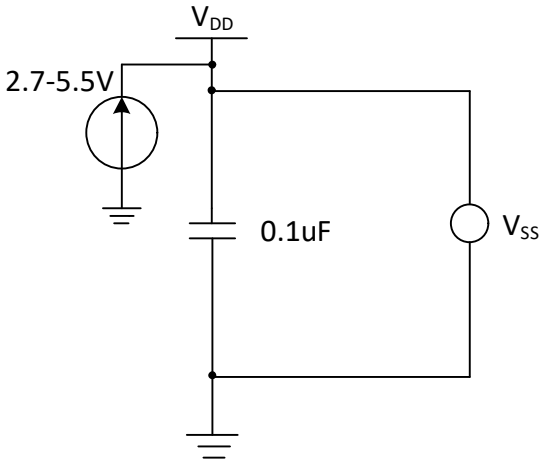
Unless otherwise specified and marked, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and V_{DD} = 3.3V or 5V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply



3.2 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (V_{DD})	-0.3	5.5	V
V_{IN}	Input voltage on the FT (5V tolerant) pin	V_{SS}-0.3	5.5	V
	Input voltage on other pins	V_{SS}-0.3	V_{DD}+0.3	
$\lvert\triangle V_{DD\_x}\rvert$	Variations between different main power supply pins		50	mV
$\lvert\triangle V_{SS\_x}\rvert$	Variations between different ground pins		50	mV

$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model, non-contact)	4K		V
I_{VDD}	Total current into V_{DD} power lines (supply current)		100	mA
I_{Vss}	Total current out of V_{SS} ground lines (outflow current)		80	
$I_{I/O}$	Sink current on any I/O and control pin		20	
	Output current on any I/O and control pin		-20	
$I_{INJ(PIN)}$	OSC_IN pin of HSE		+/-4	
	Injected current on other pins		+/-4	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-20	

3.3 Electrical characteristics

3.3.1 Operating conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK}	Internal AHB clock frequency			50	MHz
V_{DD}	Standard operating voltage	ADC not used	2.7	5.5	V
		Use ADC (recommended)	2.8	5.5	
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	105	℃

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		30	∞	

3.3.2 Embedded reset and power control block characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Programmable voltage detector level selection	PLS[2:0] = 000 (rising edge)		2.85		V
		PLS[2:0] = 000 (falling edge)		2.7		V
		PLS[2:0] = 001 (rising edge)		3.05		V
		PLS[2:0] = 001 (falling edge)		2.9		V
		PLS[2:0] = 010 (rising edge)		3.3		V
		PLS[2:0] = 010 (falling edge)		3.15		V
		PLS[2:0] = 011 (rising edge)		3.5		V
		PLS[2:0] = 011 (falling edge)		3.3		V
		PLS[2:0] = 100 (rising edge)		3.7		V
		PLS[2:0] = 100 (falling edge)		3.5		V
		PLS[2:0] = 101 (rising edge)		3.9		V
		PLS[2:0] = 101 (falling edge)		3.7		V
		PLS[2:0] = 110 (rising edge)		4.1		V

		PLS[2:0] = 110 (falling edge)		3.9		V
		PLS[2:0] = 111 (rising edge)		4.4		V
		PLS[2:0] = 111 (falling edge)		4.2		V
$V_{PVDhyst}$	PVD hysteresis			0.18		V
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	2.32	2.5	2.68	V
		Falling edge	2.3	2.48	2.66	V
$V_{PDRhyst}$	PDR hysteresis			20		mV
$t_{RSTTEMPO}$	Power on reset		12	17	22	mS
	Other resets			300		uS

Note: 1. Normal temperature test value.

3.3.3 Embedded reference voltage

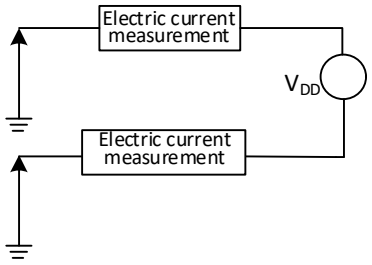
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40℃~85℃	1.17	1.2	1.23	V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage		3		500	$1/f_{ADC}$

3.3.4 Supply current characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

Normal temperature VDD = 3.3V or 5V case, when testing: all IO ports configured with pull-down inputs; HSI on when testing HSE, HSE off when testing HSI, HSE= 24M, HIS= 24M (calibrated); system clock source CLK*2 when FHCLK= 48MHz, 16MHz; clock on all peripherals only when turning on all peripherals. Enables or disables power consumption of all peripheral clocks.

Table 3-6-1 Typical current consumption in Run mode, data processing code runs from the internal Flash (V_{DD} = 3.3V)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK} = 48MHz	7.0	4.6	mA
			F_{HCLK} = 24MHz	5.2	4.2	
			F_{HCLK} = 16MHz	4.6	3.8	
			F_{HCLK} = 8MHz	3.1	2.7	
			F_{HCLK} = 750KHz	1.8	1.8	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	6.3	3.9	
			F_{HCLK} = 24MHz	4.3	3.1	
			F_{HCLK} = 16MHz	3.9	3.1	
			F_{HCLK} = 8MHz	2.3	1.9	
			F_{HCLK} = 750KHz	1.1	1.0	

Note: 1. The above are measured parameters.

2. When VDD < 3V, the current power consumption will increase.

Table 3-6-2 Typical current consumption in Run mode, data processing code runs from the internal Flash (V_{DD} = 5V)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	External clock	F_{HCLK} = 48MHz	8.0	5.6	mA
			F_{HCLK} = 24MHz	6.4	5.6	
			F_{HCLK} = 16MHz	5.8	5.0	
			F_{HCLK} = 8MHz	3.8	3.4	
			F_{HCLK} = 750KHz	2.2	2.1	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	7.3	4.9	
			F_{HCLK} = 24MHz	5.3	4.1	
			F_{HCLK} = 16MHz	5.0	4.3	
			F_{HCLK} = 8MHz	3.1	2.7	
			F_{HCLK} = 750KHz	1.4	1.4	

Note: 1. The above are measured parameters.

Table 3-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (V_{DD} = 3.3V)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply	External clock	F_{HCLK} = 48MHz	4.9	2.5	mA

	current in Sleep mode (In this case, peripheral power supply and clock are maintained)		F_{HCLK} = 24MHz	2.9	1.7	
			F_{HCLK} = 16MHz	2.5	1.7	
			F_{HCLK} = 8MHz	1.7	1.3	
			F_{HCLK} = 750KHz	1.2	1.1	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	4.2	1.8	
			F_{HCLK} = 24MHz	2.2	1.0	
			F_{HCLK} = 16MHz	1.8	1.0	
			F_{HCLK} = 8MHz	1.0	0.6	
			F_{HCLK} = 750KHz	0.4	0.4	

Note: 1. The above are measured parameters.

Table 3-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (V_{DD} = 5V)

Symbol	Parameter	Condition		Typ.		Unit
				All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{HCLK} = 48MHz	4.9	2.5	mA
			F_{HCLK} = 24MHz	2.9	1.7	
			F_{HCLK} = 16MHz	2.5	1.7	
			F_{HCLK} = 8MHz	1.7	1.3	
			F_{HCLK} = 750KHz	1.2	1.1	
		Runs on the high-speed internal RC oscillator (HSI). Uses AHB prescaler to reduce the frequency.	F_{HCLK} = 48MHz	4.2	1.8	
			F_{HCLK} = 24MHz	2.2	1.0	
			F_{HCLK} = 16MHz	1.8	1.0	
			F_{HCLK} = 8MHz	1.0	0.6	
			F_{HCLK} = 750KHz	0.4	0.4	

Note: 1. The above are measured parameters.

Table 3-8 Typical current consumption in Standby mode

Symbol	Parameter	Condition		Typ.	Unit
I_{DD}	Supply current in Standby mode	LSI on	V_{DD} = 3.3V	10.5	uA
			V_{DD} = 5V	11.1	
		LSI off	V_{DD} = 3.3V	9.0	
			V_{DD} = 5V	9.6	

Note: The above are measured parameters.

3.3.5 External clock source characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		4	24	25	MHz
V_{HSEH}(1)	OSC_IN input pin high level		0.8V_{DD}		V_{DD}	V

	voltage					
V_{HSEL}(1)	OSC_IN input pin low-level voltage		0		0.2V_{DD}	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		40	50	60	%
I_L	OSC_IN input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

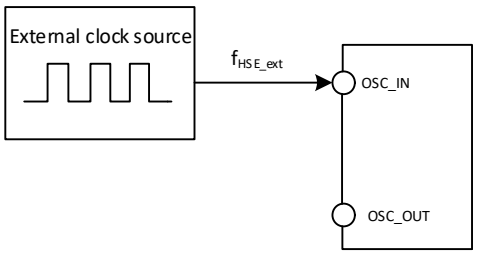


Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

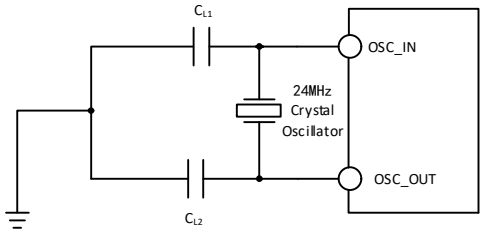
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		4	24	25	MHz
R_F	Feedback resistance			250		kΩ
C	Recommended load capacitance and corresponding crystal series impedance R_S	R_S = 60Ω(1)		20		pF
I_2	HSE drive current	V_{DD} = 3.3V, 20p load		0.32		mA
g_m	Oscillator transconductance	Startup		6.8		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable, 24M crystal		2		ms

Note 1: It is recommended that the ESR of 25M crystal should not exceed 60 Ω, and it can be relaxed if it is lower than 25M.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally $C_{L1} = C_{L2}$.

Figure 3-4 Typical circuit of external 24M crystal



3.3.6 Internal clock source characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)			24		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	TA = 0℃～70℃	-1.2		1.6	%
		TA = -40℃～85℃	-2.2		2.2	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time			10		us
$I_{DD(HSI)}$	HSI oscillator power consumption		120	180	270	uA

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		100	128	150	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time			80		us
$I_{DD(LSI)}$	LSI oscillator power consumption			1.5		uA

3.3.7 Wakeup time from low-power mode

Table 3-13 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Wake up using HSI RC clock	30	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up + code load time(2) (take 128K as example)	200	us

Note: The above parameters are measured parameters.

3.3.8 Memory characteristics

Table 3-14 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ERASE_64}	Page (64 bytes) programming time	T_A = -20℃～85℃	2.4		3.1	ms
t_{ERASE}	Page (64 bytes) erase time	T_A = -20℃～85℃	2.4		3.1	ms
t_{prog}	16-bit programming time	T_A = -20℃～85℃	2.4		3.1	ms
t_{ME}	Whole chip erase time	T_A = -20℃～85℃	2.4		3.1	ms
V_{prog}	Programming voltage		2.8		5.5	V

Table 3-15 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25℃	10K	80K(1)		times

t_{RET}	Data retention		10			year

Note: The endurance parameter is actual measured, which is not guaranteed.

3.3.9 I/O port characteristics

Table 3-16 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.22*(V_{DD}-2.7)+1.55		V_{DD}+0.3	V
	FT I/O pin, input high level voltage		0.22*(V_{DD}-2.7)+1.55		5.5	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.19*(V_{DD}-2.7)+0.65	V
	FT I/O pin, input low-level voltage		-0.3		0.19*(V_{DD}-2.7)+0.65	V
V_{hys}	Schmitt trigger voltage hysteresis		150			mV
I_{lkg}	Input leakage current	Standard I/O port			1	uA
		FT I/O port			3	
R_{PU}	Weak pull-up equivalent resistance		35	45	55	kΩ
R_{PD}	Weak pull-down equivalent resistance		35	45	55	kΩ
$C_{I/O}$	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level when 8 pins are sunk	TTL port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <5.5V	V_{DD}-0.4		
V_{OL}	Output low level when 8 pins are sunk	CMOS port, $I_{I/O}$ = +8mA		0.4	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <5.5V	2.3		
V_{OL}	Output low level when 8 pins are sunk	$I_{I/O}$ = +20mA		1.3	V
V_{OH}	Output high level when 8 pins are sourced	2.7V< V_{DD} <5.5V	V_{DD}-1.3		

Note: In the above conditions, if multiple I/O pins are driven at the same time, the total current cannot exceed the absolute maximum ratings given in Table 3.2. In addition, when multiple I/O pins are driven at the same time, the current on the power/ground point is very large, which will cause the voltage drop to make the internal I/O voltage not reach the power supply voltage in the table, resulting in the drive current being less than the nominal value.

Table 3-18 Input/output AC characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 （2MHz）	$F_{max(I/O)out}$	Maximum frequency	CL = 50pF, V_{DD} = 2.7-5.5V		2	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL = 50pF, V_{DD} = 2.7-5.5V		125	ns
	$t_{r(I/O)out}$	Output low to high rise time			125	ns
01 （10MHz）	$F_{max(I/O)out}$	Maximum frequency	CL = 50pF, V_{DD} = 2.7-5.5V		10	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL = 50pF, V_{DD} = 2.7-5.5V		25	ns
	$t_{r(I/O)out}$	Output low to high rise time			25	ns
11 （30MHz）	$F_{max(I/O)out}$	Maximum frequency	CL = 50pF, V_{DD} = 2.7-5.5V		30	MHz
	$t_{f(I/O)out}$	Output high to low fall time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
	$t_{r(I/O)out}$	Output low to high rise time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
	t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

3.3.10 NRST pin characteristics

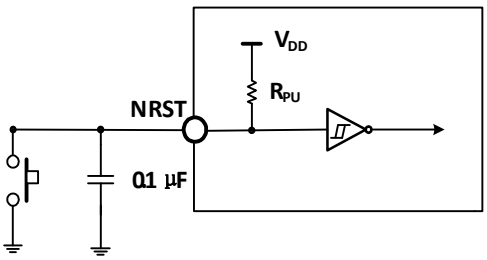
Table 3-19 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$	NRST input low-level voltage		-0.3		0.28*(V_{DD}-1.8)+0.6	V
$V_{IH(NRST)}$	NRST input high-level voltage		0.41*(V_{DD}-1.8)+1.3		V_{DD}+0.3	V
$V_{hys(NRST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}(1)	Weak pull-up equivalent resistance		35	45	55	kΩ

Note: 1. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (approximately 10%).

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



3.3.11 TIM timer characteristics

Table 3-20 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit

$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	13.9		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		59.6	s

3.3.12 I2C interface characteristics

Figure 3-6 I2C bus timing diagram

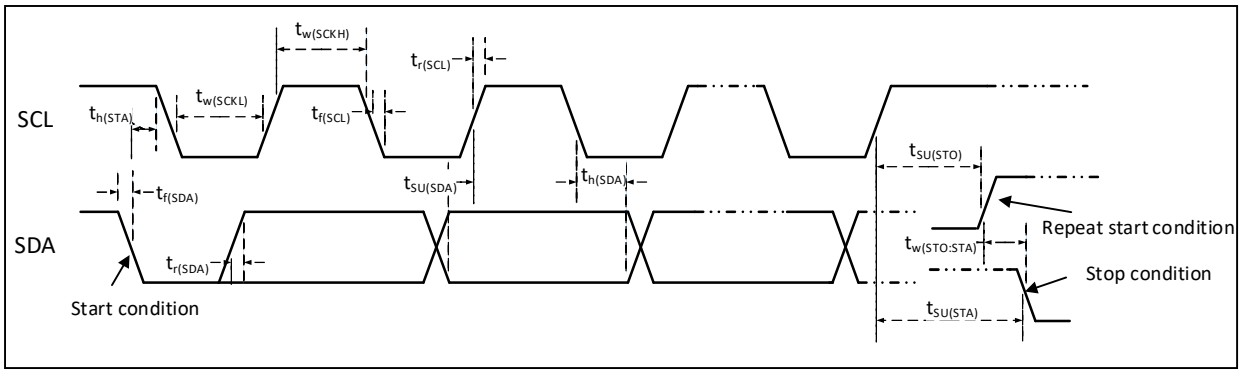


Table 3-21 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI interface characteristics

Figure 3-7 SPI timing diagram in Master mode

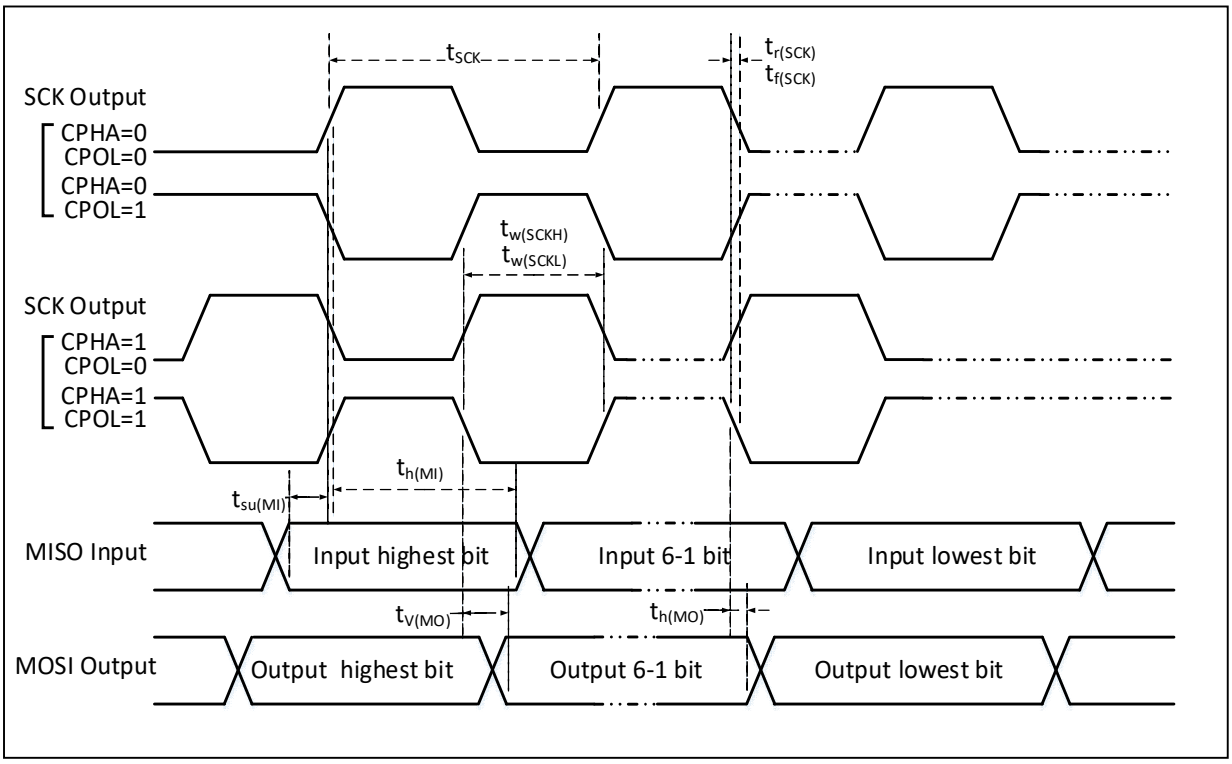


Figure 3-8 SPI timing diagram in Slave mode (CPHA = 0)

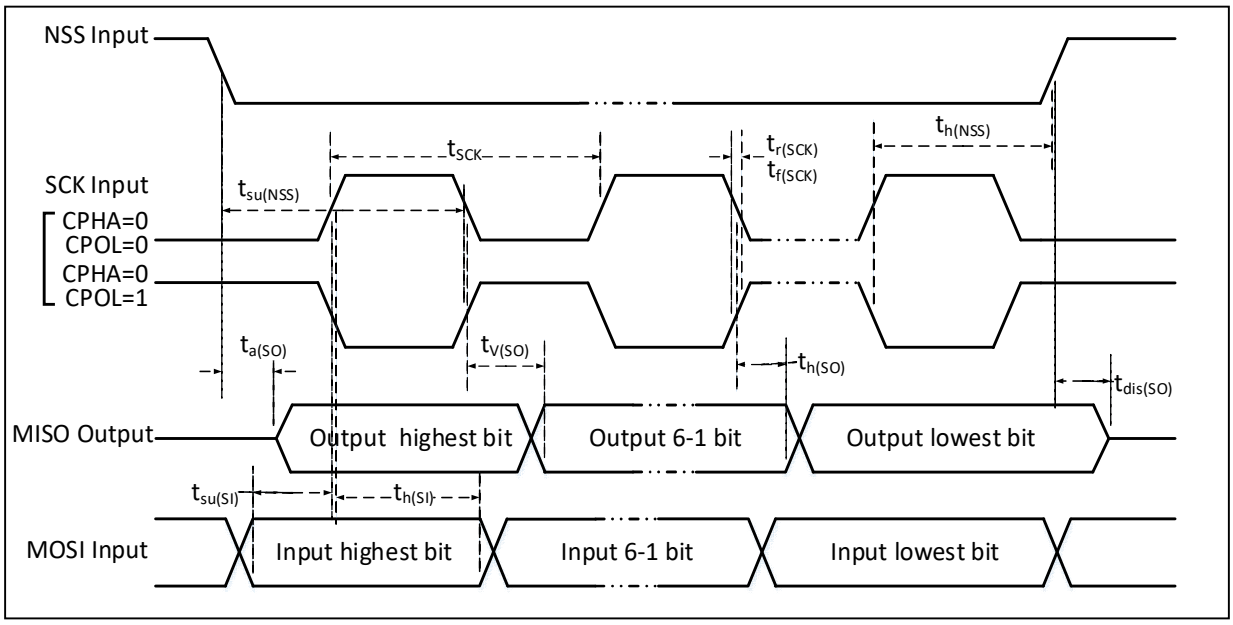


Figure 3-9 SPI timing diagram in Slave mode (CPHA = 1)

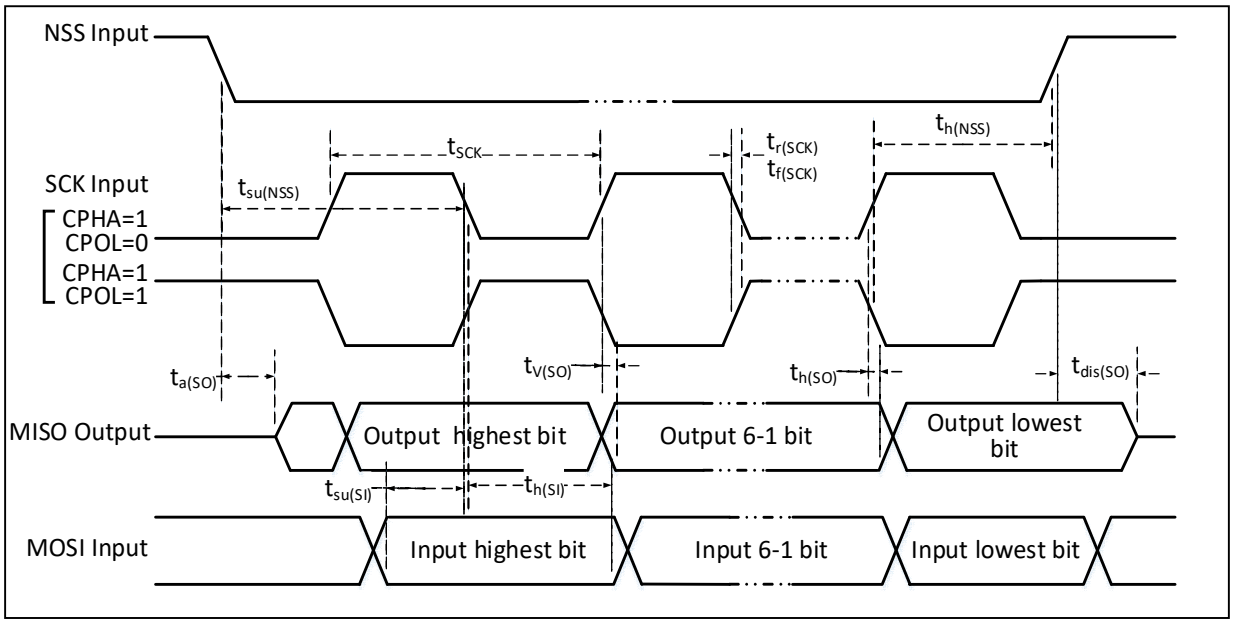


Table 3-22 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		24	MHz
		Slave mode		24	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance:C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{PCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{PCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 48MHz, Prescaler factor = 2	30	70	ns
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 24MHz	0	$1t_{PCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		5	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	2		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.14 10-bit ADC characteristics

Table 3-23 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.8		5.5	V
I_{DD}	Supply current			370		uA

f_{ADC}	ADC clock frequency	V_{DD} = 2.8 to 5.5V	1		6	MHz
		V_{DD} = 3.2 to 5.5V	1		12	
		V_{DD} = 4.5 to 5.5V	1		24	
V_{AIN}	Conversion voltage range		V_{SS}		V_{DD}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
f_S	Sampling rate	f_{ADC} = 4 MHz			285	KHz
		f_{ADC} = 6 MHz			430	
		f_{ADC} = 12 MHz			857	
		f_{ADC} = 24 MHz			1710	
t_s	Sampling time	f_{ADC} = 4 MHz		0.75		us
		f_{ADC} = 6 MHz		0.5		
		f_{ADC} = 12 MHz		0.25		
t_{STAB}	Power-on time			7		us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 4 MHz	3.5			us
		f_{ADC} = 6 MHz	2.33			us
		f_{ADC} = 12 MHz	1.17			us
		-	14			$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Table 3-24 ADC error (f_{ADC} = 12MHz:R_{AIN} < 10kΩ,V_{DD} > 2.9V)(f_{ADC} = 24MHz:R_{AIN} < 3kΩ,V_{DD} = 5V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ET	Total data deviation	f_{ADC} = 12 MHz		2	4	LSB
ETF24	f_{ADC} = 24MHz total data deviation	f_{ADC} = 24 MHz		3	6	
EO	Misalignment error	f_{ADC} = 12 MHz		1	3	
EG	Gain error	f_{ADC} = 12 MHz		1	2	
ED	Differential nonlinearity error	f_{ADC} = 12 MHz		0.5	2	
EL	Integral nonlinearity error	f_{ADC} = 12 MHz		0.6	2.5	

Note: Source simulation.

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-10 ADC typical connection diagram

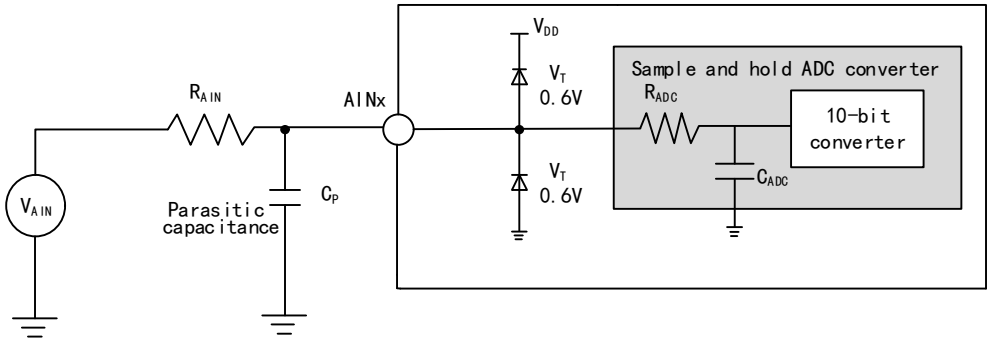
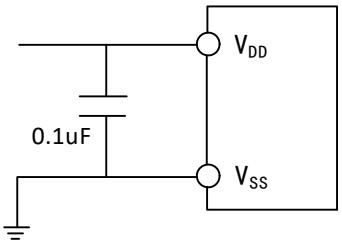


Figure 3-11 Analog power supply and decoupling circuit reference



3.3.15 OPA characteristics

Table 3-25 OPA characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		2.8		5.5	V
C_{MIR}	Common mode input voltage		0		V_{DD}	V
$V_{IOFFSET}$	Input offset voltage			3	10	mV
I_{LOAD}	Drive current				1.5	mA
$I_{DDOPAMP}$	Current consumption	No load, static mode		273		uA
C_{MRR}(1)	Common mode rejection ratio	@1KHz		81		dB
P_{SRR}(1)	Power supply rejection ratio	@1KHz		88		dB
A_V(1)	Open loop gain	C_{LOAD} = 50pF		105		dB
G_{BW}(1)	Unit gain bandwidth	C_{LOAD} = 50pF		12		MHz
P_M(1)	Phase margin	C_{LOAD} = 50pF		75		deg
S_R(1)	Slew rate limited	C_{LOAD} = 50pF		7.7		V/us
t_{WAKU}(1)	Setup time from shutdown to wake up, 0.1%	Input V_{DD}/2, C_{LOAD}=50pF,R_{LOAD}=4kΩ		520		ns
R_{LOAD}	Resistive load		4			kΩ
C_{LOAD}	Capacitive load				50	pF
V_{OHSAT}(2)	High saturation output voltage	R_{LOAD} = 4kΩ, input V_{DD}	V_{DD}-180			mV
		R_{LOAD} = 20kΩ, input V_{DD}	V_{DD}-36			
V_{OLSAT}(2)	Low saturation output voltage	R_{LOAD} = 4kΩ, input 0			5	mV
		R_{LOAD} = 20kΩ, input 0			5	
EN(1)	Equivalent input voltage noise	R_{LOAD} = 4kΩ, @1KHz		83		$\frac{nv}{\sqrt{Hz}}$
		R_{LOAD} = 4kΩ, @10KHz		28		

Note: 1. Design parameters are guaranteed.

2. The load current limits the saturated output voltage.