Chapter 5 Window Watchdog (WWDG)

A Window Watchdog is generally used to monitor system operation for software faults such as external disturbances, unforeseen logic errors, and other conditions. It requires a counter refresh (dog feeding) within a specific window time (with upper and lower limits), otherwise earlier or later than this window time the watchdog circuit will generate a system Reset.

5.1 Main Features

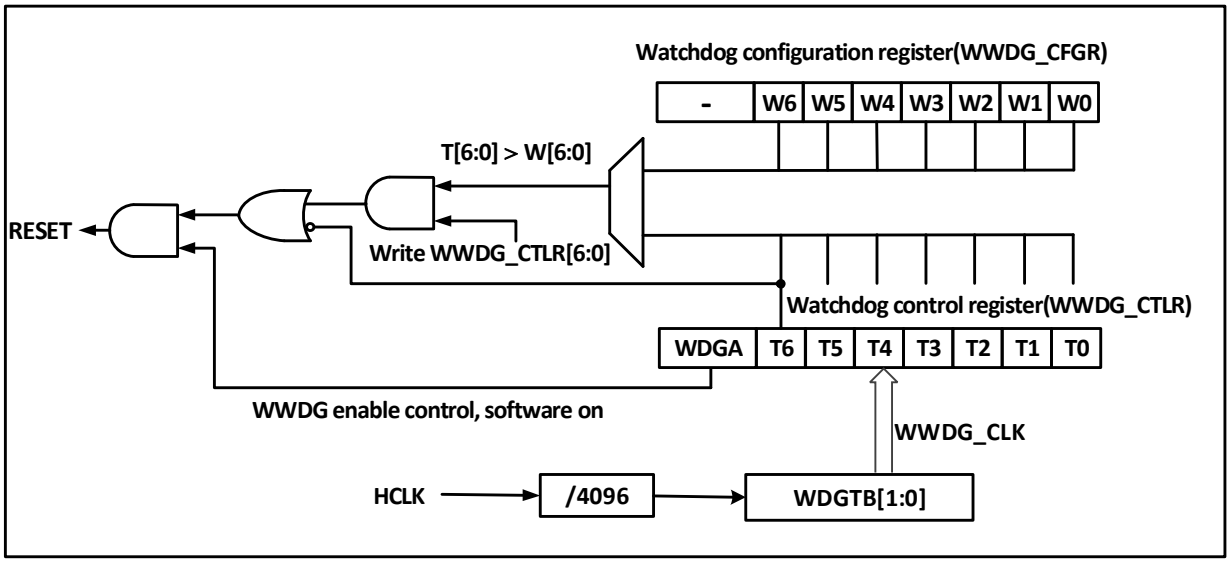
- Programmable 7-bit downcounter
- Biconditional reset: the downcounter value is less than 0x40, or the counter value is reloaded outside the window time
- Wake Up Early Notification (EWI) function for timely dog feeding action to prevent system Reset

5.2 Function Description

5.2.1 Principle and Application

The window watchdog operation is based on a 7-bit downcounter, which is mounted under the HB bus and counts the dividing frequency of the time base WWDG_CLK source (HCLK/4096) clock with the dividing factor set in the WDGTB[1:0] field in the configuration register WWDG_CFGR. The downcounter is in the free-running state, and the counter keeps cycling downcount regardless of whether the watchdog function is on or not. As shown in Figure 5-1, the block diagram of the internal structure of the window watchdog.

Figure 5-1 Block diagram of Window Watchdog structure



- Enable Window Watchdog

After a system Reset, the watchdog is off. Setting the WDGA bit of the WWDG_CTLR register enables the watchdog, and then it cannot be turned off again unless a reset occurs.

Note: The watchdog function can be stopped indirectly by setting the RCC_APB1PCENR register to turn off the clock source of WWDG and suspend the WWDG_CLK count, or by setting the RCC_APB1PRSTR register to reset the WWDG module, which is equivalent to the role of reset.

- Watchdog Configuration

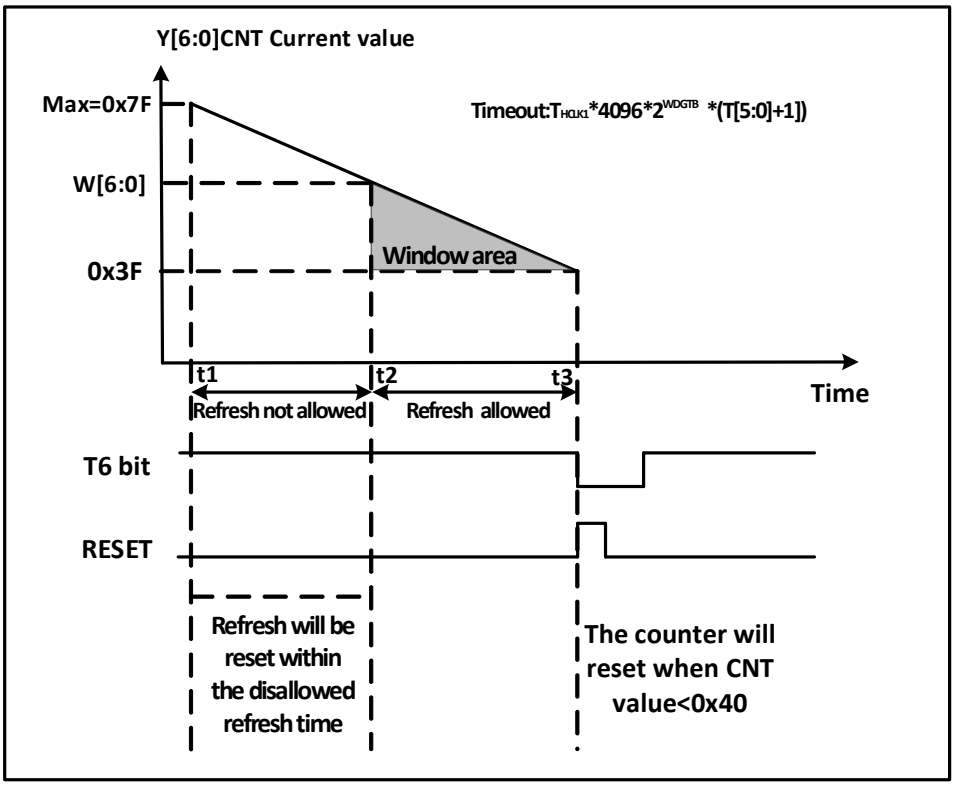
The watchdog is internally a 7-bit counter that runs in a continuous decreasing cycle and supports read and write access. To use the watchdog reset function, the following actions need to be performed.

1) Counting time base: via the WDGTB[1:0] bit field of the WWDG_CFGR register, note that the WWDG module clock of the RCC unit should be turned on.
2) Window counter: Set the W[6:0] bit field of WWDG_CFGR register, this counter is used by hardware as a comparison with the current counter, the value is configured by user software and will not change. It is used as the upper limit value of the window time.
3) Watchdog enable: WDG_CTLR register WDGA bit software set to 1, to turn on the watchdog function, you can system reset.
4) Feed the dog: i.e., refresh the current counter value and configure the T[6:0] bit field of the WWDG_CTLR register. This action needs to be executed within the periodic window time after the watchdog function is turned on, otherwise a watchdog reset action will occur.

- Dog feeding window time

As shown in Figure 5-2, the gray area is the monitoring window area of the window watchdog, whose upper time t2 corresponds to the point in time when the current counter value reaches the window value W[6:0]; its lower time t3 corresponds to the point in time when the current counter value reaches 0x3F. This area time t2<t<t3 can be fed with a dog operation (write T[6:0]) to refresh the current counter value.

- Figure 5-2 Counting mode of Window Watchdog



- Watchdog reset

1) When the value of T[6:0] counter changes from 0x40 to 0x3F due to no timely dog feeding operation, a "window watchdog reset" will occur and a system reset will be generated. That is, the T6-bit is detected as 0 by the hardware and a system reset will occur.
   Note: The application can write T6-bit to 0 by software to achieve system Reset, which is equivalent to software reset function.
2) When the counter refresh action is executed within the disallowed dog feeding time, i.e., the write T[6:0] bit field is operated within $t_1 \leqslant t \leqslant t_2$ time, a "window watchdog reset" will occur and a system Reset will be generated.

- Wake up in advance

To prevent the system Reset caused by not refreshing the counter in time, the watchdog module provides an early wakeup interrupt (EWI) notification. When the counter self-decreases to 0x40, an early wake-up signal is generated and the EWIF flag is set to 1. If the EWI bit is set, a window watchdog interrupt will be triggered at the same time. At this time, there is 1 counter clock cycle (self-decrement to 0x3F) before the hardware reset, and the application can perform the dog feeding operation instantly within this time.

5.2.2 Debug Mode

When the system enters Debug mode, the counter of WWDG can be configured by the debug module register to continue or stop.

5.3 Register Description

Table 5-1 WWDG-related registers list

Name	Access address	Description	Reset value
R16_WWDG_CTLR	0x40002C00	Control register	0x007F
R16_WWDG_CFGR	0x40002C04	Configuration Register	0x007F
R16_WWDG_STATR	0x40002C08	Status Register	0x0000

5.3.1 Control Register (WWDG_CTLR)

Offset address: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								WDGA	T[6:0]						

Bit	Name	Access	Description	Reset value
[15:8]	Reserved	RO	Reserved	0
7	WDGA	RW1	Window watchdog reset enable bit. 1: Turn on the watchdog function (which generates a reset signal). 0: Disable the watchdog function. Software write 1 is on, but only allows hardware to clear 0 after reset.	0
[6:0]	T[6:0]	RW	The 7-bit self-decrement counter decrements by 1 every $4096*2^{WDGTB}$ HCLK cycles. A watchdog reset is generated when the counter decrements from 0x40 to 0x3F, i.e., when T6 jumps to 0.	7Fh

5.3.2 Configuration Register (WWDG_CFGR)

Offset address: 0x04

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						EWI	WDGTB[1:0]		W[6:0]						

Bit	Name	Access	Description	Reset value
[15:10]	Reserved	RO	Reserved	0
9	EWI	RW1	Early wakeup interrupt enable bit. If this position is 1, an interrupt is generated when the counter value reaches 0x40. This bit can only be invited to 0 by hardware after a reset.	0
[8:7]	WDGTB[1:0]	RW	Window watchdog clock division selection. 00: Divided by 1, counting time base = HCLK/4096. 01: Divided by 2, counting time base = HCLK /4096/2.	0

			10: Divided by 4, counting time base = HCLK /4096/4. 11: Divided by 8, counting time base = HCLK /4096/8.	
[6:0]	W[6:0]	RW	Window watchdog 7-bit window value. Used to compare with the counter value. The feed dog operation can only be performed when the counter value is less than the window value and greater than 0x3F.	7Fh

5.3.3 Status Register (WWDG_STATR)

Offset address: 0x08

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															EWIF

Bit	Name	Access	Description	Reset value
[15:1]	Reserved	WO	Reserved	0
0	EWIF	RW0	Wake up the interrupt flag bit early. When the counter reaches 0x40, this bit is set in hardware and must be cleared to 0 by software; the user setting is invalid. Even if the EWI is not set, this bit will still be set as usual when the event occurs.	0