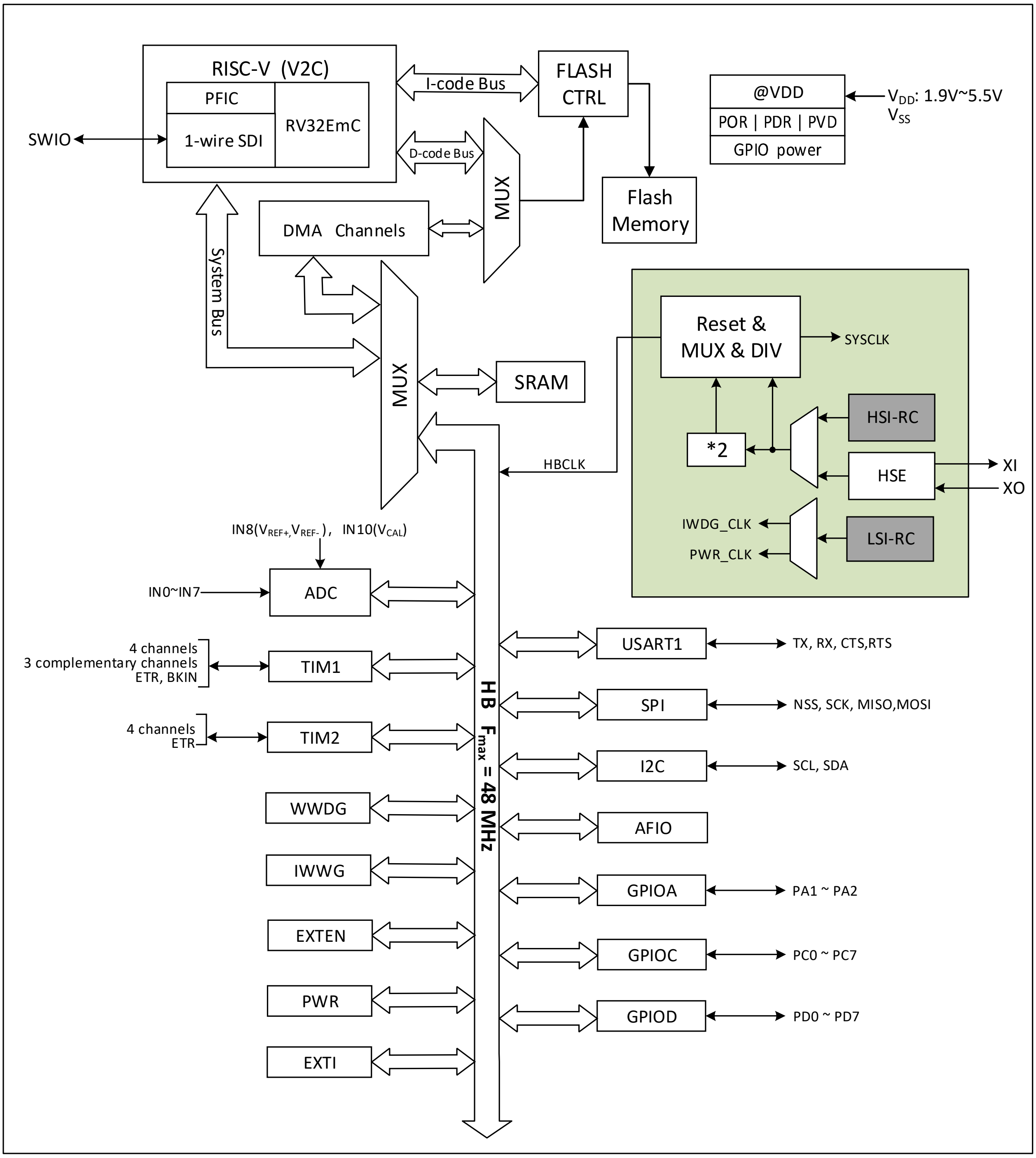
Chapter 1 Specification Information

1.1 System Structure

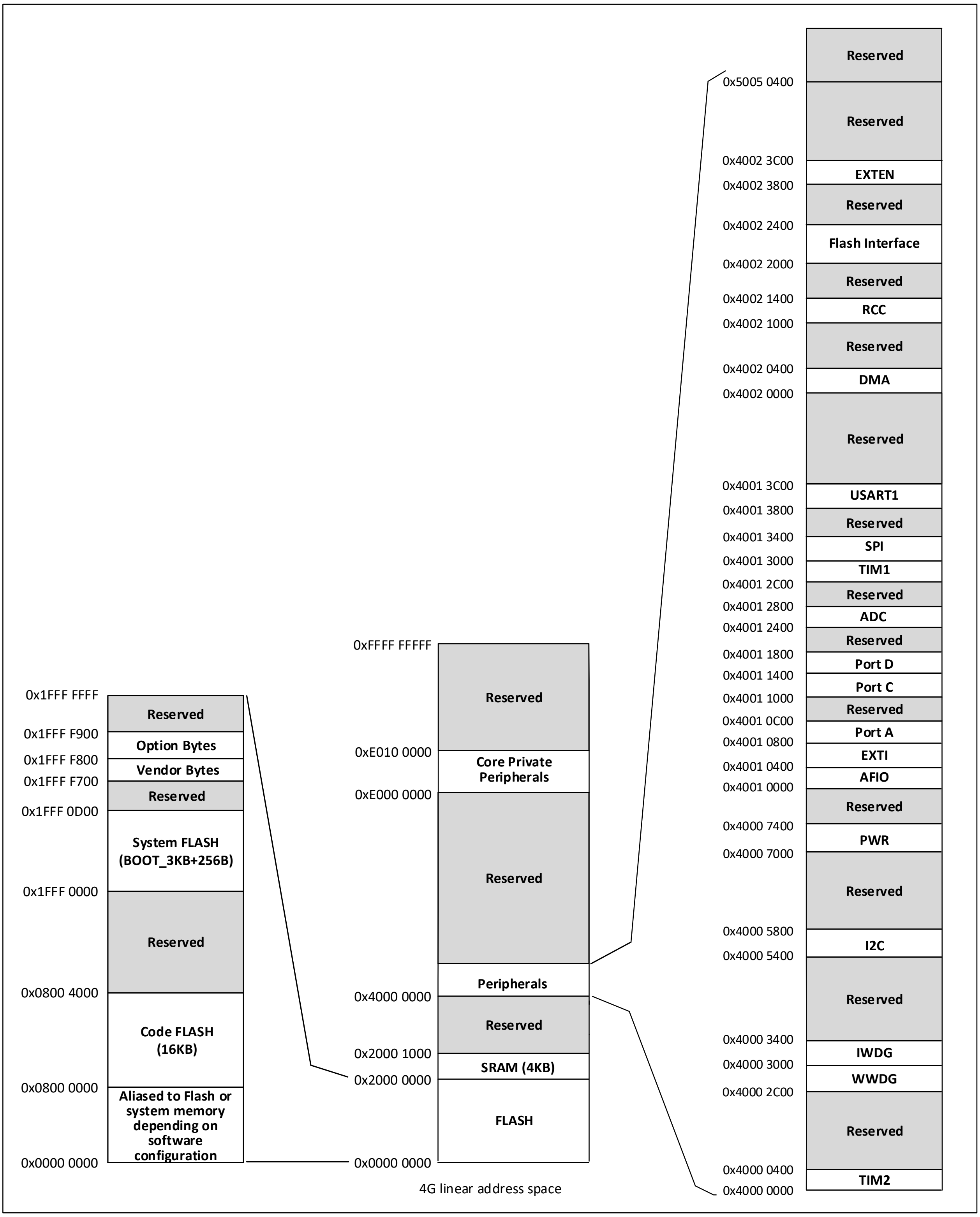
The microcontroller is based on the RISC-V instruction set design, its architecture will be QingKe microprocessor core, arbitration unit, DMA module, SRAM storage and other components through multiple buses to achieve interaction. The design integrates a general-purpose DMA controller to reduce the burden on the CPU, improve access efficiency. Multi-level clock management mechanism is applied to reduce the power consumption of peripherals, while both data protection mechanisms, automatic clock switching protection and other measures to increase system stability. The following diagram shows the overall architecture.

Figure 1-1 MCU system block diagram



1.2 Memory Map

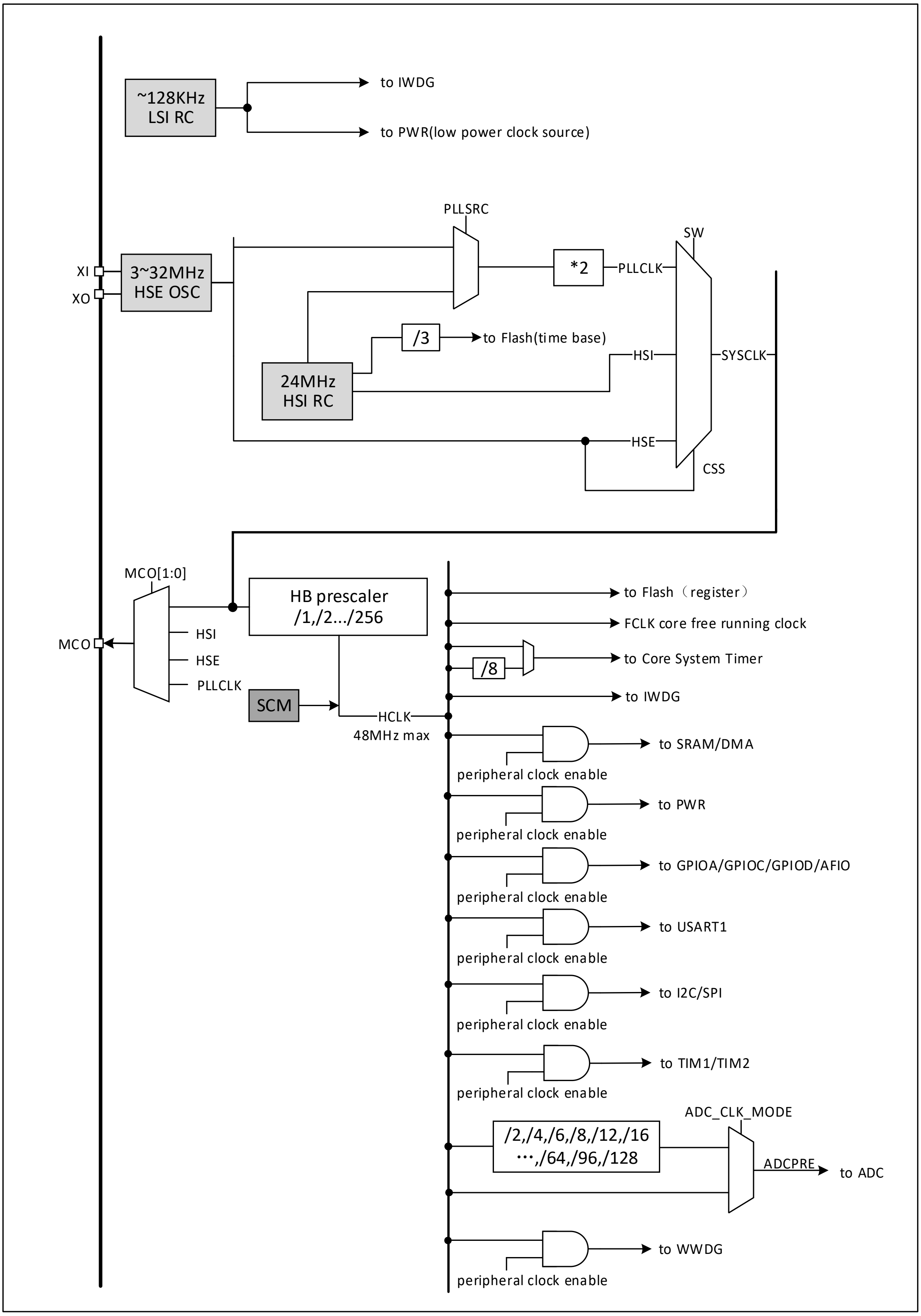
Figure 1-2 Memory address map



1.3 Clock Tree

3 sets of clock sources are introduced into the system: Internal high-frequency RC oscillator (HSI), internal low-frequency RC oscillator (LSI) and external high-frequency oscillator (HSE). Among them, the low-frequency clock source provides a clock reference for the automatic wake-up unit, and the high-frequency clock source is directly or indirectly output as the system bus clock (SYSCLK) through a 2x multiplier, and the system clock is then provided by the pre-scaler for the HB domain peripheral control clock and sampling or interface output clock. Part of the module working need to be provided by PLL clock directly.

Figure 1-3 Clock tree block diagram



1.4 Functional Description

1.4.1 QingKe RISC-V2A Processor

RISC-V2C supports RISC-V instruction set EmC[(1)] subset. The processor is internally managed in a modular fashion and contains units such as a programmable fast interrupt controller (PFIC), extended instruction support, and so on. The bus is connected to external unit modules to enable interaction between external function modules and the core. QingKe processor with its minimalist instruction set, a variety of operating modes, modular customization and expansion features can be flexibly applied to different scenarios MCU design, such as small area low-power embedded scenarios.

- Support machine and user privileged modes
- Fast Programmable Interrupt Controller (PFIC)
- 2-level hardware interrupt stack
- Support 1-wire /2-wire serial debug interface (SDI)
- Custom extension instructions

Note: 1. The "m" extension in EmC implements the multiplication subset of the M extension.

1.4.2 On-chip Memory

Built-in 4K-byte SRAM area, which is used to store data, which is lost after power loss.

Built-in 16K-byte program flash memory area (Code FLASH), that is, the user area, is used for users' applications and constant data storage.

Built-in 3328-byte system storage area (System FLASH), that is, BOOT area, is used for system boot program storage (factory-solidified bootloader).

Built-in 256-byte system non-volatile configuration information storage area, used for manufacturer configuration word storage, solidified before leaving the factory, users can not be modified.

Built-in 256-byte user-defined information store for user option byte storage.

1.4.3 Power Supply Scheme

V_{DD} = 1.9 ~ 5.5V: Supplies power to the I/O pins as well as the internal regulator; when using an ADC, V_{DD} must not be less than 2.4V.

1.4.4 Power Supply Monitor

The power-on reset (POR) / power-down reset (PDR) circuit is integrated inside the chip, which is always in the operating state to ensure that the system works when the power supply exceeds 1.9V; when the V_{HV} is lower than the set threshold ($V_{POR/PDR}$), the device is placed in the reset state without the need to use an external reset circuit.

In addition, the system has a programmable voltage detector (PVD), which needs to be turned on by software, which is used to compare the voltage of V_{HV} power supply with the set threshold V_{PVD}. When the corresponding edge interrupt of the PVD is turned on, an interrupt notification can be generated when the V_{HV} falls to the PVD threshold or rises to the PVD threshold. Refer to Chapter 3 for the values of $V_{POR/PDR}$ and V_{PVD}.

1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are two modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.

1.4.6 Low-power Mode

The system supports two low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.
Exit condition: Any interruption or wake-up event.

- Standby mode (STANDBY)

A peripheral clock control mechanism is combined with the SLEEPDEEP of the core and allows the voltage regulator to operate in a lower power state. The high-frequency clock (HSI/HSE/PLL) domain is turned off, SRAM and register contents are maintained, and I/O pin states are maintained. The system can continue to run after this mode wakes up, with HSI as the default system clock.
Exit conditions: Any external interrupt / event (EXTI signal), external reset signal on NRST, IWDG reset, in which EXTI signal includes one of 18 external I/O ports, PVD output, automatic wake-up, etc.

1.4.7 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 255 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. Currently the chip manages 4 core private interrupts and 25 peripheral interrupt management, with other interrupt sources reserved. the PFIC registers are all accessible in both user and machine privileged modes.

- 2 individually maskable interrupts
- Provide one non-maskable interrupt NMI
- Support Hardware Prologue/Epilogue (HPE) without instruction overhead
- Provide 2 Vector Table Free (VTF) for faster access to interrupt service routines
- Vector table support address or instruction mode
- Interrupt nesting depth can be configured up to 2 levels
- Support interrupt tail linking

1.4.8 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 10 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect clock cycles with pulse widths less than the internal HB. Up to 18 general-purpose I/O ports are optionally connected to the same external interrupt line.

1.4.9 General-purpose DMA Controller

The system has built-in general-purpose DMA controller, manages 7 channels, flexibly handles high-speed data transmission from memory to memory, peripheral to memory and memory to peripheral devices, and supports ring buffer mode. Each channel has special hardware DMA request logic, which supports one or more peripheral access requests to memory. Access priority, transmission length, source address and destination address of transmission can be configured.
DMA for the main peripherals include: general / advanced timer TIMx, ADC, USART, I2C, SPI.
Note: DMA and CPU access the system SRAM after arbitration by the arbitrator.

1.4.10 Clock and Boot

The system clock source HSI is on by default. After no clock is configured or reset, the RC oscillator of the internal 24MHz is used as the default CPU clock, and then the external 3~25MHz clock or PLL clock can be selected. When clock safe mode is turned on, if HSE is used as the system clock (directly or indirectly), if an external clock failure is detected, the system clock will automatically switch to the internal RC oscillator, while HSE and PLL will automatically turn off; for low-power mode with clock off, the system will also automatically switch to the internal RC oscillator after waking up. If the clock interrupt is enabled, the software can receive the corresponding interrupt. In addition, in order to improve the reliability of the system, System Clock Monitor (SCM) module is added. When the enable bit is turned on, if the system clock fails, a brake signal will be generated to the advanced timer TIM1, and the system clock failure interrupt flag will be set. If the enable is interrupted in advance, the interrupt will be entered.

1.4.11 Analog-to-digital Converter (ADC)

The chip has a built-in 12-bit ADC that provides up to 8 external channels and 3 internal channels for sampling at sampling rates up to 3Msps, providing programmable channel sampling time for single, continuous, scan or intermittent conversion. The analog watchdog function allows very accurate monitoring of one or more selected channels for monitoring the channel signal voltage, and when the voltage exceeds a set threshold, the system can be configured to generate a reset and protect the system.

The internal channel of ADC is ADC_IN8~ADC_IN10. The internal reference voltage V_{REF} is connected to the IN8 input channel; the OPA internal output channel is connected to the IN9 input channel for converting the output of the OPA into digital values; and the internal calibration voltage VCAL is connected to the IN10 input channel, which is half of the system power supply voltage V_{DD}.

1.4.12 Timer and Watchdog

- Advanced-control Timer (TIM1)

The advanced-control timer is a 16-bit automatic load increment / decrement counter with a 16-bit programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to 6 channels, with a complementary PWM output function with dead-zone insertion, allowing the timer to be updated after a specified number of counter cycles for repeated counting cycles, braking functions, etc. Advanced control timers have the same functions as general timers and have the same internal structure, so advanced control timers can cooperate with other TIM timers through timer linking function to provide synchronization or event linking functions.

- General-purpose timer (TIM2)

The general-purpose timer is a 16-bit auto-load add / subtract counter with a programmable 16-bit prescaler and 4 independent channels, each of which supports input capture, output comparison, PWM generation and monopulse mode output. By multiplexing channels 3 and 4, channels 1 and 2 also have complementary PWM output with dead-time insertion. In addition, it can work with the advanced-control timer TIM1 through the timer linking function to provide synchronization or event linking functions. In debug mode, counters can be frozen and any general-purpose timer can be used to generate PWM output.

- Independent Watchdog (IWDG)

Independent watchdog is a free-running 12-bit decreasing counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 128KHz; the LSI is independent of the master clock and can operate in standby mode. IWDG works completely independently of the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware startup watchdog. Counters can be frozen in debug mode.

- Window Watchdog (WWDG)

Window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- SysTick Timer (SysTick)

QingKe microprocessor core comes with a 32-bit incremental counter for generating SYSTICK exceptions (exception number: 15), which can be specially used in real-time operating systems to provide "heartbeat" rhythm for the system, and can also be used as a standard 32-bit counter. It has automatic reload function and programmable clock source.

1.4.13 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 1 set of USART. Support full-duplex asynchronous serial communication and half-duplex single-wire communication, also support LIN (Local Internet), compatible with IrDA SIR ENDEC transmission codec specification, and modem (CTS/RTS hardware flow control) operation, but also support multiprocessor communication. It adopts fractional baud rate generator system and supports continuous communication of DMA operation.

1.4.14 Serial Peripheral Interface (SPI)

The chip provides a serial peripheral SPI interface, which supports master or slave operation and dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit choice, reliable communication hardware CRC generation / check, support DMA operation continuous communication.

1.4.15 I2C Bus

The chip provides an I2C bus interface, which can work in multi-host mode or slave mode, and complete all I2C bus specific timing, protocol, arbitration and so on. Both standard and fast communication speeds are supported.
The I2C interface provides 7-bit or 10-bit addressing and supports double-slave address addressing in 7-bit slave mode. Built-in hardware CRC generator / verifier.

1.4.16 General-purpose Input and Output (GPIO)

The system provides 3 sets of GPIO ports (PA0~PA7, PB0~PB6, PC0~PC7, PD0~PD7) with a total of 18 GPIO pins. Most pins can be configured by software to output (push-pull or open-drain), input (with or without pull-up or pull-down), or reused peripheral function ports.
When PA1PA2_REMAP=1, PA1 and PA2 only support push-pull output and reuse push-pull output.
All GPIO pins support controllable pull-up and pull-down resistors. When PD7/RST and PC5/RST_2 are used as reset pins, the pull-up resistor is turned on and the pull-down resistor is turned off by default.
All GPIO pins are shared with digital or analog multiplexing peripherals. All GPIO pins have a large current drive capability. A locking mechanism is provided to freeze the I/O configuration to avoid accidental writing to the I/O register.
The power supply of all the I/O pins in the system is provided by the V_{DD}. By changing the V_{DD} power supply, the

output level of the I/O pin will be changed to adapt to the external communication interface level. Please refer to the pin description for the specific pin.

1.4.18 1-wire Serial Debug Interface (SDI)

The core comes with 1-wire SDI Serial Debug Interface, which corresponds to SWIO pin (Single Wire Input Output). The debug interface pin function is turned on by default after the system is powered on or reset, and the SDI can be turned off according to the need after the main program is running.