Chapter 4 Independent Watchdog (IWDG)

The system is equipped with an independent watchdog (IWDG) to detect logic errors and software faults caused by external environmental disturbances. the IWDG clock source is derived from the LSI and can run independently of the main program, making it suitable for applications requiring low accuracy.

4.1 Main Features

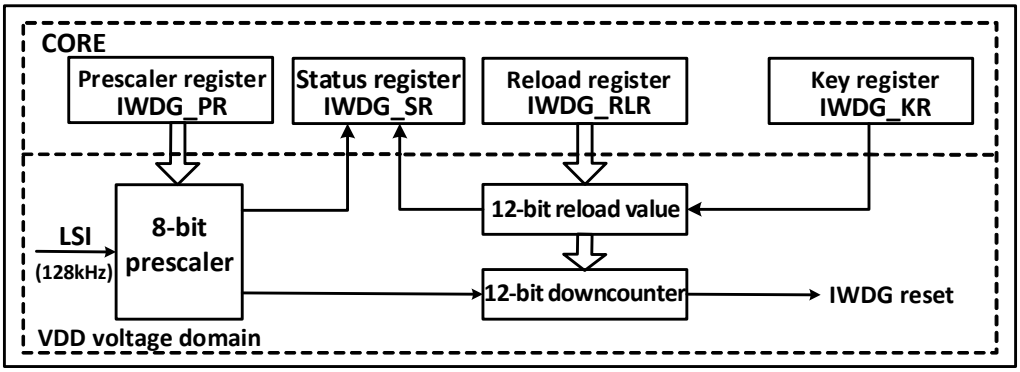
- 12-bit self-subtracting counter
- Clock source LSI divider, can run in low-power mode
- Reset condition: Counter value is reduced to 0

4.2 Function Description

4.2.1 Principle and Application

The independent watchdog is clocked from the LSI clock and its function remains functional during shutdown and Standby modes. When the watchdog counter self-decreases to 0, a system Reset will be generated, so the timeout is (reload value + 1) clock.

Figure 4-1 Block diagram of the structure of the independent watchdog



- Enable independent watchdog

After a system reset, the watchdog is off and writing 0xCCCC to the IWDG_CTLR register turns the watchdog on, after which it cannot be turned off again unless a reset occurs.

If the hardware independent watchdog enable bit (IWDG_SW) is turned on at the user-option bytes, IWDG will be fixed on after a microcontroller reset.

- Watchdog configuration

The watchdog is internally a 12-bit counter that runs decreasingly. When the counter value decreases to 0, a system Reset will occur. To turn on the IWDG function, the following actions need to be performed.

1) Counting time base: IWDG clock source LSI, set the LSI crossover value clock as the counting time base of IWDG through the IWDG_PSCR register. The operation method first writes 0x5555 to the IWDG_CTLR register, and then modifies the crossover value in the IWDG_PSCR register. the PVU bit in the IWDG_STATR register indicates the update status of the crossover value, and the crossover value can be modified and read out only when the update is completed.
2) Reload value: Used to update the current value of the counter in the standalone watchdog and the counter is decremented by this value. The RVU bit in the IWDG_STATR register indicates the update status of the reload value, and the IWDG_RLDR register can be modified and read out only when the update is completed.
3) Watchdog enable: write 0xCCCC to the IWDG_CTLR register to enable the watchdog function.

4) Feed the dog: i.e., flush the current counter value before the watchdog counter decrements to 0 to prevent a system reset from occurring. Write 0xAAAA to the IWDG_CTLR register to allow the hardware to update the IWDG_RLDR register value to the watchdog counter. This action needs to be executed regularly after the watchdog function is turned on, otherwise a watchdog reset action will occur.

4.2.2 Debug Mode

When the system enters Debug mode, the counter of IWDG can be configured by the debug module register to continue or stop.

4.3 Register Description

Table 4-1 IWDG-related registers list

Name	Access address	Description	Reset value
R16_IWDG_CTLR	0x40003000	Control register	0x0000
R16_IWDG_PSCR	0x40003004	Prescaler register	0x0000
R16_IWDG_RLDR	0x40003008	Reload register	0x0FFF
R16_IWDG_STATR	0x4000300C	Status register	0x0000

4.3.1 Control Register (IWDG_CTLR)

Offset address: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEY[15:0]															

Bit	Name	Access	Description	Reset value
[15:0]	KEY	WO	Operate the key value lock. 00xAAAA: Feed the dog. Loading of the IWDG_RLDR register value into the independent watchdog counter. 0x5555: Allows modification of the R16_IWDG_PSCR and R16_IWDG_ RLDR registers. 0xCCCC: Start the watchdog, but not if the hardware watchdog is enabled (user-option bytes configuration).	0

4.3.2 Prescaler Register (IWDG_PSCR)

Offset address: 0x04

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PR[2:0]		

Bit	Name	Access	Description	Reset value
[15:3]	Reserved	RO	Reserved	0
[2:0]	PR[2:0]	RW	IWDG clock division factor, write 0x5555 to KEY before modifying this field. 000: Divided by 4; 001: Divided by 8. 010: Divided by 16; 011: Divided by 32. 100: Divided by 64; 101: Divided by 128. 110: Divided by 256; 111: Divided by 256. IWDG counting time base = LSI/divide factor. *Note: Before reading the value of this field, make sure the PVU bit in the IWDG_STATR register is 0, otherwise the read value is invalid.*	0

4.3.3 Reload Register (IWDG_RLDR)

Offset address: 0x08

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				RL[11:0]											

Bit	Name	Access	Description	Reset value
[15:12]	Reserved	RO	Reserved	0
[11:0]	RL[11:0]	RW	Counter reload value. Write 0x5555 to the KEY before modifying this field. When 0xAAAA is written to the KEY, the value of this field will be loaded into the counter by hardware, and the counter will then count decreasingly from this value. *Note: Before reading or writing the value of this field, make sure the RVU bit in the IWDG_STATR register is 0, otherwise reading or writing this field is invalid.*	FFFh

4.3.4 Status Register (IWDG_STATR)

Offset address: 0x0C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														RVU	PVU

Bit	Name	Access	Description	Reset value
[15:2]	Reserved	RO	Reserved	0
1	RVU	RO	Reload value update flag bit. Hardware set or clear 0. 1: Reload value update is in progress. 0: End of reload update (up to 5 LSI cycles). *Note: The reload value register IWDG_RLDR can only be accessed read or write after the RVU bit is cleared to 0.*	0
0	PVU	RO	Clock division factor update flag bit. Hardware set or clear 0. 1: Clock division value update is in progress. 0: End of clock division value update (up to 5 LSI cycles). *Note: The crossover factor register IWDG_PSCR can only be accessed read or write after the PVU bit is cleared to 0.*	0

Note: After the prescaler or reload value is updated, it is not necessary to wait for the RVU or PVU to reset, and the following code can continue to be executed. (This write operation will continue to be executed to completion even in low-power mode.)