Chapter 3 Reset and Clock Control (RCC)

The controller provides different forms of resets and configurable clock tree structures based on the division of power areas and peripheral power management considerations in the application. This section describes the scope of each clock in the system.

3.1 Main Features

- Multiple reset forms
- Multiple clock sources, bus clock management
- Built-in external crystal oscillation monitoring and clock security system
- Independent management of each peripheral clock: reset, on, off
- Supports internal clock output

3.2 Reset

The controller provides 2 forms of reset: power Reset and system Reset.

3.2.1 Power Reset

When a power Reset occurs, it will reset all registers.
A power Reset is generated when the following event occurs:

- Power-up/power-down reset (POR/PDR)

3.2.2 System Reset

When a system Reset occurs, it will reset the reset flag in addition to the control/status register RCC_RSTSCKR and all the registers. The source of the reset event is identified by looking at the reset status flag bit in the RCC_RSTSCKR register.

A system Reset is generated when one of the following events occurs:

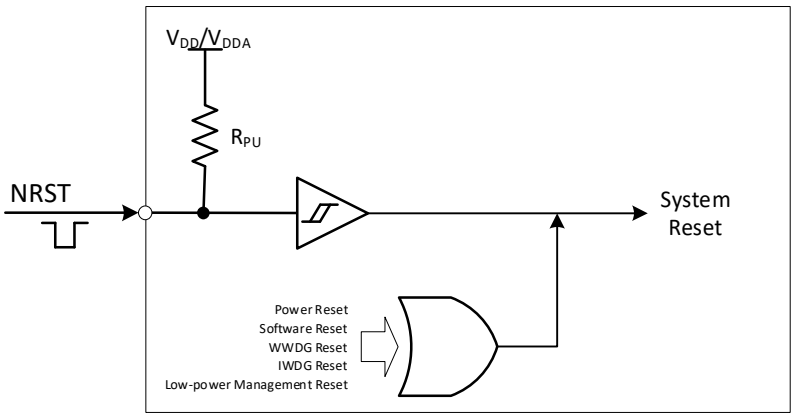
- Low signal on NRST pin (external reset)
- Window watchdog count termination (WWDG reset)
- Independent watchdog count termination (IWDG reset)
- Software reset (SW reset)
- Low-power management reset

Window/Independent Watchdog Reset: Generated by the window/independent watchdog peripheral timer count cycle overflow trigger, see its corresponding section for detailed description.

Software reset: The CH32V003 product resets the system via the RSTSYS position 1 of the interrupt configuration register PFIC_CFGR in the programmable interrupt controller PFIC or the SYSRST position 1 of the configuration register PFIC_SCTLR to reset the system cabinet, refer to the corresponding chapter for details.

Low Power Management Reset: Standby mode reset will be enabled by setting the STANDBY_RST position 1 in the user select byte. This will perform a system reset instead of entering standby mode after the process of entering standby mode is executed.

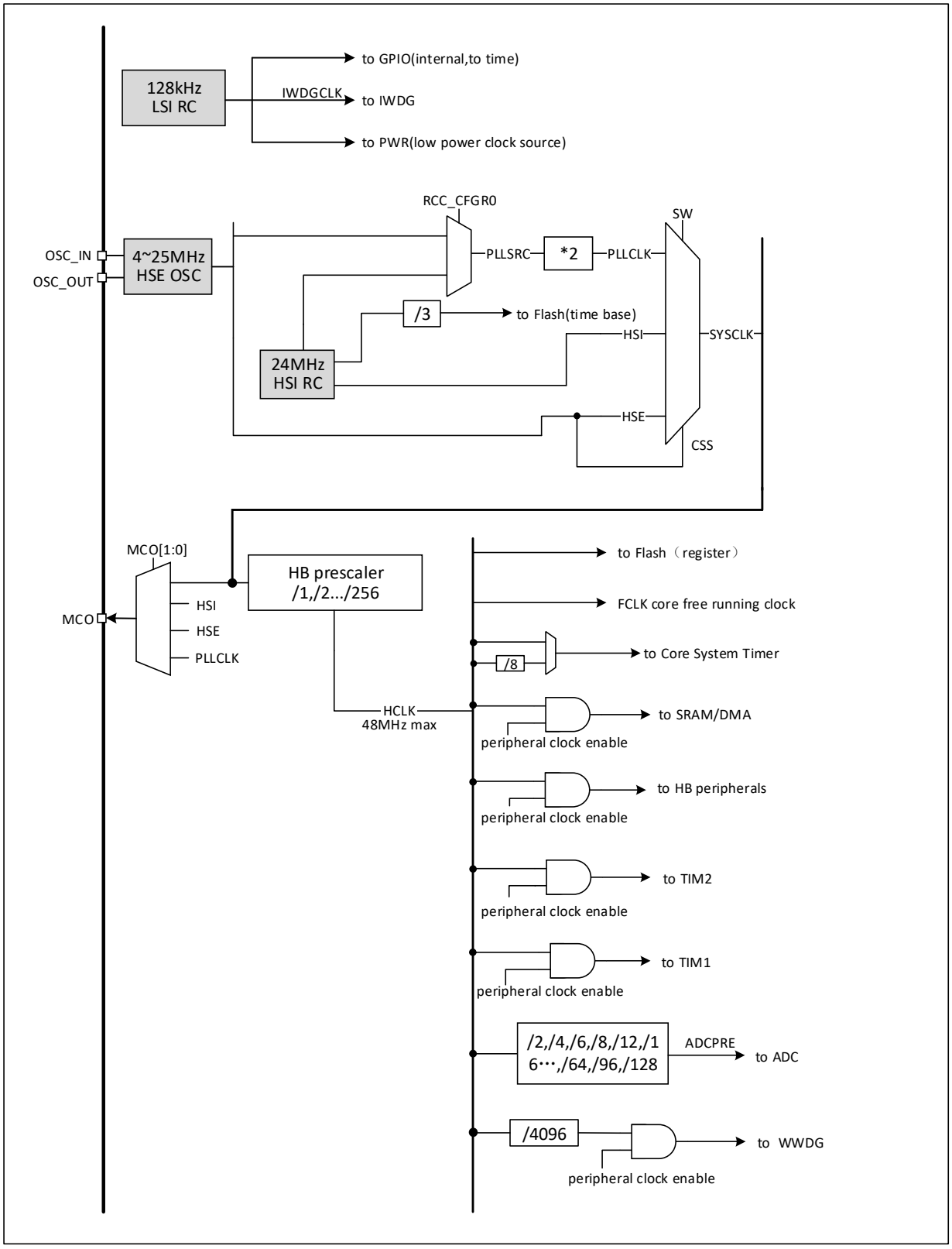
Figure 3-1 System reset structure



3.3 Clock

3.3.1 System Clock Structure

Figure 3-2 CH32V003 clock tree block diagram



3.3.2 High-speed Clock (HSI/HSE)

HSI is a high-speed clock signal generated by the system's internal 24MHz RC oscillator. HSI RC oscillator can provide system clock without any external devices. It has a short start-up time. HSI is enabled and disabled by setting the HSION bit in the RCC_CTLR register, and the HSIRDY bit indicates whether the HSI RC oscillator is stable or not. The system defaults HSION and HSIRDY to 1 (it is recommended not to turn them off). If the HSIRDYIE bit in the RCC_INTR register is set, the corresponding interrupt will be generated.

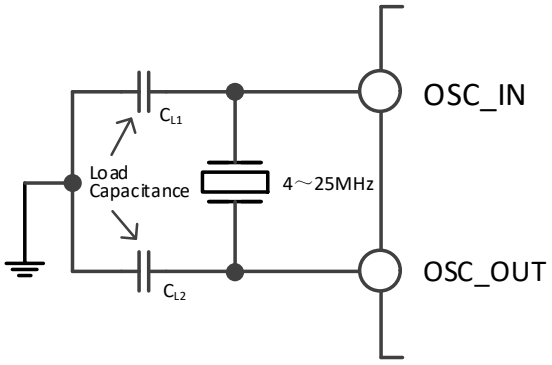
- Factory calibration: The difference of manufacturing process will cause different RC oscillation frequency for each chip, so HSI calibration is performed for each chip before it is shipped. After system reset, the factory calibration value is loaded into HSICAL[7:0] of the RCC_CTLR register.
- User tuning: Based on different voltages or ambient temperatures, the application can adjust the HSI frequency by using the HSITRIM[4:0] bits in the RCC_CTLR register.

Note: If the HSE crystal oscillator fails, the HSI clock is used as a backup clock source (clock safety system).

HSE is an external high speed clock signal, including external crystal/ceramic resonator generation or external high speed clock feed.

- External Crystal/Ceramic Resonator (HSE Crystal): An external 4-25MHz oscillator provides a more accurate clock source for the system. Further information can be found in the Electrical Characteristics section of the datasheet. The HSE crystal can be turned on and off by setting the HSEON bit in the RCC_CTLR register. The HSERDY bit indicates whether the HSE crystal oscillation is stable or not, and the hardware feeds the clock into the system only after HSERDY position 1. If the HSERDYIE bit of the RCC_INTR register is set, the corresponding interrupt will be generated.

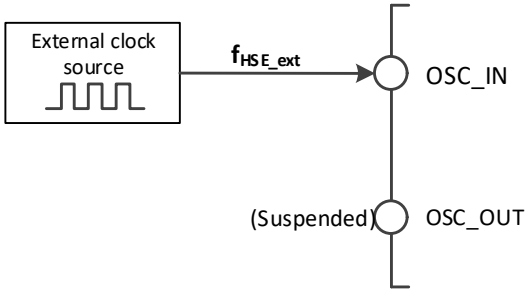
Figure 3-3 High-speed external crystal circuit



Note: The load capacitor needs to be as close to the oscillator pin as possible and the capacitance value should be selected according to the crystal manufacturer's parameters.

- External High-speed Clock Source (HSE Bypass): This mode feeds the clock source directly from the external to the OSC_IN pin, with the OSC_OUT pin dangling. The maximum frequency supported is 25MHz. The application needs to set the HSEBYP bit to turn on the HSE bypass function with the HSEON bit at 0, and then set the HSEON bit again.

Figure 3-4 High-speed clock source circuit



3.3.3 Low-speed Clock (LSI)

The LSI is a low-speed clock signal generated by the system's internal RC oscillator of approximately 128 KHz. It can be kept running in shutdown and standby modes and provides the clock reference for the RTC clock, independent watchdog and wake-up unit. Further information can be found in the Electrical Characteristics section of the datasheet. the LSI can be enabled and disabled by setting the LSION bit in the RCC_RSTSCKR register and then detecting whether the LSI RC oscillation is stable by interrogating the LSIRDY bit, and the hardware feeds the clock in only after LSIRDY position 1. If the LSIRDYIE bit in the RCC_INTR register is set, the corresponding interrupt will be generated.

3.3.4 PLL Clock

By configuring the RCC_CFGR0 register and the extended register EXTEND_CTR, the internal PLL clock can select 2 clock sources, these settings must be done before PLL is turned on, once PLL is started these parameters cannot be changed. Set the PLLON bit in the RCC_CTLR register to be enabled and disabled, the PLLRDY bit to indicate whether the PLL clock is stable, and the hardware to feed the clock into the system only after PLL position 1. If the PLLRDYIE bit of the RCC_INTR register is set, the corresponding interrupt will be generated.

PLL clock source:

- HSI clock
- HSE Clock

3.3.5 Bus/Peripheral Clock

3.3.5.1 System Clock (SYSCLK)

Configure the system clock source by configuring the RCC_CFGR0 register SW[1:0] bits, SWS[1:0] indicates the current system clock source.

- HSI as system clock
- HSE as system clock
- PLL as system clock

After a controller reset, the default HSI clock is selected as the system clock source. Switching between clock sources must occur only when the target clock source is ready.

3.3.5.2 HB Bus Peripheral Clock (HCLK)

The HB bus clocks can be configured by configuring the HPRE[3:0] bits of the RCC_CFGR0 register. The bus clock determines the peripheral interface access clock reference that is mounted below them. Applications can adjust different values to reduce the power consumption when some of the peripherals are operating.

The various bits in the RCC_APB1PRSTR and RCC_APB2PRSTR registers can reset the different peripheral modules to their initial state.

Each bit in the RCC_AHBPCENR, RCC_APB1PCENR, and RCC_APB2PCENR registers can be used to individually turn on or off the communication clock interface for different peripheral modules. When using a peripheral, you first need to turn on its clock enable bit in order to access its registers.

3.3.5.3 Independent Watchdog Clock

If the independent watchdog has been set by hardware configuration or started by software, the LSI oscillator will be forced on and cannot be turned off. After the LSI oscillator is stabilized, the clock is supplied to the IWDG.

3.3.5.4 Microcontroller Clock Output (MCO)

The microcontroller allows outputting clock signals to the MCO pins. The following 4 clock signals can be selected as MCO clock outputs by configuring the multiplexed push-pull output mode in the corresponding

GPIO port registers by configuring the MCO[2:0] bits of the RCC_CFGR0 register.

- System clock (SYSCLK) output
- HSI clock output
- HSE clock output
- PLL clock output

3.3.6 Clock Security System

The clock safety system is an operational protection mechanism for the controller that switches to the HSI clock in the event of an HSE clock transmit failure and generates an interrupt notification to allow the application software to complete a rescue operation.

The clock security system is activated by setting CSSON position 1 of the RCC_CTLR register. At this point, the clock monitor will be enabled after the HSE oscillator start (HSERDY=1) delay and will be turned off after the HSE clock is turned off. Once the HSE clock fails during system operation, the HSE oscillator will be turned off, the clock failure event will be sent to the brake input of the advanced-control timer (TIM1) and a clock safety interrupt will be generated with CSSF position 1 and the application enters the NMI non-maskable interrupt. By setting the CSSC bit, the CSSF bit flag can be cleared and the NMI interrupt pending bit can be undone.

If the current HSE is used as the system clock, or if the current HSE is used as the PLL input clock and the PLL is used as the system clock, the clock safety system will automatically switch the system clock to the HSI oscillator and turn off the HSE oscillator and PLL in case of HSE failure.

3.4 Register Description

Table 3-1 RCC-related registers list

Name	Access address	Description	Reset value
R32_RCC_CTLR	0x40021000	Clock control register	0x0000xx83
R32_RCC_CFGR0	0x40021004	Clock configuration register 0	0x00000020
R32_RCC_INTR	0x40021008	Clock interrupt register	0x00000000
R32_RCC_APB2PRSTR	0x4002100C	PB2 peripheral reset register	0x00000000
R32_RCC_APB1PRSTR	0x40021010	PB1 peripheral reset register	0x00000000
R32_RCC_AHBPCENR	0x40021014	HB peripheral clock enable register	0x00000004
R32_RCC_APB2PCENR	0x40021018	PB2 peripheral clock enable register	0x00000000
R32_RCC_APB1PCENR	0x4002101C	PB1 peripheral clock enable register	0x00000000
R32_RCC_RSTSCKR	0x40021024	Control/status register	0x0C000000

3.4.1 Clock Control Register (RCC_CTLR)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						PLL RDY	PLL ON	Reserved				CSSO N	HSE BYP	HSE RDY	HSE ON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSICAL[7:0]								HSITRIM[4:0]					Reser ved	HSI RDY	HSIO N

Bit	Name	Access	Description	Reset value
[31:26]	Reserved	RO	Reserved	0
25	PLLRDY	RO	PLL clock-ready lock flag bit. 1: PLL clock lock. 0: PLL clock is not locked.	0
24	PLLON	RW	PLL clock enable control bit.	0

			1: Enables the PLL clock. 0: Turn off the PLL clock. *Note: After entering Standby low-power mode, this bit is cleared by hardware to 0.*	
[23:20]	Reserved	RO	Reserved	0
19	CSSON	RW	Clock security system enable control bit. 1: Enable the clock security system. When HSE is ready (HSERDY set to 1), the hardware turns on the clock monitoring function of HSE and triggers CSSF flag and NMI interrupt when HSE is found to be abnormal; when HSE is not ready, the hardware turns off the clock monitoring function of HSE. 0: Turns off the clock security system.	0
18	HSEBYP	RW	External high-speed crystal bypass control bit. 1: Bypass external high-speed crystal/ceramic resonators (using an external clock source). 0: No bypass of high-speed external crystal/ceramic resonators. *Note: This bit needs to be written with HSEON at 0.*	0
17	HSERDY	RO	External high-speed crystal oscillation stabilization ready flag bit (set by hardware). 1: Stable external high-speed crystal oscillation. 0: External high-speed crystal oscillation is not stabilized. *Note: After the HSEON bit is cleared to 0, it takes 6 HSE cycles for this bit to clear to 0.*	0
16	HSEON	RW	External high-speed crystal oscillation enable control bit. 1: Enables the HSE oscillator. 0: Turn off the HSE oscillator. *Note: This bit is cleared to 0 by hardware after entering Standby low-power mode.*	0
[15:8]	HSICAL	RO	Internal high-speed clock calibration values, which are automatically initialized at system startup.	xxh
[7:3]	HSITRIM	RW	Internal high-speed clock adjustment value. The user can enter an adjustment value to superimpose on the HSICAL[7:0] value to adjust the frequency of the internal HSI RC oscillator based on voltage and temperature variations. The default value is 16, which can adjust the HSI to 24MHz ±1%; the change of HSICAL is adjusted about 60KHz per step.	10000
2	Reserved	RO	Reserved	0
1	HSIRDY	RO	Internal high-speed clock (24MHz) Stable Ready flag bit (set by hardware). 1: The internal high-speed clock (24MHz) is stable; 0: The internal high-speed clock (24MHz) is not stable. *Note: After the HSION bit is cleared to 0, it takes 6 HSI cycles for the bit to be cleared to 0.*	1
0	HSION	RW	Internal high-speed clock (24MHz) enable control bit. 1: Enable the HSI oscillator. 0: Disable the HSI oscillator. *Note: This bit is set to 1 by hardware to start the internal 24MHz RC oscillator when returning from standby mode or when the external oscillator HSE used as the system clock fails.*	1

3.4.2 Clock Configuration Register0 (RCC_CFGR0)

Offset address: 0x04

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16

Reserved	MCO[2:0]	Reserved	PLL SRC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCPRE[4:0]					Reserved			HPRE[3:0]				SWS[1:0]		SW[1:0]	

Bit	Name	Access	Description	Reset value
[31:27]	Reserved	RO	Reserved	0
[26:24]	MCO[2:0]	RW	Microcontroller MCO pin clock output control. 0xx: no clock output. 100: System clock (SYSCLK) output. 101: Internal 24 MHz RC oscillator clock (HSI) output. 110: External oscillator clock (HSE) output. 111: PLL clock output.	0
[23:17]	Reserved	RO	Reserved	0
16	PLLSRC	RW	Input clock source for PLL (write only when PLL is off). 1: HSE is fed into PLL without dividing the frequency. 0: HSI is not divided and sent to PLL.	0
[15:11]	ADCPRE[4:0]	RW	ADC clock source prescaler control {13:11,15:14}. 000xx: HBCLK divided by 2 as ADC clock. 010xx: HBCLK divided by 4 as ADC clock. 100xx: HBCLK divided by 6 as ADC clock. 110xx: HBCLK divided by 8 as ADC clock. 00100: HBCLK divided by 4 as ADC clock. 01100: HBCLK divided by 8 as ADC clock. 10100: HBCLK divided by 12 as ADC clock. 11100: HBCLK divided by 16 as ADC clock. 00101: HBCLK divided by 8 as ADC clock. 01101: HBCLK divided by 16 as ADC clock. 10101: HBCLK divided by 24 as ADC clock. 11101: HBCLK divided by 32 as ADC clock. 00110: HBCLK divided by 16 as ADC clock. 01110: HBCLK divided by 32 as ADC clock. 10110: HBCLK divided by 48 as ADC clock. 11110: HBCLK divided by 64 as ADC clock. 00111: HBCLK divided by 32 as ADC clock. 01111: HBCLK divided by 64 as ADC clock. 10111: HBCLK divided by 96 as ADC clock. 11111: HBCLK divided by 128 as ADC clock. *Note: The ADC clock should not exceed a maximum of 24MHz.*	0
[10:8]	Reserved	RW	Reserved	0
[7:4]	HPRE[3:0]	RW	HB clock source prescaler control. 0000: Prescaler off. 0001: SYSCLK divided by 2. 0010: SYSCLK divided by 3. 0011: SYSCLK divided by 4. 0100: SYSCLK divided by 5. 0101: SYSCLK divided by 6. 0110: SYSCLK divided by 7. 0111: SYSCLK divided by 8. 1000: SYSCLK divided by 2. 1001: SYSCLK divided by 4. 1010: SYSCLK divided by 8. 1011: SYSCLK divided by 16. 1100: SYSCLK divided by 32.	0010

			1101: SYSCLK divided by 64. 1110: SYSCLK divided by 128. 1111: SYSCLK divided by 256. *Note: When the prescaler factor of the HB clock source is greater than 1, the prefetch buffer must be turned on.*	
[3:2]	SWS[1:0]	RO	System clock (SYSCLK) status (hardware set). 00: the system clock source is HSI. 01: The system clock source is HSE. 10: The system clock source is a PLL. 11: Not available.	0
[1:0]	SW[1:0]	RW	Select the system clock source. 00: HSI as system clock. 01: HSE as system clock. 10: PLL output as system clock. 11: Not available. *Note: With Clock Safe enabled (CSSON=1), HSI is forced by hardware to be selected as the system clock when returning from Standby and Stop mode or when the external oscillator HSE used as the system clock fails.*	0

3.4.3 Clock Interrupt Register (RCC_INTR)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								CSSC	Reserved		PLLRDYC	HSERDYC	HSIRDYC	Reserved	LSIRDYC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PLLRDYIE	HSERDYIE	HSIRDYIE	Reserved	LSIRDYIE	CSSF	Reserved		PLLRDYF	HSERDYF	HSIRDYF	Reserved	LSIRDYF

Bit	Name	Access	Description	Reset value
[31:24]	Reserved	RO	Reserved	0
23	CSSC	WO	Clear the clock security system interrupt flag bit (CSSF). 1: Clear the CSSF interrupt flag. 0: No action.	0
[22:21]	Reserved	RO	Reserved	0
20	PLLRDYC	WO	Clear the PLL-ready interrupt flag bit. 1: Clear the PLLRDYF interrupt flag. 0: No action.	0
19	HSERDYC	WO	Clear the HSE oscillator ready interrupt flag bit. 1: Clear the HSERDYF interrupt flag. 0: No action.	0
18	HSIRDYC	WO	Clear the HSI oscillator ready interrupt flag bit. 1: Clear the HSIRDYF interrupt flag. 0: No action.	0
17	Reserved	RO	Reserved	0
16	LSIRDYC	WO	Clear the LSI oscillator ready interrupt flag bit. 1: Clear the LSIRDYF interrupt flag. 0: No action.	0
[15:13]	Reserved	RO	Reserved	0
12	PLLRDYIE	RW	PLL-ready interrupt enable bit. 1: Enable the PLL-ready interrupt. 0: Disable the PLL-ready interrupt.	0
11	HSERDYIE	RW	HSE-ready interrupt enable bit.	0

			1: Enable HSE-ready interrupt. 0: Disable HSE-ready interrupt.	
10	HSIRDYIE	RW	HSI-ready interrupt enable bit. 1: Enable HSI-ready interrupt. 0: Disable HSI-ready interrupt.	0
9	Reserved	RO	Reserved	0
8	LSIRDYIE	RW	LSI-ready interrupt enable bit. 1: Enable LSI-ready interrupt. 0: Disable LSI-ready interrupt.	0
7	CSSF	RO	Clock security system interrupt flag bit. 1: HSE clock failure, which generates a clock safety interrupt CSSI. 0: No clock security system interrupt. Hardware set, software write CSSC bit 1 cleared.	0
[6:5]	Reserved	RO	Reserved	0
4	PLLRDYF	RO	PLL clock-ready lockout interrupt flag. 1: PLL clock lock generating interrupt. 0: No PLL clock lock interrupt. Hardware set, software write PLLRDYC bit 1 cleared.	0
3	HSERDYF	RO	HSE clock-ready interrupt flag. 1: HSE clock-ready interrupt generation. 0: No HSE clock-ready interrupt. Hardware set, software write HSERDYC bit 1 cleared.	0
2	HSIRDYF	RO	HSI clock-ready interrupt flag. 1: HSI clock-ready interrupt generation. 0: No HSI clock-ready interrupt. Hardware set, software write HSIRDYC bit 1 cleared.	0
1	Reserved	RO	Reserved	0
0	LSIRDYF	RO	LSI clock-ready interrupt flag. 1: LSI clock-ready interrupt generation. 0: No LSI clock-ready interrupt. Hardware set, software write LSIRDYC bit 1 cleared.	0

3.4.4 PB2 Peripheral Reset Register (RCC_APB2PRSTR)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	USART1 RST	Reserved	SPI1 RST	TIM1 RST	Reserved	ADC1 RST	Reserved			IOPD RST	IOPC RST	Reserved	IOPA RST	Reserved	AFIO RST

Bit	Name	Access	Description	Reset value
[31:15]	Reserved	RO	Reserved	0
14	USART1RST	RW	USART1 interface reset control. 1: Reset module; 0: No effect.	0
13	Reserved	RO	Reserved	0
12	SPI1RST	RW	SPI1 interface reset control. 1: Reset module; 0: No effect.	0
11	TIM1RST	RW	TIM1 module reset control. 1: Reset module; 0: No effect.	0
10	Reserved	RO	Reserved	0
9	ADC1RST	RW	ADC1 module reset control. 1: Reset module; 0: No effect.	0
[8:6]	Reserved	RO	Reserved	0

5	IOPDRST	RW	PD port module reset control for I/O. 1: Reset module; 0: No effect.	0
4	IOPCRST	RW	PC port module reset control for I/O. 1: Reset module; 0: No effect.	0
3	Reserved	RO	Reserved	0
2	IOPARST	RW	PA port module reset control for I/O. 1: Reset module; 0: No effect.	0
1	Reserved	RO	Reserved	0
0	AFIORST	RW	I/O auxiliary function module reset control. 1: Reset module; 0: No effect.	0

3.4.5 PB1 Peripheral Reset Register (RCC_APB1PRSTR)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			PWR RST	Reserved						I2C1 RST	Reserved				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WW DG RST	Reserved										TIM 2 RST

Bit	Name	Access	Description	Reset value
[31:29]	Reserved	RO	Reserved	0
28	PWRRST	RW	Power interface module reset control. 1: Reset module; 0: No effect.	0
[27:22]	Reserved	RO	Reserved	0
21	I2C1RST	RW	I2C 1 interface reset control. 1: Reset module; 0: No effect.	0
[20:12]	Reserved	RO	Reserved	0
11	WWDGRST	RW	Window watchdog reset control. 1: Reset module; 0: No effect.	0
[10:1]	Reserved	RO	Reserved	0
0	TIM2RST	RW	Timer 2 module reset control. 1: Reset module; 0: No effect.	0

3.4.6 HB Peripheral Clock Enable Register (RCC_AHBPCENR)

Offset address: 0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													SRA MEN	Reser ved	DMA 1EN

Bit	Name	Access	Description	Reset value
[31:3]	Reserved	RO	Reserved	0
2	SRAMEN	RW	SRAM interface module clock enable bit. 1: SRAM interface module clock on during Sleep mode. 0: The SRAM interface module clock is turned off in Sleep mode.	1
1	Reserved	RO	Reserved	0
0	DMA1EN	RW	DMA1 module clock enable bit.	0

			1: Module clock is on; 0: Module clock is off.	

3.4.7 PB2 Peripheral Clock Enable Register (RCC_APB2PCENR)

Offset address: 0x18

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	USART1 EN	Reserved	SPI1 EN	TIM1 EN	Reserved	ADC1 EN	Reserved			IOPD EN	IOPC EN	Reserved	IOPA EN	Reserved	AFIO EN

Bit	Name	Access	Description	Reset value
[31:15]	Reserved	RO	Reserved	0
14	USART1EN	RW	USART1 interface clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
13	Reserved	RO	Reserved	0
12	SPI1EN	RW	SPI1 interface clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
11	TIM1EN	RW	TIM1 module clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
10	Reserved	RO	Reserved	0
9	ADC1EN	RW	ADC1 module clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
[8:6]	Reserved	RO	Reserved	0
5	IOPDEN	RW	PD port module clock enable bit for I/O. 1: Module clock is on; 0: Module clock is off.	0
4	IOPCEN	RW	PC port module clock enable bit for I/O. 1: Module clock is on; 0: Module clock is off.	0
3	Reserved	RO	Reserved	0
2	IOPAEN	RW	PA port module clock enable bit for I/O. 1: Module clock is on; 0: Module clock is off.	0
1	Reserved	RO	Reserved	0
0	AFIOEN	RW	I/O auxiliary function module clock enable bit. 1: Module clock is on; 0: Module clock is off.	0

3.4.8 PB1 Peripheral Clock Enable Register (RCC_APB1PCENR)

Offset address: 0x1C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			PWREN	Reserved						I2C1 EN	Reserved				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				WWDG EN	Reserved										TIM2 EN

Bit	Name	Access	Description	Reset value
[31:29]	Reserved	RO	Reserved	0
28	PWREN	RW	Power interface module clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
[27:22]	Reserved	RO	Reserved	0
21	I2C1EN	RW	I2C 1 interface clock enable bit.	0

			1: Module clock is on; 0: Module clock is off.	
[20:12]	Reserved	RO	Reserved	0
11	WWDGEN	RW	Window watchdog clock enable bit. 1: Module clock is on; 0: Module clock is off.	0
[10:1]	Reserved	RO	Reserved	0
0	TIM2EN	RW	Timer 2 module clock enable bit. 1: Module clock is on; 0: Module clock is off.	0

3.4.9 Control/Status Register (RCC_RSTSCKR)

Offset address: 0x24

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPWR RSTF	WWDG RSTF	IWDG RSTF	SFT RSTF	POR RSTF	PIN RSTF	Reserved	RMVF	Reserved							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LSIRDY	LSION

Bit	Name	Access	Description	Reset value
31	LPWRRSTF	RO	Low-power reset flag. 1: Occurrence of low-power resets. 0: No low-power reset occurs. Set to 1 by hardware when a low-power management reset occurs; cleared by software writing of the RMVF bit.	0
30	WWDGRSTF	RO	Window watchdog reset flag. 1: Occurrence of a window watchdog reset. 0: No window watchdog reset occurs. Set to 1 by hardware when a window watchdog reset occurs; cleared by software writing of the RMVF bit.	0
29	IWDGRSTF	RO	Independent watchdog reset flag. 1: Occurrence of an independent watchdog reset. 0: No independent watchdog reset occurs. Set to 1 by hardware when an independent watchdog reset occurs; cleared by software writing of the RMVF bit.	0
28	SFTRSTF	RO	Software reset flag. 1: Software reset occurs. 0: No software reset occurs. Set to 1 by hardware when a software reset occurs; software write RMVF bit cleared.	0
27	PORRSTF	RO	Power-up/power-down reset flag. 1: Power-up/power-down reset occurs. 0: No power-up/power-down reset occurs. Set to 1 by hardware when power-up/power-down reset occurs; cleared by software writing of RMVF bit.	1
26	PINRSTF	RO	External manual reset (NRST pin) flag. 1: Occurrence of NRST pin reset. 0: No NRST pin reset occurs. Set to 1 by hardware when NRST pin reset occurs; cleared by software writing of RMVF bit.	0
25	Reserved	RO	Reserved	0
24	RMVF	RW	Clear reset flag control. 1: Clear the reset flag. 0: No effect.	0
[23:2]	Reserved	RO	Reserved。	0
1	LSIRDY	RO	Internal Low Speed Clock (LSI) Stable Ready flag bit (set	0

			by hardware). 1: Stable internal low-speed clock (128KHz). 0: The internal low-speed clock (128KHz) is not stable. *Note: After the LSION bit is cleared to 0, the bit requires 3 LSI cycles to clear 0.*	
0	LSION	RW	Internal low-speed clock (LSI) enable control bit. 1: Enable the LSI (128KHz) oscillator. 0: Disable the LSI (128KHz) oscillator.	0

Note: The Write Clear Reset flag can be cleared except for BIT1 which is cleared by a power-on reset.