Chapter 16 Flash Memory and User Option Bytes

16.1 Flash Memory Organization

The internal flash memory of the chip is organized as follows.

Table 16-1 Flash Memory Organization

Block	Name	Address Range	Size(byte)
Main memory	Page 0	0x0800 0000 – 0x0800 003F	64
	Page 1	0x0800 0040 – 0x0800 007F	64
	Page 2	0x0800 0080 – 0x0800 00BF	64
	Page 3	0x0800 00C0 – 0x0800 00FF	64
	…	…	…
	Page 256	0x0800 3FC0 – 0x0800 3FFF	64
Information block	Launcher code	0x1FFF F000 – 0x1FFF F77F	2K-128
	User option bytes	0x1FFF F800 – 0x1FFF F83F	64

Notes: The above main memory area is used for user's application storage and is write-protected in 1K byte (16 pages) units; except for the "vendor configuration word" area which is factory locked and inaccessible to the user, the other areas are user-operable under certain conditions.

16.2 Flash Memory Programming and Security

16.2.1 Two Programming/Erasing Methods

- Standard programming: This mode is the default programming mode (compatible mode). In this mode, the CPU performs programming in single 2-byte mode and performs erase and whole erase operation in single 1K byte.
- Fast programming: This method uses page operation (recommended). After a specific sequence of unlocking, it performs a single 64-byte programming and 64-byte erasing, 1K-byte erasing (standard 1K whole chip erasing is also applicable to fast programming).

16.2.2 Security - Prevent Illegal Access (read, write, erase)

- Page write protection
- Read protection

When the chip is in the read-protected state.

1) Main memory pages 0-32 (2K bytes) are automatically write-protected state, not controlled by FLASH_WPR register; unread-protected state, all main memory pages are controlled by FLASH_WPR register.
2) The system boot code area, SDI mode, and RAM area are not erasable or programmable for main memory, except for whole chip erasure. User-option bytes areas can be erased or programmed. If an attempt is made to unprotect the read (program the user word), the chip will automatically erase the entire user area.

Note: The internal RC oscillator (HSI) must be turned on when performing a program/erase operation of the flash memory.

16.3 Register Description

Table 16-2 FLASH-related registers list

Name	Access address	Description	Reset value
R32_FLASH_ACTLR	0x40022000	Control register	0x00000000

R32_FLASH_KEYR	0x40022004	FPEC key register	X
R32_FLASH_OBKEYR	0x40022008	OBKEY register	X
R32_FLASH_STATR	0x4002200C	Status register	0x00008000
R32_FLASH_CTLR	0x40022010	Configuration register	0x00008080
R32_FLASH_ADDR	0x40022014	Address register	X
R32_FLASH_OBR	0x4002201C	Option byte register	0x0XXXXXXX
R32_FLASH_WPR	0x40022020	Write protection register	0xFFFFFFF
R32_FLASH_MODEKEYR	0x40022024	Extended key register	X
R32_FLASH_BOOT_MODEKEYR	0x40022028	Unlock BOOT key register	X

16.3.1 Control Register (FLASH_ACTLR)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														LATENCY	

Bit	Name	Access	Description	Reset value
[31:2]	Reserved	RO	Reserved	0
[1:0]	LATENCY[1:0]	RW	Number of FLASH wait states 00:0 wait (recommended 0=<SYSCLK=<24MHz) 01:1 wait (recommended 24=<SYSCLK=<48MHz) Other: Invalid	0

16.3.2 FPEC Key Register (FLASH_KEYR)

Offset address: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
KEYR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KEYR[15:0]															

Bit	Name	Access	Description	Reset value
[31:0]	KEYR[31:0]	WO	FPEC keys for entering FPEC unlocking keys include. RDPRT key = 0x000000A5. KEY1 = 0x45670123. KEY2 = 0xCDEF89AB.	X

16.3.3 OBKEY Register (FLASH_OBKEYR)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OBKEYR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OBKEYR[15:0]															

Bit	Name	Access	Description	Reset value
[31:0]	OBKEYR[31:0]	WO	Option bytes key for entering the option bytes key to release OPTWRE.	X

16.3.4 Status Register (FLASH_STATR)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCK	MODE	Reserved								EOP	WRPRT ERR	Reserved			BSY

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
15	LOCK	RW	BOOT Lock 1: Locked, cannot perform a write operation to the FLASH_STATA[14] field. 0: Unlocked, can perform write operation to FLASH_STATR[14] field. *Note: Write 1 is set, write 0 is invalid.*	1
14	MODE	RW	Control the switch between user area and BOOT area 1：After software reset, you can switch to the BOOT area. 0: After software reset, you can switch to the user area.	0
[13:6]	Reserved	RO	Reserved	0
5	EOP	RW1	Indicates the end of the operation, and write 1 clears 0. The hardware is set each time it is successfully erased or programmed.	0
4	WRPRTERR	RW1	Indicates a write protection error, write 1 clear. The hardware will set the address if it is programmed for write protection.	0
[3:1]	Reserved	RO	Reserved	0
0	BUSY	RO	Indicates busy status. 1: Indicates that a flash operation is in progress. 0: End of operation.	0

Note: When performing the programming operation, you need to make sure the STRT bit of FLASH_CTLR register is 0.

16.3.5 Configuration Register (FLASH_ CTLR)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												BUF RST	BUF LOAD	FTER	FTPG

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLOCK	Reserved		EOPIE	Reserved	ERRIE	OBWRE	Reserved	LOCK	STRT	OBER	OBPG	Reserved	MER	PER	PG

Bit	Name	Access	Description	Reset value
[31:20]	Reserved	RO	Reserved	0
19	BUFRST	RW	BUF reset operation	0
18	BUFLOAD	RW	Cache data into BUF	0
17	FTER	RW	Performs a fast page (64Byte) erase operation.	0
16	FTPG	RW	Performs quick page programming operations.	0
15	FLOCK	RW1	Fast programming lock. Write '1' only. When this bit is '1' it indicates that fast programming/erase mode is not available. Hardware clears this bit to '0' after the correct unlock sequence is detected. The software is set to 1 and re-locked.	1
[14:13]	Reserved	RO	Reserved	0
12	EOPIE	RW	Operation completion interrupt control (EOP set in FLASH_STATR register). 1: Allow generation of interrupts. 0: Interrupt generation is disabled.	0
11	Reserved	RO	Reserved	0
10	ERRIE	RW	Error status interrupt control (PGERR/WRPRTERR set in FLASH_STATR register). 1: Allow generation of interrupts. 0: Interrupt generation is disabled.	0
9	OBWRE	RW0	User selects word lock, software clears 0. 1: Indicates that the user option bytes can be programmed for operation. It needs to be set by hardware after writing the correct sequence in FLASH_OBKEYR register. 0: Re-lock the user selection word after the software is cleared.	0
8	Reserved	RO	Reserved	0
7	LOCK	RW1	Lock. Only '1' can be written. When this bit is '1' it means that FPEC and FLASH_CTLR are locked and unwritable. Hardware clears this bit to '0' after the correct unlock sequence is detected. After an unsuccessful unlock operation, the bit will not be changed again until the next system reset.	1
6	STRT	RW1	Start. Set 1 to start an erase action and the hardware automatically clears 0 (BSY becomes '0').	0
5	OBER	RW	Perform user-option bytes erasure	0
4	OBPG	RW	Perform user-option bytes programming	0
3	Reserved	RO	Reserved	0
2	MER	RW	Performs a full-erase operation (erases the entire user area).	0
1	PER	RW	Perform sector erase (1K)	0
0	PG	RW	Performs standard programming operations.	0

16.3.6 Address Register (FLASH_ ADDR)

Offset address: 0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FAR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAR[15:0]															

Bit	Name	Access	Description	Reset value
[31:0]	FAR[31:0]	WO	The flash memory address, when programming, is the programmed address, and when erasing, is the start address of the erase. When the BSY bit in FLASH_SR register is '1', this register cannot be written.	0

16.3.7 Option Byte Register (FLASH_OBR)

Offset address: 0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved						DATA1								DATA0	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA0						2'b11		STATR_MODE	RST_MODE		STANDY RST	Reserved	IWDG SW	RDPRT	OBERR

Bit	Name		Access	Description	Reset value
[31:26]	Reserved		RO	Reserved	0
[25:18]	DATA1[7:0]		RO	Data byte 1	X
[17:10]	DATA0[7:0]		RO	Data byte 0	X
[9:8]			RO	2'b11	11b
7	USER	STATR_MODE	RO	Power-on startup mode 1: Boot from BOOT area 0: Boot from user area *Note: This function is not applicable to products whose lot number has 0 in the penultimate 5 digits.*	1
[6:5]		RST_MODE	RO	Configuration word reset delay time	X
4		STANDY_RST	RO	System reset control in Standby mode.	X
3		Reserved	RO	Reserved	X
2		IWDG_SW	RO	Independent Watchdog (IWDG) hardware enable bit.	1
1	RDPRT		RO	Read protection status. 1: Indicates that the flash memory is currently read protected.	1
0	OBERR		RO	Wrong choice of words. 1: Indicates that the selection word and its inverse code do not match.	0

Note: USER and RDPRT are loaded from the user-option bytes area after a system reset.

16.3.8 Write Protect Register (FLASH_WPR)

Offset address: 0x20

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPR[15:0]															

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	X
[15:0]	WPR[15:0]	RO	Flash memory write protect state.	X

			1: Write protection failure. 0: Write protection is valid. Each bit represents 1K bytes (16 pages) of storage write protection status.	

Note: WPR is loaded from the user-option bytes area after a system reset.

16.3.9 Extended Key Register (FLASH_MODEKEYR)

Offset address: 0x24

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODEKEYR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODEKEYR[15:0]															

Bit	Name	Access	Description	Reset value
[31:0]	MODEKEYR [31:0]	WO	Enter the following sequence to unlock the fast programming/erase mode. KEY1 = 0x45670123. KEY2 = 0xCDEF89AB.	X

16.3.10 BOOT Key Register (FLASH_BOOT_MODEKEYP)

Offset address: 0x28

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODEKEYR[31:16]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODEKEYR[15:0]															

Bit	Name	Access	Description	Reset value
[31:0]	MODEKEYR [31:0]	WO	Enter the following sequence to unlock the BOOT area KEY1 = 0x45670123. KEY2 = 0xCDEF89AB.	X

16.4 Flash Memory Operation Flow

16.4.1 Read Operations

With direct addressing in the general address space, any read operation of 8/16/32-bit data can access the contents of the flash module and get the corresponding data.

16.4.2 Unlocking the Flash Memory

After a system reset, the flash controller (FPEC) and FLASH_CTLR registers are locked and inaccessible. The flash controller module can be unlocked by writing a sequence to the FLASH_KEYR register.

Unlock sequence.

1) Write KEY1 = 0x45670123 to the FLASH_KEYR register (step 1 must be KEY1).
2) Write KEY2 = 0xCDEF89AB to FLASH_KEYR register (step 2 must be KEY2).

The above operations must be executed sequentially and consecutively, otherwise they are error operations and will lock the FPEC module and FLASH_CTLR registers and generate bus errors until the next system reset.

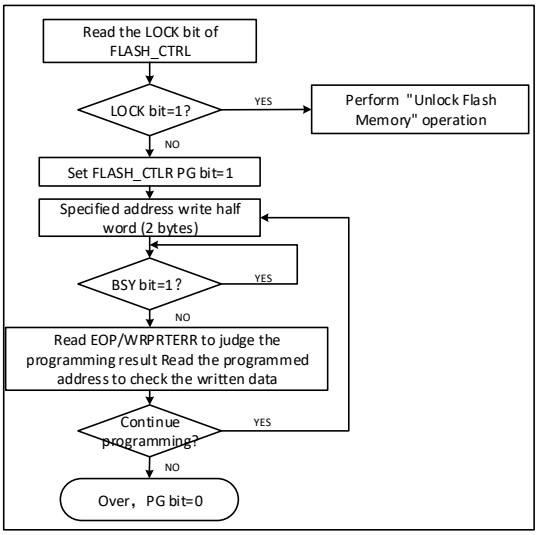
The flash memory controller (FPEC) and FLASH_CTLR registers can be locked again by setting the "LOCK" bit of the FLASH_CTLR register to 1.

16.4.3 Main Memory Standard Programming

Standard programming can be written 2 bytes at a time. When the PG bit of FLASH_CTLR register is '1', each half-word (2 bytes) written to the flash address will initiate programming once, and writing any non-half-word data will cause the FPEC to generate a bus error. During programming, the BSY bit is '1', and at the end of programming, the BSY bit is '0' and the EOP bit is '1'.

Note: When the BSY bit is '1', it will prohibit to perform write operation to any register.

Figure 16-1 FLASH Programming

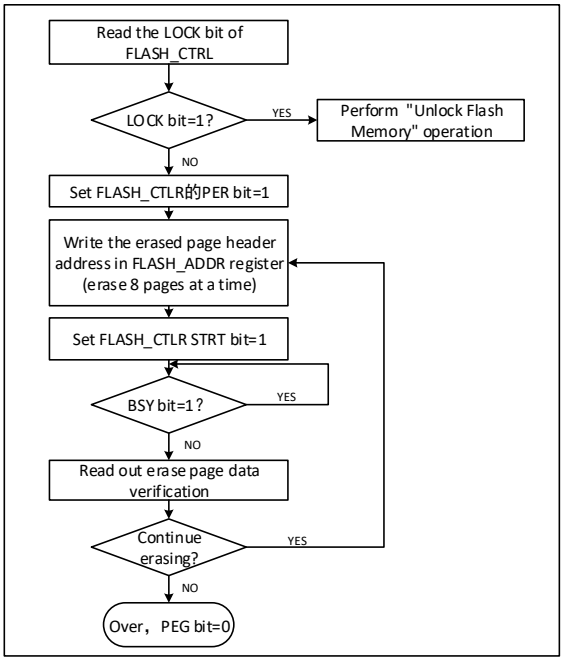


1) Check the FLASH_CTLR register LOCK, if it is 1, you need to execute the "Unlock Flash" operation.
2) Set the PG bit of FLASH_CTLR register to '1' to enable the standard programming mode.
3) Write the half word to be programmed to the specified flash address (even address).
4) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of programming, and clear the EOP bit to 0.
5) Query the FLASH_STATR register to see if there is an error or read the programmed address data checksum.
6) Continue programming you can repeat steps 3-5 and end programming to clear the PG bit to 0.

16.4.4 Main Memory Standard Erase

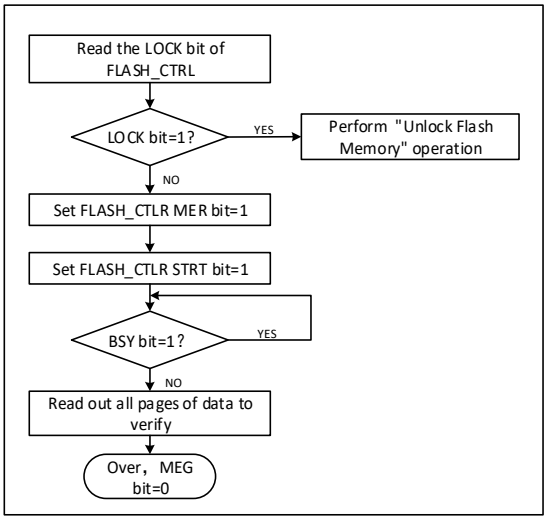
Flash memory can be erased by standard page (1K bytes) or by whole chip.

Figure 16-2 FLASH Page Erase



1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Set the PER bit of FLASH_CTLR register to '1' to enable the standard page erase mode.
3) Write the page header address of the selected erase to FLASH_ADDR register.
4) Set the STRT bit of FLASH_CTLR register to '1' to initiate an erase action.
5) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of erase, and clear the EOP bit to 0.
6) Read the data of the erased page for verification.
7) Continue the standard page erase can repeat steps 3-5 and end the erase to clear the PEG bit to 0.

Figure 16-3 FLASH whole chip erase



1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Set the MER bit of FLASH_CTLR register to '1' to enable the whole chip erase mode.
3) Set the STRT bit of FLASH_CTLR register to '1' to start the erase action.
4) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of erase, and clear the EOP bit to 0.

5) Read the data of the erased page for verification.
6) Clear the MER bit to 0.

16.4.5 Fast Programming Mode Unlocking

Fast programming mode operation can be unlocked by writing a sequence to the FLASH_MODEKEYR register. After unlocking, the FLOCK bit of FLASH_CTLR register will be cleared to 0, indicating that fast erase and programming operations can be performed. The FLASH_CTLR register is locked again by software setting the "FLOCK" bit to 1.

Unlock sequence.

1) Write KEY1 = 0x45670123 to the FLASH_MODEKEYR register.
2) Write KEY2 = 0xCDEF89AB to FLASH_MODEKEYR register.

The above operations must be performed sequentially and consecutively, otherwise they are wrong operations will be locked and cannot be unlocked again until the next system reset.

Note: Quick programming operation requires unlocking the "LOCK" and "FLOCK" layers.

16.4.6 Main Memory Fast Programming

Fast programming by page (64 bytes).

1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Check the BSY bit of the FLASH_STATR register to confirm that there are no other programming operations in progress.
3) Check the FLASH_CTLR register FLOCK bit, if it is 1, you need to execute the "fast programming mode unlock" operation.
4) Set the FTPG bit of FLASH_CTLR register to enable the fast programming mode function.
5) Set the BUFRST bit of FLASH_CTLR register to perform the operation of clearing the internal 64-byte buffer.
6) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of clearing, and clear the EOP bit to 0.
7) Start writing 4 bytes of data to the specified address (4 bytes/operation), then set the BUFLOAD bit of FLASH_CTLR register and execute loading to the buffer.
8) Wait for the BYS bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of loading, and clear the EOP bit to 0.
9) Repeat steps 7-8 a total of 16 times to load all 64 bytes of data into the buffer (16 rounds of operation addresses should be consecutive).
10) Write the first address of the fast programming page to the FLASH_ADDR register.
11) Set the STRT bit of FLASH_CTLR register to '1' to start a fast page programming action.
12) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of programming, and clear the EOP bit to 0.
13) Query FLASH_STATR register to see if there is an error, or read the programmed address data checksum.
14) Continue the Quick Page programming can repeat steps 5-13 and end the programming to clear the FTPG bit to 0.

16.4.7 Main Memory Fast Erase

Fast Erase erases by page (64 bytes).

1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Check the FLASH_CTLR register FLOCK bit, if it is 1, you need to execute the "fast programming mode unlock" operation.
3) Check the BSY bit of the FLASH_STATR register to confirm that there are no other programming operations in progress.

4) Set the FTER bit of FLASH_CTLR register to '1' to enable the fast page erase (64 bytes) mode function.
5) Write the first address of the fast erase page to the FLASH_ADDR register.
6) Set the STRT bit of FLASH_CTLR register to '1' to initiate a fast page erase (64 bytes) action.
7) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of erase, and clear the EOP bit to 0.
8) Query FLASH_STATR register to see if there is an error, or read the erase page address data checksum.
9) Continue fast page erase can repeat steps 5-8, end erase will FTER bit clear 0.

16.5 User Option Bytes

The user-option bytes is solidified in FLASH and will be reloaded into the corresponding register after system reset, and can be erased and programmed by the user at will. The user option bytes information block has a total of 8 bytes (4 bytes for write protection, 1 byte for read protection, 1 byte for configuration options, and 2 bytes for storing user data), and each bit has its inverse code bit for checksum during loading. The following describes the structure and meaning of the option bytes information.

Table 16-3 32-bit option byte format division

[31:24]	[23:16]	[15:8]	[7:0]
Option bytes byte 1 inverse code	Option bytes byte 1	Option bytes byte 0 inverse code	Option bytes byte 0

Table 16-4 User option byte information structure

Address / Bit	[31:24]	[23:16]	[15:8]	[7:0]
0x1FFFF800	nUSER	USER	nRDPR	RDPR
0x1FFFF804	nData1	Data1	nData0	Data0
0x1FFFF808	nWRPR1	WRPR1	nWRPR0	WRPR0
0x1FFFF80C	Reserved	Reserved	Reserved	Reserved

Name/Byte			Description	Reset value
RDPR			Read protection control bit to configure whether the code in the flash memory can be read out. 0xA5: if this byte is 0xA5 (nRDP must be 0x5A), it means that the current code is in a non-read protected state and can be read out. Other values: indicates code read protection status, not readable, pages 0-31 (4K) will be automatically write protected and not controlled by WRPR0.	0x01
USER	[7:6]	Reserved	Reserved (must be 1)	11b
	5	START_MODE	Power-on startup mode 1: Boot from BOOT area 0: Boot from user area *Note: This function is not applicable to products with 0 in the penultimate digit of the lot number.*	1
	[4:3]	RST_MODE	PD7 multiplexed as external pin reset. 00: Ignoring pin states within 128us after turning on the multiplexing function. 01: Ignoring pin states within 1ms after turning on the multiplexing function. 10: Ignoring pin states within 12ms after turning on the multiplexing function. 11: Multiplexing function off, PD7 for I/O function.	10b
	2	STANDYRST	System reset control in Standby mode: 1: Not enabled, does not reset when entering Standby	1

			mode system; 0: Enabled, generates a system reset when entering Standby mode.	
	1	Reserved	Reserved	1
	0	IWDGSW	Independent Watchdog (IWDG) hardware enable configuration. 1: IWDG is enabled by software and disabled from being enabled by hardware. 0: IWDG is turned on by hardware itself (since the clock for IWDG is provided by LSI, it is automatically turned on by LSI). *Note: The core stops in debug mode and the watchdog hardware enable will be disabled.*	1
Data0–Data1			Store 2 bytes of user data.	FFFFh
WRPR0 - WRPR3			Write-protect control bits. Each bit is used to control the write-protect status of 1 sector (1K bytes/sector) in main memory. 1: Disable write protection. 0: Enable Write protection. 2 bytes are used to protect a total of 16K bytes of main memory. WRP0: Sector 0-7 storage write protection control. WRP1: Sector 8-15 storage write protection control. WRP2: Reserved. WRP3: Reserved.	FFFFh

16.5.1 User Option Bytes Unlocking

The user option bytes operation can be unlocked by writing a sequence to the FLASH_OBKEYR register. After unlocking, the OBWRE bit of FLASH_CTLR register will be set to 1, indicating that the user option bytes can be erased and programmed. It can be locked again by clearing the "OBWRE" bit of FLASH_CTLR register to 0 by software.

Unlock sequence.

1) Write KEY1 = 0x45670123 to FLASH_OBKEYR register.
2) Write KEY2 = 0xCDEF89AB to FLASH_OBKEYR register.

Note: User-option bytes operation requires unlocking the "LOCK" and "OBWRE" layers.

16.5.2 User Option Bytes Programming

Only the standard programming method is supported, writing half-words (2 bytes) at a time. In practice, when programming the user-option bytes, FPEC uses only the low byte in the half-word and automatically calculates the high byte (the high byte is the inverse of the low byte) and then starts the programming operation, which will ensure that the byte in the user option bytes and its inverse code are always correct.

1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Check the BSY bit of the FLASH_STATR register to confirm that there are no other programming operations in progress.
3) Set the OBPG bit of FLASH_CTLR register to '1', after that set the STAT bit of FLASH_CTLR register to '1' to turn on the user option bytes programming.
4) Set the OBPG bit of FLASH_CTLR register to '1'.
5) Write the half word (2 bytes) to be programmed to the specified address.
6) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of programming, and clear the EOP bit to 0.
7) Read the programmed address data checksum.
8) Continue programming you can repeat steps 5-7 and end programming to clear the OBPG bit to 0.

Note: When "Read Protected" in the modified selection word becomes "Unprotected", a whole-slice erase of the main memory will be performed automatically. If the selection other than "read protected" is modified, the whole erase operation will not occur.

16.5.3 User Option Bytes Erasure

Directly erase the entire 64-byte user option bytes area.

1) Check the LOCK bit of FLASH_CTLR register, if it is 1, you need to execute the "Unlock Flash" operation.
2) Check the BSY bit of the FLASH_STATR register to confirm that there is no programming operation in progress.
3) Check the OBWRE bit of FLASH_CTLR register, if it is 0, it is necessary to execute the operation of "user option bytes unlock".
4) Set the OBER bit of FLASH_CTLR register to '1', after that set the STAT bit of FLASH_CTLR register to '1' to enable the user option bytes erase.
5) Wait for the BSY bit to become '0' or the EOP bit of FLASH_STATR register to be '1' to indicate the end of erase, and clear the EOP bit to 0
6) Read and erase the address data checksum.
7) End to clear the OBER bit to 0.

16.5.4 Unprotecting Reads

Whether the flash memory is read protected or not is determined by the user option bytes. Read the FLASH_OBR register, when the RDPRT bit is '1' indicates that the flash memory is currently in the read-protected state, and the flash memory is operationally protected by a series of security guards for the read-protected state. The process of unprotecting the read protection is as follows.

1) Erase the entire user-option bytes area, at which point the read protection field RDPR, at which point the read protection remains in effect.
2) User-option bytes programming and writes the correct RDPR code 0xA5 to unprotect the flash memory from reads. (This step will first cause the system to automatically perform an entire erase operation on the flash memory)
3) Perform a power-on reset to reload the selection byte (including the new RDPR code), at which point the read protection is removed.