CH32V002 Datasheet

V1.0

Overview

CH32V002 is an industrial-grade general-purpose microcontroller designed based on QingKe RISC-V core, which supports 48MHz system main frequency, with wide voltage, low-power consumption, 1-wire SDI and other features. Its pins and functions are compatible with CH32V003. CH32V002 has a built-in 12-bit ADC, with a sampling rate of up to 3Msps; it provides rich peripheral resources, such as 7-channel DMA controller, multi-group timer, USART, I2C, SPI and so on.

Features

- **Core**
  - QingKe 32-bit RISC-V core, RV32EmC instruction set
  - Fast programmable interrupt controller + hardware interrupt stack
  - Support 2-level interrupt nesting
  - Support system main frequency 48MHz
- **Memory**
  - 4KB volatile data storage area SRAM
  - 16KB program memory CodeFlash
  - 3328B BootLoader
  - 256B non-volatile system configuration memory
  - 256B user-defined memory
- **Power management and low-power consumption**
  - System power supply V_{DD}: 2~5V
  - Low-power mode: Sleep, Standby
- **Clock & Reset**
  - Built-in factory-trimmed 24MHz RC oscillator
  - Built-in 128KHz RC oscillator
  - High-speed external 3~25MHz oscillator
  - Built-in system clock monitoring (SCM) module
  - Power on/down reset, programmable voltage detector
- **7-channel general-purpose DMA controller**
  - 7 channels, support ring buffer
  - Support TIMx/ADC /USART/I2C/SPI
- **12-bit ADC**
  - Analog input range: V_{SS}~V_{DD}
  - 8 external signals + 3 internal signals
  - Support 3M sampling rate
- **8-channel touch-key channel detection**
- **Multiple timers**
  - 1×16-bit advanced-control timers, with dead zone control and emergency brake; can offer PWM complementary output for motor control
  - 1×16-bit general-purpose timers, provide input capture/output comparison/PWM/pulse counting/incremental encoder input
  - 2 watchdog timers (independent watchdog and window watchdog)
  - SysTick: 32-bit counter
- **1 set of USART**
  - Support LIN, support multiple pin mapping
- **1 I2C interface**
- **1 SPI interface**
- **GPIO port**
  - 3 sets of GPIO ports, 18 I/O ports
  - Mapping 1 external interrupt
- **Security features: Chip unique ID**
- **Debug mode: 1-wire serial debug interface (SDI)**
- **Package: QFN, TSSOP or SOP**