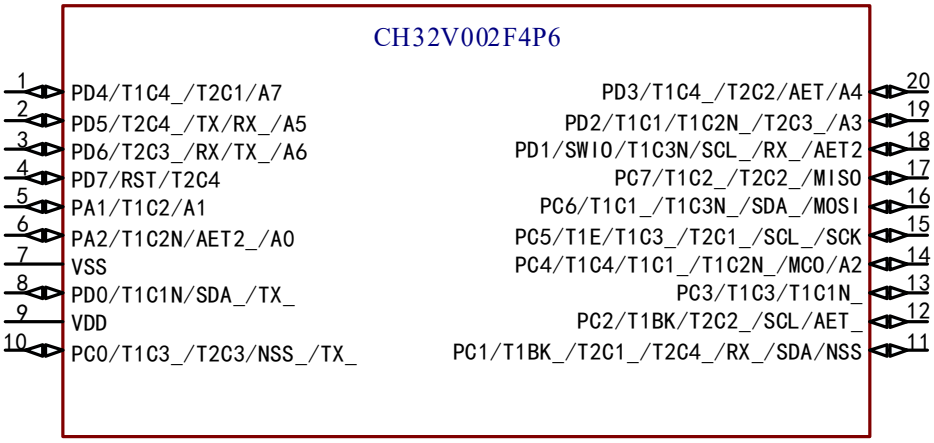
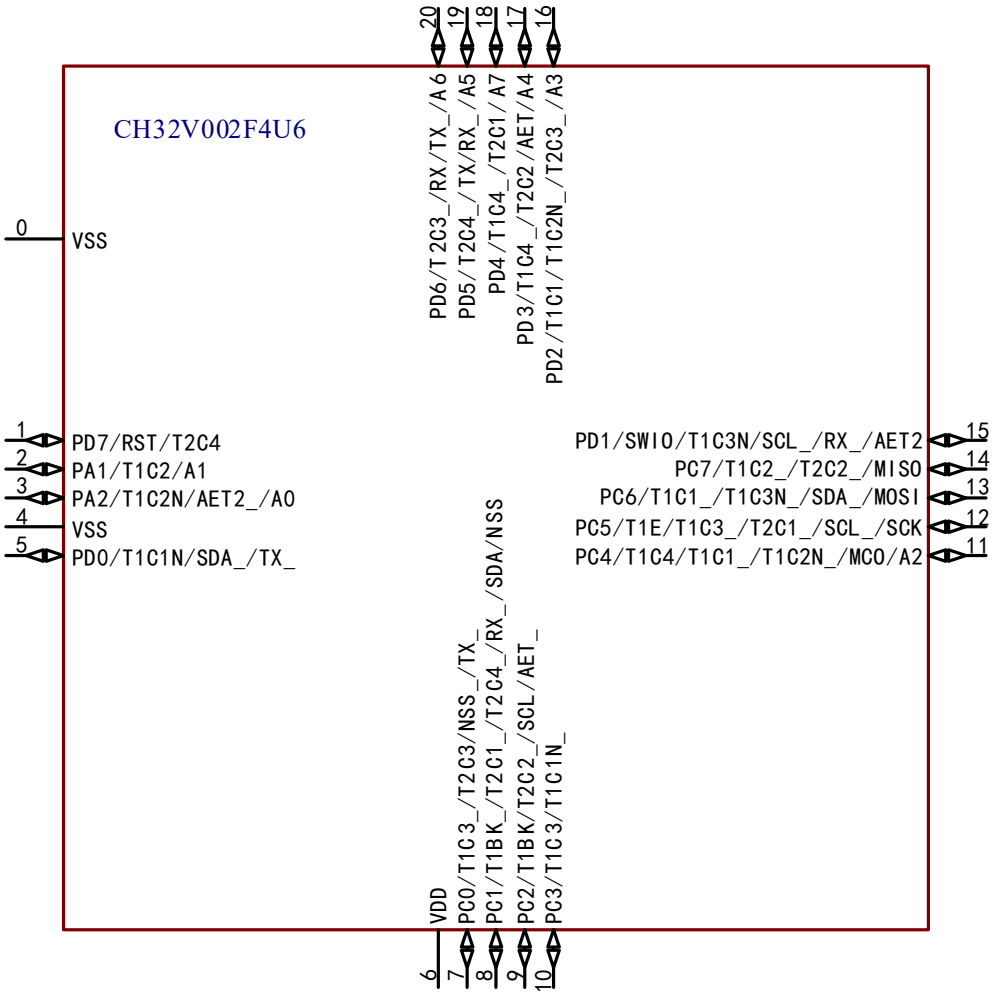
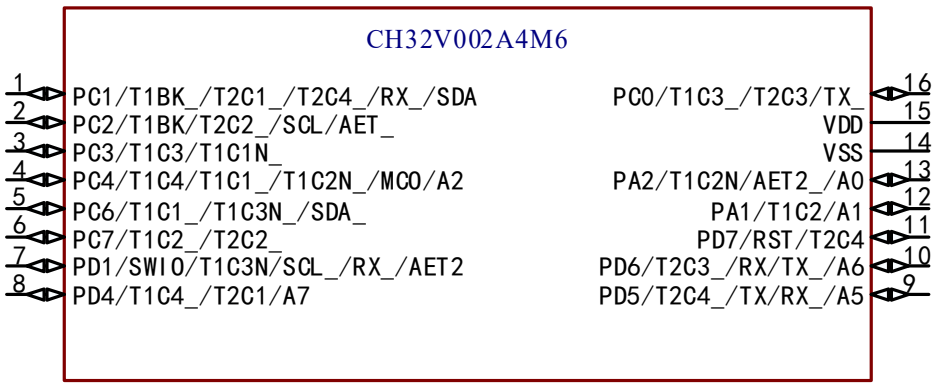
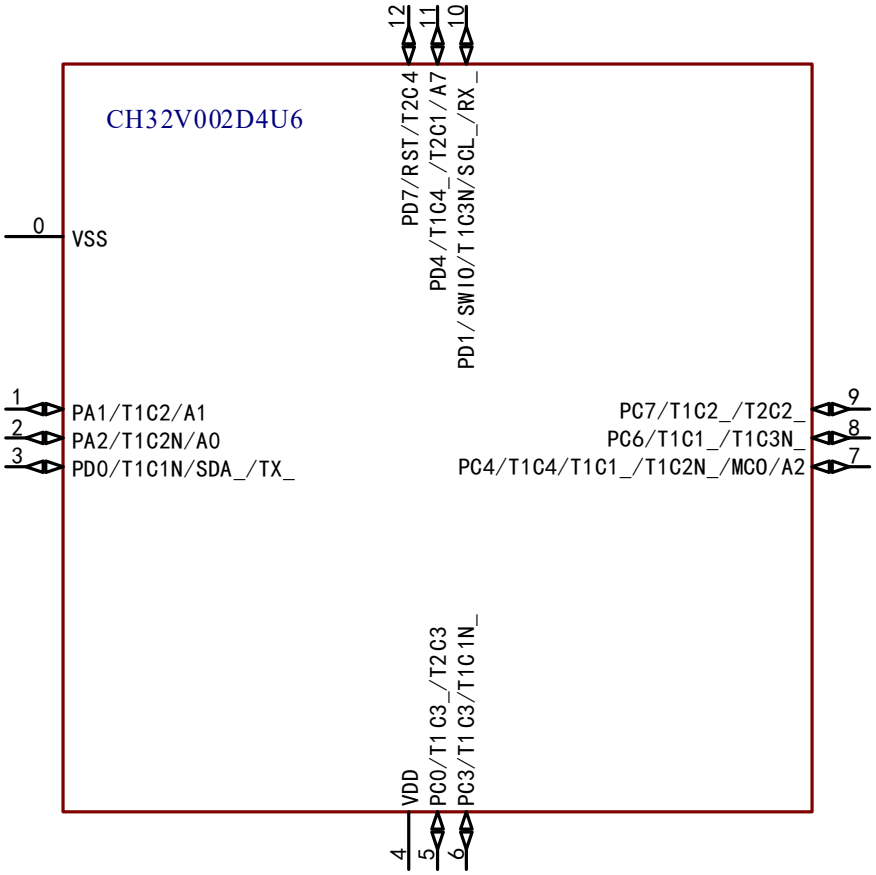
Chapter 2 Pinouts and Pin Definition

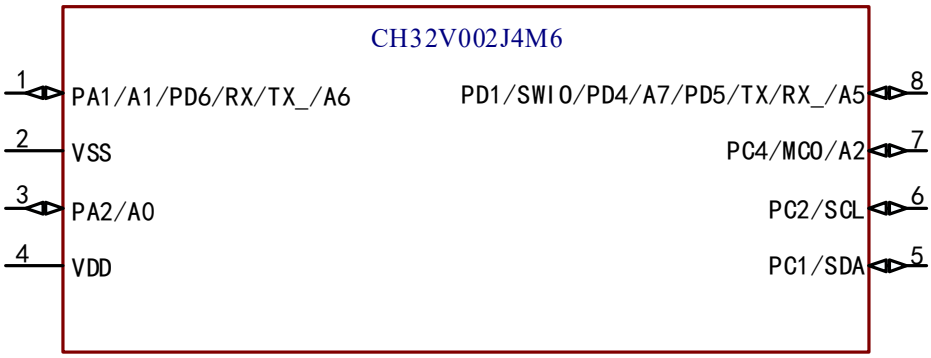
2.1 Pinouts






CH32V002A4M6
1 PC1/T1BK_/T2C1_/T2C4_/RX_/SDA
2 PC2/T1BK/T2C2_/SCL/AET_
3 PC3/T1C3/T1C1N_
4 PC4/T1C4/T1C1_/T1C2N_/MCO/A2
5 PC6/T1C1_/T1C3N_/SDA_
6 PC7/T1C2_/T2C2_
7 PD1/SWIO/T1C3N/SCL_/RX_/AET2
8 PD4/T1C4_/T2C1/A7
16 PC0/T1C3_/T2C3/TX_
15 VDD
14 VSS
13 PA2/T1C2N/AET2_/A0
12 PA1/T1C2/A1
11 PD7/RST/T2C4
10 PD6/T2C3_/RX/TX_/A6
9 PD5/T2C4_/TX/RX_/A5


CH32V002D4U6
12 PD7/RST/T2C4
11 PD4/T1C4_/T2C1/A7
10 PD1/SWIO/T1C3N/SCL_/RX_
0 VSS
1 PA1/T1C2/A1
2 PA2/T1C2N/A0
3 PD0/T1C1N/SDA_/TX_
9 PC7/T1C2_/T2C2_
8 PC6/T1C1_/T1C3N_
7 PC4/T1C4/T1C1_/T1C2N_/MCO/A2
4 VDD
5 PC0/T1C3_/T2C3
6 PC3/T1C3/T1C1N_


CH32V002J4M6
1 PA1/A1/PD6/RX/TX_/A6
2 VSS
3 PA2/A0
4 VDD
8 PD1/SWIO/PD4/A7/PD5/TX/RX_/A5
7 PC4/MCO/A2
6 PC2/SCL
5 PC1/SDA

Note: The multiplexed functions in the pin diagram are abbreviated.

Example: A: ADC_ (A1: ADC_IN1, AET: ADC_RETR, AET2: ADC_IETR)

T1: TIM1_ (T1C1: TIM1_CH1、T1C1N: TIM1_CH1N, T1BK: TIM1_BKIN, T1E: TIM1_ETR)

T2: TIM2_ (T2C1: TIM2_CH1_ETR, T2C2: TIM2_CH2)

USART1_ (RX: USART1_RX, TX: USART1_TX)

I2C_ (SDA: I2C_SDA, SCL: I2C_SCL)

SPI_ (SCK: SPI_SCK, NSS: SPI_NSS, MISO: SPI_MISO, MOSI: SPI_MOSI)

2.2 Pin Description

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-1 CH32V002 Pin definitions

Pin No.					Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
SOP8	QFN12	SOP16	QFN20	TSSOP20					
-	0	-	0	-	V_{SS}	P	V_{SS}		
8	11	8	18	1	PD4(4)	I/O/A	PD4	ADC_IN7/TIM2_CH1_ETR	TIM1_CH4_3/TIM1_ETR_1/ TIM1_ETR_4/TIM1_ETR_5/ TIM1_ETR_6/TIM2_CH2_7/ USART1_RTS_9/SPI_SCK_4
8	-	9	19	2	PD5(4)	I/O/A	PD5	ADC_IN5/USART1_TX	TIM2_CH4_3/USART1_RX_1/ USART1_CTS_9/SPI_MISO_4
1	-	10	20	3	PD6(3)	I/O/A	PD6	ADC_IN6/USART1_RX	TIM2_CH3_3/USART1_TX_1/ SPI_MOSI_4
-	12	11	1	4	PD7	I/O	PD7	TIM2_CH4/RST	TIM2_CH4_1/USART1_CTS_4/ USART1_CTS_5
1	1	12	2	5	PA1(3)	I/O/A	PA1	ADC_IN1/TIM1_CH2	XI/TIM1_CH2_1/TIM1_CH2_9/ TIM2_CH2_5/TIM2_CH2_6/ USART1_RX_8/SPI_SCK_5
3	2	13	3	6	PA2	I/O/A	PA2	ADC_IN0/TIM1_CH2N	X0/TIM1_CH3_9/TIM1_CH2N_1/ TIM1_CH2N_4/TIM1_CH2N_5/ TIM1_CH2N_6/TIM2_CH3_5/ TIM2_CH3_6/TIM2_CH3_7/ SPI_MOSI_5/ADC_IETR_1
2	-	14	4	7	V_{SS}	P	V_{SS}		
-	3	-	5	8	PD0	I/O	PD0	TIM1_CH1N	TIM1_CH1N_1/TIM1_CH3N_4/

Pin No.					Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
SOP8	QFN12	SOP16	QFN20	TSSOP20					
									TIM1_CH3N_5/TIM1_CH3N_6/ USART1_TX_2/I2C_SDA_1
4	4	15	6	9	V_{DD}	P	V_{DD}		
-	5	16	7	10	PC0	I/O	PC0	TIM2_CH3	TIM1_CH3_2/TIM1_CH1N_7/ TIM1_CH1N_9/TIM2_CH1_ETR _4/ TIM2_CH3_1/USART1_TX_3/ SPI_NSS_1/SPI_MOSI_3
5	-	1	8	11	PC1	I/O	PC1	I2C_SDA/SPI_NSS	TIM1_CH2N_7/TIM1_CH2N_9/ TIM1_BKIN_2/TIM1_BKIN_3/ TIM2_CH1_ETR_1/TIM2_CH2_4 / TIM2_CH1_ETR_3/TIM2_CH4_2 / USART1_RX_3/SPI_NSS_5
6	-	2	9	12	PC2	I/O	PC2	TIM1_BKIN/USART1_RTS / I2C_SCL	TIM1_CH3N_7/TIM1_CH3N_9/ TIM2_CH2_2/USART1_RTS_2/ TIM1_BKIN_1/TIM1_ETR_3/ ADC_RETR_1
-	6	3	10	13	PC3	I/O	PC3	TIM1_CH3	TIM1_CH3_1/TIM1_CH3_5/ TIM1_CH1N_2/TIM1_CH1N_3/ TIM2_CH3_4/USART1_CTS_2
7	7	4	11	14	PC4	I/O	PC4	ADC_IN2/TIM1_CH4/MC O	TIM1_CH1_3/TIM1_CH1_7/ TIM1_CH1_8/TIM1_CH4_1/ TIM1_CH2N_2/USART1_RX_9/

Pin No.					Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
SOP8	QFN12	SOP16	QFN20	TSSOP20					
									SPI_NSS_2/SPI_NSS_6/
-	-	-	12	15	PC5	I/O	PC5	TIM1_ETR/SPI_SCK	TIM1_CH2_7/TIM1_CH2_8/ TIM1_CH3_3/TIM1_ETR_2/ TIM2_CH1_ETR_2/USART1_TX _6/ RST_2/I2C_SCL_2/SPI_SCK_1
-	8	5	13	16	PC6	I/O	PC6	SPI_MOSI	TIM1_CH1_2/TIM1_CH3_7/ TIM1_CH3_8/TIM1_CH3N_3/ USART1_RX_6/USART1_CTS_1/ USART1_CTS_3/SPI_MOSI_1/ I2C_SDA_2
-	9	6	14	17	PC7	I/O	PC7	SPI_MISO	TIM1_CH2_2/TIM1_CH2_3/ TIM1_CH4_7/TIM1_CH4_8/ TIM2_CH2_3/USART1_CTS_6/ USART1_CTS_7/USART1_RTS_ 1/ USART1_RTS_3/SPI_MISO_1/ SPI_MISO_6
8	10	7	15	18	PD1(4)	I/O/A	PD1	TIM1_CH3N/SWIO/ ADC_IETR	TIM1_CH4_4/TIM1_CH4_5/ TIM1_CH3N_1/TIM1_CH3N_2/ USART1_TX_4/USART1_RX_2/ USART1_RX_5/I2C_SCL_1/ I2C_SDA_4
-	-	-	16	19	PD2	I/O/A	PD2	ADC_IN3/TIM1_CH1	TIM1_CH1_1/TIM1_CH2N_3/ TIM2_CH3_2/USART1_CTS_8/

Pin No.					Pin name	Pin type(1)	Main function (after reset)	Default alternate function	Remapping function(2)
SOP8	QFN12	SOP16	QFN20	TSSOP20					
									SPI_SCK_2
-	-	-	17	20	PD3	I/O/A	PD3	ADC_IN4/TIM2_CH2/ USART1_CTS/ADC_RETR	TIM1_CH4_2/TIM2_CH1_ETR_7 / TIM2_CH2_1/USART1_RTS_8/ SPI_NSS_4/SPI_MOSI_2

Note 1: Explanation of table abbreviations:

I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output.

A = Analog signal input or output; P = Power supply.

Note 2: The underlined value of the remapping function indicates the configuration value of the corresponding bit in the AFIO register. For example: TIM1_CH4_3 indicates that the corresponding bit configuration of the AFIO register is 011b.

Note 3: For the CH32V002J4M6 chip, the PA1 and PD6 pins are short-connected and sealed inside the chip, which forbids the two I/O to be configured as the output function.

Note 4: For the CH32V002J4M6 chip, the PD1, PD4 and PD5 pins are short connected and sealed inside the chip, and any two or more of the three I/O are prohibited from being configured as output functions.

2.3 Pin Alternate Functions

Note: The pin function descriptions in the table below are for all functions and do not relate to specific model products. Peripheral resources may vary between models, so please check the availability of this function according to the product model resource table before viewing.

Table 2-3 Pin alternate and remapping functions

Alternate / Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI
PA1	ADC_IN1	TIM1_CH2 TIM1_CH2_1 TIM1_CH2_9	TIM2_CH2_5 TIM2_CH2_6	USART1_RX_8	XI		SPI_SCK_5
PA2	ADC_IN0 ADC_IETR_1	TIM1_CH3_9 TIM1_CH2N TIM1_CH2N_1 TIM1_CH2N_4 TIM1_CH2N_5 TIM1_CH2N_6	TIM2_CH3_5 TIM2_CH3_6 TIM2_CH3_7		XO		SPI_MOSI_5
PC0		TIM1_CH3_2 TIM1_CH1N_7 TIM1_CH1N_9	TIM2_CH1_ETR_4 TIM2_CH3 TIM2_CH3_1	USART1_TX_3			SPI_NSS_1 SPI_MOSI_3
PC1		TIM1_CH2N_7 TIM1_CH2N_9 TIM1_BKIN_2 TIM1_BKIN_3	TIM2_CH1_ETR_1 TIM2_CH1_ETR_3 TIM2_CH2_4 TIM2_CH4_2	USART1_RX_3		I2C_SDA	SPI_NSS SPI_NSS_5
PC2	ADC_RETR_1	TIM1_CH3N_7 TIM1_CH3N_9 TIM1_BKIN TIM1_BKIN_1 TIM1_ETR_3	TIM2_CH2_2	USART1_RTS USART1_RTS_2		I2C_SCL	
PC3		TIM1_CH3 TIM1_CH3_1 TIM1_CH3_5 TIM1_CH1N_2 TIM1_CH1N_3	TIM2_CH3_4	USART1_CTS_2			
PC4	ADC_IN2	TIM1_CH1_3 TIM1_CH1_7 TIM1_CH1_8 TIM1_CH4 TIM1_CH4_1 TIM1_CH2N_2		USART1_RX_9	MCO		SPI_NSS_2 SPI_NSS_6
PC5		TIM1_CH2_7	TIM2_CH1_ET	USART1_TX_6	RST_2	I2C_SCL_2	SPI_SCK

Alternate Pin	ADC	TIM1	TIM2	USART	SYS	I2C	SPI
		TIM1_CH2_8 TIM1_CH3_3 TIM1_ETR TIM1_ETR_2	R_2				SPI_SCK_1
PC6		TIM1_CH1_2 TIM1_CH3_7 TIM1_CH3_8 TIM1_CH3N_3		USART1_RX_6 USART1_CTS_1 USART1_CTS_3		I2C_SDA_2	SPI_MOSI SPI_MOSI_1
PC7		TIM1_CH2_2 TIM1_CH2_3 TIM1_CH4_7 TIM1_CH4_8	TIM2_CH2_3	USART1_CTS_6 USART1_CTS_7 USART1_RTS_1 USART1_RTS_3			SPI_MISO SPI_MISO_1 SPI_MISO_6
PD0		TIM1_CH1N TIM1_CH1N_1 TIM1_CH3N_4 TIM1_CH3N_5 TIM1_CH3N_6		USART1_TX_2		I2C_SDA_1	
PD1	ADC_IETR	TIM1_CH4_4 TIM1_CH4_5 TIM1_CH3N TIM1_CH3N_1 TIM1_CH3N_2		USART1_TX_4 USART1_RX_2 USART1_RX_5	SWIO SWDIO	I2C_SCL_1 I2C_SDA_4	
PD2	ADC_IN3	TIM1_CH1 TIM1_CH1_1 TIM1_CH2N_3	TIM2_CH3_2	USART1_CTS_8			SPI_SCK_2
PD3	ADC_IN4 ADC_RETR	TIM1_CH4_2	TIM2_CH1_ETR_7 TIM2_CH2 TIM2_CH2_1	USART1_CTS USART1_RTS_8			SPI_NSS_4 SPI_MOSI_2
PD4	ADC_IN7	TIM1_CH4_3 TIM1_ETR_1 TIM1_ETR_4 TIM1_ETR_5 TIM1_ETR_6	TIM2_CH1_ETR TIM2_CH2_7	USART1_RTS_9			SPI_SCK_4
PD5	ADC_IN5		TIM2_CH4_3	USART1_TX USART1_RX_1 USART1_CTS_9			SPI_MISO_4
PD6	ADC_IN6		TIM2_CH3_3	USART1_TX_1 USART1_RX			SPI_MOSI_4
PD7			TIM2_CH4 TIM2_CH4_1	USART1_CTS_4 USART1_CTS_5	RST		