Chapter 3 Electrical Characteristics

3.1 Test Condition

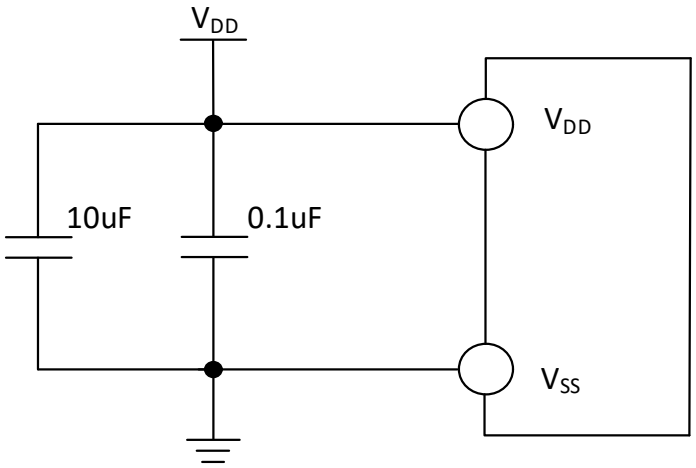
Unless otherwise specified and marked, all voltages are based on V_{SS}.

All minimum and maximum values will be guaranteed under the worst ambient temperature, supply voltage and clock frequency. Typical values are based on room temperature 25℃ and V_{DD}=3.3V or 5V for design guidance.

Data obtained through comprehensive evaluation, design simulation or process characteristics will not be tested on the production line. On the basis of comprehensive evaluation, the minimum and maximum values are obtained through sample testing. Unless the special instructions are measured, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply



3.2 Absolute Maximum Ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	125	℃
V_{DD}-V_{SS}	External main supply voltage (V_{DD})	-0.3	5.5	V
V_{IN}	Input voltage on the I/O pin	V_{SS}-0.3	V_{DD}+0.3	V
$\|\triangle V_{DD\_x}\|$	Variations between different main power supply pins		50	mV
$\|\triangle V_{SS\_x}\|$	Variations between different ground pins		50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (HBM) of ordinary I/O pin	4K		V

I_{VDD}	Total current of all V_{DD} main power pins		100	mA
I_{VSS}	Total current of all V_{SS} common ground pins		200	mA
I_{IO}	Sink current on any I/O and control pin		30	mA
	Output current on any I/O and control pin		-30	
$I_{INJ(PIN)}$	XI pin of HSE		+/-4	
	Injected current on other pins		+/-4	
$\sum I_{INJ(PIN)}$	Total injected current on all I/Os and control pins		+/-20	

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{HCLK} Or F_{SYS}	Internal system bus frequency Or microprocessor main frequency			48	MHz
V_{DD}	Standard operating voltage	ADC feature is not used	1.9	5.5	V
		Use the ADC feature	2.4	5.5	
T_A	Ambient temperature		-40	85	℃
T_J	Junction temperature range		-40	105	℃

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rising rate		0	∞	us/V
	V_{DD} falling rate		20	∞	

3.3.2 Embedded Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(1)	Programmable voltage detector level selection	PLS[1:0] = 00 rising edge		1.86		V
		PLS[1:0] = 00 falling edge		1.85		
		PLS[1:0] = 01 rising edge		2.22		V

		PLS[1:0] = 01 falling edge		2.21		
		PLS[1:0] = 10 rising edge		2.42		V
		PLS[1:0] = 10 falling edge		2.4		
		PLS[1:0] = 11 rising edge		2.64		V
		PLS[1:0] = 11 falling edge		2.59		
$V_{PVDhyst}$	PVD hysteresis		5	20	6	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Rising edge	1.6	1.76	1.96	V
		Falling edge	1.54	1.68	1.9	V
$V_{PDRhyst}$	PDR hysteresis		60	80	100	mV
$t_{RSTTEMPO}$	Power-on reset	RST_MODE[1:0] = 11		2		ms
	Other reset			300		us

Note: 1. Normal temperature test value.

3.3.3 Embedded Reference Voltage

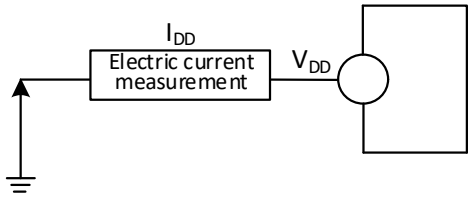
Table 3-5 Embedded reference voltage

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Internal reference voltage	T_A = -40°C~85°C		1.2		V
$T_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling is recommended.	3		240	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, the software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

In the case of room temperature V_{DD} = 3.3V or 5V, during the test: all I/O ports are configured with pull-down input,

HSI = 24MHz (calibrated), and the bit LDO_MODE of register PWR_CTLR is 10. Enable or disable the power consumption of all peripheral clocks.

Table 3-6-1 Typical current consumption in Run mode, data processing code runs from the internal Flash (V_{DD} = 3.3V)

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	Runs on the high-speed external clock (HSE) (HSE_SI = 01, HSE_LP = 1)	X	F_{HCLK} = 48MHz	3.82	3.00	mA
				F_{HCLK} = 24MHz	2.73	2.36	
				F_{HCLK} = 16MHz	2.24	2.03	
				F_{HCLK} = 8MHz	2.00	1.88	
				F_{HCLK} = 750KHz	1.26	1.24	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	3.43	2.58	
				F_{HCLK} = 24MHz	2.35	1.97	
				F_{HCLK} = 16MHz	1.86	1.64	
				F_{HCLK} = 8MHz	1.63	1.51	
				F_{HCLK} = 750KHz	0.89	0.87	
			1	F_{HCLK} = 40KHz	0.55	0.55	

Note: The above are measured parameters.

Table 3-6-2 Typical current consumption in Run mode, data processing code runs from the internal Flash (V_{DD} = 5V)

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Run mode	Runs on the high-speed external clock	X	F_{HCLK} = 48MHz	3.85	3.01	mA
				F_{HCLK} = 24MHz	2.76	2.39	
				F_{HCLK} = 16MHz	2.26	2.05	

		(HSE) (HSE_SI = 01, HSE_LP = 1)		F_{HCLK} = 8MHz	2.02	1.91	
				F_{HCLK} = 750KHz	1.28	1.27	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	3.46	2.59	
				F_{HCLK} = 24MHz	2.38	1.98	
				F_{HCLK} = 16MHz	1.89	1.65	
				F_{HCLK} = 8MHz	1.68	1.52	
				F_{HCLK} = 750KHz	0.90	0.87	
			1	F_{HCLK} = 40KHz	0.56	0.56	

Note: The above are measured parameters.

Table 3-7-1 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (V_{DD} = 3.3V)

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed external clock (HSE) (HSE_SI = 01, HSE_LP = 1)	X	F_{HCLK} = 48MHz	2.51	1.62	mA
				F_{HCLK} = 24MHz	1.78	1.37	
				F_{HCLK} = 16MHz	1.67	1.37	
				F_{HCLK} = 8MHz	1.39	1.25	
				F_{HCLK} = 750KHz	1.19	1.19	
		Runs on the high-speed internal RC	0	F_{HCLK} = 48MHz	2.11	1.24	
				F_{HCLK} =	1.40	0.99	

		oscillator (HSI)		24MHz			
				F_{HCLK} = 16MHz	1.29	0.99	
				F_{HCLK} = 8MHz	1.01	0.87	
				F_{HCLK} = 750KHz	0.82	0.81	
			1	F_{HCLK} = 40KHz	0.55	0.55	

Note: The above are measured parameters.

Table 3-7-2 Typical current consumption in Sleep mode, data processing code runs from internal Flash or SRAM (V_{DD} = 5V)

Symbol	Parameter	Condition			Typ.		Unit
		HSI/HSE	HSI_LP	F_{HCLK}	All peripherals enabled	All peripherals disabled	
I_{DD}(1)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	Runs on the high-speed external clock (HSE) (HSE_SI = 01, HSE_LP = 1)	X	F_{HCLK} = 48MHz	2.54	1.65	mA
				F_{HCLK} = 24MHz	1.81	1.40	
				F_{HCLK} = 16MHz	1.70	1.40	
				F_{HCLK} = 8MHz	1.42	1.27	
				F_{HCLK} = 750KHz	1.22	1.22	
		Runs on the high-speed internal RC oscillator (HSI)	0	F_{HCLK} = 48MHz	2.12	1.25	
				F_{HCLK} = 24MHz	1.42	1.00	

				F_{HCLK} = 16MHz	1.30	0.99	
				F_{HCLK} = 8MHz	1.02	0.87	
				F_{HCLK} = 750KHz	0.82	0.81	
			1	F_{HCLK} = 40KHz	0.56	0.55	

Note: The above are measured parameters.

Table 3-8 Typical current consumption in Standby mode

Symbol	Parameter	Condition			Typ.	Unit
		Independent watchdog	LSI	V_{DD}		
I_{DD}	Supply current in Standby mode	Enable	Disable	3.3V	9.69	uA
				5V	10.14	
		Enable	Enable	3.3V	9.72	
				5V	10.20	
		Disable	Disable	3.3V	9.22	
				5V	9.68	
		Disable	Enable	3.3V	9.67	
				5V	10.14	

Note: The above are measured parameters.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency		3	24	32	MHz
V_{HSEH}(1)	XI input pin high level voltage		0.8V_{DD}		V_{DD}	V
V_{HSEL}(1)	XI input pin low-level voltage		0		0.2V_{DD}	V

$C_{in(HSE)}$	XI input capacitance			5		pF
$DuCy_{(HSE)}$	Duty cycle		40	50	60	%
I_L	XI input leakage current				±1	uA

Note: 1. Failure to meet this condition may cause level recognition error.

Figure 3-3 External high-frequency clock source circuit

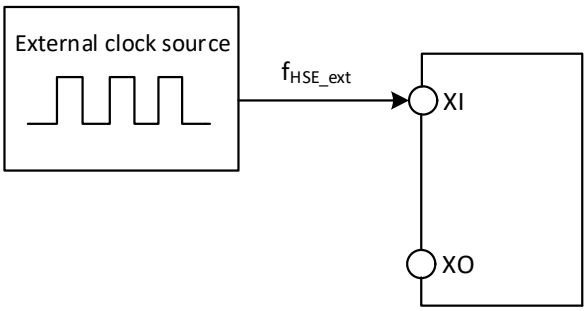


Table 3-10 High-speed external clock generated from a crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{XI}	Resonator frequency		3	24	32	MHz
R_F	Feedback resistor (no external)			250		kΩ
C_{LOAD}	Recommended load capacitance and corresponding crystal series impedance R_S	R_S = 60Ω(1)		20		pF
I_{HSE}	HSE drive current	HSE_LP = 0, 20p load		0.91		mA
		HSE_LP = 1, 20p load		0.48		
g_m	Oscillator transconductance	Startup		21		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} is stable		1.5(2)		ms

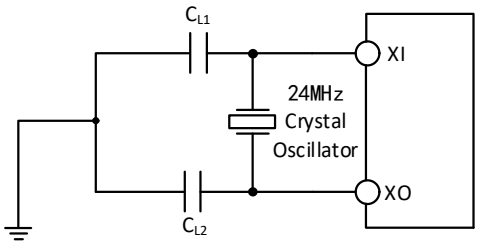
Note: 1. 25M crystal ESR is recommended not more than 80Ω, less than 25m can be appropriately relaxed.

2. Startup time refers to the time difference between when HSEON is turned on and when HSERDY is set.

Circuit reference design and requirements:

The load capacitance of the crystal is subject to the recommendation of the crystal manufacturer, generally C_{L1} = C_{L2}.

Figure 3-4 Typical circuit of external 24M crystal



3.3.6 Internal Clock Source Characteristics

Table 3-11 Internal high-speed (HSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency (after calibration)	HSI_LP = 0		24		MHz
		HSI_LP = 1	30	42	58	KHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator (after calibration)	HSI_LP = 0, TA = 0℃~70℃	-1.8		1.8	%
		HSI_LP = 0, TA = -40℃~85℃	-3		2.5	%
$t_{SU(HSI)}$(1)	HSI oscillator startup stabilization time			3	8	us
$I_{DD(HSI)}$	HSI oscillator power consumption	HSI_LP = 0		200		uA
		HSI_LP = 1		8.5		

Note: 1. Register RCC_CTLR HSION is set to 1 and wait for HSIRDY to be set to 1.

Table 3-12 Internal low-speed (LSI) RC oscillator characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		90	128	172	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$(1)	LSI oscillator startup stabilization time			30	100	us
$I_{DD(LSI)}$(1)	LSI oscillator power consumption			550		nA

Note: 1. Register RCC_CTLR LSION is set to 1 and wait for LSIRDY to be set to 1.

3.3.7 Wakeup Time from Low-power Mode

Table 3-13 Wakeup time from low-power mode(1)

Symbol	Parameter	Condition	Typ.	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	Use HSI RC clock to wakeup	10	us
$t_{WUSTDBY}$	Wakeup from Standby mode	LDO stabilization time + HSI RC clock wake up	250	us

Note: The above are measured parameters.

3.3.8 Memory Characteristics

Table 3-14 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{prog_page}	Page (256 bytes) program time			1.5	2.0	ms
t_{erase_page}	Page (256 bytes) erase time			2.5	3.0	ms
t_{erase_sec}	Sector (1K bytes) erase time			2.7	3.3	ms

Table 3-15 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Erase and write times	T_A = 25℃	100K			Times
t_{RET}	Data retention period		10			Years

3.3.9 I/O Port Characteristics

Table 3-16 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Standard I/O pin, input high level voltage		0.20*(V_{DD}-2.7)+1.55		V_{DD}+0.3	V
V_{IL}	Standard I/O pin, input low-level voltage		-0.3		0.20*(V_{DD}-2.7)+0.65	V
V_{hys}	Schmitt trigger voltage hysteresis		150			mV
I_{lkg}	Input leakage current				1	uA
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ
R_{PD}	Pull-down equivalent resistance		35	45	55	kΩ
C_{IO}	I/O pin capacitance			5		pF

Output drive current characteristics

GPIO (General-Purpose Input/Output Port) can sink or output up to ±8mA current, and sink or output ±20mA current (not strictly to V_{OL}/V_{OH}). In user applications, the total driving current of all I/O pins cannot exceed the absolute maximum ratings given in Section 3.2:

Table 3-17 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, 8 pins input current	TTL port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, 8 pin output current		V_{DD}-0.4		
V_{OL}	Output low level, 8 pins input current	CMOS port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, 8 pin output current		2.3		
V_{OL}	Output low level, 8 pins input current	I_{IO} = +20mA 2.7V< V_{DD} <5.5V		1.3	V
V_{OH}	Output high level, 8 pin output current		V_{DD}-1.3		

Note: The sum of current must not exceed the absolute maximum rating given in Section 3.2 of the table if more than one I/O pin is driven at the same time in the above conditions. When multiple I/O pins are driven at the same time, the current on the power supply/ground wire point is very large, which will cause the voltage drop so that the voltage of the internal I/O cannot reach the power supply voltage in the meter, resulting in the drive current less than the nominal value.

Table 3-18 Input/output AC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$F_{max(IO)out}$	Maximum frequency	CL = 50pF, V_{DD} = 2.7-5.5V		30	MHz
$t_{f(IO)out}$	Output high to low fall time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
$t_{r(IO)out}$	Output low to high rise time	CL = 50pF, V_{DD} = 2.7-5.5V		10	ns
t_{EXTIpw}	The EXTI controller detects the pulse width of the external signal		10		ns

Note: Above parameters are guaranteed by design.

3.3.10 NRST Pin Characteristics

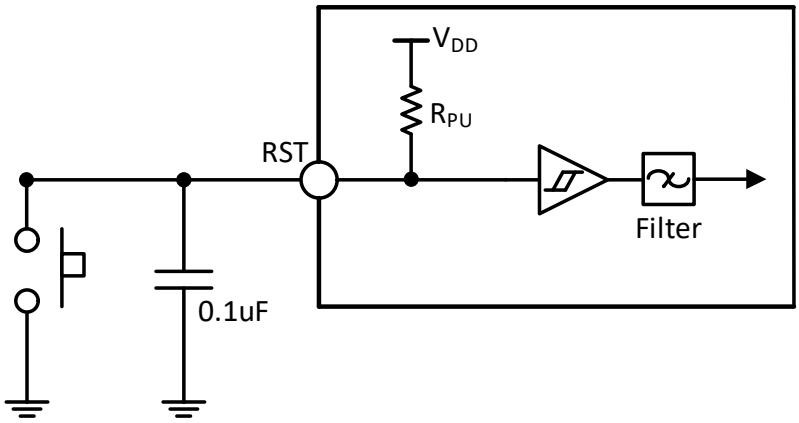
Table 3-19 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit

$V_{IL(RST)}$	RST input low-level voltage		-0.3		0.20*(V_{DD}-2.7)+0.65	V
$V_{IH(RST)}$	RST input high-level voltage		0.20*(V_{DD}-2.7)+1.55		V_{DD}+0.3	V
$V_{hys(RST)}$	NRST Schmitt Trigger voltage hysteresis		150			mV
R_{PU}	Pull-up equivalent resistance		35	45	55	kΩ
$V_{F(RST)}$	RST input can be filtered pulse width				100	ns
$V_{NF(RST)}$	RST input cannot be filtered pulse width		300			ns

Circuit reference design and requirements:

Figure 3-5 Typical circuit of external reset pin



Note: The capacitance in the figure is optional and can be used to filter out key jitter.

3.3.11 TIM Timer Characteristics

Table 3-20 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	20.8		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 48MHz	0	24	MHz

R_{esTIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz	0.0208	1363	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48MHz		1363	us

3.3.12 I2C Interface Characteristics

Figure 3-6 I2C bus timing diagram

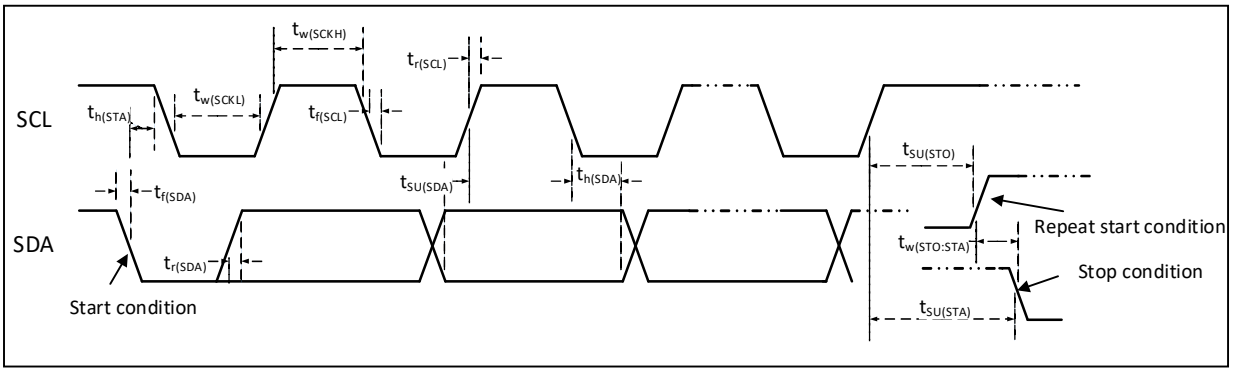


Table 3-21 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low-level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high-level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.13 SPI Interface Characteristics

Figure 3-7 SPI timing diagram in Master mode

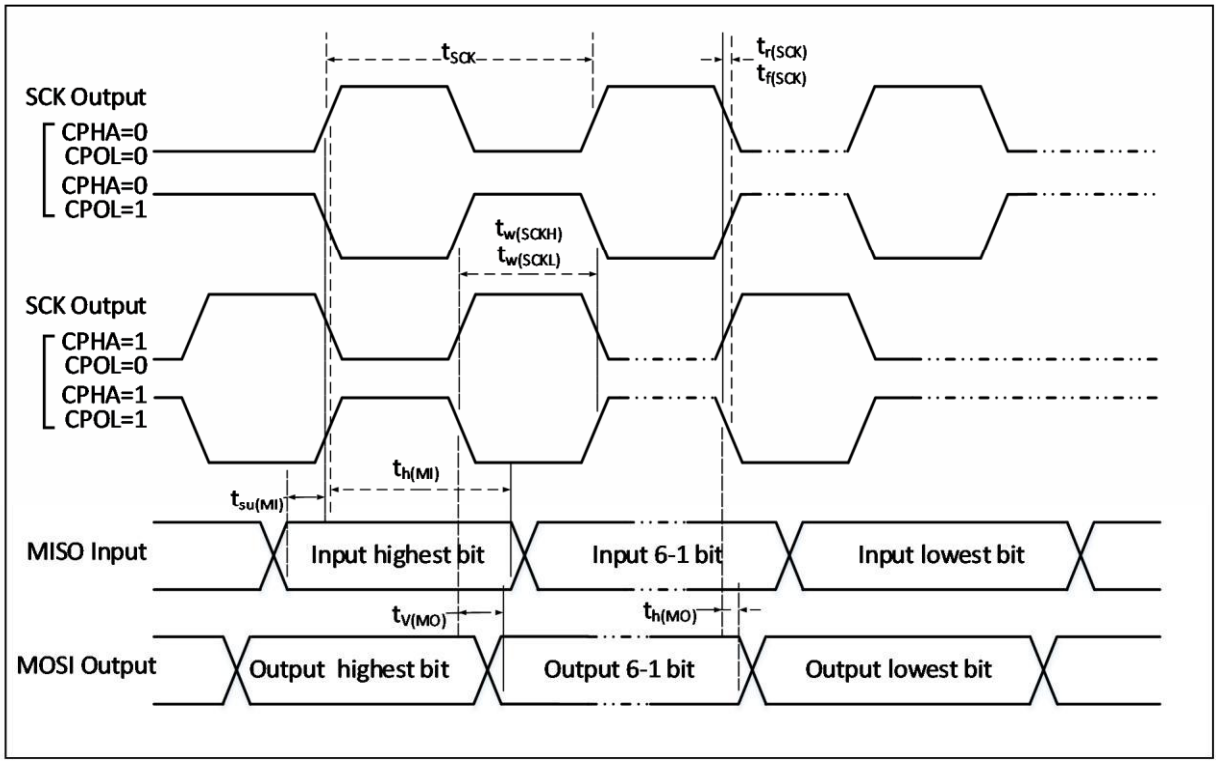


Figure 3-8 SPI timing diagram in Slave mode (CPHA = 0)

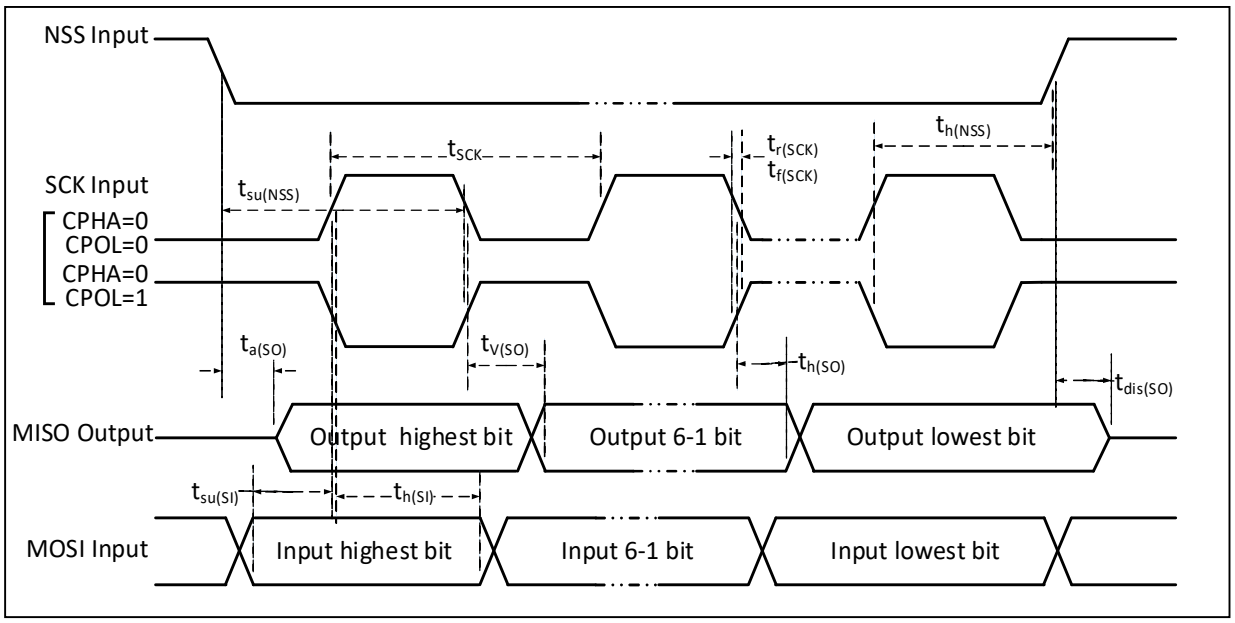


Figure 3-9 SPI timing diagram in Slave mode (CPHA = 1)

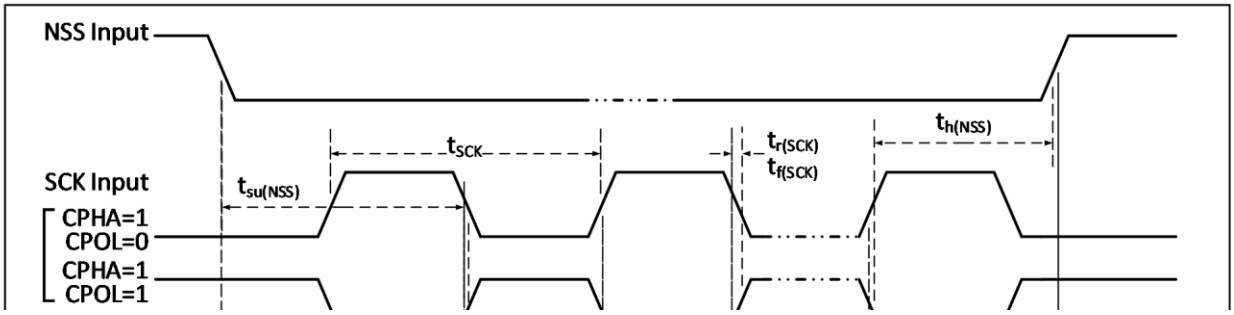


Table 3-22 SPI interface characteristics

Symbol	Parameter	Condition		Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode			24	MHz
		Slave mode			24	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF			10	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode		$2t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode		$2t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high and low time	Master mode, f_{HCLK} = 24MHz, Prescaler factor = 4		70	97	ns
$t_{SU(MI)}$	Data input setup time	Master mode	HSRXEN = 0	15		ns
			HSRXEN = 1	$15-0.5t_{SCK}$		
$t_{SU(SI)}$		Slave mode				ns
$t_{h(MI)}$	Data input hold time	Master mode	HSRXEN = 0	-4		ns
			HSRXEN = 1	$0.5t_{SCK}-4$		
$t_{h(SI)}$		Slave mode				ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{HCLK} = 20MHz		0	$1t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode		0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)			15	ns

$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	6		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.14 10-bit ADC Characteristics

Table 3-23 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	f_S < 1MHz	2.4		5.5	V
		f_S = 3MHz	4.5		5.5	V
I_{DDA}	ADC supply current (Without buffer)	f_S = 3MHz		0.67		mA
		f_S = 1MHz		0.21		mA
I_{BUF}	ADC buffer own current	ADC_LP = 0		0.68		mA
		ADC_LP = 1		0.13		mA
f_{ADC}	ADC clock frequency			16	48	MHz
f_S	Sampling rate		0.06		3	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 16MHz			900	KHz
		f_{ADC} = 48MHz			2.7	MHz
					18	$1/f_{ADC}$
V_{AIN}	Switching voltage range		0		V_{DD}	V
R_{AIN}	External input impedance				50	kΩ
R_{ADC}	Sampling switch resistance			0.6	1.5	kΩ
C_{ADC}	Internal sample and hold capacitance			4		pF
t_{CAL}	Calibration time	f_{ADC} = 16MHz			6.25	us
					100	$1/f_{ADC}$
t_{Iat}	Injection trigger conversion delay	f_{ADC} = 16MHz			0.125	us
		f_{ADC} = 48MHz			0.042	us
					2	$1/f_{ADC}$
t_{Iatr}	Conventional trigger conversion	f_{ADC} = 16MHz			0.125	us

	delay	f_{ADC} = 48MHz			0.042	us
					2	$1/f_{ADC}$
t_s	Sampling time	f_{ADC} = 16MHz	0.218		14.97	us
			3.5		239.5	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.073		0.739	us
			3.5		35.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16MHz	1		15.75	us
			16		252	$1/f_{ADC}$
		f_{ADC} = 48MHz	0.33		1	us
			16		48	$1/f_{ADC}$

Note: Above parameters are guaranteed by design.

Formula: Maximum R_{AIN}

The above formula is used to determine the maximum external impedance so that the error can be less than 1/4 LSB. Where N = 12 (represents a 12-bit resolution).

Table 3-24-1 Maximum R_{AIN} when f_{ADC} = 16MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)
3.5	0.22	4
7.5	0.47	10
13.5	0.84	20
28.5	1.78	45
41.5	2.59	65
55.5	3.47	/
71.5	4.47	/
239.5	14.97	/

Table 3-24-2 Maximum R_{AIN} (High-speed) when f_{ADC} = 48MHz

T_S(Cycle)	t_S(us)	Maximum R_{AIN}(kΩ)

3.5	0.073	1.5
7.5	0.16	3
11.5	0.24	5
19.5	0.41	9
35.5	0.74	17
55.5	1.16	28
71.5	1.49	37
239.5	4.99	/

Table 3-25 ADC error (f_{ADC} = 16MHz, ADC_LP = 1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
EO	Offset error	R_{AIN} < 10kΩ, V_{DD} = 5V	±1		±2	LSB
ED	Differential nonlinear error		±1		±2	
EL	Integral nonlinear error		±1		±2	

Note: Above parameters are guaranteed by design.

C_p represents the parasitic capacitance on the PCB and the pad (about 5pF), which may be related to the quality of the pad and PCB layout. A larger C_p value will reduce the conversion accuracy, the solution is to reduce the f_{ADC} value.

Figure 3-10 ADC typical connection diagram

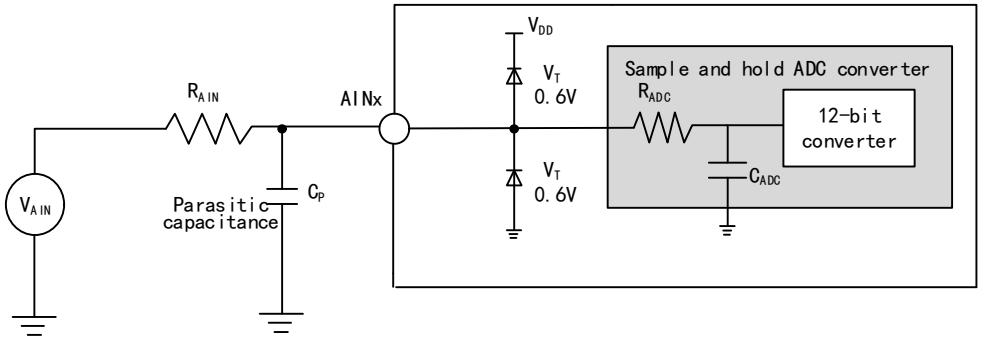


Figure 3-11 Analog power supply and decoupling circuit reference