Chapter 7 GPIO and Alternate Function (GPIO/AFIO)

The GPIO port can be configured for multiple input or output modes, with built-in pull-up or pull-down resistors that can be turned off, and can be configured for push-pull or open-drain functions. the GPIO port can also be multiplexed for other functions.

7.1 Main Features

Each pin of the port can be configured to one of the following multiple modes.

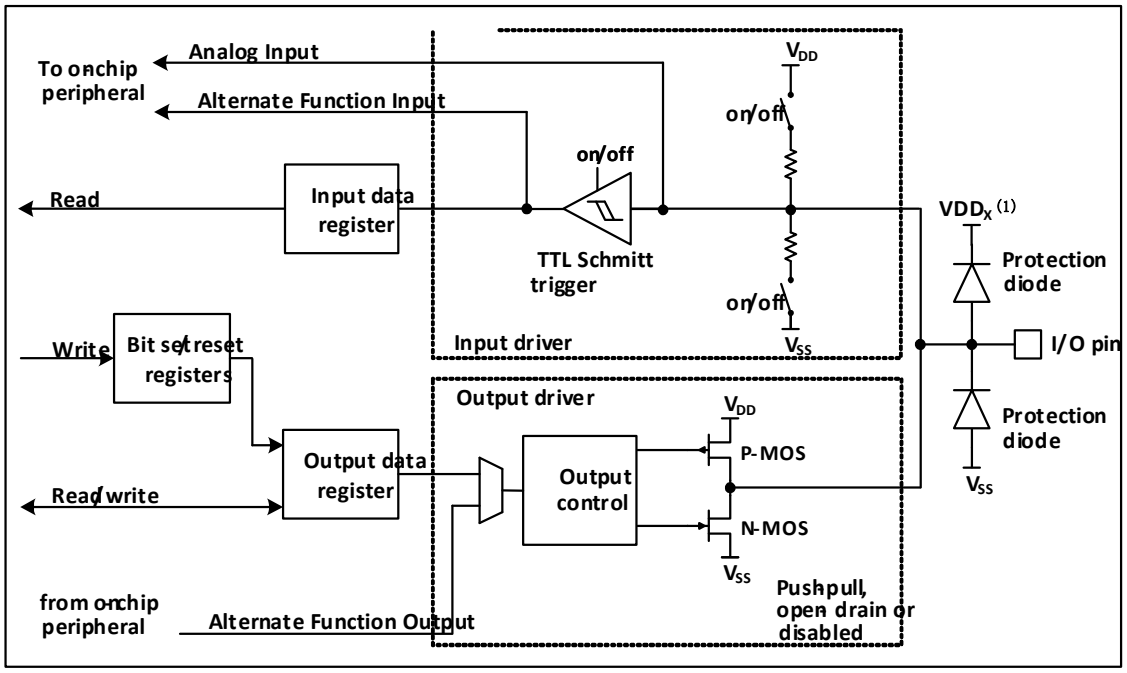
- Floating input
- Pull-up input
- Dropdown input
- Analog input
- Open drain output
- Push-pull output
- Multiplexing the inputs and outputs of functions

Many pins have multiplexing capabilities, and many other peripherals map their output and input channels to these pins. The specific usage of these multiplexed pins needs to be referred to the individual peripherals, and the content of whether these pins are multiplexed and remapped is explained in this chapter.

7.2 Function Description

7.2.1 Overview

Figure 7-1 GPIO module basic structure block diagram



Note: (1) VDDx is VDD when GPIO is normal IO, and VDDx is VDD_FT when GPIO is FT IO.

As shown in Figure 7-1 IO port structure, each pin has two protection diodes inside the chip, and the IO port can be divided into input and output driver modules internally. Among them, the input driver has a weak pull-up and pull-down resistor optional, which can be connected to AD and other analog input peripherals; if the input is to a digital peripheral, it needs to go through a TTL Schmitt trigger and then connect to GPIO input registers or other multiplexed peripherals. The output driver has a pair of MOS tubes, and the IO port can be configured as open-drain or push-pull output by configuring whether the upper and lower MOS tubes are enabled or not; the output driver can also be configured internally to control the output by GPIO or by other multiplexed peripherals.

7.2.2 GPIO Initialization Function

Just after reset, the GPIO ports run in the initial state, when most IO ports are running in the floating input state, but there are also peripheral related pins such as HSE that are running on the peripheral multiplexing function. Please refer to the chapter related to pin description for the specific initialization function.

7.2.3 External Interrupts

All GPIO ports can be configured with external interrupt input channels, but an external interrupt input channel can only be mapped to at most one GPIO pin, and the serial number of the external interrupt channel must be the same as the bit number of the GPIO port, for example, PA1 (or PC1, PD1, etc.) can only be mapped to EXTI1, and EXTI1 can only accept one of PA1, PC1 or PD1, etc. The mapping of both parties is one-to-one.

7.2.4 Multiplexing Functions

It is important to note that using the multiplexing function.

- To use the multiplexing function in the input direction, the port must be configured in multiplexed input mode, and the pull-down settings can be set according to actual needs.
- Using the multiplexing function in the output direction, the port must be configured in multiplexed output mode, push-pull or open-drain can be set according to the actual situation.
- For bidirectional multiplexing, the port must be configured in multiplexed output mode, when the driver is configured in floating input mode

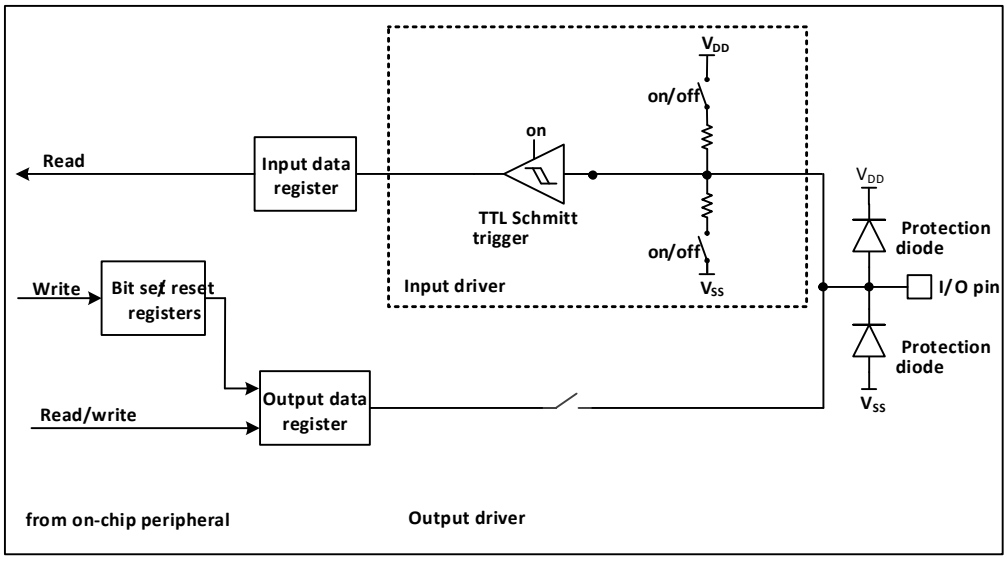
The same IO port may have multiple peripherals multiplexed to this pin, so in order to maximize the space for each peripheral, the multiplexed pins of peripherals can be remapped to other pins in addition to the default multiplexed pins, avoiding the occupied pins.

7.2.5 Locking Mechanism

The locking mechanism locks the configuration of the IO port. After a specific write sequence, the selected IO pin configuration will be locked and cannot be changed until the next reset.

7.2.6 Input Configuration

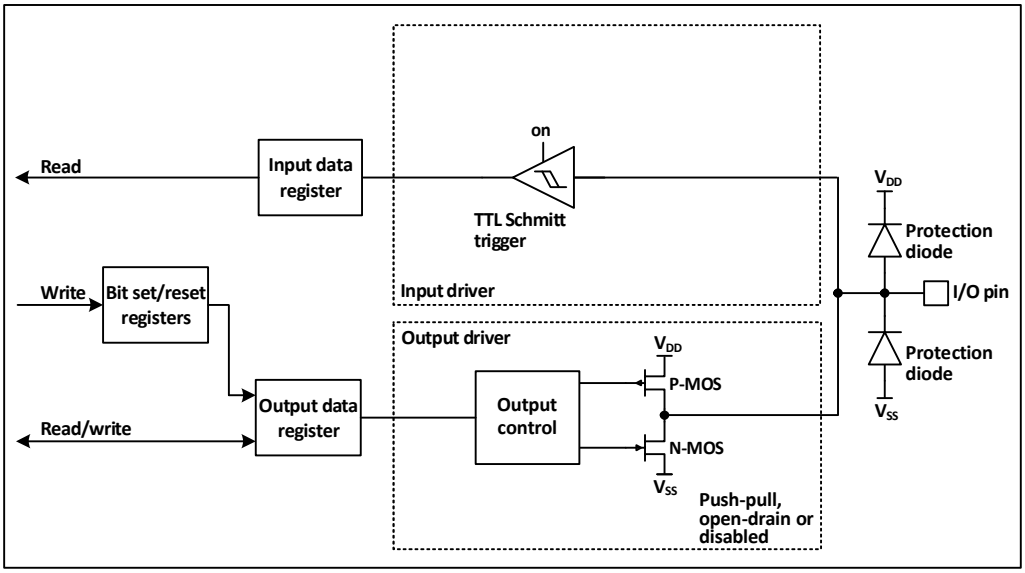
Figure 7-2 GPIO module input configuration structure block diagram



When the IO port is configured in input mode, the output driver is disconnected, the input pull-up and pull-down are selectable, and no multiplexed functions or analog inputs are connected. The data on each IO port is sampled into the input data register at each HB clock, and the level status of the corresponding pin is obtained by reading the corresponding bit of the input data register.

7.2.7 Output Configuration

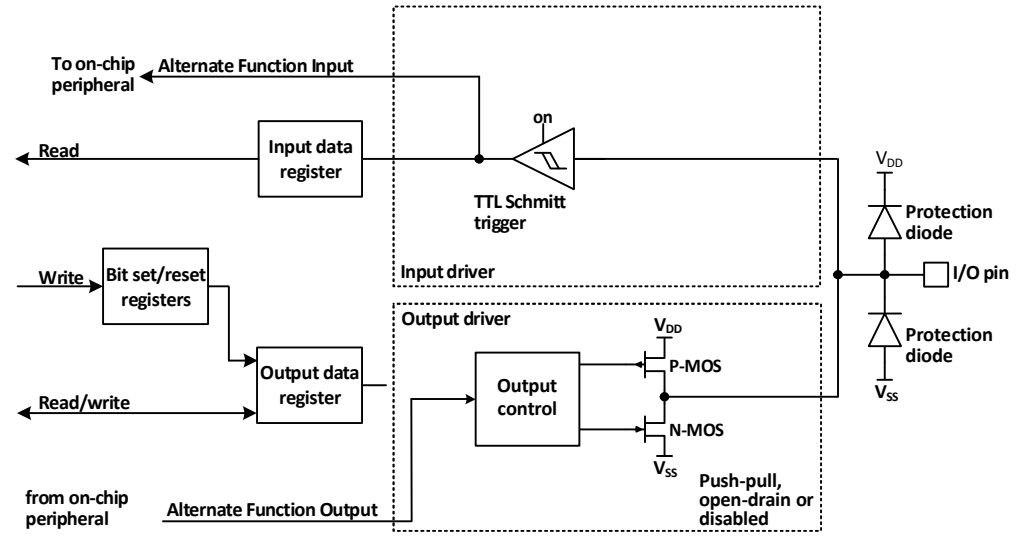
Figure 7-3 GPIO module output configuration structure block diagram



When the IO port is configured to output mode, the pair of MOS in the output driver can be configured to push-pull or open-drain mode as needed, without using the multiplexing function. The pull-up and pull-down resistors of the input driver are disabled, the TTL Schmitt trigger is activated, and the levels appearing on the IO pins will be sampled into the input data registers at each HB clock, so reading the input data registers will give the IO status, and in push-pull output mode, access to the output data registers will give the last written value.

7.2.8 Multiplexing Function Configuration

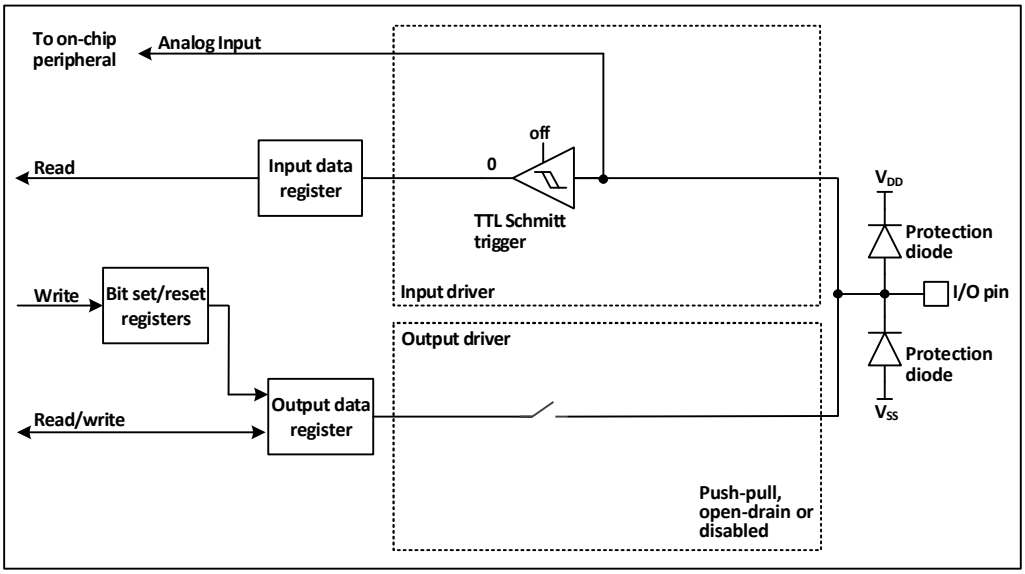
Figure 7-4 The structure of GPIO module when it is multiplexed by other peripherals



When multiplexing is enabled, the output driver is enabled and can be configured to open-drain or push-pull mode as desired, the Schmitt trigger is turned on, the input and output lines of the multiplexing function are connected, but the output data registers are disconnected, and the levels appearing on the IO pins will be sampled into the input data registers at each HB clock. In open-drain mode, reading the input data register will give the current status of the IO port; in push-pull mode, reading the output data register will give the last written value.

7.2.9 Analog Input Configuration

Figure 7-5 The configuration structure when the GPIO module is used as an analog input



When the analog input is enabled, the output buffer is disconnected, the input of the Schmitt trigger in the input driver is disabled to prevent the generation of consumption on the IO port, the pull-up and pull-down resistors are disabled, and the read input data register will always be 0.

7.2.10 GPIO Settings for Peripherals

The following table recommends the corresponding GPIO port configuration for each peripheral pin.

Table 7-1 Advanced-control timer (TIM1)

TIM1 pins	Configuration	GPIO configuration
TIM1_CHx	Input capture channel x	Floating input
	Output comparison channel x	Push-pull multiplexed output
TIM1_CHxN	Complementary output channels x	Push-pull multiplexed output
TIM1_BKIN	Brake input	Floating input
TIM1_ETR	Externally triggered clock input	Floating input

Table 7-2 General-purpose timer (TIM2)

TIM2 pins	Configuration	GPIO configuration
TIM2_CHx	Input capture channel x	Floating input
	Output comparison channel x	Push-pull multiplexed output
TIM2_ETR	Externally triggered clock input	Floating input

Table 7-3 Universal synchronous asynchronous serial transceiver (USART)

USART pins	Configuration	GPIO configuration
USARTx_TX	Full-duplex mode	Push-pull multiplexed outputs
	Half-duplex synchronous mode	Open-drain multiplexed outputs
USARTx_RX	Full-duplex mode	Floating input or pull-up input
	Half-duplex synchronous mode	Not used
USARTx_CK	Synchronous mode	Push-pull multiplexed output
USARTx_RTS	Hardware flow control	Push-pull multiplexed output
USARTx_CTS	Hardware flow control	Floating input or pull-up input

Table 7-4 Serial peripheral interface (SPI) modules

SPI pins	Configuration	GPIO configuration
SPIx_SCK	Master mode	Push-pull multiplexed output
	Slave mode	Floating input

SPIx_MOSI	Full-duplex Master mode	Push-pull multiplexed output
	Full-duplex Slave mode	Floating input or pull-up input
	Simple bi-directional data line/Master mode	Push-pull multiplexed output
	Simple bi-directional data line/Slave mode	Not used
SPIx_MISO	Full-duplex Master mode	Floating input or pull-up input
	Full-duplex Slave mode	Push-pull multiplexed output
	Simple bi-directional data line/Master mode	Not used
	Simple bi-directional data line/Slave mode	Push-pull multiplexed output
SPIx_NSS	Hardware Master or Slave mode	Float, pull-up or pull-down input
	Hardware Master mode/NSS output enable mode	Push-pull multiplexed output
	Software mode	Not used

Table 7-5 Internal integrated bus (I2C) module

I2C pins	Configuration	GPIO configuration
I2C_SCL	I2C clock	Open-drain multiplexed output
I2C_SDA	I2C data	Open-drain multiplexed output

Table 7-6 Analog-to-digital converters (ADCs)

ADC pin	GPIO configuration
ADC	Analog input

Table 7-7 Other I/O function settings

Pins	Configuration features	GPIO configuration
MCO	Clock output	Push-pull multiplexed output
EXTI	External interrupt input	Float, pull-up or pull-down input
OPA	Operational Amplifier Input	Floating input

7.2.11 Alternate Function Remapping GPIO Configuration

7.2.11.1 Timer Alternate Function Remapping

Table 7-8 TIM1 alternate function remapping

Alternate function	TIM1_RM=00 Default mapping	TIM1_RM=01 Partial mapping	TIM1_RM=10 Partial mapping	TIM1_RM=11 Full mapping
TIM1_ETR	PC5	PC5	PD4	PC2
TIM1_CH1	PD2	PC6	PD2	PC4
TIM1_CH2	PA1	PC7	PA1	PC7
TIM1_CH3	PC3	PC0	PC3	PC5
TIM1_CH4	PC4	PD3	PC4	PD4
TIM1_BKIN	PC2	PC1	PC2	PC1
TIM1_CH1N	PD0	PC3	PD0	PC3
TIM1_CH2N	PA2	PC4	PA2	PD2
TIM1_CH3N	PD1	PD1	PD1	PC6

Note: For the mapping function of TIM1_CH1 in the table, the condition is TIM1_1_RM=0. When TIM1_1_RM=1, TIM1_CHI is mapped to LSI (for LSI calibration).

Table 7-9 TIM2 alternate function remapping

Alternate function	TIM2_RM=00 Default mapping	TIM2_RM=01 Partial mapping	TIM2_RM=10 Partial mapping	TIM2_RM=11 Full mapping
TIM2_ETR	PD4	PC5	PC1	PC1
TIM2_CH1	PD4	PC5	PC1	PC1
TIM2_CH2	PD3	PC2	PD3	PC7
TIM2_CH3	PC0	PD2	PC0	PD6
TIM2_CH4	PD7	PC1	PD7	PD5

7.2.11.2 USART Alternate Function Remapping

Table 7-10 USART1 alternate function remapping

Alternate function	USART1_RM=00 Default mapping	USART1_RM=01 Partial mapping	USART1_RM=10 Partial mapping	USART1_RM=11 Full mapping
USART1_CK	PD4	PD7	PD7	PC5
USART1_TX	PD5	PD0	PD6	PC0
USART1_RX	PD6	PD1	PD5	PC1
USART1_CTS	PD3	PC3	PC6	PC6
USART1_RTS	PC2	PC2	PC7	PC7

7.2.11.3 SPI Alternate Function Remapping

Table 7-11 SPI alternate function remapping

Alternate function	SPI1_RM=0 Default mapping	SPI1_RM=1 Remapping
SPI1_NSS	PC1	PC0
SPI1_SCK	PC5	PC5
SPI1_MISO	PC7	PC7
SPI1_MOSI	PC6	PC6

7.2.11.4 I2C Alternate Function Remapping

Table 7-12 I2C alternate function remapping

Alternate function	I2C1_RM=00 Default mapping	I2C1_RM=01 Remapping	I2C1_RM=1x Remapping
I2C1_SCL	PC2	PD1	PC5
I2C1_SDA	PC1	PD0	PC6

7.2.11.4 ADC Alternate Function Remapping

Table 7-13 ADC external trigger injection conversion alternate function remapping

Alternate function	ADC_ETRGINJ_RM=0 Default mapping	ADC_ETRGINJ_RM=1 Remapping
ADC external trigger injection conversion	ADC externally triggered injection conversion connected to PD1	ADC externally triggered injection conversion connected to PA2

Table 7-13 ADC external trigger rule conversion alternate function remapping

Alternate function	ADC_ETRGREG_RM=0 Default mapping	ADC_ETRGREG_RM=1 Remapping
ADC external trigger rule conversion	ADC externally triggered rule conversion connected to PD3	ADC externally triggered rule conversion connected to PC2

7.3 Register Description

7.3.1 GPIO Register Description

Unless otherwise specified, the registers of the GPIO must be operated as words (operate these registers with 32 bits).

Table 7-8 GPIO-related registers list

Name	Access address	Description	Reset value
R32_GPIOA_CFGLR	0x40010800	PA port configuration register low	0x44444444
R32_GPIOC_CFGLR	0x40011000	PC port configuration register low	0x44444444
R32_GPIOD_CFGLR	0x40011400	PD port configuration register low	0x44444444
R32_GPIOA_INDR	0x40010808	PA port input data register	0x000000XX
R32_GPIOC_INDR	0x40011008	PC port input data register	0x000000XX
R32_GPIOD_INDR	0x40011408	PD port input data register	0x000000XX
R32_GPIOA_OUTDR	0x4001080C	PA port output data register	0x00000000
R32_GPIOC_OUTDR	0x4001100C	PC port output data register	0x00000000
R32_GPIOD_OUTDR	0x4001140C	PD port output data register	0x00000000
R32_GPIOA_BSHR	0x40010810	PA port set/reset register	0x00000000
R32_GPIOC_BSHR	0x40011010	PC port set/reset register	0x00000000
R32_GPIOD_BSHR	0x40011410	PD port set/reset register	0x00000000
R32_GPIOA_BCR	0x40010814	PA port reset register	0x00000000
R32_GPIOC_BCR	0x40011014	PC port reset register	0x00000000
R32_GPIOD_BCR	0x40011414	PD port reset register	0x00000000
R32_GPIOA_LCKR	0x40010818	PA port configuration lock register	0x00000000
R32_GPIOC_LCKR	0x40011018	PC port configuration lock register	0x00000000
R32_GPIOD_LCKR	0x40011418	PD port configuration lock register	0x00000000

7.3.1.1 Port Configuration Register Low (GPIOx_CFGLR) (x=A/C/D)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF7[1:0]		MODE7[1:0]		CNF6[1:0]		MODE6[1:0]		CNF5[1:0]		MODE5[1:0]		CNF4[1:0]		MODE4[1:0]	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNF3[1:0]		MODE3[1:0]		CNF2[1:0]		MODE2[1:0]		CNF1[1:0]		MODE1[1:0]		CNF0[1:0]		MODE0[1:0]	

Bit	Name	Access	Description	Reset value
[31:30] [27:26] [23:22] [19:18] [15:14] [11:10] [7:6] [3:2]	CNFy[1:0]	RW	(y=0-7), the configuration bits for port x, by which the corresponding port is configured. When in input mode (MODE=00b). 00: Analog input mode. 01: Floating input mode. 10: With pull-up and pull-down mode. 11: Reserved. In output mode (MODE>00b). 00: Universal push-pull output mode. 01: Universal open-drain output mode. 10: Multiplexed function push-pull output mode. 11: Multiplexing function open-drain output mode.	01b

[29:28] [25:24] [21:20] [17:16] [13:12] [9:8] [5:4] [1:0]	MODEy[1:0]	RW	(y=0-7), port x mode selection, configure the corresponding port by these bits. 00: Input mode. 01: Output mode, maximum speed 10MHz; 10: Output mode, maximum speed 2MHz. 11: Output mode, maximum speed 30MHz.	00b

7.3.1.2 Port Input Register (GPIOx_INDR) (x=A/C/D)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0

Bit	Name	Access	Description	Reset value
[31:8]	Reserved	RO	Reserved	0
[7:0]	IDRy	RO	(y=0-7), the port input data. These bits are read-only and can only be read out in 16-bit form. The value read is the high and low state of the corresponding bit.	X

7.3.1.3 Port Output Register (GPIOx_OUTDR) (x=A/C/D)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0

Bit	Name	Access	Description	Reset value
[31:8]	Reserved	RO	Reserved	0
[7:0]	ODRy	RW	For output modes. (y=0-7), the data output by the port. These data can only be operated in 16-bit form. the I/O port outputs the values of these registers externally. For modes with drop-down inputs. 0: Drop-down input. 1: Pull-up input.	0

7.3.1.4 Port Reset/Set Register (GPIOx_BSHR) (x=A/C/D)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved								BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0

Bit	Name	Access	Description	Reset value
[31:24]	Reserved	R0	Reserved	0
[23:16]	BRy	WO	(y=0-7), the corresponding OUTDR bits are	0

			cleared for these location bits, and writing 0 has no effect. These bits can only be accessed in 16-bit form. If both BR and BS bits are set, the BS bit takes effect.	
[15:8]	Reserved	RO	Reserved	0
[7:0]	BSy	WO	(y=0-7), for which the location bits will make the corresponding OUTDR location bits, writing 0 has no effect. These bits can only be accessed in 16-bit form. If both BR and BS bits are set, the BS bit takes effect.	0

7.3.1.5 Port Reset Register (GPIOx_BCR) (x=A/C/D)

Offset address: 0x14

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

Bit	Name	Access	Description	Reset value
[31:8]	Reserved	RO	Reserved	0
[7:0]	BRy	WO	(y=0-7), the corresponding OUTDR bits are cleared for these location bits, and writing 0 has no effect. These bits can only be accessed in 16-bit form.	0

7.3.1.6 Port Configuration Lock Register (GPIOx_LCKR) (x=A/C/D)

Offset address: 0x18

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							LCKK	LCK7	LCK6	LCK5	LCK4	LCK3	LCK2	LCK1	LCK0

Bit	Name	Access	Description	Reset value
[31:9]	Reserved	RO	Reserved	0
8	LCKK	RW	The lock key, which can be written in a specific sequence to achieve locking, but which can be read out at any time. It reads 0 to indicate that no locking is in effect, and reads 1 to indicate that locking is in effect. The write sequence for the lock key is: write 1 - write 0 - write 1 - read 0 - read 1. The last step is not necessary, but can be used to confirm that the lock key is active. Any error while writing the sequence will not enable the activation of the lock and the value of LCK[7:0] cannot be changed while the sequence is being written. After the lock is in effect, the port configuration can only be changed after the next reset.	0
[7:0]	LCKy	RW	(y=0-7), these bits are 1 to indicate locking the configuration of the corresponding port. These bits can only be changed before the LCKK is unlocked. The locked configuration refers to the	0

			configuration registers GPIOx_CFGLR.	

Note: After the LOCK sequence is executed for the corresponding port bit, the configuration of the port bit will not be changed again until the next system reset.

7.3.2 AFIO Register Description

Unless otherwise specified, AFIO registers must be operated as words (operate these registers with 32 bits).

Table 7-9 List of AFIO-related registers

Name	Access address	Description	Reset value
R32_AFIO_PCFR1	0x40010004	Remap Register 1	0x00000000
R32_AFIO_EXTICR	0x40010008	External interrupt configuration register 1	0x00000000

7.3.2.1 Remap Register 1 (AFIO_PCFR1)

Offset address: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved					SWCFG[2:0]			TIM1_1_RM	I2C1__RM1	USART1_RM1	Reserved		ADC_ETRGREG_RM	ADC_ETRGINJ_RM	Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA12_RM	Reserved					TIM2_RM[1:0]		TIM1_RM[1:0]		Reserved			USART1_RM	I2C1_RM	SPI1_RM

Bit	Name	Access	Description	Reset value
[31:27]	Reserved	RO	Reserved	0
[26:24]	SWCFG[2:0]	RW	These bits are used to configure the I/O ports for SW function and trace function. SWD (SDI) is the debug interface to access the core. It is always used as a SWD port after system reset. 0xx: SWD (SDI) enabled. 100: Turn off SWD (SDI), which functions as a GPIO. Others: Invalid.	0
23	TIM1_IREMAP	RW	Control timer 1 channel 1 selection 0: Select external pins 1: Select internal LSI clock	0
22	I2C1REMAP1	RW	I2C1 remapping high bit (used in conjunction with AFIO_PCFR1 register bit1 I2C1_RM [22,1]). 00: default mapping (SCL/PC2, SDA/PC1). 01: Remapping (SCL/ PD1, SDA/ PD0). 1X: Remapping (SCL/PC5, SDA/PC6)	0
21	USART1_RM1	RW	USART1 mapping configuration high (used in conjunction with AFIO PCFR1 register bit2 USART1RM [21,2]). 00: default mapping (CK/PD4, TX/PD5, RX/PD6, CTS/PD3, RTS/PC2). 01: Remapping (CK/PD7, TX/PD0, RX/PD1, CTS/PC3, RTS/PC2, SW_RX/PD0). 10: Remapping (CK/PD7, TX/PD6, RX/PD5, CTS/PC6, RTS/PC7, SW_RX/PD6). 11: Remapping (CK/PC5, TX/PC0, RX/PC1,	0

			CTS/PC6, RTS/PC7, SW_RX/PC0).	
[20:19]	Reserved	RO	Reserved	0
18	ADC_ETRGREG_RM	RW	Remap bit for ADC external trigger rule conversion. 0: ADC external trigger rule conversion connected to PD3. 1: ADC external trigger rule conversion connected to PC2.	0
17	ADC_ETRGINJ_RM	RW	Remap bit for ADC external trigger rule conversion. 0: ADC external trigger rule conversion connected to PD3. 1: ADC external trigger rule conversion connected to PC2.	0
16	Reserved	RO	Reserved	0
15	PA12_RM	RW	Pin PA1 & PA2 remapping bit, this bit can be read or written by user. It controls the proper function of PA1 and PA2 (set to 1 when connected to an external crystal pin) 0: Pin is used as GPIO and multiplexed function 1: No functional role for pins	0
[14:10]	Reserved	RO	Reserved	0
[9:8]	TIM2_RM[1:0]	RW	Remap bits for timer 2. These bits can be read and written by the user. It controls the mapping of Timer 2's channels 1 through 4 and external trigger (ETR) on the GPIO ports. 00: Default mapping (CH1/ETR/PD4, CH2/PD3, CH3/PC0, CH4/PD7). 01: Partial mapping (CH1/ETR/PC5, CH2/PC2, CH3/PD2, CH4/PC1). 10: Partial mapping (CH1/ETR/PC1, CH2/PD3, CH3/PC0, CH4/PD7). 11: Complete mapping (CH1/ETR/PC1, CH2/PC7, CH3/PD6, CH4/PD5).	0
[7:6]	TIM1_RM[1:0]	RW	Remap bits for timer 1. These bits can be read and written by the user. It controls the mapping of channels 1 to 4, 1N to 3N, external trigger (ETR) and brake input (BKIN) of timer 1 to the GPIO ports. 00: Default mapping (ETR/PC5, CH1/PD2, CH2/PA1, CH3/PC3, CH4/PC4, BKIN/PC2, CH1N/PD0, CH2N/PA2, CH3N/PD1). 01: Partial mapping (ETR/PC5, CH1/PC6, CH2/PC7, CH3/PC0, CH4/PD3, BKIN/PC1, CH1N/PC3, CH2N/PC4, CH3N/PD1). 10: Partial mapping (ETR/PD4, CH1/PD2, CH2/PA1, CH3/PC3, CH4/PC4, BKIN/PC2, CH1N/PD0, CH2N/PA2, CH3N/PD1). 11: Complete mapping (ETR/PC2, CH1/PC4, CH2/PC7, CH3/PC5, CH4/PD4, BKIN/PC1, CH1N/PC3, CH2N/PD2, CH3N/PC6).	0
[5:3]	Reserved	RO	Reserved	0
2	USART1_RM	RW	USART1 mapping configuration low bit (used in conjunction with AFIO PCFR1 register bit21 USART1REMAP1 [21,2]). 00: Default mapping (CK/PD4, TX/PD5, RX/PD6, CTS/PD3, RTS/PC2). 01: Remapping (CK/PD7, TX/PD0, RX/PD1, CTS/PC3, RTS/PC2, SW_RX/PD0).	0

			10: Remapping (CK/PD7, TX/PD6, RX/PD5, CTS/PC6, RTS/PC7, SW_RX/PD6). 11: Remapping (CK/PC5, TX/PC0, RX/PC1, CTS/PC6, RTS/PC7, SW_RX/PC0).	
1	I2C1_RM	RW	I2C1 remapping low bit (used in conjunction with AFIO_PCFR1 register bit22 I2C1_RM1 [22,1]). 00: Default mapping (SCL/PC2, SDA/PC1). 01: Remapping (SCL/ PD1, SDA/ PD0). 1X: Remapping (SCL/PC5, SDA/PC6)	0
0	SPI1_RM	RW	Remapping of SPI1. This bit can be read or written by the user. It controls the mapping of SPI1's NSS, SCK, MISO, and MOSI multiplexing functions to the GPIO ports. 0: Default mapping (NSS/PC1, CK/PC5, MISO/PC7, MOSI/PC6). 1: Remapping (NSS/PC0, CK/PC5, MISO/PC7, MOSI/PC6).	0

7.3.2.2 External Interrupt Configuration Register 1 (AFIO_EXTICR)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTI7[1:0]		EXTI6[1:0]		EXTI5[1:0]		EXTI4[1:0]		EXTI3[1:0]		EXTI2[1:0]		EXTI1[1:0]		EXTI0[1:0]	

Bit	Name	Access	Description	Reset value
[31:16]	Reserved	RO	Reserved	0
[15:14] [13:12] [11:10] [9:8] [7:6] [5:4] [3:2] [1:0]	EXTIx[1:0]	RW	(x=0-7), external interrupt input pin configuration bit. Used to determine to which port pins the external interrupt pins are mapped. 00: xth pin of the PA pin. 10: xth pin of the PC pin. 11: xth pin of the PD pin.	0