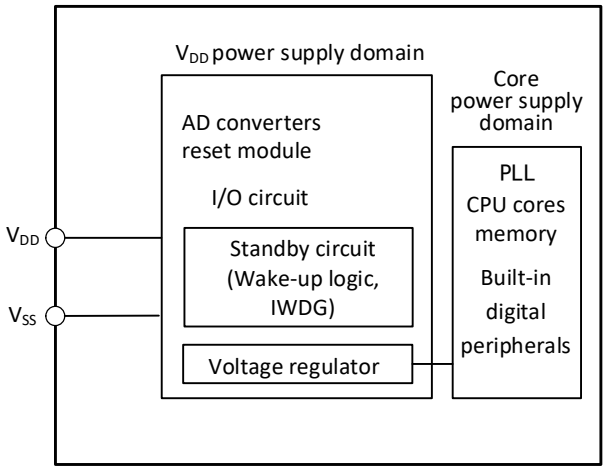
Chapter 2 Power Control (PWR)

2.1 Overview

The system operating voltage V_{DD} ranges from 2.7 to 5.5V, and the built-in voltage regulator provides the working power supply required by the core.

Figure 2-1 Block diagram of power supply structure

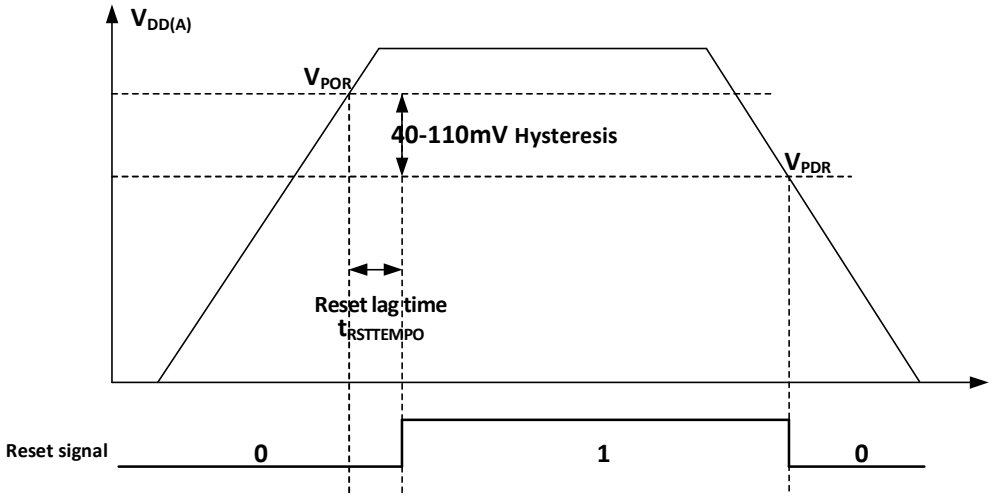


2.2 Power Management

2.2.1 Power-on Reset and Power-down Reset

The system has an internal power-on reset POR and a power-down reset PDR circuit. When the chip supply voltage V_{DD} falls below the corresponding threshold voltage, the system is reset by the relevant circuit, and no additional external reset circuit is required. Please refer to the corresponding datasheet for the parameters of the power-on threshold voltage V_{POR} and the power-down threshold voltage V_{PDR}.

Figure 2-2 Schematic diagram of the operation of POR and PDR



2.2.2 Programmable Voltage Detector

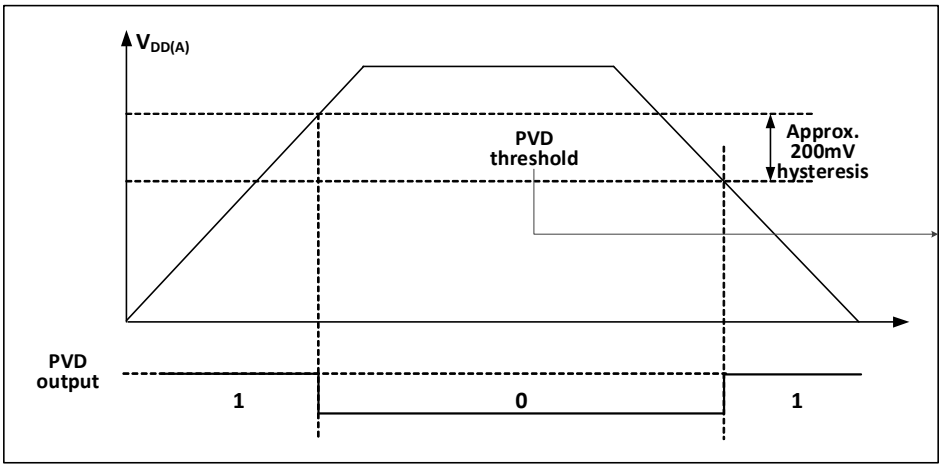
The programmable voltage monitor, PVD, is mainly used to monitor the change of the main power supply of the system and compare it with the threshold voltage set by PLS[2:0] of the power control register PWR_CTLR, and with the external interrupt register (EXTI) setting, it can generate relevant interrupts to notify the system

in time for pre-power down operations such as data saving.

The specific configuration is as follows.

1) Set the PLS[2:0] field of the PWR_CTLR register to select the voltage threshold to be monitored.
2) Optional interrupt handling. the PVD function internally connects to the rising/falling edge trigger setting of line 8 of the EXTI module, turns on this interrupt (configures EXTI), and generates a PVD interrupt when VDD drops below the PVD threshold or rises above the PVD threshold.
3) Set the PVDE bit of PWR_CTLR register to enable the PVD function.
4) Read the PVD0 bit of PWR_CSR status register to obtain the current system main power and PLS[2:0] setting threshold relationship, and perform the corresponding soft processing. When the VDD voltage is higher than the threshold set by PLS[2:0], PVD0 position 0; when the VDD voltage is lower than the threshold set by PLS[2:0], PVD0 position 1.

Figure 2-3 Schematic diagram of PVD operation



2.3 Low-power Modes

After a system reset, the microcontroller is in a normal operating state (run mode), where system power can be saved by reducing the system main frequency or turning off the unused peripheral clock or reducing the operating peripheral clock. If the system does not need to work, you can set the system to enter low-power mode and let the system jump out of this state by specific events.

Microcontrollers currently offer 2 low-power modes, divided in terms of operating differences between processors, peripherals, voltage regulators, etc.

- Sleep mode: The core stops running and all peripherals (including core private peripherals) are still running.
- Standby mode: Stop all clocks, wake up and switch the clock to HSI.

Table 2-1 Low-power mode list

Mode	Entry	Wake-up source	Effect on clock	Voltage regulator
Sleep	WFI	Any interrupt	Core clock OFF, no effect on other clocks	ON
	WFE	Wake-up event		
Standby	Set SLEEPDEEP to 1 Set PDDS to 1 WFI or WFE	AWU event *Note: Any event can also wake up the system, but the system does not reset after waking up.*	HSE, HSI, PLL and peripheral clock OFF	OFF

Note: The SLEEPDEEP bit belongs to the core private peripheral control bit, CH32V003 product reference PFIC_SCTLR register.

2.3.1 Low-power Configuration Options

- WFI and WFE

WFI: The microcontroller is woken up by an interrupt source with interrupt controller response, and the interrupt service function will be executed first after the system wakes up (except for microcontroller reset).
WFE: The wakeup event triggers the microcontroller to exit low-power mode. Wake-up events include.

1) Configure an external or internal EXTI line to event mode, when no interrupt controller needs to be configured.
2) Or configure an interrupt source, equivalent to a WFI wakeup, where the system prioritizes the execution of the interrupt service function.
3) Or configure the SLEEPONPEN bit to turn on peripheral interrupt enable, but not interrupt enable in the interrupt controller, and the interrupt pending bit needs to be cleared after the system wakes up.

- SLEEPONEXIT

  Enable: After executing the WFI or WFE instruction, the microcontroller ensures that all pending interrupt services are exited and then enters low-power mode.

  Not enabled: The microcontroller enters low-power mode immediately after executing the WFI or WFE command.

- SEVONPEND

  Enable: All interrupts or wake-up events can wake up the low-power consumption entered by executing WFE.

  Not enabled: Only interrupts or wake-up events enabled in the interrupt controller can wake up the low-power consumption entered by executing WFE.

2.3.2 Sleep Mode (SLEEP)

In this mode, all I/O pins keep their state in Run mode and all peripheral clocks are normal, so try to turn off useless peripheral clocks before entering Sleep mode to reduce low-power consumption. This mode takes the shortest time to wake up.
Enter: Configure core register control bit SLEEPDEEP=0, power control register PDDS=0, execute WFI or WFE, optionally SEVONPEND and SLEEPONEXIT.
Exit: Arbitrary interrupt or wakeup event.

2.3.3 Standby Mode (STANDBY)

Standby mode is a combination of peripheral clock control mechanisms based on the core's deep Sleep mode (SLEEPDEEP) and allows the voltage regulator to operate at a much lower-power consumption. This mode has the high frequency clock (HSE/HSI/PLL) domain turned off, the SRAM and register contents held, and the I/O pin state held. The system can continue to run after this mode wakes up, and the HSI is called the default system clock.
If flash programming is in progress, the system does not enter Standby mode until access to memory is complete.
Standby mode can work modules: Independent Watchdog (IWDG), Low Frequency Clock (LSI).
Enter: Configure the core register control bit SLEEPDEEP=1, PDDS=1 in the power control register, and execute WFI or WFE, optionally SEVONPEND and SLEEPONEXIT.
Exit:

1) Any interrupt/event (set in the external interrupt register).
2) AWU event, clock switches to HSI after this wakeup, system does not reset.

2.3.4 Auto-wakeup (AWU)

Auto-wakeup without external interrupts can be implemented. The time base can be programmed to wake up periodically from Standby mode.
The optional internal low-frequency 128KHz clock oscillator LSI is used as the automatic wake-up counting

time base.

When turning on the AWU interrupt function, you need to set the rising/falling edge trigger of the 9th line internally connected to the EXTI module and turn on this interrupt (configuration EXTI).

2.4 Register Description

Table 2-2 PWR-related registers list

Name	Access address	Description	Reset value
R32_PWR_CTLR	0x40007000	Power control register	0x00000000
R32_PWR_CSR	0x40007004	Power control/status register	0x00000000
R32_PWR_AWUCSR	0x40007008	Auto-wakeup control/status register	0x00000000
R32_PWR_AWUWR	0x4000700C	Auto-wakeup window comparison value register	0x0000003f
R32_PWR_AWUPSC	0x40007010	Auto-wakeup crossover factor register	0x00000000

2.4.1 Power Control Register (PWR_CTLR)

Offset address: 0x00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								PLS[2:0]			PVDE	Reserved		PDDS	Reserved

Bit	Name	Access	Description	Reset value
[31:8]	Reserved	RO	Reserved	0
[7:5]	PLS[2:0]	RW	PVD voltage monitoring threshold setting. See the Electrical Characteristics section of the datasheet for detailed instructions. 000: 2.85V rising edge/2.7V falling edge. 001: 3.05V rising edge/2.9V falling edge. 010: 3.3V rising edge/3.15V falling edge. 011: 3.5V rising edge/3.3V falling edge. 100: 3.7V rising edge/3.5V falling edge. 101: 3.9V rising edge/3.7V falling edge. 110: 4.1V rising edge/3.9V falling edge. 111: 4.4V rising edge/4.2V falling edge.	0
4	PVDE	RW	Power supply voltage monitoring function enable flag bit 1: Enable the power supply voltage monitoring function. 0: Disable the power supply voltage monitoring function.	0
[3:2]	Reserved	RO	Reserved	0
1	PDDS	RW	Standby/ Sleep mode selection bit in power-down deep sleep scenario. 1: Enter Standby mode. 0: Enter Sleep mode.	0
0	Reserved	RO	Reserved	0

2.4.2 Power Control/Status Register (PWR_CSR)

Offset address: 0x04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													PVD0	Reserved	

Bit	Name	Access	Description	Reset value
[31:3]	Reserved	RO	Reserved	0
2	PVD0	RO	PVD output status flag bit. This bit is valid when PVDE=1 of PWR_CTLR register. 1: VDD and VDDA are below the PVD threshold set by PLS[2:0]. 0: VDD and VDDA are above the PVD threshold set by PLS[2:0].	0
[1:0]	Reserved	RO	Reserved	0

2.4.3 Auto-wakeup Control/Status Register (PWR_AWUCSR)

Offset address: 0x08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved														AWUEN	Reserved

Bit	Name	Access	Description	Reset value
[31:2]	Reserved	RO	Reserved	0
1	AWUEN	RW	Enable Automatic wake-up 1: Turn on auto-wakeup; 0: Invalid.	0
0	Reserved	RO	Reserved	0

2.4.4 Auto-wakeup Window Comparison Value Register (PWR_AWUWR)

Offset address: 0x0C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										AWUUWR[5:0]					

Bit	Name	Access	Description	Reset value
[31:6]	Reserved	RO	Reserved	0
[5:0]	AWUWR[5:0]	RW	AWU window value: The AWU window value is equal to the input value of the AWU window value + 1; The AWU window value is used to compare with the up counter value. When the counter value is equal to the window value, a wake-up signal is generated.	0x3f

2.4.5 Auto-wakeup Crossover Factor Register (PWR_ AWUPSC)

Offset address: 0x10

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												AWUPSC[3:0]			

Bit	Name	Access	Description	Reset value
[31:4]	Reserved	RO	Reserved	0
[3:0]	AWUPSC[3:0]	RW	Counting time base 0000: Prescaler off. 0001: Prescaler off. 0010: Divided by 2. 0011: Divided by 4. 0100: Divided by 8. 0101: Divided by 16. 0110: Divided by 32. 0111: Divided by 64. 1000: Divided by 128. 1001: Divided by 256. 1010: Divided by 512. 1011: Divided by 1024. 1100: Divided by 2048. 1101: Divided by 4096. 1110: Divided by 10240. 1111: Divided by 61440.	0