CO PROJECT – RISC-V SIMULATOR

TEAM NAME: TECH PHANTOMS

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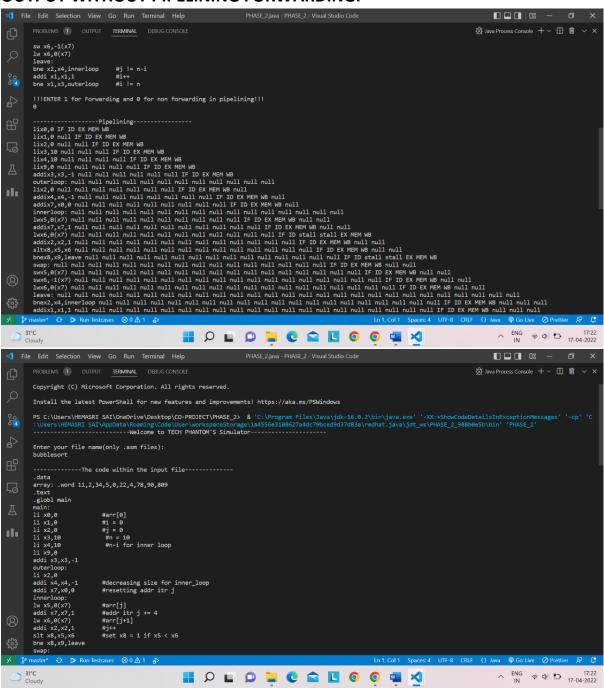
WHAT WE TRIED:

- After taking the input of the file, the code within the input file is being stored in an array.
- Then, we do check for data and text sections and if they are correct proceed to the next part.
- We check for the main index to start and then store the instructions into another array.
- While the program counter is less than or equal to the total number of lines in the code, we implement the code within the input file by updating the pipeline 2-D array.
- Now, we fill the pipeline 2-D array according to the instructions.
- We then check for the instruction in each line and then check if the source register is same as the destination register of the previous instruction.
- If in case they are same, then we check whether the instruction is branch instruction in both forwarding and non-forwarding cases.
- Now we check where the previous instruction's IF, ID, EX, MEM, WB are located and if the previous instruction's contain stalls, then continue them further.
- Now, fill the pipeline 2-D array accordingly.
- While filling the 2-D array, we also check for stalls and continue them in further rows
- The same method is followed every instruction line.
- Finally, we checked where the last WB is located and calculated the number of clock cycles. And then we calculated total number of stalls, number of instructions per cycle and found the list of instructions where stalls occurred.

WHAT DID NOT WORK:

- The stalls for every instruction are being printed but they aren't being continued to
 further rows that is if a instruction results in 2 stalls in 11th and 12th location in 3rd
 row, then all the instructions in the succeeding rows should contain stalls in 11th and
 12th location, but here in this code those stalls are being re-written by null or any one
 of the IF/ID/EX/MEM/WB.
- In this implementation, we are able to cross-check between source and destination registers only for current instruction line and previous instruction line but not the line before the previous instruction line. If we try to do that, the stalls are not being seen in the output.

OUTPUT WITHOUT PIPELINING FORWARDING:



OUTPUT WITH PIPELINE FORWARDING:

