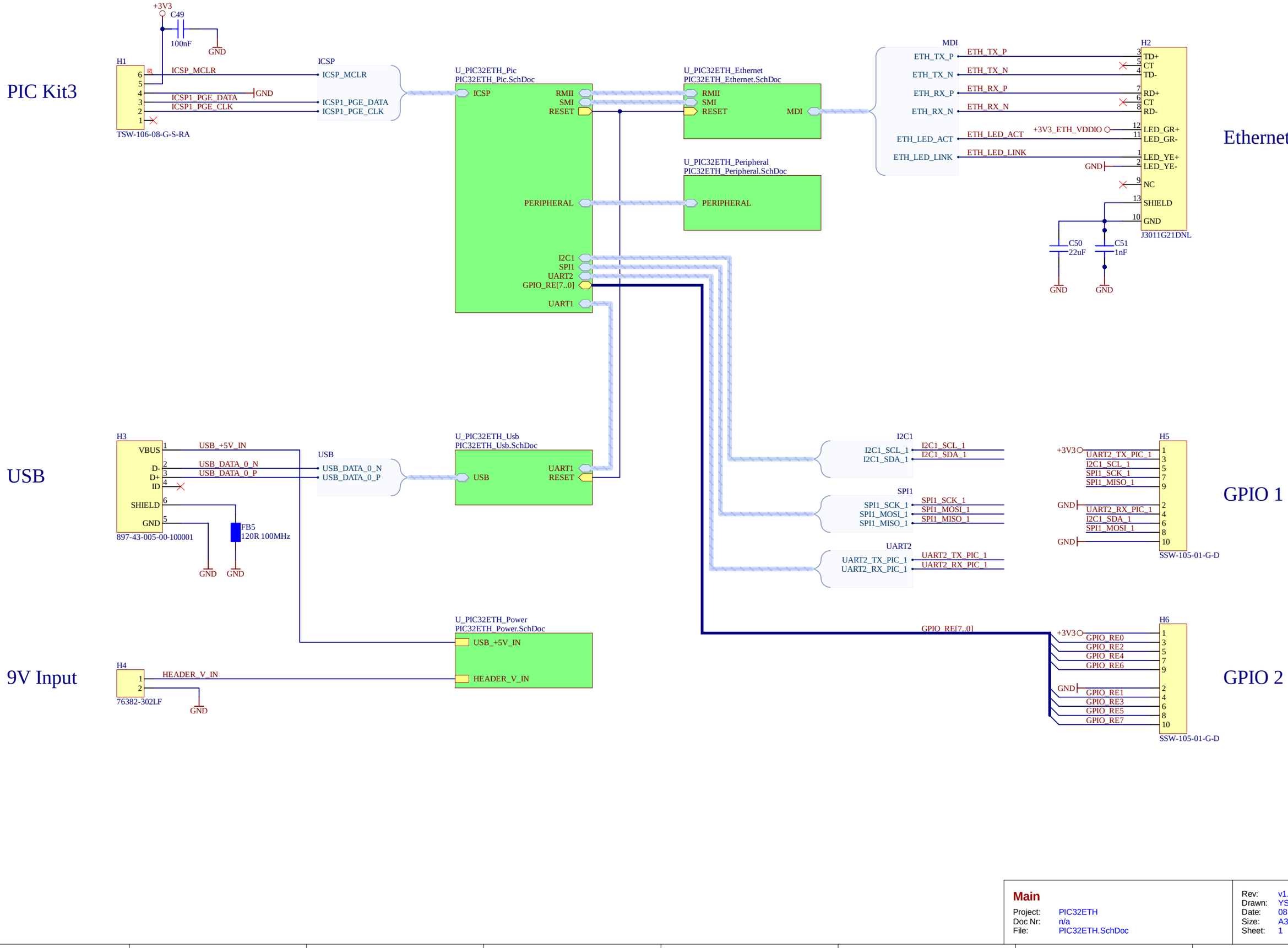
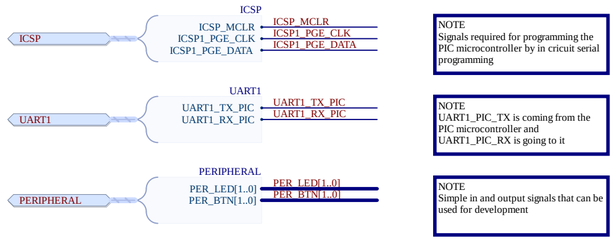
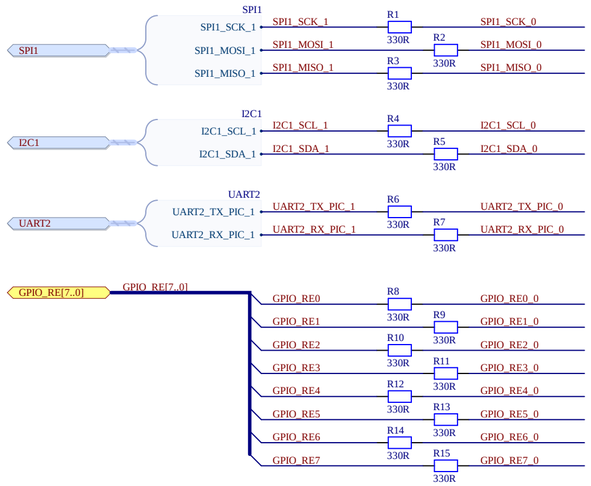

PIC Kit3
+3V3
C49
100nF
GND
H1
ICSP_MCLR
GND
ICSP1_PGE_DATA
ICSP1_PGE_CLK
TSW-106-08-G-S-RA
ICSP
ICSP_MCLR
ICSP1_PGE_DATA
ICSP1_PGE_CLK
U_PIC32ETH_Pic
PIC32ETH_Pic.SchDoc
ICSP
RMII
SMI
RESET
PERIPHERAL
I2C1
SPI1
UART2
GPIO_RE[7..0]
UART1
U_PIC32ETH_Ethernet
PIC32ETH_Ethernet.SchDoc
RMII
SMI
RESET
MDI
U_PIC32ETH_Peripheral
PIC32ETH_Peripheral.SchDoc
PERIPHERAL
MDI
ETH_TX_P
ETH_TX_N
ETH_RX_P
ETH_RX_N
ETH_LED_ACT
ETH_LED_LINK
H2
TD+
CT
TD-
RD+
CT
RD-
LED_GR+
LED_GR-
LED_YE+
LED_YE-
NC
SHIELD
GND
J3011G21DNL
+3V3_ETH_VDDIO
C50
22uF
C51
1nF
Ethernet
USB
H3
VBUS
D-
D+
ID
SHIELD
GND
USB_+5V_IN
USB_DATA_0_N
USB_DATA_0_P
897-43-005-00-100001
FB5
120R 100MHz
USB
USB_DATA_0_N
USB_DATA_0_P
U_PIC32ETH_Usb
PIC32ETH_Usb.SchDoc
USB
UART1
RESET
9V Input
H4
HEADER_V_IN
76382-302LF
U_PIC32ETH_Power
PIC32ETH_Power.SchDoc
USB_+5V_IN
HEADER_V_IN
I2C1
I2C1_SCL_1
I2C1_SDA_1
SPI1
SPI1_SCK_1
SPI1_MOSI_1
SPI1_MISO_1
UART2
UART2_TX_PIC_1
UART2_RX_PIC_1
H5
SSW-105-01-G-D
GPIO 1
GPIO_RE[7..0]
H6
GPIO_RE0
GPIO_RE2
GPIO_RE4
GPIO_RE6
GPIO_RE1
GPIO_RE3
GPIO_RE5
GPIO_RE7
GPIO 2
Main
Project: PIC32ETH
Doc Nr: n/a
File: PIC32ETH.SchDoc
Rev: v1.0.0
Drawn: YS
Date: 08.01.2022
Size: A3
Sheet: 1 of 6



NOTE
Signals required for programming the PIC microcontroller by in cricuit serial programming

NOTE
UART1_PIC_TX is coming from the PIC microcontroller and UART1_PIC_RX is going to it

NOTE
Simple in and output signals that can be used for development



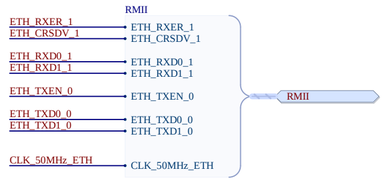
NOTE
SPI bus which will be connected to the header

NOTE
I2C bus which will be connected to the header

NOTE
UART bus which will be connected to the header. UART2_PIC_TX is coming from the PIC microcontroller and UART2_PIC_RX is going to it

NOTE
GPIO pins which will be connected to the header

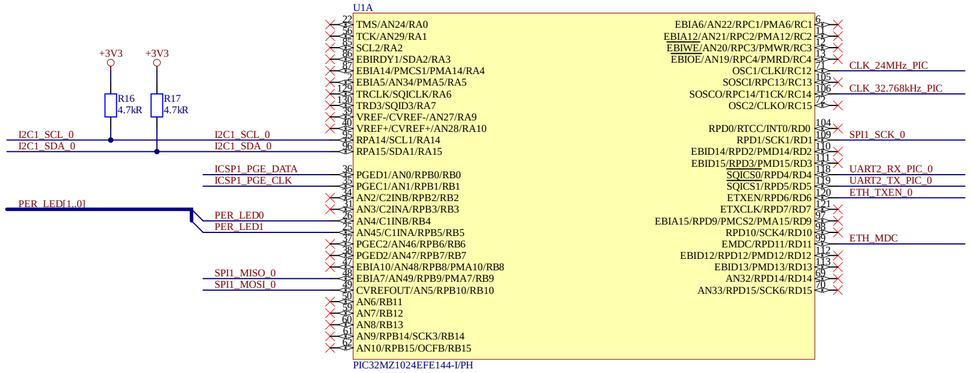
NOTE
RMII between the PIC microcontroller and the ethernet transceiver. TXD signals come from the PIC and RXD ones go to the PIC

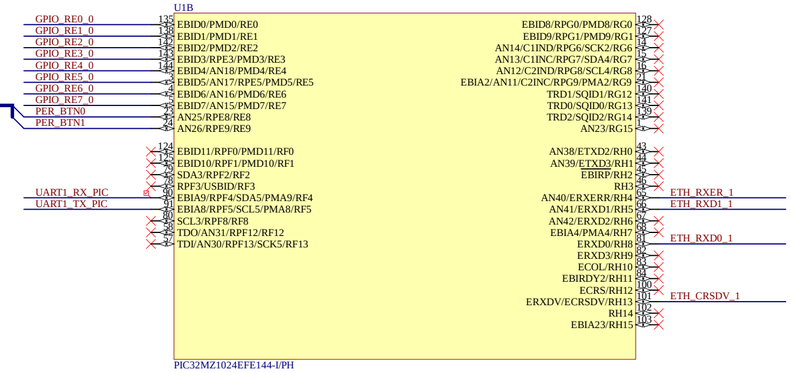


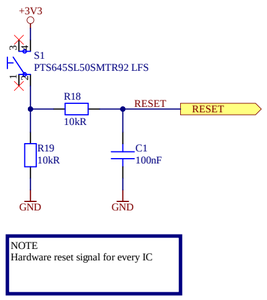
NOTE
Serial Managment interface coming from the PIC microcontroller

DESIGN NOTE
Selected PPS pins of the PIC microcontroller

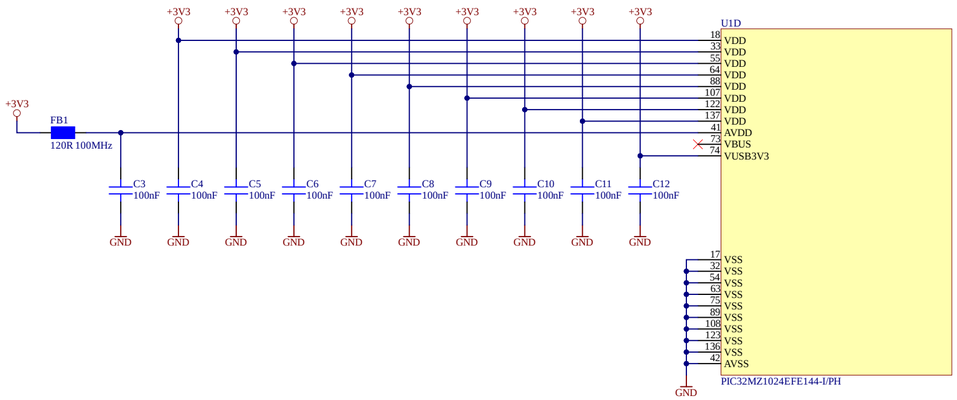
UART1_RX_PIC: RD10
UART1_TX_PIC: RD11
UART2_RX_PIC_1: RD4
UART2_TX_PIC_1: RD5
SPI1_MISO_1: RD2
SPI1_MOSI_1: RD3

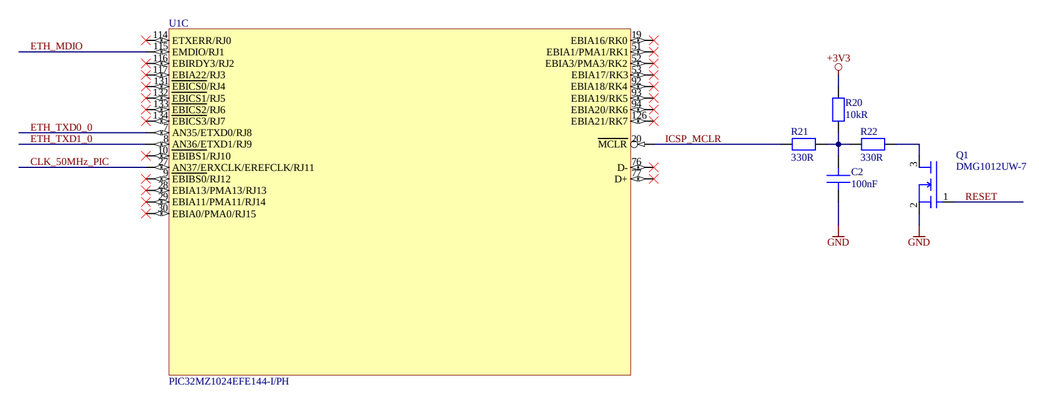


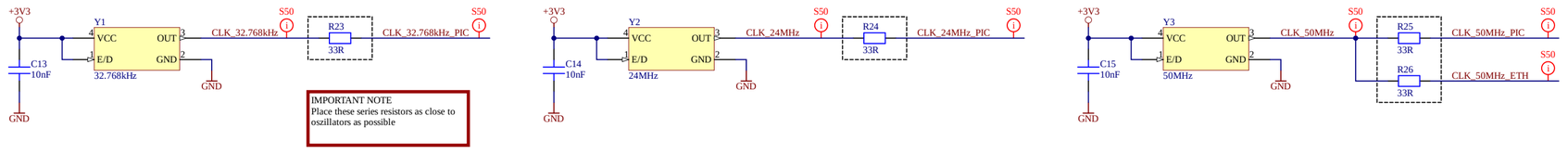




NOTE
Hardware reset signal for every IC







IMPORTANT NOTE
Place these series resistors as close to oszillators as possible

Pic

Project:	PIC32ETH
Doc Nr:	n/a
File:	PIC32ETH_Pic.SchDoc
Rev:	v1.0.0
Drawn:	YS
Date:	08.01.2022
Size:	A2
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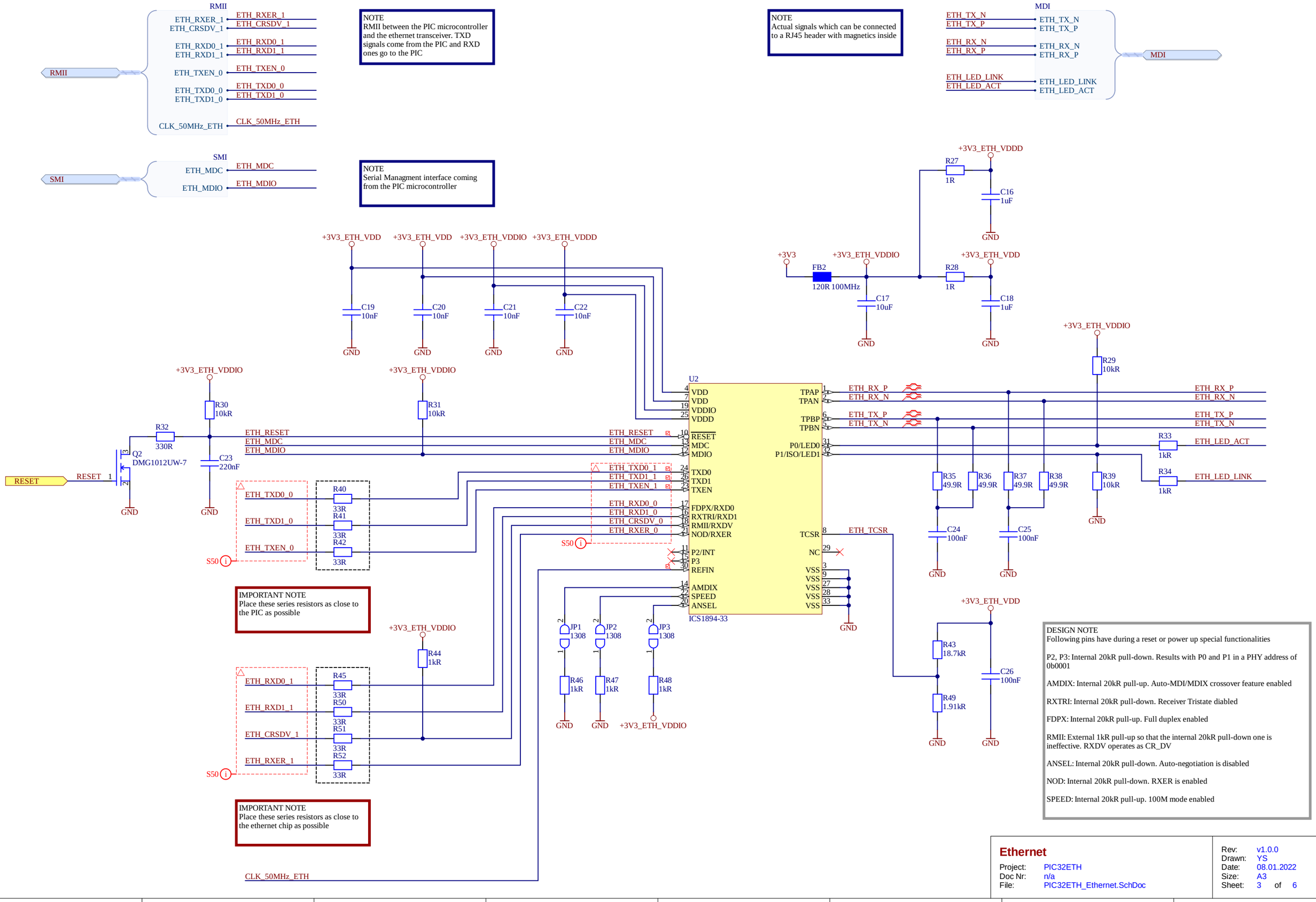
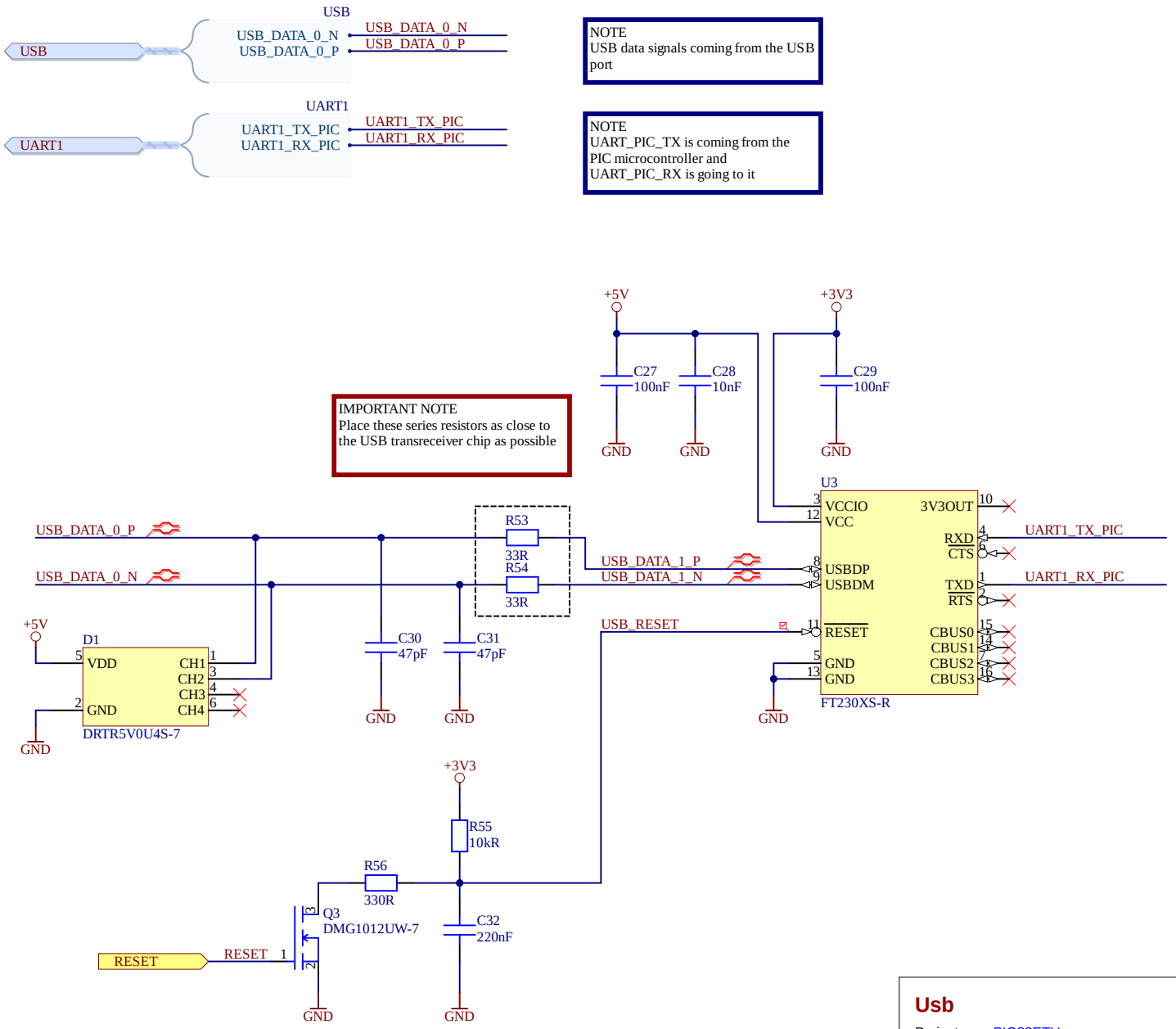
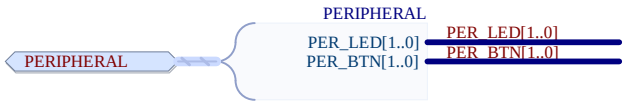

RMII
ETH_RXER_1
ETH_CRSDV_1
ETH_RXD0_1
ETH_RXD1_1
ETH_TXEN_0
ETH_TXD0_0
ETH_TXD1_0
CLK_50MHz_ETH
NOTE
RMII between the PIC microcontroller and the ethernet transceiver. TXD signals come from the PIC and RXD ones go to the PIC
NOTE
Actual signals which can be connected to a RJ45 header with magnetics inside
MDI
ETH_TX_N
ETH_TX_P
ETH_RX_N
ETH_RX_P
ETH_LED_LINK
ETH_LED_ACT
SMI
ETH_MDC
ETH_MDIO
NOTE
Serial Managment interface coming from the PIC microcontroller
+3V3_ETH_VDD
+3V3_ETH_VDDIO
+3V3_ETH_VDDD
+3V3
FB2
120R 100MHz
R27
1R
R28
1R
C16
1uF
C17
10uF
C18
1uF
C19
10nF
C20
10nF
C21
10nF
C22
10nF
GND
U2
VDD
VDDIO
VDDD
RESET
MDC
MDIO
TXD0
TXD1
TXEN
FDPX/RXD0
RXTRI/RXD1
RMII/RXDV
NOD/RXER
P2/INT
P3
REFIN
AMDIX
SPEED
ANSEL
TPAP
TPAN
TPBP
TPBN
P0/LED0
P1/ISO/LED1
TCSR
NC
VSS
ICS1894-33
R29
10kR
R30
10kR
R31
10kR
R32
330R
Q2
DMG1012UW-7
C23
220nF
RESET
R33
1kR
R34
1kR
R35
49.9R
R36
49.9R
R37
49.9R
R38
49.9R
R39
10kR
C24
100nF
C25
100nF
C26
100nF
R40
33R
R41
33R
R42
33R
R43
18.7kR
R44
1kR
R45
33R
R50
33R
R51
33R
R52
33R
R46
1kR
R47
1kR
R48
1kR
R49
1.91kR
JP1
1308
JP2
1308
JP3
1308
S50
IMPORTANT NOTE
Place these series resistors as close to the PIC as possible
IMPORTANT NOTE
Place these series resistors as close to the ethernet chip as possible
DESIGN NOTE
Following pins have during a reset or power up special functionalities
P2, P3: Internal 20kR pull-down. Results with P0 and P1 in a PHY address of 0b0001
AMDIX: Internal 20kR pull-up. Auto-MDI/MDIX crossover feature enabled
RXTRI: Internal 20kR pull-down. Receiver Tristate diabled
FDPX: Internal 20kR pull-up. Full duplex enabled
RMII: External 1kR pull-up so that the internal 20kR pull-down one is ineffective. RXDV operates as CR_DV
ANSEL: Internal 20kR pull-down. Auto-negotiation is disabled
NOD: Internal 20kR pull-down. RXER is enabled
SPEED: Internal 20kR pull-up. 100M mode enabled
Ethernet
Project: PIC32ETH
Doc Nr: n/a
File: PIC32ETH_Ethernet.SchDoc
Rev: v1.0.0
Drawn: YS
Date: 08.01.2022
Size: A3
Sheet: 3 of 6



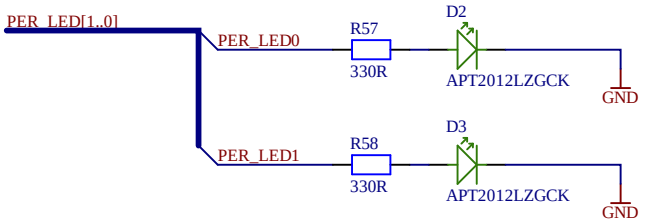
Usb

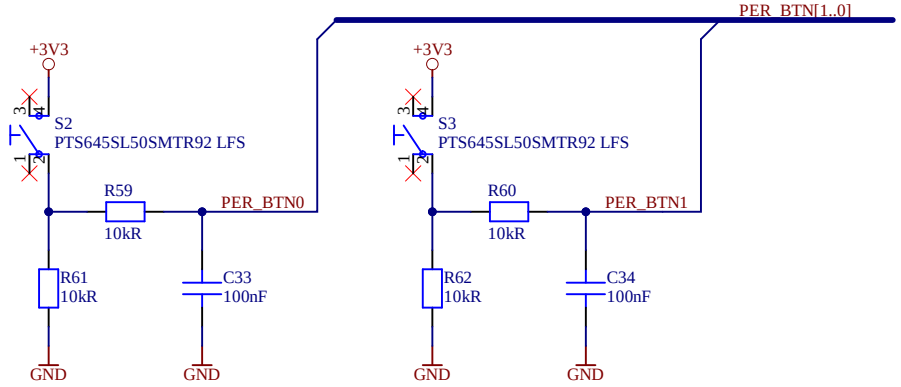
Project:	PIC32ETH
Doc Nr:	n/a
File:	PIC32ETH_Usb.SchDoc

Rev:	v1.0.0
Drawn:	YS
Date:	08.01.2022
Size:	A4
Sheet:	4 of 6



NOTE
Simple in and output signals that can be used for development

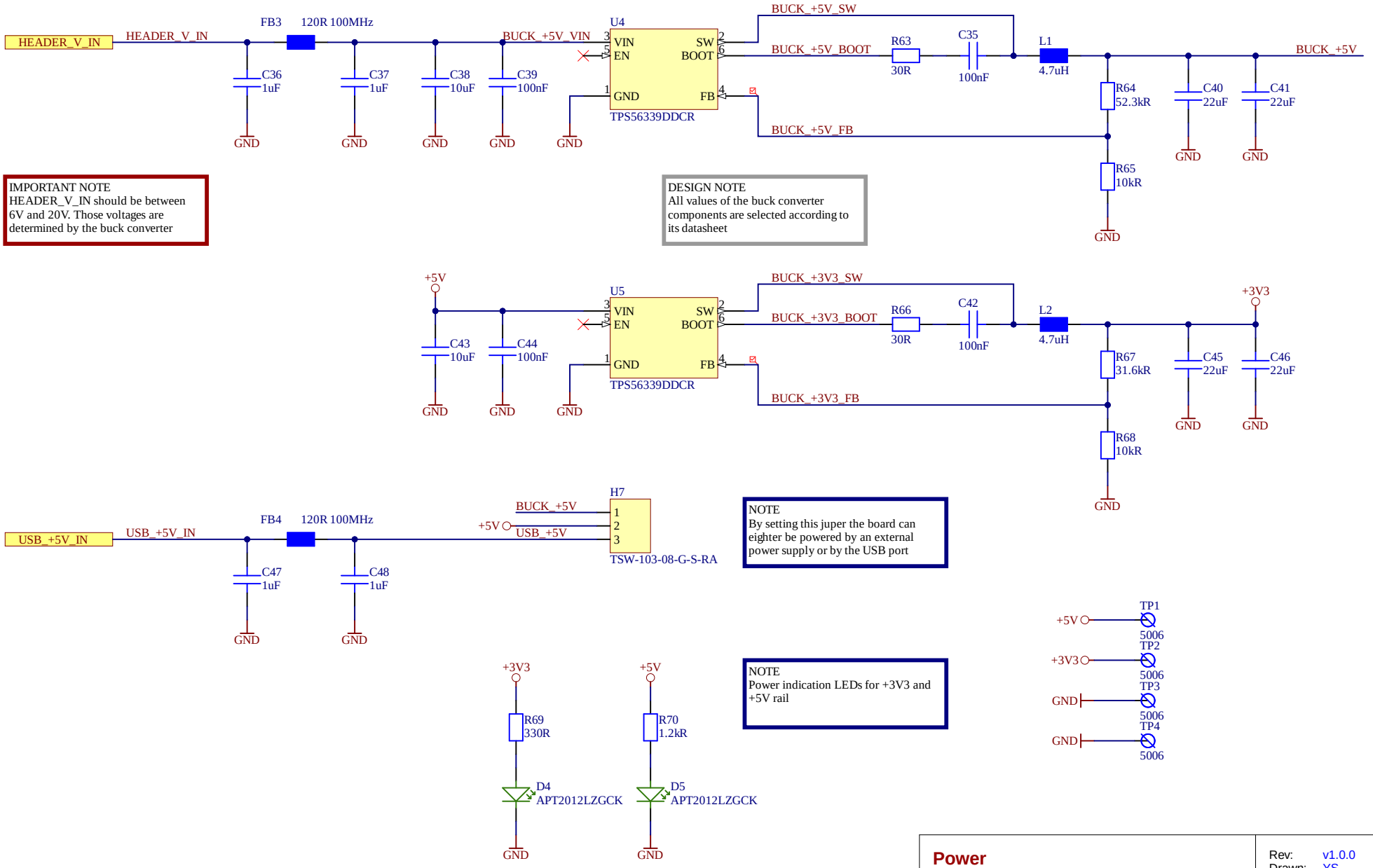




Peripheral

Project:	PIC32ETH
Doc Nr:	n/a
File:	PIC32ETH_Peripheral.SchDoc

Rev:	v1.0.0
Drawn:	YS
Date:	08.01.2022
Size:	A4
Sheet:	5 of 6



Power

Project:	PIC32ETH
Doc Nr:	n/a
File:	PIC32ETH_Power.SchDoc

Rev:	v1.0.0
Drawn:	YS
Date:	08.01.2022
Size:	A4
Sheet:	6 of 6