Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Electronic Circuits
Course Number:	ELE404
Semester/Year	Spring 2023

Instructor:	Sandeep Kaler

Assignment/Lab Number:	8
Assignment/Lab Title:	Design Project

Submission Date	Jun 23, 2023
Due Date:	Jun 23, 2023

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Yang			04	

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ELE404 BJT Amplifier Design Project

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Course: ELE404
Section: 04
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Introduction:

The design project involved creating a BJT amplifier that satisfied the criteria listed below.

Objectives:

Requirements of the project:

- Power supply: +15 V relative to ground
- Total quiescent current drawn from the power supply: No larger than 8 mA
- No-load voltage gain (at 1 kHz): |Avo| = 50(±10%)
- Loaded voltage gain (at 1 kHz, with RL = 1kΩ): No smaller than 90% of the no-load
- voltage gain
- Maximum loaded output voltage swing (at 1 kHz and RL = 1kΩ): No smaller than 4 V
- peak to peak
- Input resistance (at 1 kHz): No smaller than 50 kΩ
- Amplifier type: Inverting or non-inverting
- Frequency response: 20 Hz to 50 kHz (−3 dB response)
- Type of transistor: BJT
- Number of stages (transistors): No more than 3
- Resistances permitted: Values smaller than 220 kΩ from the E24 series.
- Other components (BJTs, diodes, Zener diodes, etc.): Only those present in the ELE404 lab kit.

Additional Requirements:

- The output voltage must be free from distortions (clipping, etc.) under all test conditions.
- The source resistance, Rs, must be 600 Ω under all test conditions
- The designed amplifier must be AC-coupled for the load and the signal source, but the coupling between its intermediate stages may be of AC or DC type as per the designer's choice. There are no restrictions in terms of using NPN or PNP transistors.

Design Planning:

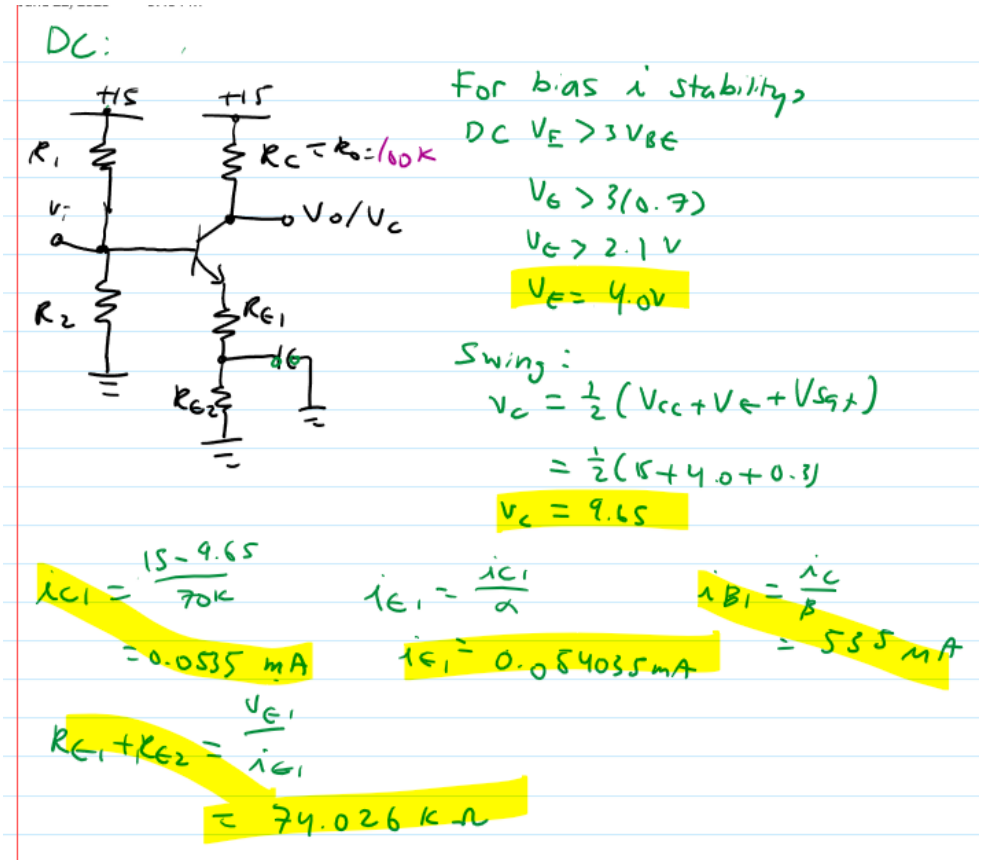
A Common Emitter-Common Collector style amplifier will be used, as the common emitter stage is good at coupling to low signals and can provide the voltage gain needed by the common collector. The common collector will help maintain the net gain of the amplifier, and . In addition, the CE-CC amplifier has good stability and reduces possible feedback by decoupling input and output stages.

Calculations:

Givens:

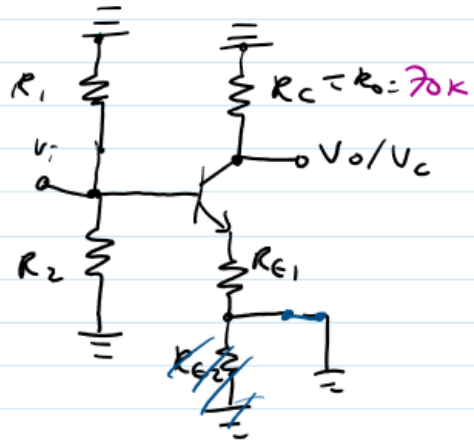
1. Vcc= 15V
2. |Avo| = 50(±5)
3. Rin >= 50k
4. RL=1k
5. Beta = 100

CE-CC Design pattern was used.



V_{C1}	V_{E1}	I_{C1}	I_{E1}	I_{B1}	$R_{E1} + R_{E2}$
9.65 V	4.0 V	0.0535 mA	0.054035 mA	535 uA	74.026 kΩ

AC:



$g_{m1} = \frac{40 I_{C1}}{} = 2.14$

$A_{V0} = \frac{g_{m1} R_{C1}}{1 + g_{m1} R_{E1}}$

$R_{E1} = \left(\frac{g_{m1} R_{C1}}{A_{V0}} - 1\right)\left(\frac{1}{g_{m1}}\right)$

$R_{E1} = 1.53271\ k\Omega$

$R_{E2} = 72.493\ k\Omega$

$R_{in1} = R_1 // R_2 // R_i \geq 50k$

$R_i' = \frac{\beta}{g_m} + (\beta + 1) R_{E2}$

$R_i' = 141.0875\ k\Omega$

$\frac{1}{\frac{1}{50} - \frac{1}{R_i}} = \frac{R_1 R_2}{R_1 + R_2}$

$\frac{V_B}{V_{CC}} = \frac{R_2}{R_1 + R_2}$

$\frac{1}{\frac{1}{50} - \frac{1}{R_i}} = \frac{2.19149\ R_2}{3.19149}$

$0.31333 = \frac{R_2}{R_1 + R_2}$

$R_1 = 2.19149\ R_2$

$R_2 = 96.842\ k\Omega$

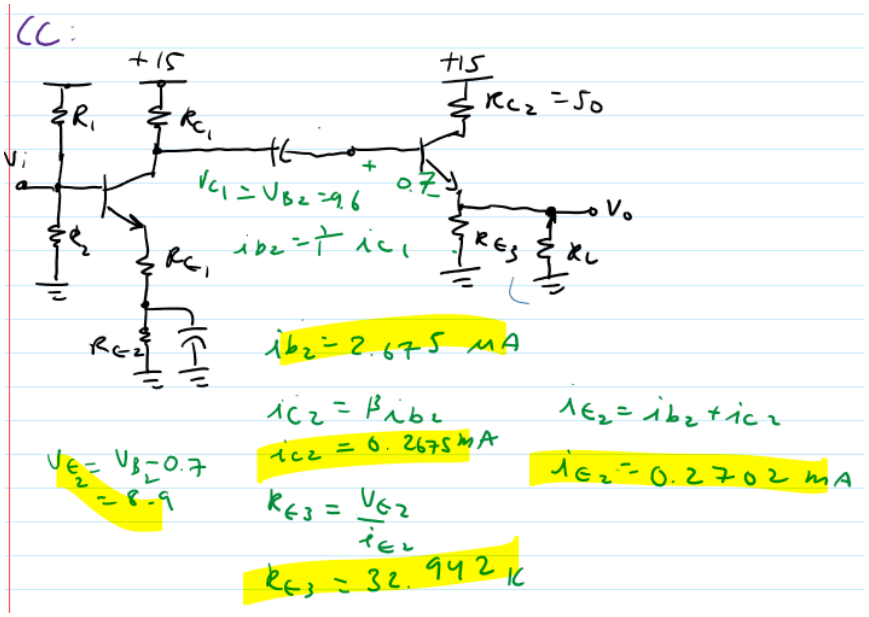
$R_1 = 212.2279\ k\Omega$

Check:

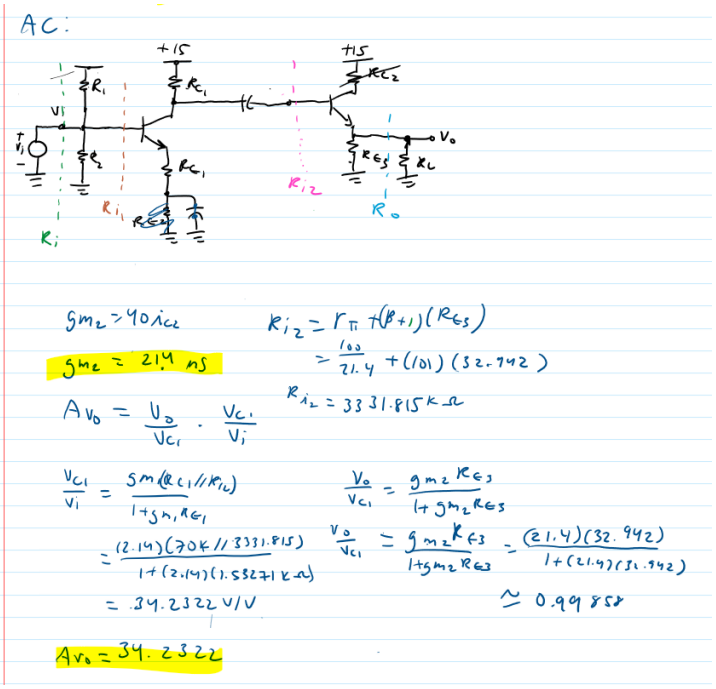
$\frac{R_1 R_2}{R_1 + R_2} = 66.4981 = \frac{1}{\frac{1}{50} - \frac{1}{R_i}}$ $\quad \frac{R_2}{R_1 + R_2} = 0.31333 = \frac{V_B}{V_{CC}}$

values valid

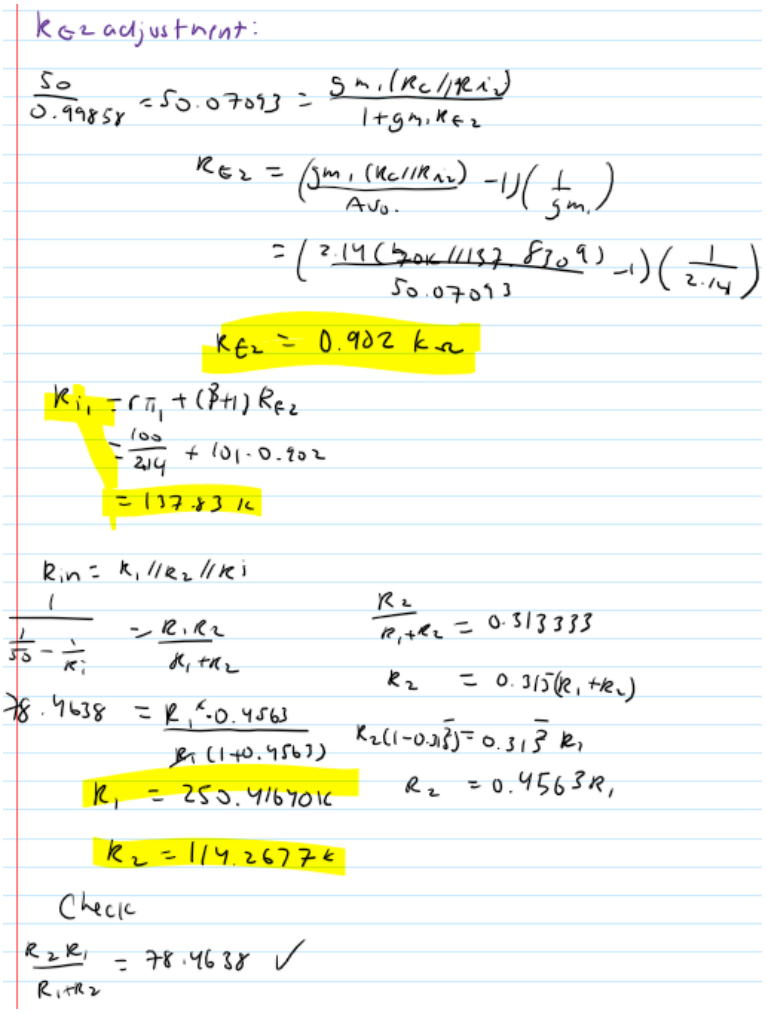
g_{m1}	R_{E1}	R_{E2}	R_1	R_2
2.14	1.53271 kΩ	72.493 kΩ	212.228 kΩ	96.842 kΩ



V_{E2}	I_{C2}	I_{E2}	I_{B2}	R_{E3}
8.9 V	0.2675 mA	0.2702 mA	2.675 uA	32.942 kΩ

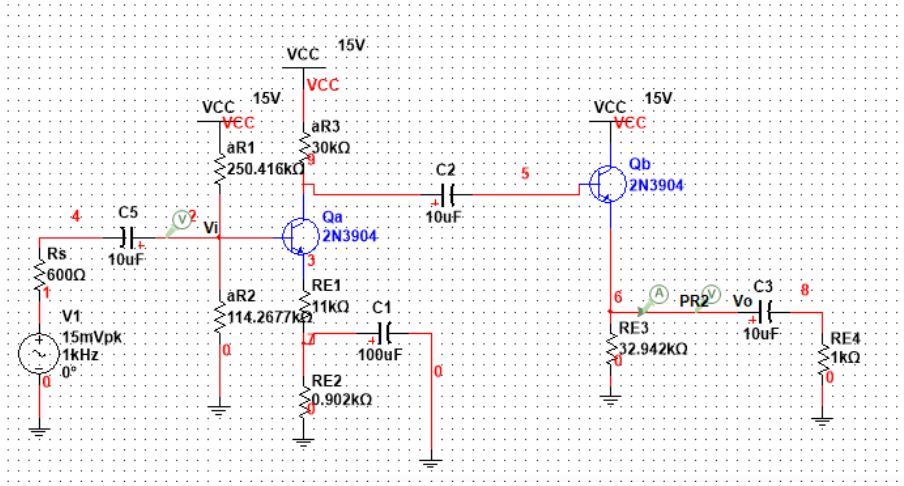


g_{m1}	A_{Vo}
2.14	34.2322 V/V



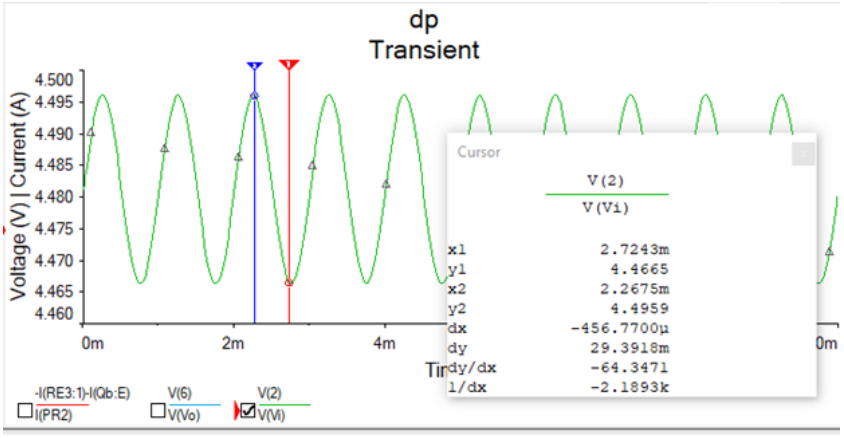
R_{E2}	R_1	R_2
0.902 kΩ	250.416 kΩ	114.268 kΩ

Final Design:

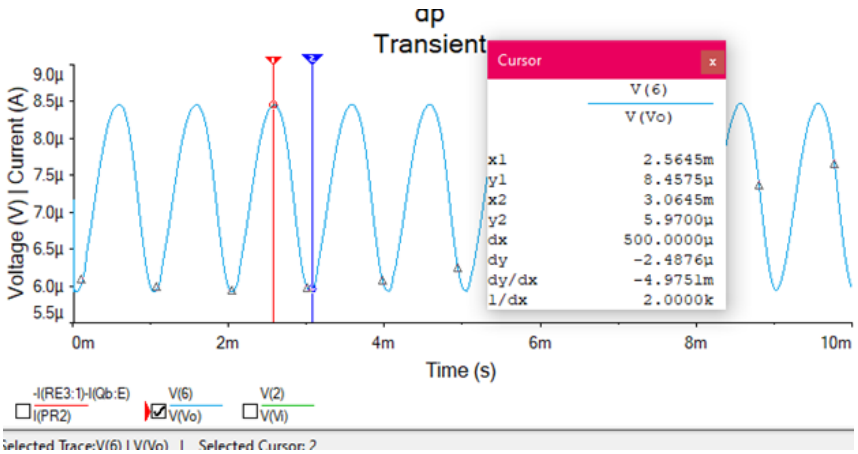


Simulation Results:

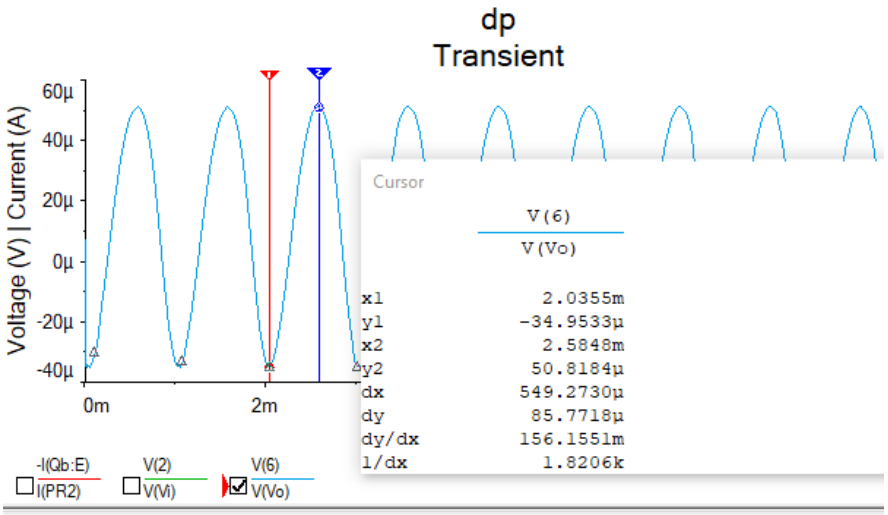
Vi



Vo (no load)



Vo (load)

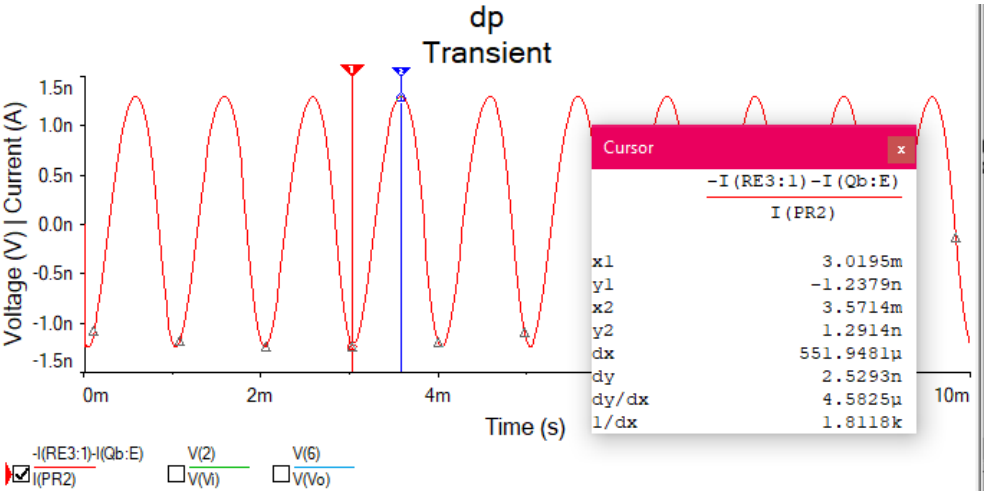


Voltage gain calculations:

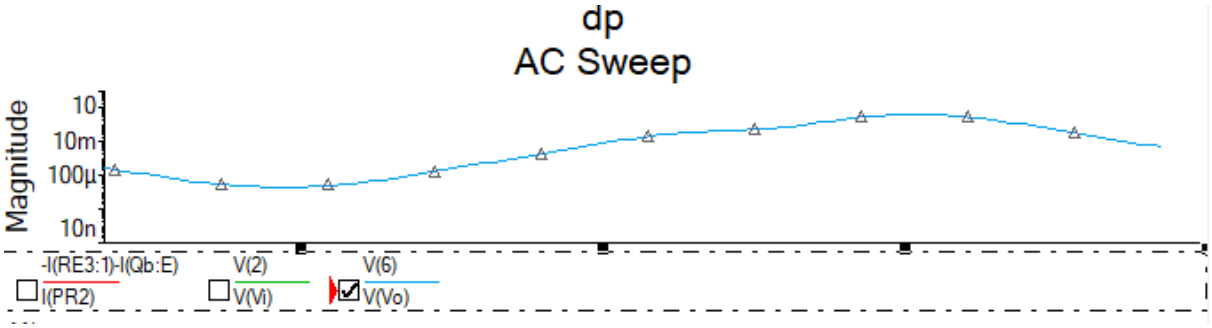
$$|A_{V_0}| = \frac{V_{opk}}{V_{ipk}} = \frac{8.4575_M}{4.4955} = 1.881 \times 10^{-6}$$

$$A_V = \frac{V_{opk}}{V_{ipk}} = \frac{50.81P4_M}{4.4955} = 1.13 \times 10^{-5}$$

The voltage gains are invalid as they differ greatly from the accepted voltage gain value. The loaded gain is over 90% smaller than the non-loaded gain.



The current drawn from the power supply remains in the 8 mA requirement.



The frequency response is invalid as it is not between the 20-50 Hz threshold.

Conclusion:

Ultimately, this project was not successful. Although some of the requirements were met, the circuit failed to maintain all of the specifications provided. These were likely due to calculation and design errors. Rounding differences could be the basis of some of these errors, however the values obtained are far beyond the acceptable scopes. In conclusion, the design project was unsuccessful.