Function Implementation and Minimization

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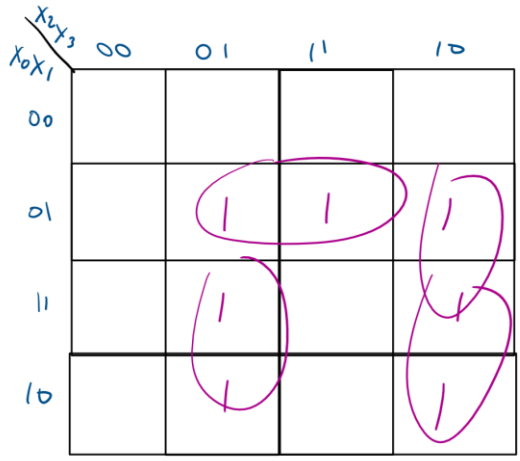
Introduction

The objective of this lab was to implement simple functions using NAND gates, and to build and test logic functions created from K maps. NAND gate implementation was discussed in the pre-lab, while the K map logic functions were implemented during the lab.

Experiment

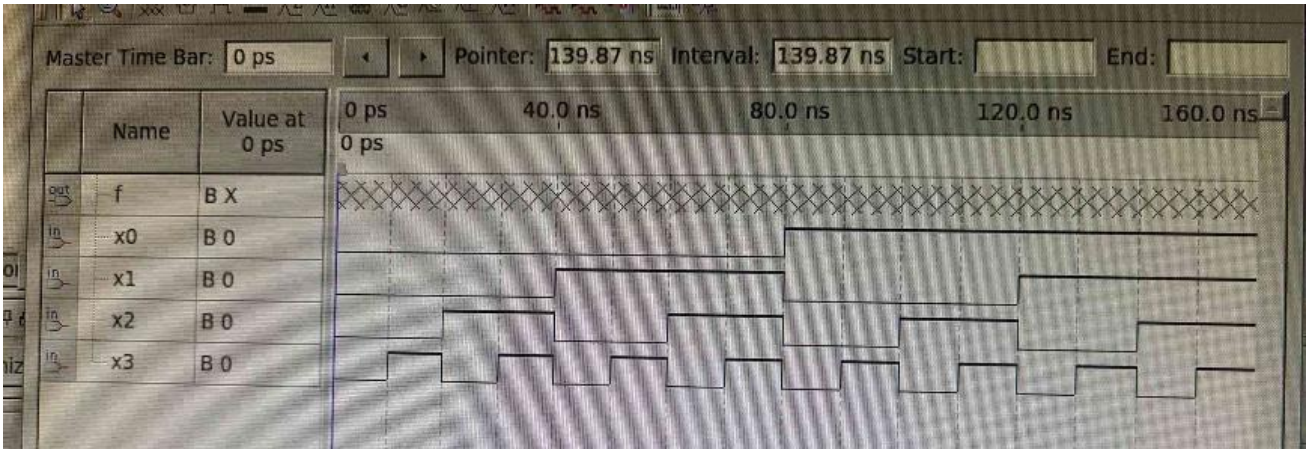
A customized function was given to base a K-map off. The K-map below represents the function F=(5,6,7,9,10,13,14).

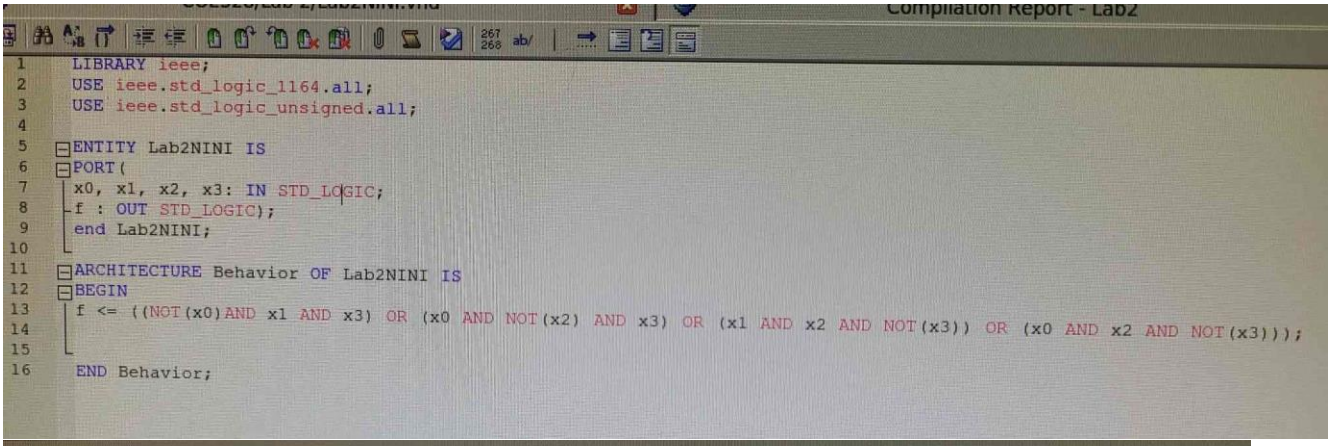


Therefore, the function should be $\overline{x}_0x_1x_3 + x_0\overline{x}_2x_3 + x_1x_2\overline{x}_3 + x_0x_2\overline{x}_3$. The truth table for the equation is below:

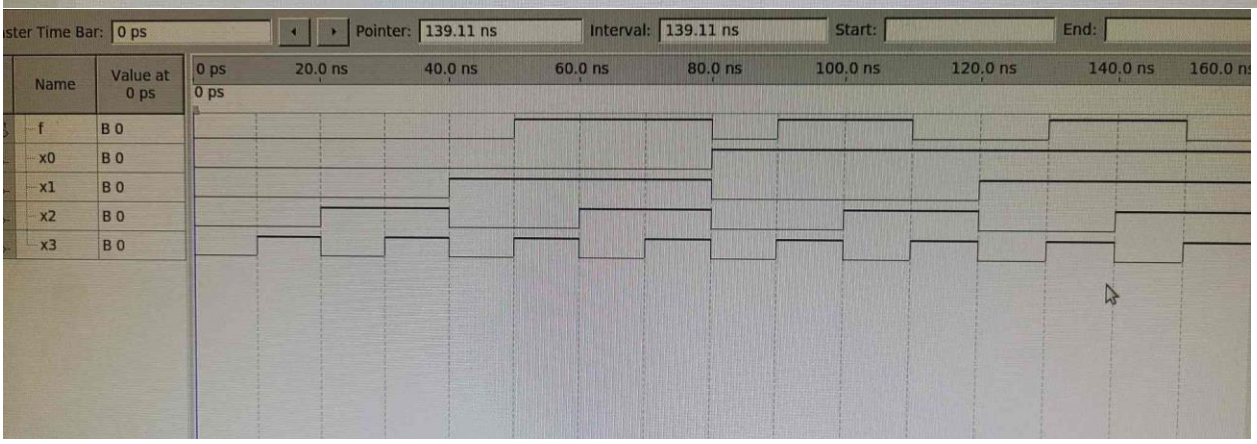
x_0	x_1	x_2	x_3	f
0	0	0	0	F
0	0	0	1	F
0	0	1	0	F
0	0	1	1	F
0	1	0	0	F
0	1	0	1	T
0	1	1	0	T
0	1	1	1	T
1	0	0	0	F
1	0	0	1	T
1	0	1	0	T
1	0	1	1	F
1	1	0	0	F
1	1	0	1	T
1	1	1	0	T
1	1	1	1	F

By inserting the function into the VHDL code from lab 1, a waveform was generated. The output matched the expected results calculated from the truth table.





```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.all;
3   USE ieee.std_logic_unsigned.all;
4
5   ENTITY Lab2NINI IS
6   PORT(
7    x0, x1, x2, x3: IN STD_LOGIC;
8    f : OUT STD_LOGIC);
9    end Lab2NINI;
10
11  ARCHITECTURE Behavior OF Lab2NINI IS
12  BEGIN
13   f <= ((NOT(x0) AND x1 AND x3) OR (x0 AND NOT(x2) AND x3) OR (x1 AND x2 AND NOT(x3)) OR (x0 AND x2 AND NOT(x3)));
14
15
16   END Behavior;
```



Conclusion

Initially, the final output was didn't match the truth table, however that was the result of mixing up the input values. Once the correct input values matched the input variable the output became the expected values.