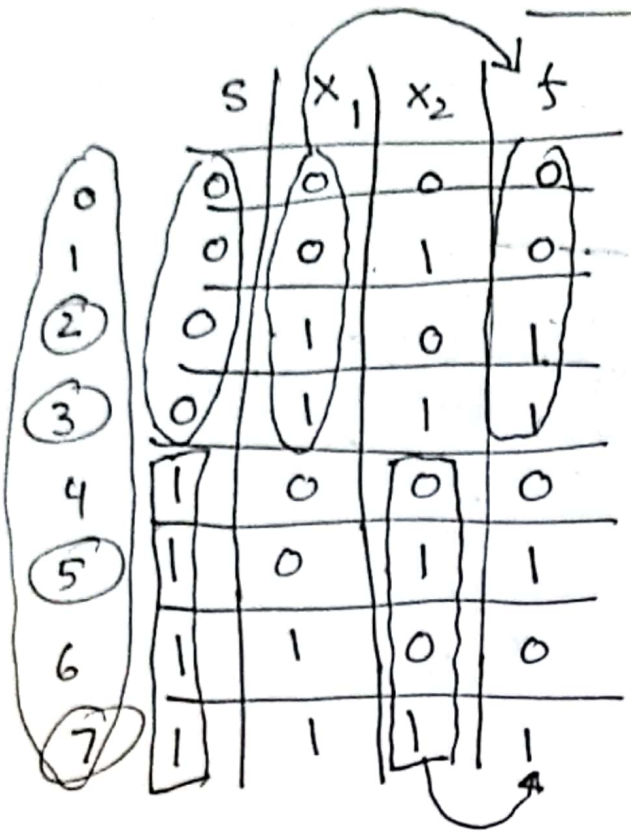
Multiplexer

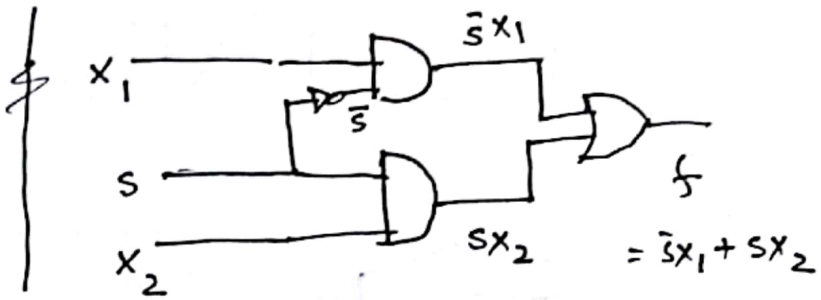


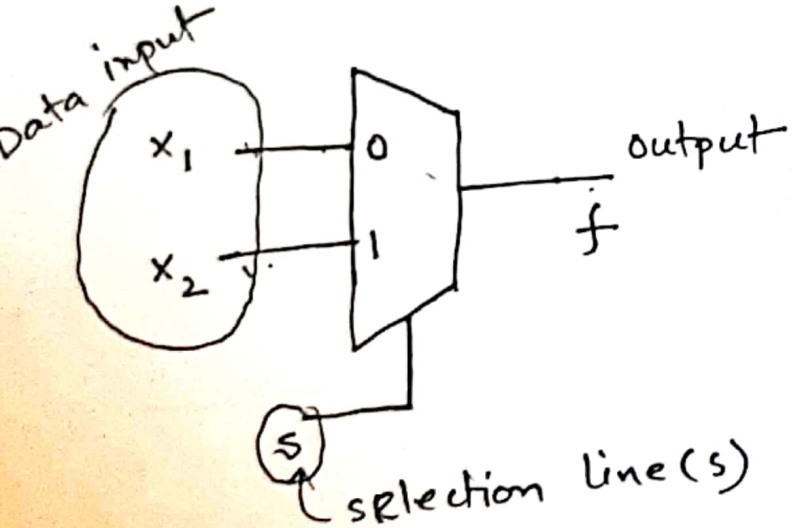
SOP $f = \Sigma m(2, 3, 5, 7)$

$f = \bar{S} x_1 \bar{x}_2 + \bar{S} x_1 x_2 + S \bar{x}_1 x_2 + S x_1 x_2$

$= \bar{S} x_1 (\bar{x}_2 + x_2) + S x_2 (\bar{x}_1 + x_1)$

$= \bar{S} x_1 + S x_2$





Multiplexer

2^n → input

(n) → selection line

1 → output

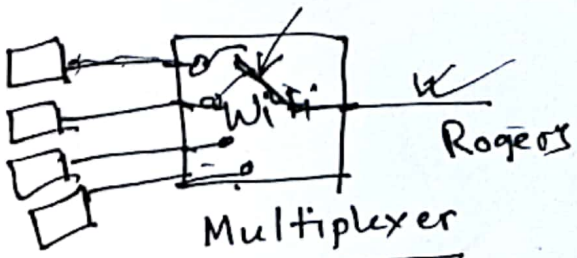
n → 1 — 2X1.

$2^1 \rightarrow 2$

n → 2

$2^2 \rightarrow 4$ — 4X1

8X1

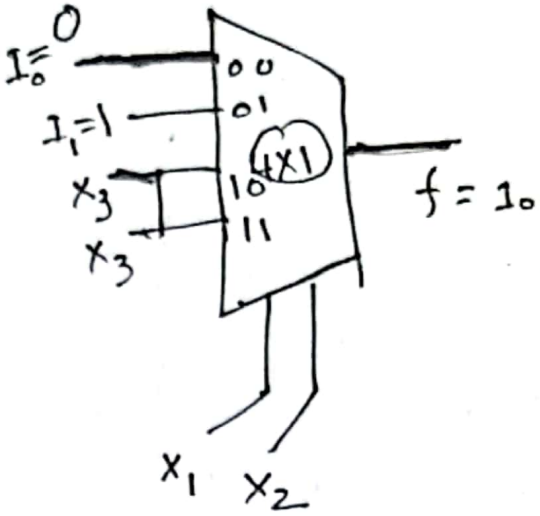


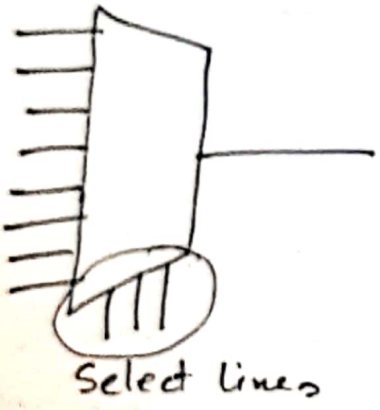
Multiplexer

16X 1

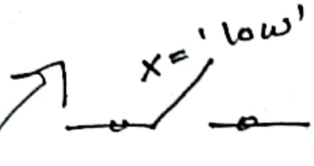
selection → data I/P

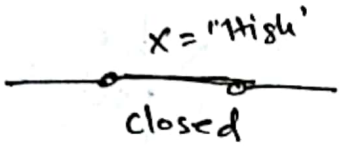
x_1	x_2	x_3	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



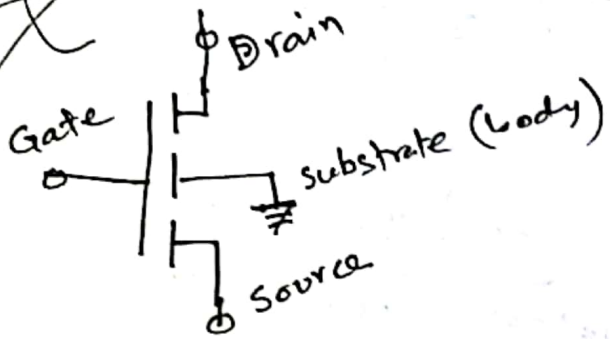


Implementation Technology

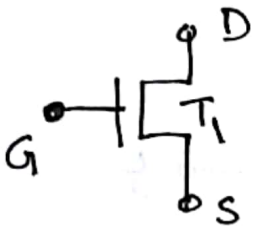




MOSFET
- NMOS
- PMOS



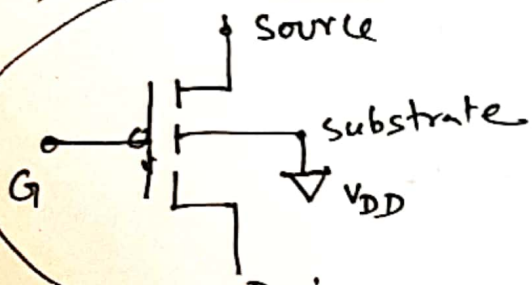
NMOS

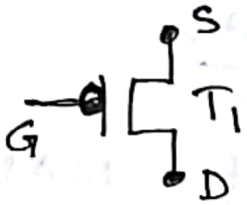


Simple NMOS

G	T_1
High	ON
low	OFF

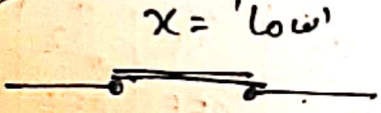
T_1





PMOS

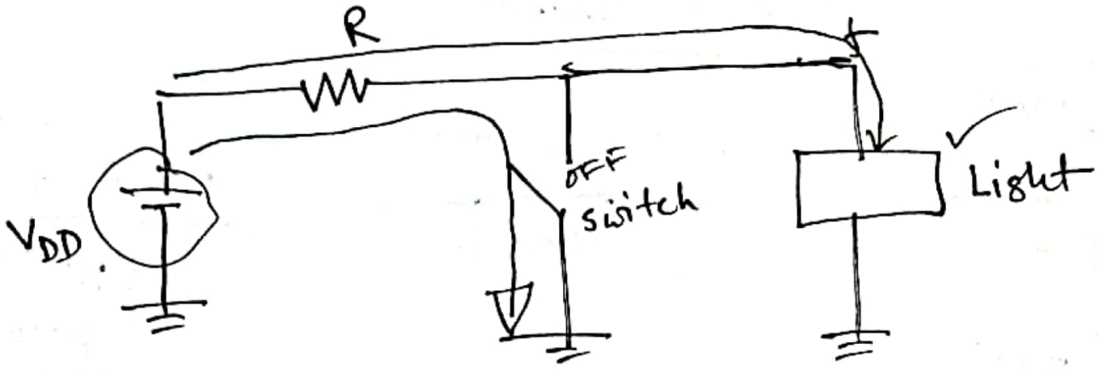
G	T_1
High	OFF
Low	ON

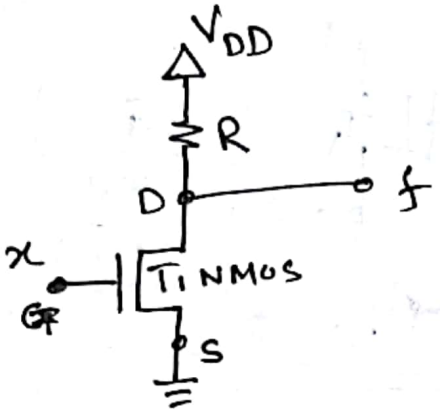


switch = closed

x = "High"

switch = open

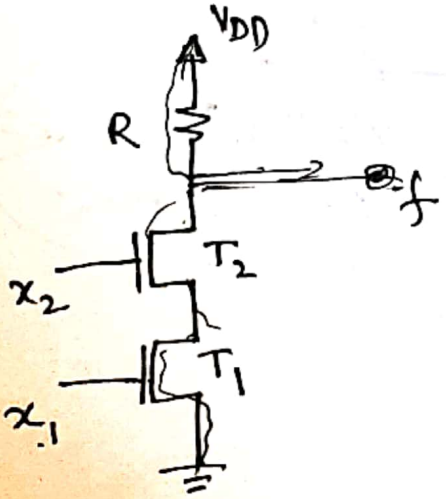




NOT gate

x	T_1	f
0 = Low	OFF	1
1 = High	ON	0

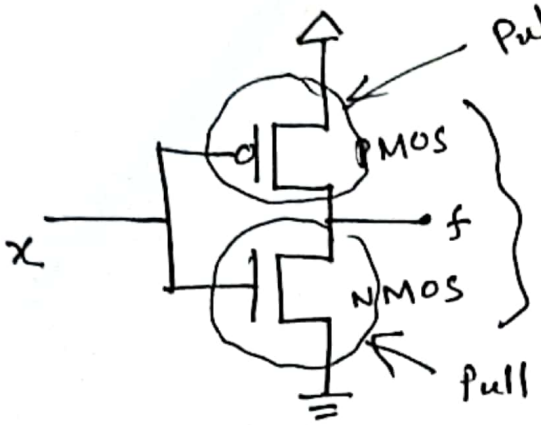
Implement NAND gate with NMOS



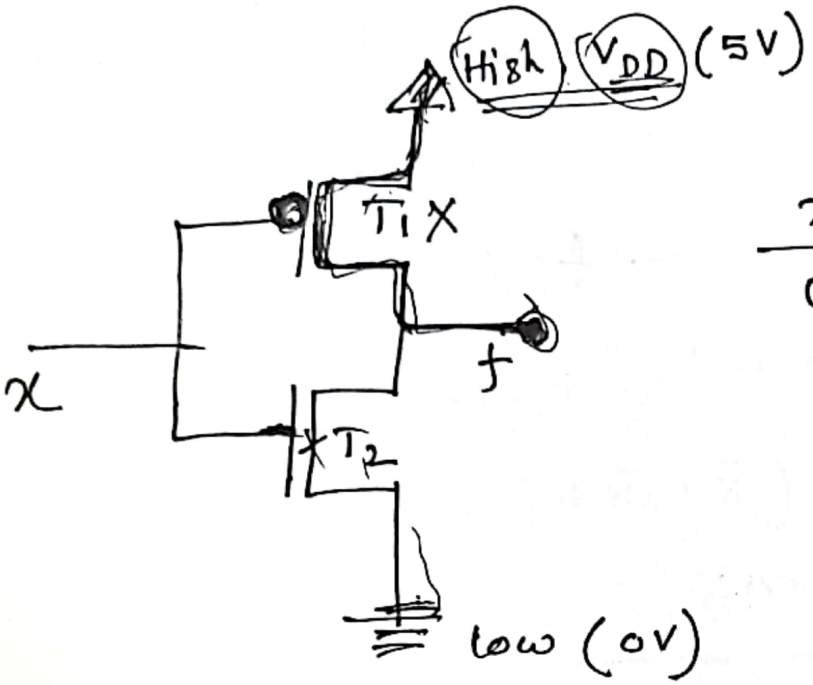
x_1	x_2	T_1	T_2	f
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

NAND

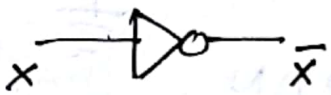
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0



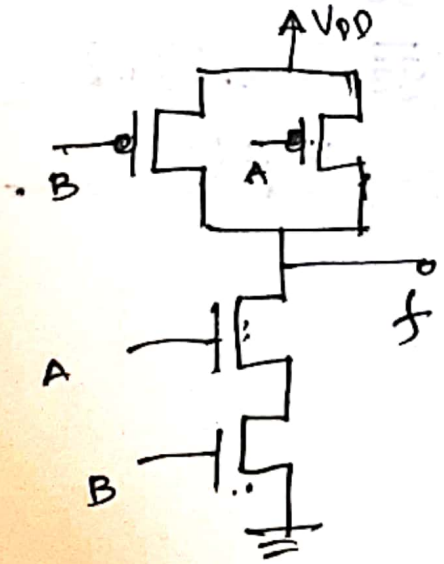
CMOS = PMOS + NMOS



x	PMOS T_1	NMOS T_2	f
0	ON	OFF	1
1	OFF	ON	0



Implement NAND gate with CMOS



NAND gate

How to design PUN,

$f = \overline{A \cdot B}$

$= \bar{A} + \bar{B}$.

↑ Parallel

How to design PDN

$\bar{f} = \overline{\overline{A \cdot B}} = A \cdot B$.

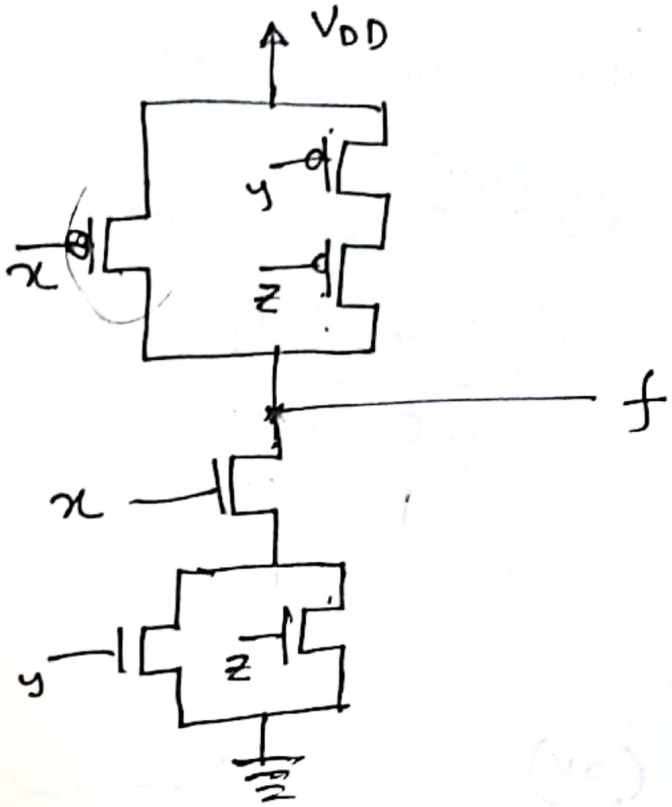
↑ series

~~AND~~

$f = \bar{x} + \bar{y}\bar{z}$

↑ parallel ↑ series

PUN

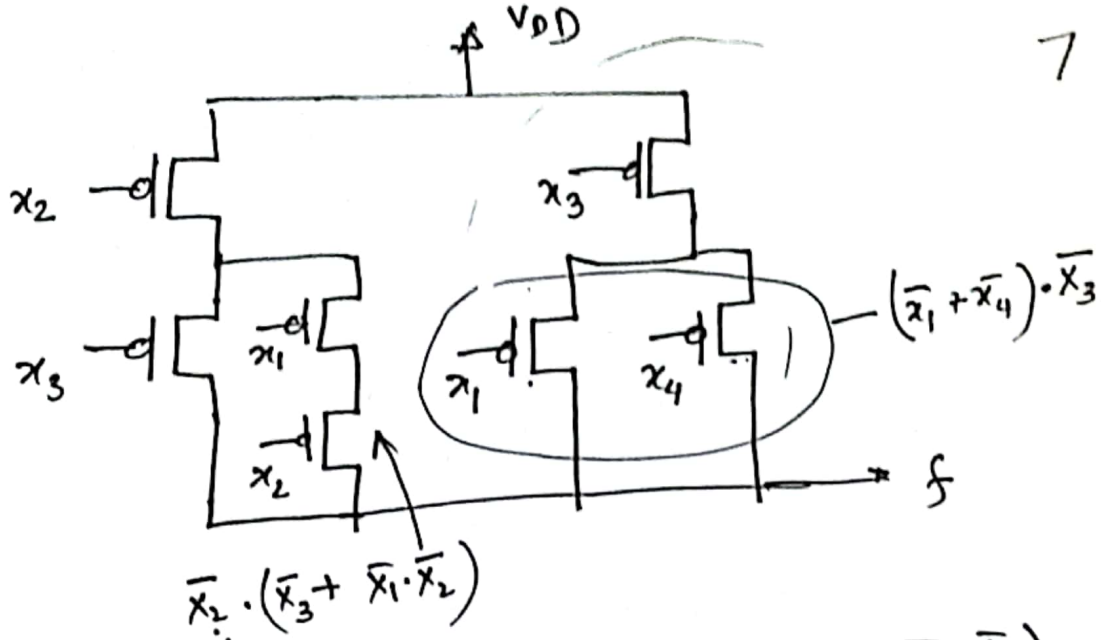


PDN

$$\bar{f} = \overline{\bar{x} + \bar{y}\bar{z}}$$

$$= \bar{\bar{x}} \cdot \overline{\bar{y}\bar{z}} = x \cdot (\bar{\bar{y}} + \bar{\bar{z}})$$

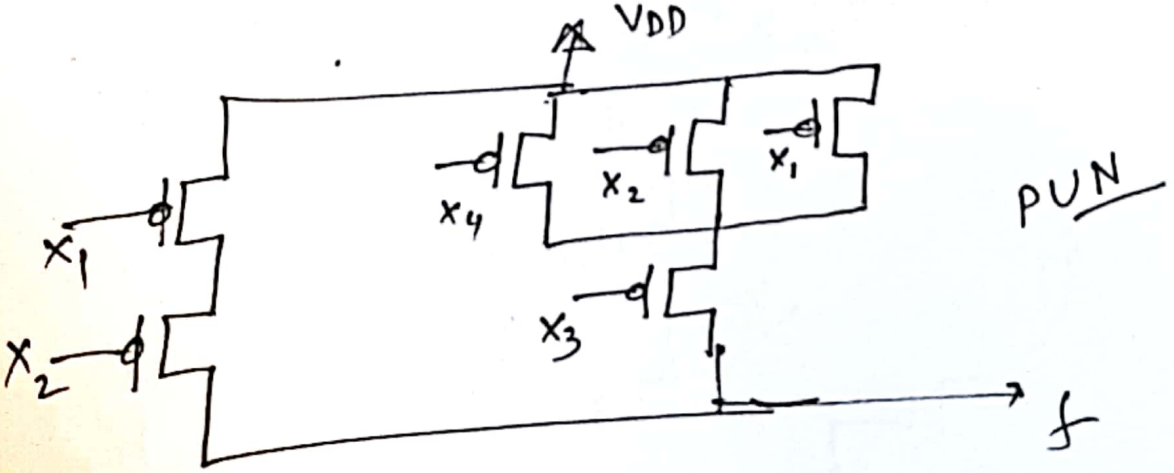
$$= x(y + z)$$



$$f = (\bar{x}_1 + \bar{x}_4)\cdot\bar{x}_3 + \bar{x}_2\cdot(\bar{x}_3 + \bar{x}_1\cdot\bar{x}_2)$$

$$= \bar{x}_1\cdot\bar{x}_3 + \bar{x}_3\cdot\bar{x}_4 + \bar{x}_2\cdot\bar{x}_3 + \bar{x}_1\cdot\bar{x}_2$$

$$= \bar{x}_3(\bar{x}_1 + \bar{x}_4 + \bar{x}_2) + \bar{x}_1\cdot\bar{x}_2$$



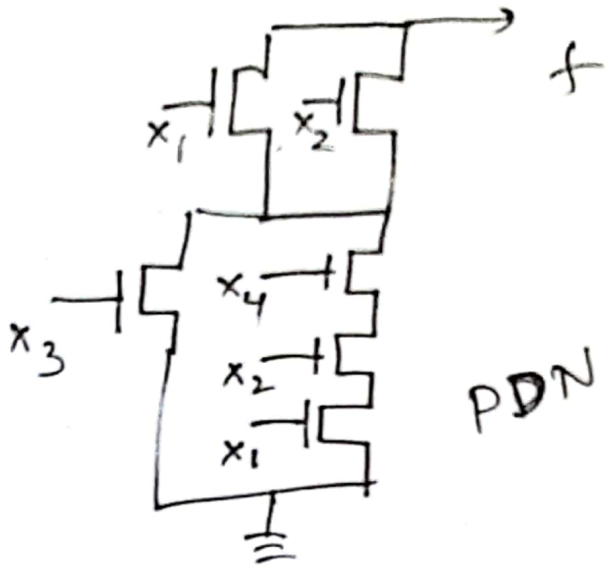
$$\bar{f} = \overline{\bar{x}_3(\bar{x}_1 + \bar{x}_2 + \bar{x}_4) + \bar{x}_1\cdot\bar{x}_2}$$

$$= \overline{\bar{x}_3\cdot(\bar{x}_1 + \bar{x}_2 + \bar{x}_4)}\cdot\overline{\bar{x}_1\bar{x}_2}$$

$$= \left[\bar{\bar{x}}_3 + \overline{(\bar{x}_1 + \bar{x}_2 + \bar{x}_4)}\right]\cdot(\bar{\bar{x}}_1 + \bar{\bar{x}}_2)$$

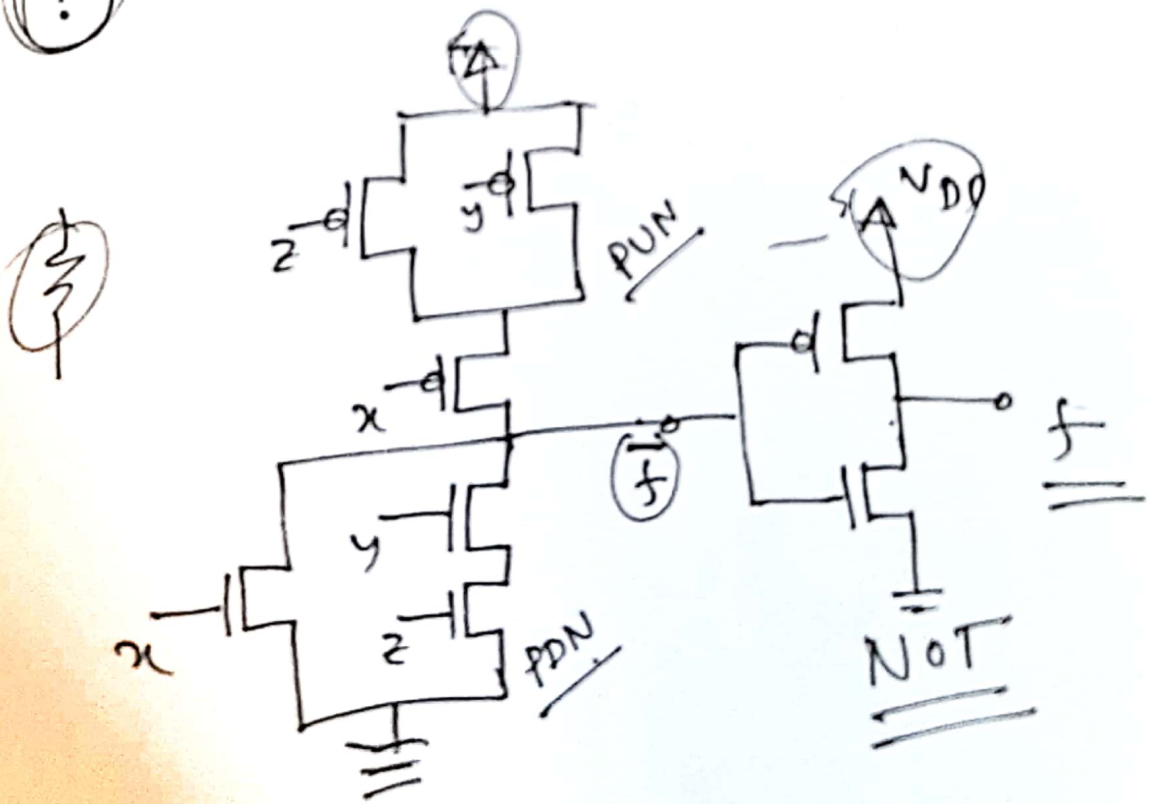
$$= \left[x_3 + (\bar{\bar{x}}_1\cdot\bar{\bar{x}}_2\cdot\bar{\bar{x}}_4)\right]\cdot(x_1 + x_2)$$

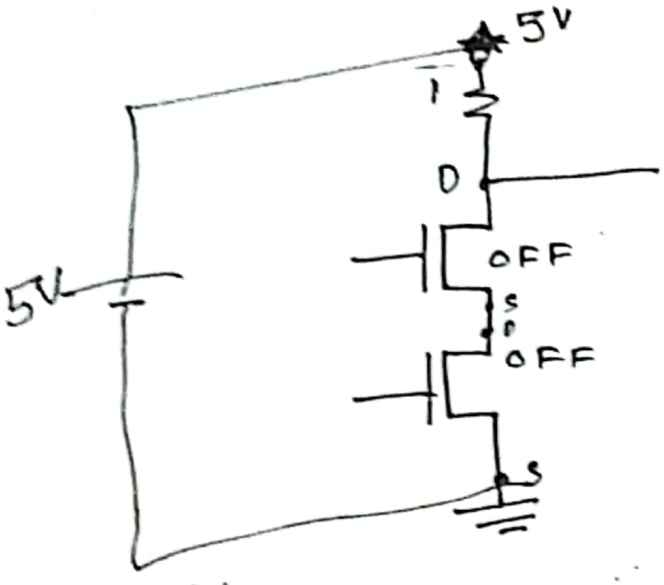
$$\bar{f} = \left[x_3 + (x_1x_2x_4)\right]\cdot(x_1 + x_2)$$



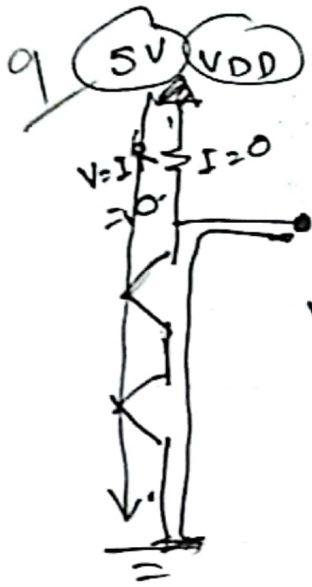
$F = x + yz$

$\overline{F} = \overline{x + yz} = \bar{x} \cdot (\overline{yz}) = \bar{x} \cdot (\bar{y} + \bar{z})$





9

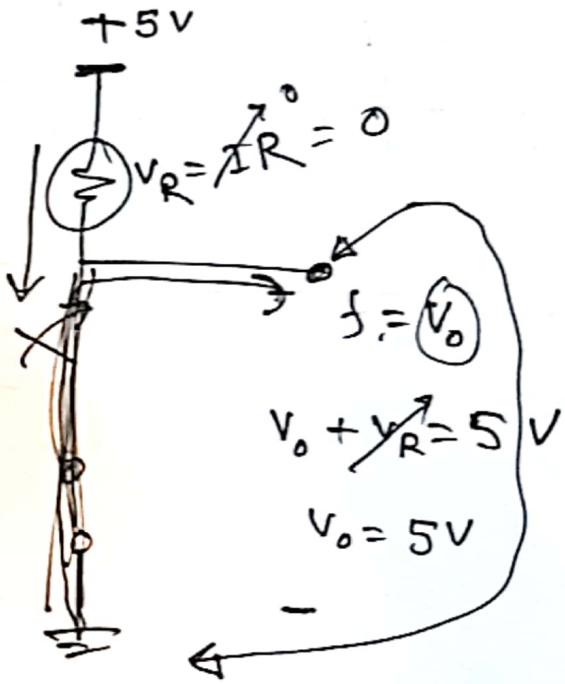


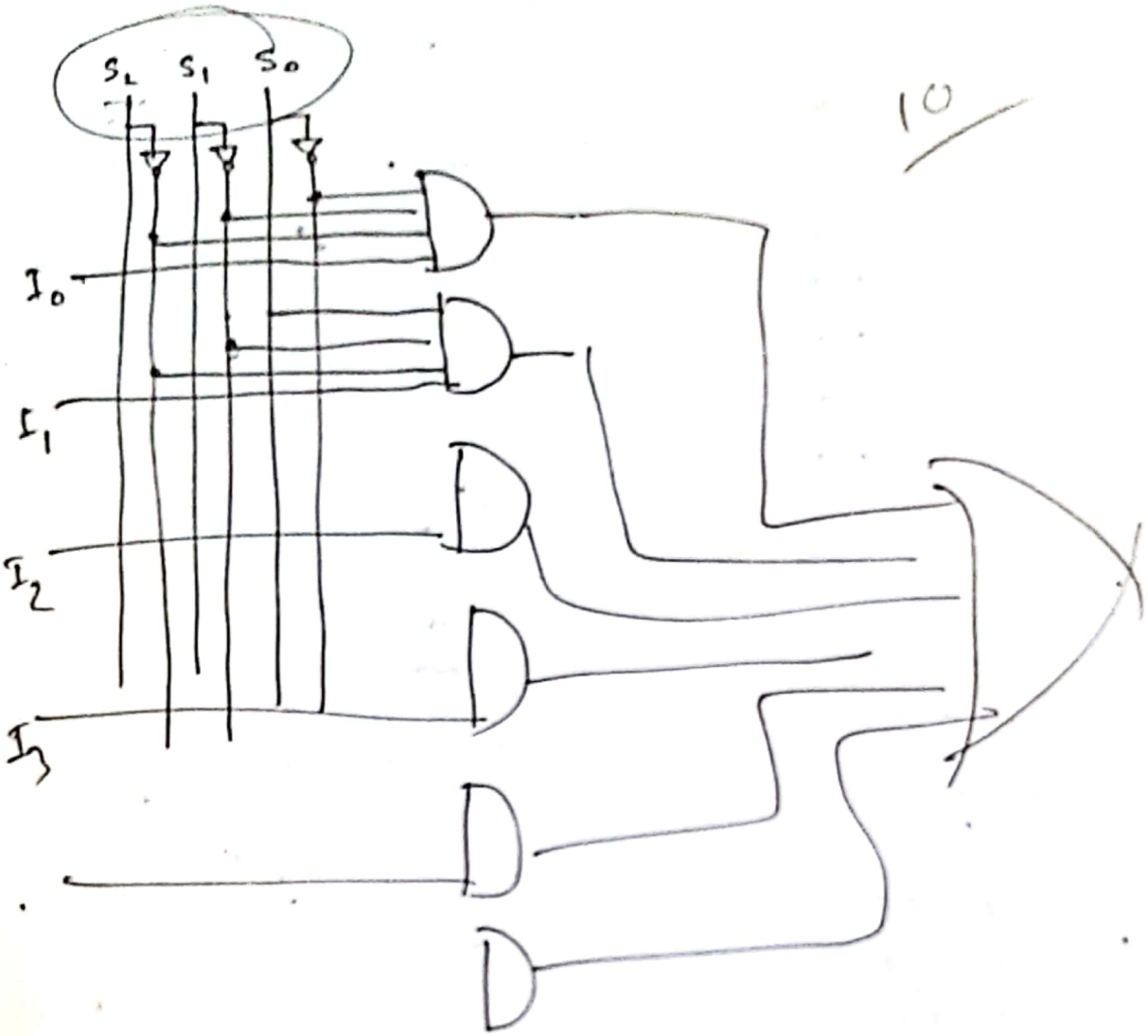
$V_f + 0 = V_{DD}$

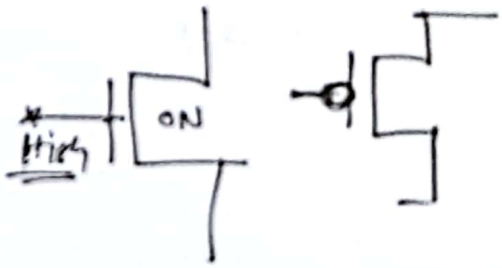
$V_f = V_{DD} = 1$ V

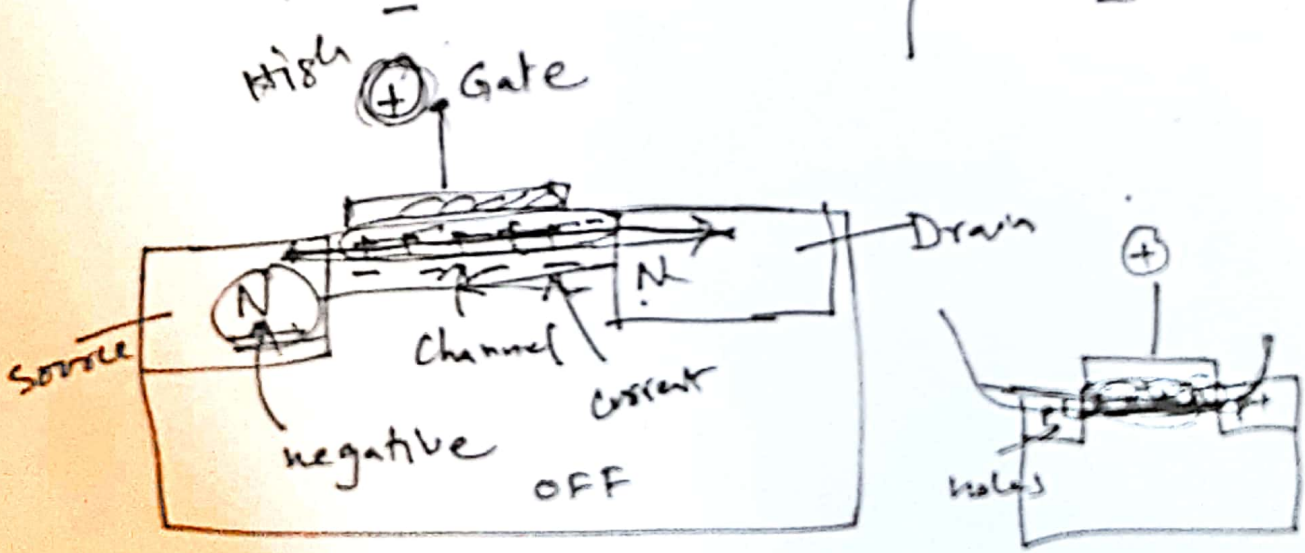
S → 0 V / 1 V

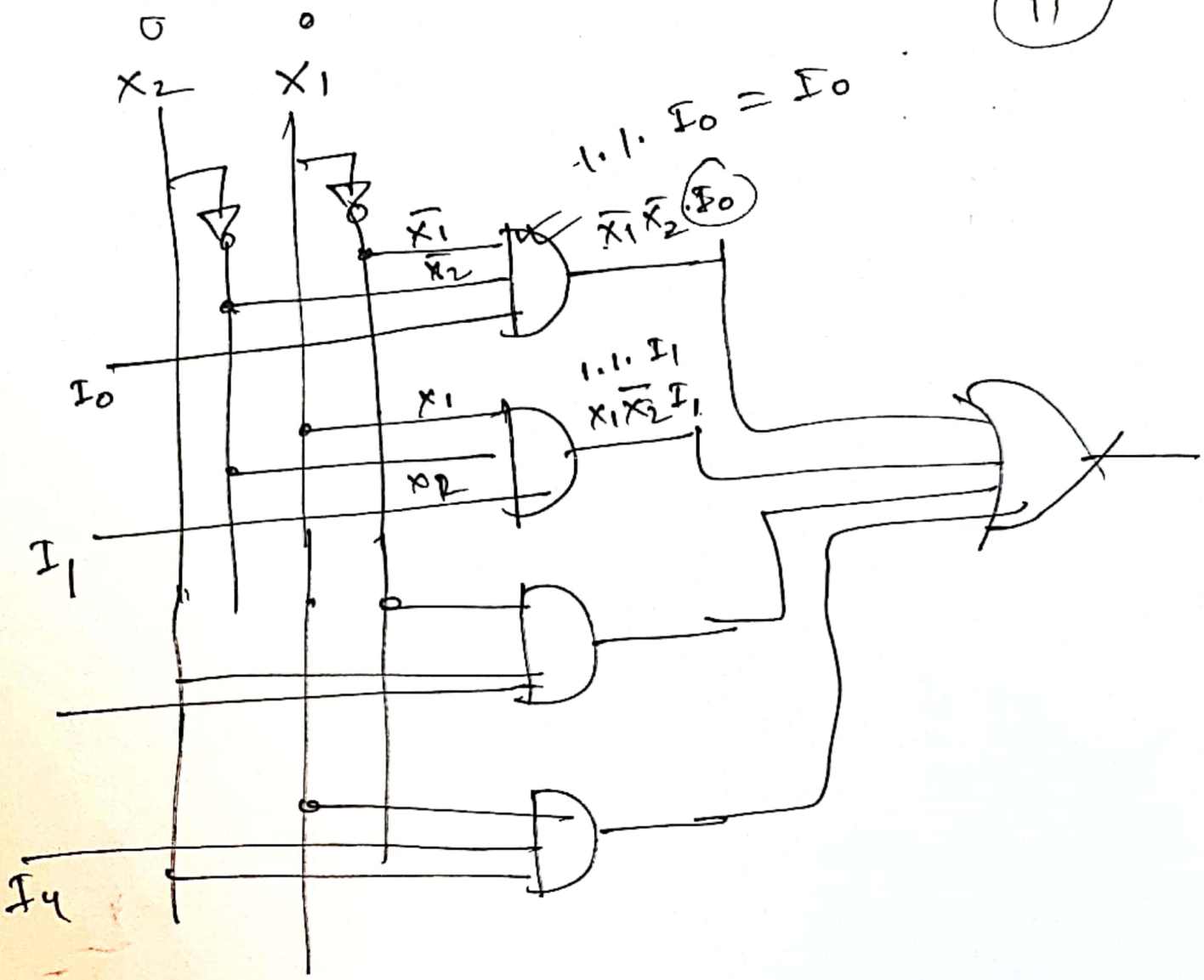
$S_1\ S_2$ → 00, 01, 10, 11




S2
S1
S0
I0
I1
I2
I3


ON
High


High
Gate
Drain
N
N
Source
Channel
current
negative
OFF
holes


0
0
X_2
X_1
1.1. $I_0 = I_0$
$\bar{X}_1$
$\bar{X}_2$
$\bar{X}_1\bar{X}_2 I_0$
I_0
1.1. I_1
X_1
$X_1\bar{X}_2 I_1$
X_2
I_1
I_4