Adder and Subtractor Unit

COE 328-022 Pei Yang

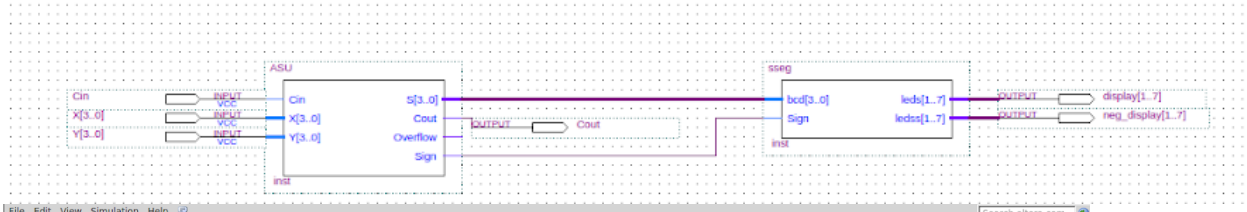
Oct 11 2022

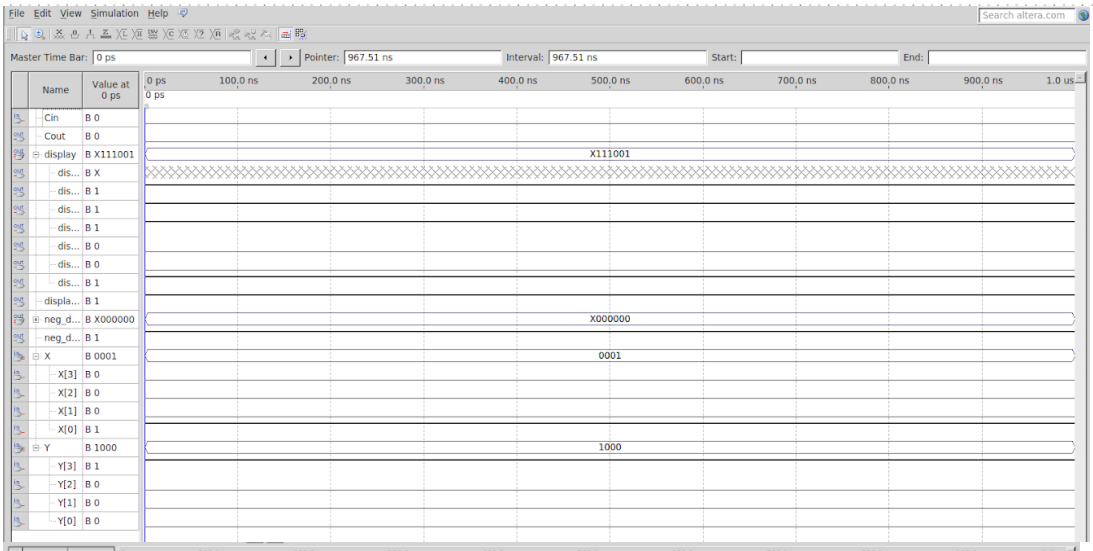
Introduction

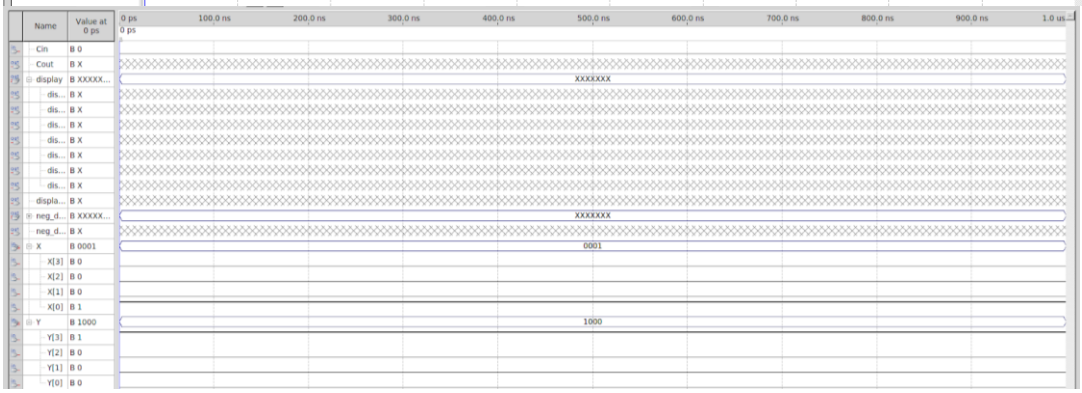
The objective of this lab was to design an adder/subtracter unit using VHDL code and block diagrams that would add or subtract values depending on a Cin input. The experiment was split into two parts.

Experiment

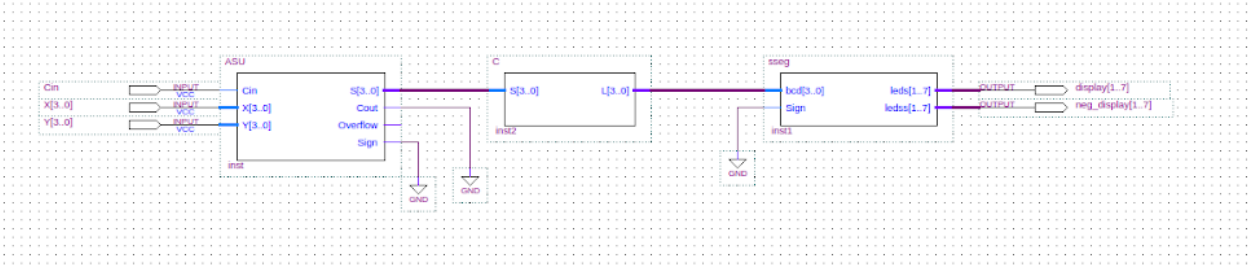
Part A:

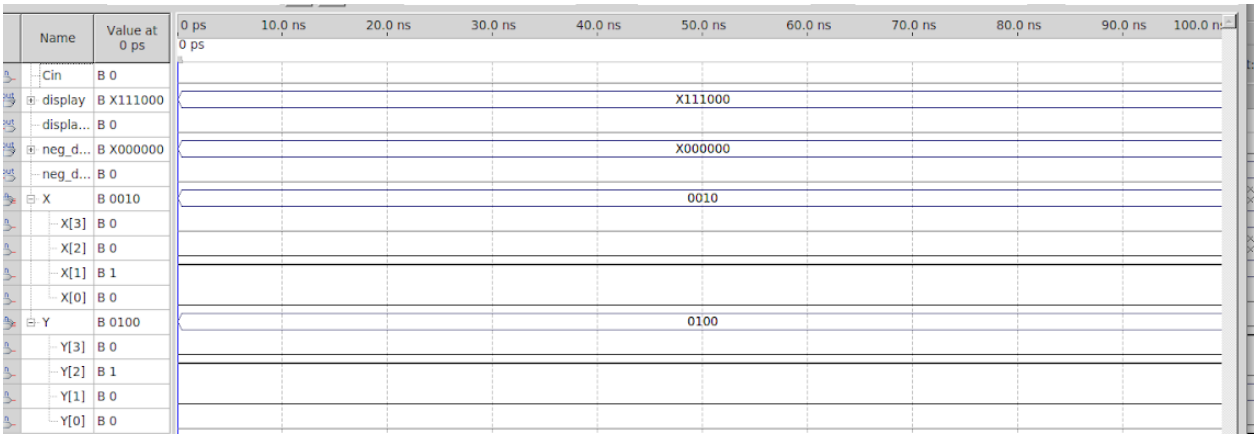






Part B:






```
library ieee;
USE ieee.std_logic_1164.all;

ENTITY C IS
PORT(
   S : IN STD_logic_vector(3 DOWNTO 0);
    L : OUT STD_logic_vector(3 DOWNTO 0)
    );
END C;

ARCHITECTURE Behavior OF C IS
BEGIN
                L(3) <= (S(3) AND NOT S(2) AND NOT S(1) AND S(0));
    L(2) <= (S(3) AND NOT S(2) AND NOT S(1) AND NOT S(0)) OR (S(3) AND NOT S(2) AND NOT S(1) AND NOT S(0)) OR (NOT S(3) AND S(2) AND S(1));
    L(1) <= (NOT S(3) AND S(2) AND S(0)) OR (NOT S(3) AND S(2) AND S(1));
    L(0) <= (NOT S(3) AND NOT S(1)) OR (NOT S(3) AND NOT S(2) AND S(0)) OR (NOT S(3) AND S(2) AND S(1) AND NOT S(0)) OR (S(3) AND NOT S(2) AND NOT S(1));
END Behavior;
```

Conclusion

In part B, the circuit output the sum of two numbers, to a maximum of 9. This number corresponds a digit in our student numbers. Initially, we expected the waveform output to resemble the actual sum of the numbers and thought there was an error in our file. Eventually, we realized the waveform output matched a digit to our student numbers, not the actual sum of the input numbers.