COE 608 Lab 1

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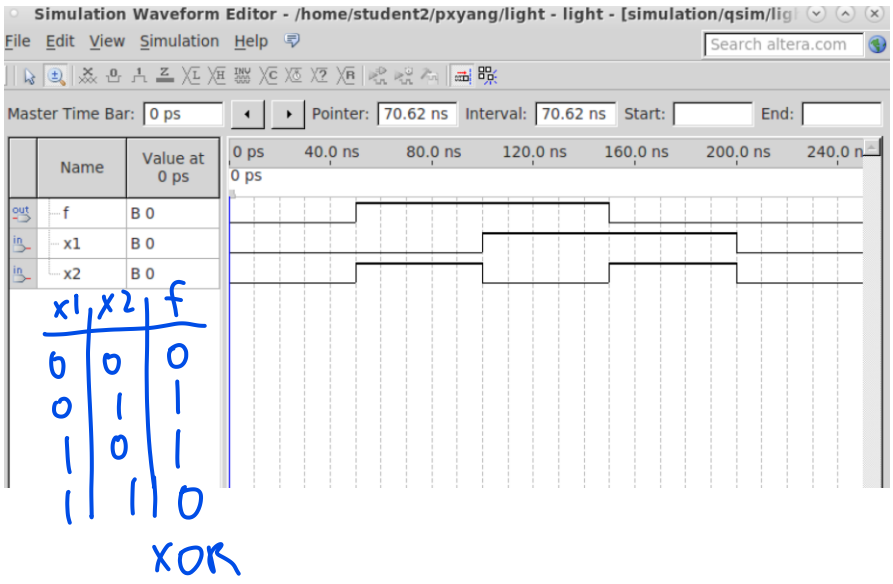
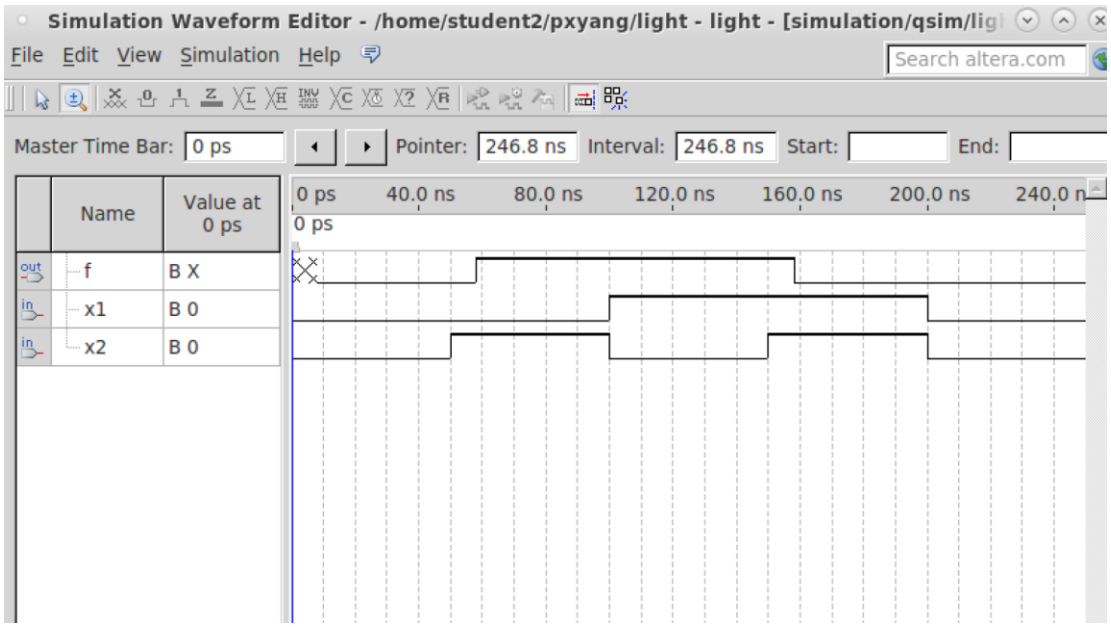
light.vhd | Compilation Report - light

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.all;
3  ENTITY light IS
4      PORT (x1,x2: IN STD_LOGIC; f: OUT STD_LOGIC);
5  END light;
6  ARCHITECTURE LogicFunction OF light IS
7  BEGIN
8  f <= (x1 AND NOT x2) OR (NOT x1 AND x2);
9  END LogicFunction ;
```

Functional Simulation



Timing Simulation



The output is slightly delayed due to logic elements and wires in the FPGA device