VHDL for Sequential Circuits

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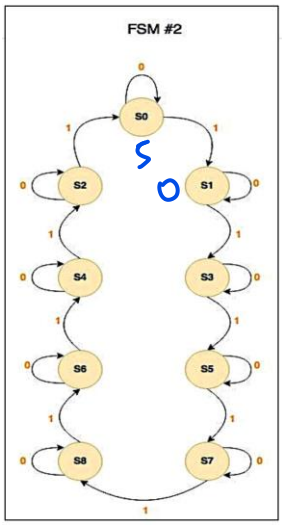
Pre Lab:

The machine given was a mealy FSM # 2.

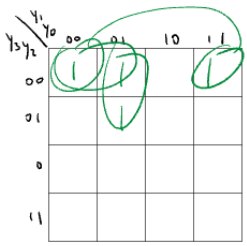


State/State Assigned table:

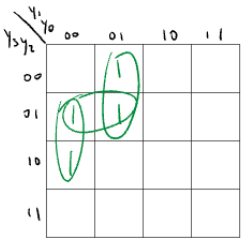
present state	next state w=0	next state w=1	output w=0	output w=1
S_0	S_0	S_1	d_1	d_2
S_1	S_1	S_3	d_2	d_3
S_2	S_2	S_0	d_9	d_1
S_3	S_3	S_5	d_3	d_4
S_4	S_4	S_2	d_8	d_9
S_5	S_5	S_7	d_4	d_5
S_6	S_6	S_4	d_7	d_8
S_7	S_7	S_8	d_5	d_6
S_8	S_8	S_6	d_6	d_0

	present state $Y_3Y_2Y_1Y_0$	next state $Y_3Y_2Y_1Y_0$ w=0	next state w=1	output $Z_3Z_2Z_1Z_0$ w=0	output w=1
S_0	0000	0000	0001	d_1	d_2
S_1	0001	0001	0011	d_2	d_3
S_3	0011	0011	0101	d_9	d_1
S_5	0101	0101	0111	d_3	d_4
S_7	0111	0111	1000	d_8	d_9
S_8	1000	1000	0110	d_4	d_5
S_6	0110	0110	0100	d_7	d_8
S_4	0100	0100	0010	d_5	d_6
S_2	0010	0010	0000	d_6	d_0

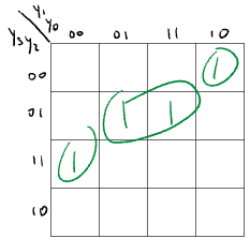
w = 1



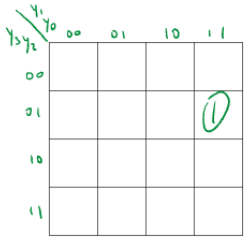
$Y_0 = \bar{Y}_3\bar{Y}_2\bar{Y}_1 + \bar{Y}_3\bar{Y}_2 + \bar{Y}_3\bar{Y}_1Y_0$



$Y_1 = \bar{Y}_3\bar{Y}_1Y_0 + \bar{Y}_3Y_2\bar{Y}_1 + \bar{Y}_1\bar{Y}_0$

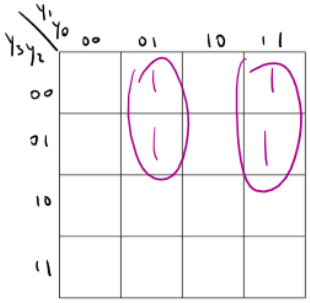


$Y_2 = Y_3\bar{Y}_2\bar{Y}_1\bar{Y}_0 + \bar{Y}_3Y_2 + \bar{Y}_3\bar{Y}_2Y_1Y_0$

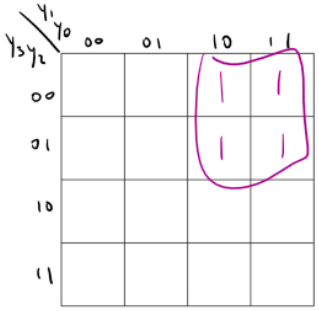


$Y_3 = \bar{Y}_3Y_2Y_1Y_0$

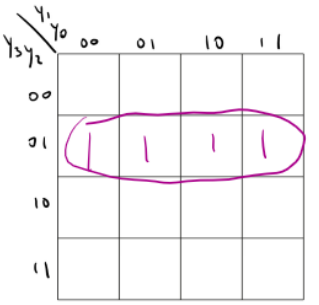
w = 0



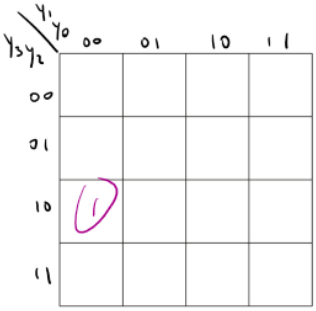
$Y_0 = \bar{Y}_3Y_1\bar{Y}_0 + \bar{Y}_3Y_1Y_0$



$Y_1 = \bar{Y}_3Y_1$



$Y_2 = \bar{Y}_3Y_2$



$Y_3 = Y_3\bar{Y}_2\bar{Y}_1\bar{Y}_0$

Logic Diagram: