Finite State Machine

Q1. The state table of a finite-state machine (FSM) with one input w and 2 outputs z_1 and z_0 is given below:

State table

Present State	Next State $w=0$	Next State $w=1$	Output z_1	Output z_0
S0 00	S2 10	S1 01	0	0
S1 01	S2 10	S1 01	0	1
S2 10	S2 10	S3 11	1	0
S3 11	S1 01	S3 11	0	0

(a) Explain weather the given FSM is a Moore-type or Mealy-type state machine?

(b) The given FSM is to be implemented as a synchronous sequential circuit with T flip-flops using the state assignments: S0=00, S1=01, S2=10, S3=11. Derive the equations for the inputs to the T flip-flops, and the equations for the outputs z_1 and z_0.

Present state $y_1 y_0$ | Next state $w=0$: $Y_1 Y_0$, $T_1 T_0$ | Next state $w=1$: $Y_1 Y_0$, $T_1 T_0$ | output z_1 | output z_0

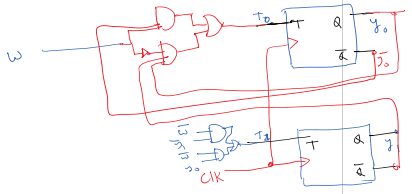
State-assigned table & excitation table

For T_1

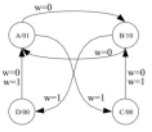
$T_1 = \bar{w} y_1 + w \bar{y}_0$

For T_0

$T_0 = w \bar{y}_0 + \bar{w} \bar{y}_1 y_0$



Q2. The state diagram for a finite state machine (FSM) with one input w and two outputs z2 and z1 is given below:



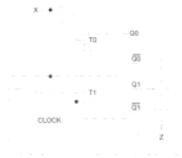
(a) Does the above state diagram use a Moore or Mealy-type model to represent the FSM? Explain your answer.

(b) What is the minimum number of state variables required to represent the sates.

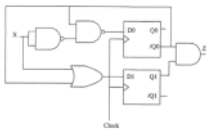
(c) Using the state-assignment: A=00, B=01, C=11, and D=10, develop the next state and output equation for implemenenting the FSM.

Q3. In the circuit below:

(a) Is the design a Moore or Mealy Model?
(b) Derive the state table assuming the states are: S0=00, S1=01, S2=10, S3=11.
(c) Draw the state diagram showing the state, input, and output.

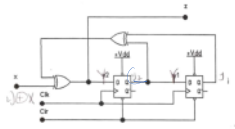


Q4. Consider the following circuit which implements a finite-state machine (FSM):



(a) Derive the state assigned table for the FSM.
(b) Complete the following timing diagram for the circuit by assuming Q1=Q0=0 at the beginning.
(c) Derive the state assigned table if JK flip-flops (instead of D flip-flops) are to be used to implement the FSM.

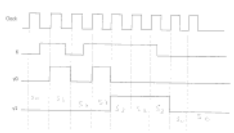
Q5. Given the following logic circuit, derive its state table and state diagram. If the following sequence 10101101001 is applied to the x input of the circuit with initial state 01, determine the resulting output sequence on z output.

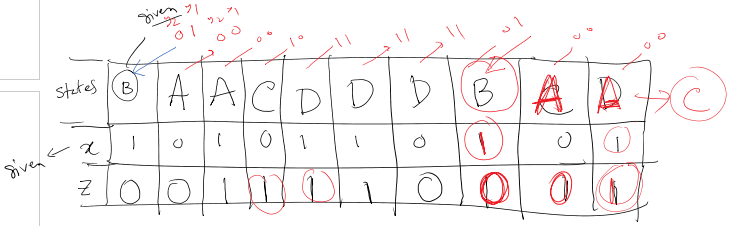


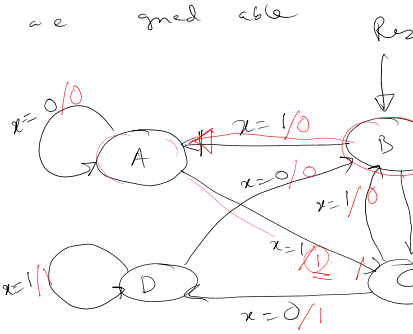
logic equation

Q6. Given is the following timing diagram, clock signal, and input waveforms:

a) Derive the state-assigned table.
b) Draw the state diagram.
c) Derive the circuit that implement the FSM.







Mealy machine

given Y_2 for odd no of (1)

$Y_2 = y_2 \oplus y_1 \oplus x$

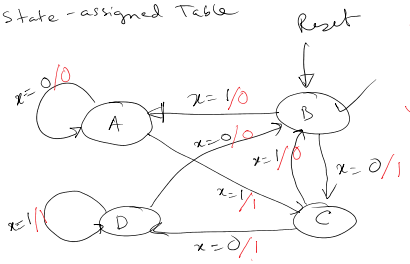
$Y_1 = y_2$

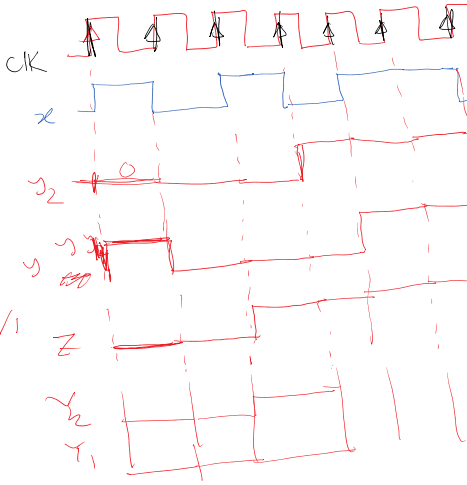
$z = Y_2 = y_2 \oplus y_1 \oplus x$

Present state $y_2\ y_1$	Next state $x=0$ $Y_2\ Y_1$	Next state $x=1$ $Y_2\ Y_1$	output Z $x=0$	output Z $x=1$
A 0 0	0 A	1 0 C	0	1
B 0 1	0 C	0 0 A	1	0
C 1 0	1 D	0 1 B	1	0
D 1 1	0 B	1 1 D	0	1

State-assigned Table

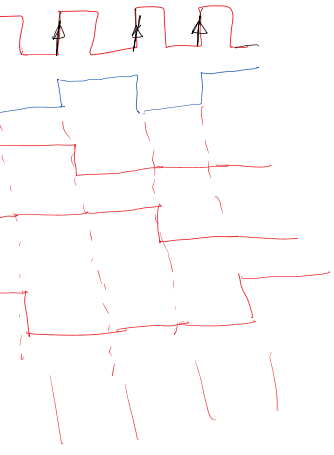
x	y_1	y_2	Y_2
0	0	0	0
0	0	1	1
0	1	0	1





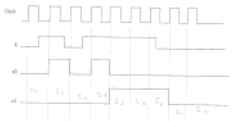
ut

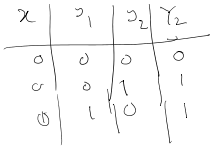
x = 0/1

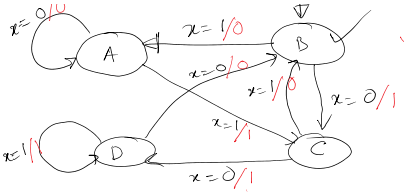


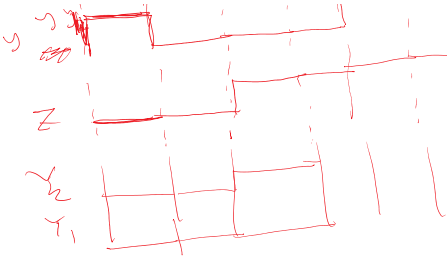
Q6. Given is the following timing diagram, clock signal, and input waveforms:

a) Derive the state-assigned table.
b) Draw the state diagram.
c) Derive the circuit that implement the FSM.









Given the following logic circuit, clock signal, and input waveforms:

a) Derive the state-assigned table
b) Sketch the waveforms for Q1, Q2, Y1, and Y2 in the space provided.
Note: Assume zero delay for all gates and flip-flops.

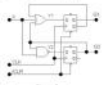


Figure 1

$$Y_1 = X + \overline{Q_1} + Q_2$$

$$Y_2 = \overline{X} \cdot \overline{Q_2}$$

$Q_1\,Q_2$	X=0	X=1
0 0	1 1	1 1
0 1	1 0	1 1
1 0	1 1	0 1
1 1	1 1	0 1