Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Ele 404
Course Number:	ELE404-042
Semester/Year	2023 Spring Sem

Instructor:	Sandeep Kaler

Assignment/Lab Number:	Lab 5
Assignment/Lab Title:	Wave Shaping Circuits

Submission Date	June 13th, 2023
Due Date:	June 13th, 2023

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
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Gohir	Usba	501014491	04	Usba Gohir

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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Introduction:

To capture the voltage-current characteristics of a diode, one can employ a diode to produce waveforms that meet the desired specifications. The diode achieves this by altering the input signals.

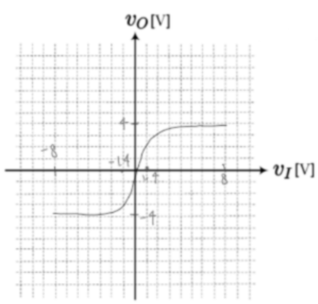
Objectives:

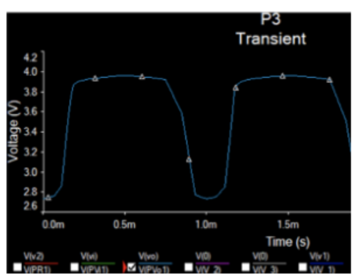
The purpose of this laboratory experiment was to examine the impact of the quantity of resistors and capacitors connected to diodes on the waveform of the output voltage. Additionally, the objective was to gain insight into the voltage-current behavior of a diode within a non-linear circuit.

Pre-lab:

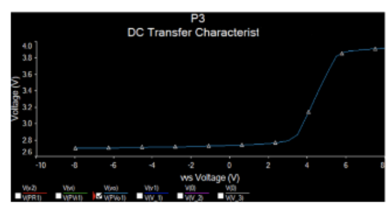
Usba:

PART1:





OUTPUT VOLTAGE WAVEFORM



INPUT OUTPUT TRANSFER CHARACTERISTICS

PART 2
a.) and b.)

R1 & R2 = 3.4 kΩ

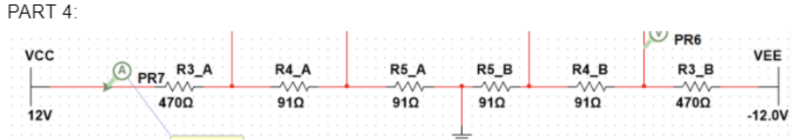
Rt = R2/ (R2 + R1)

Rt = 3.4 / (3.4 + 3.4)
=0.5kΩ

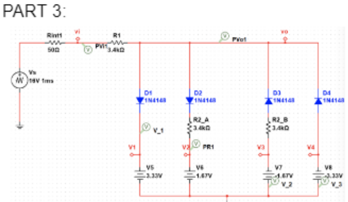
Therefore the resistors are 3.4kΩ

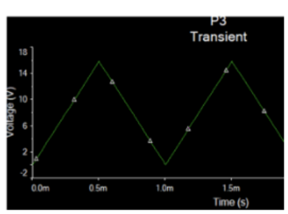
c.)
I = Vbias/ R
= 1.67 / 3.4
= 0.49 mA

PART 4:



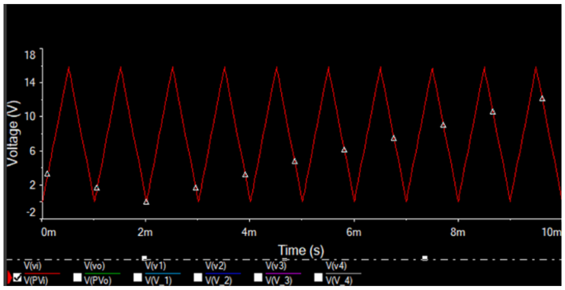
PART 3:

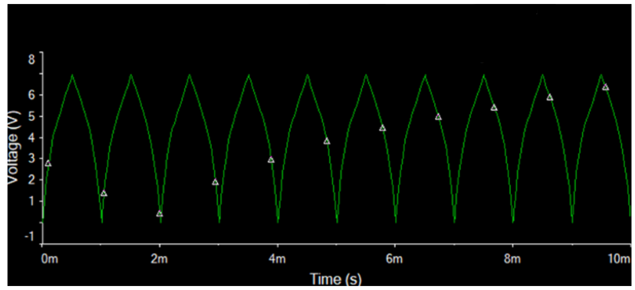


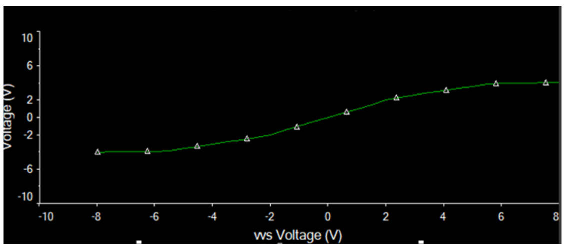


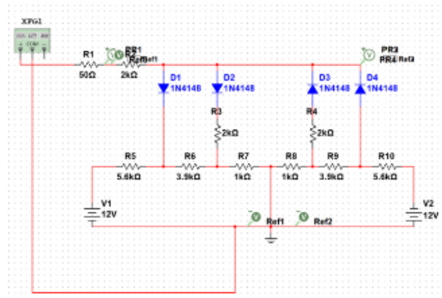
INPUT VOLTAGE WAVEFORM

P5:

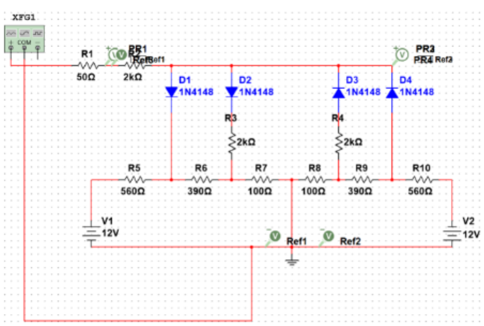

Voltage (V)
Time (s)
V(vi)
V(vo)
V(v1)
V(v2)
V(v3)
V(v4)
V(PVi)
V(PVo)
V(V_1)
V(V_2)
V(V_3)
V(V_4)

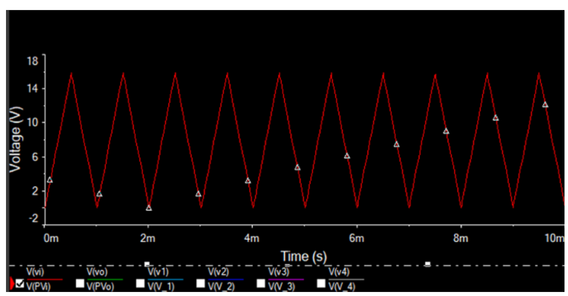

Voltage (V)
Time (s)

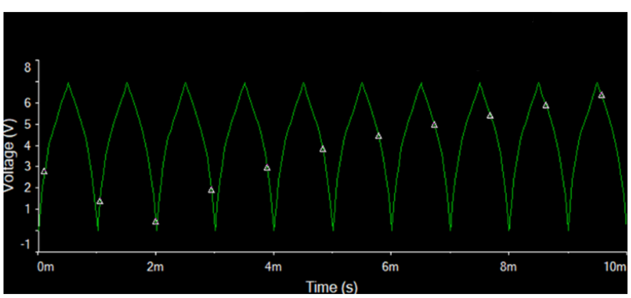

Voltage (V)
vvs Voltage (V)

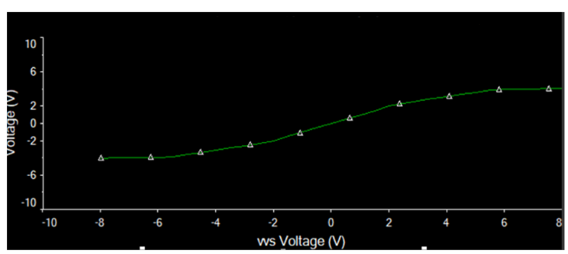

XFG1
R1
50Ω
R2
2kΩ
PR1
PR2
D1
1N4148
D2
1N4148
D3
1N4148
D4
1N4148
R3
2kΩ
R4
2kΩ
R5
5.6kΩ
R6
3.9kΩ
R7
1kΩ
R8
1kΩ
R9
3.9kΩ
R10
5.6kΩ
V1
12V
V2
12V
Ref1
Ref2

P6:

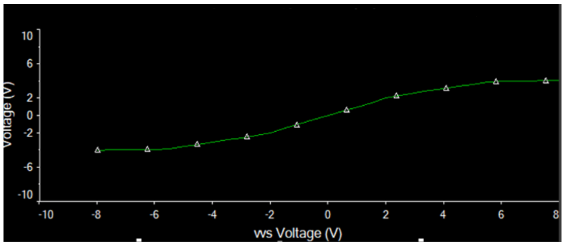

XFG1
R1
50Ω
R2
2kΩ
PR1
PR2
D1
1N4148
D2
1N4148
D3
1N4148
D4
1N4148
R3
2kΩ
R4
2kΩ
R5
560Ω
R6
390Ω
R7
100Ω
R8
100Ω
R9
390Ω
R10
560Ω
V1
12V
V2
12V
Ref1
Ref2

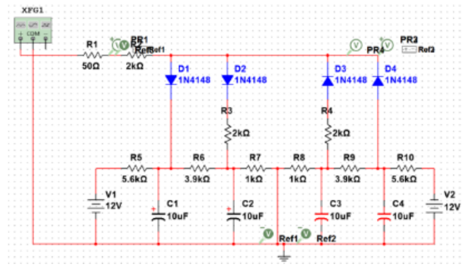

Voltage (V)
Time (s)
V(vi)
V(vo)
V(v1)
V(v2)
V(v3)
V(v4)
V(PVi)
V(PVo)
V(V_1)
V(V_2)
V(V_3)
V(V_4)

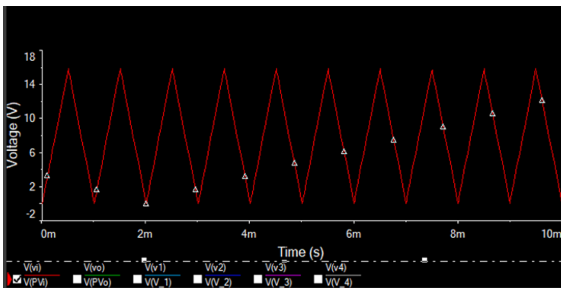

Voltage (V)
Time (s)

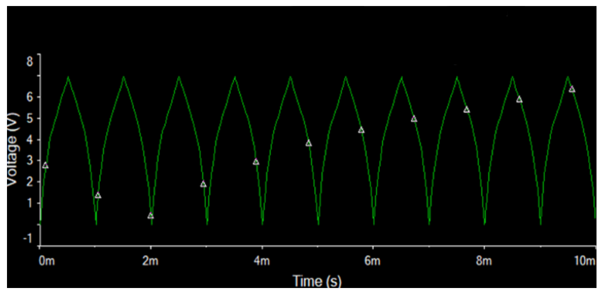

Voltage (V)
vvs Voltage (V)

P7:


Voltage (V)
vs Voltage (V)

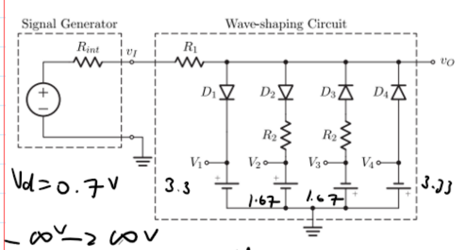

XFG1
R1
50Ω
2kΩ
D1
1N4148
D2
1N4148
D3
1N4148
D4
1N4148
R3
2kΩ
R4
2kΩ
R5
5.6kΩ
R6
3.9kΩ
R7
1kΩ
R8
1kΩ
R9
3.9kΩ
R10
5.6kΩ
V1
12V
V2
12V
C1
10uF
C2
10uF
C3
10uF
C4
10uF
Ref1
Ref2


Voltage (V)
Time (s)
V(vi)
V(vo)
V(v1)
V(v2)
V(v3)
V(v4)
V(PVi)
V(PVo)
V(V_1)
V(V_2)
V(V_3)
V(V_4)


Voltage (V)
Time (s)

Nini:

1.



$V_d = 0.7V$

$-\infty V \to \infty V$

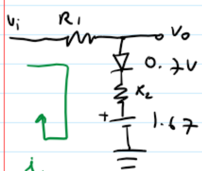
$V_I =$

$-\infty < V_i < 1.67$

OFF: D_1, D_2, D_3, D_4

$1.67 < V_i < 3.3$

ON: D_2



$\frac{R_1}{R_1+R_2} = 0.8$

$R_1 = R_2 = 2K$

$-2.5 + i\,2K\Omega + 0.7V + i\,2K\Omega + 1.67 = 0$

$4K\,i = 2.5 - 1.67 - 0.7$

$i = 0.0475\ mA$

$V_0 = 1.67 + 0.7 - 2K \cdot i$

$= 2.275$

$3.33 < V_i$:

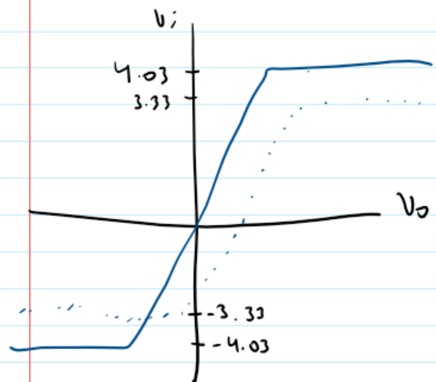
OFF: D_3 & D_4

ON: D_1 & D_4

$-4.6 + 2K \cdot i_1 + 0.7 i_1 - 0.7 i_2 + 2i - 2i_2 \to 3.67$

$4.7 i_1 - 2.7 i_2 = 0.75$

$0.7V + 2i_2 - 2i_1 - 3.67 + 0.7$



2.

$- R > 500$

$- V_i = 8V$

$i_D > 0.5\ mA$

$\frac{R_1}{R_1+R_2} = 0.5$

$\downarrow$

$R_1 = R_2$

$-V_{D_1} + V_{D_2} - 3.33 + 2(1.67) + i_{D_2} R_2 = 0$

$-3.3 + 1.67 - 3.33 + 3.34 + 0.5mA \cdot R_2 = 0$

$R_2 = \frac{6.63 - 1.67 - 3.34}{0.5\ mA}$

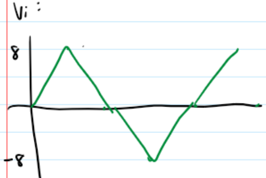
$R_2 = 3.3K = R_1$

$V_0 = V_i \cdot \frac{R_2}{R_1+R_2}$

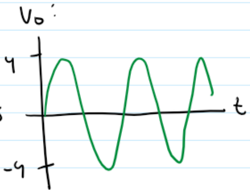
$= 8 \cdot 0.5$

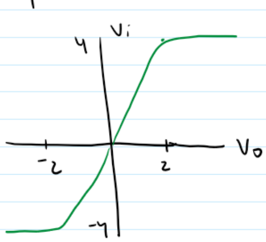
$= 4$

V_i:



V_o:

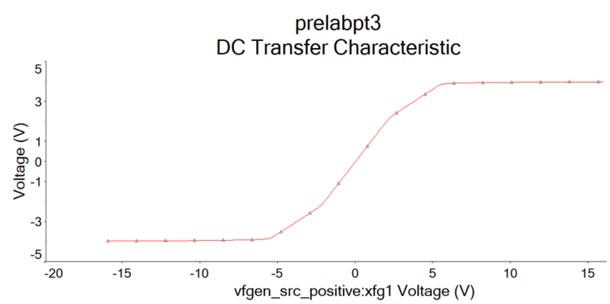


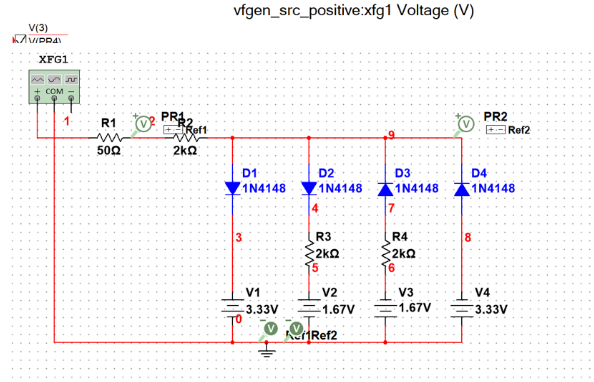


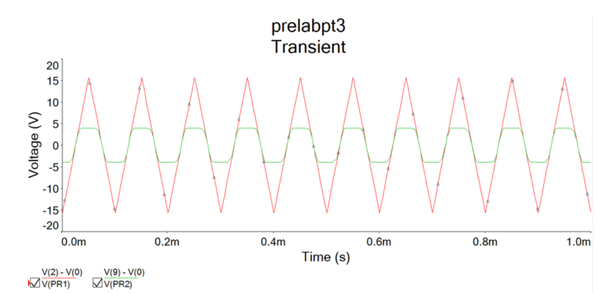
$V_0 = V_i \cdot 0.5$

$=$

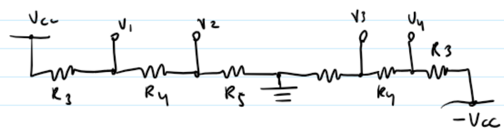
Pt 3







4.

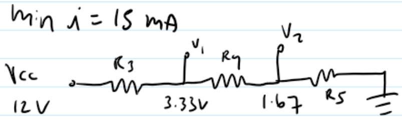


$V_1 = -V_4 = 3.33\,V$

$V_2 = -V_3 = 1.67$

$|V_{cc}| = 12\,V$

min $i = 15\ mA$



$V_{R3} = 12V - 3.33$ $= 8.67\,V$

$V_{R4} = 8.67 - 1.67$ $= 7\,V$

$i = 15\ mA$

$i = 15\ mA$

$R_3 = \frac{8.67}{15mA}$

$R_4 = \frac{7V}{15mA}$

$R_3 = 578\ \Omega$

$= 466.\overline{66}\ \Omega$

$V_{R5} = 7 - 0$

$=$

$R_5 = \frac{1.67}{15mA} = 111.\overline{33}$

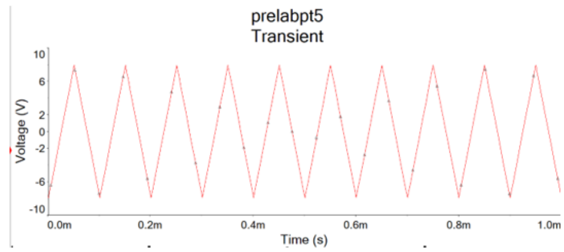
$=$

$R_1 = 3.33K$ $R_3 = 470$ $R_5 = 91$

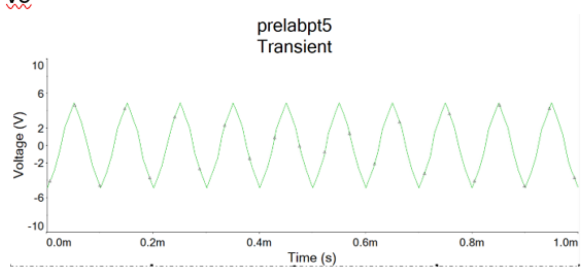
$R_2 = 3.33K$ $R_4 = 91$

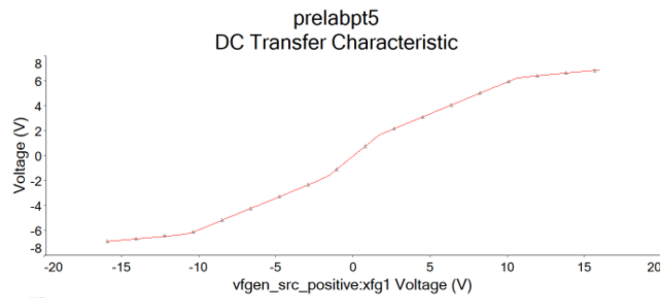
Pt 5

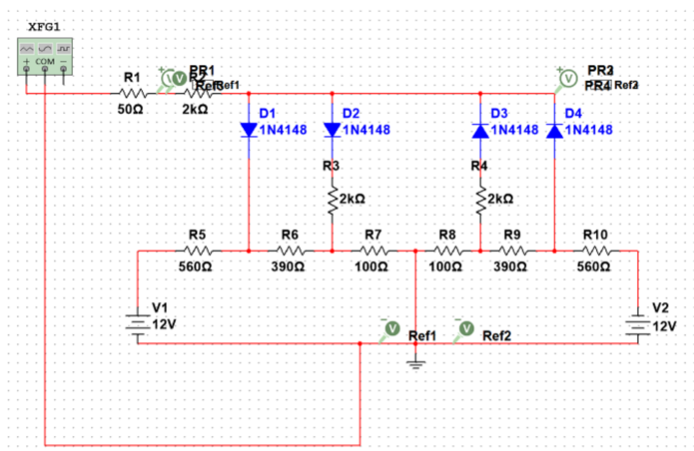
vi:



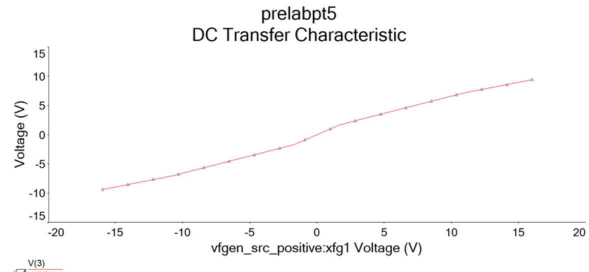
vo

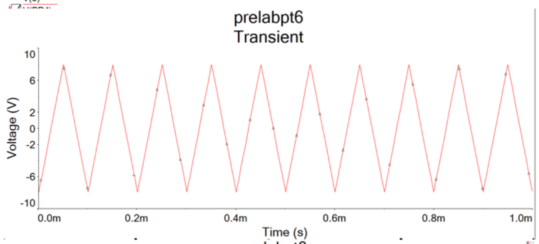


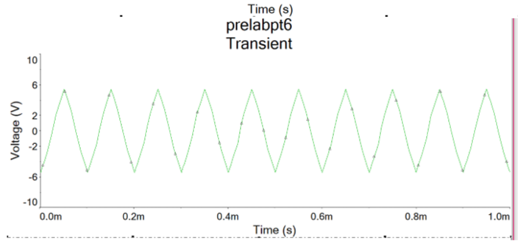


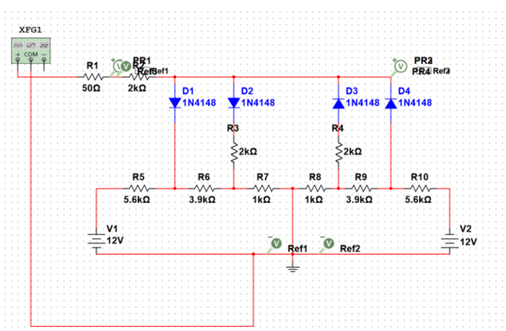


Pt 6

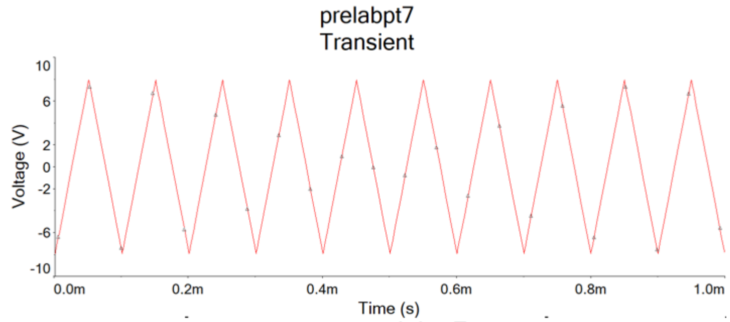

prelabpt5
DC Transfer Characteristic
Voltage (V)
vfgen_src_positive:xfg1 Voltage (V)
V(3)


prelabpt6
Transient
Voltage (V)
Time (s)


prelabpt6
Transient
Voltage (V)
Time (s)


XFG1
R1
50Ω
2kΩ
D1
1N4148
D2
1N4148
D3
1N4148
D4
1N4148
R3
2kΩ
R4
2kΩ
R5
5.6kΩ
R6
3.9kΩ
R7
1kΩ
R8
1kΩ
R9
3.9kΩ
R10
5.6kΩ
V1
12V
V2
12V
Ref1
Ref2

Pt 7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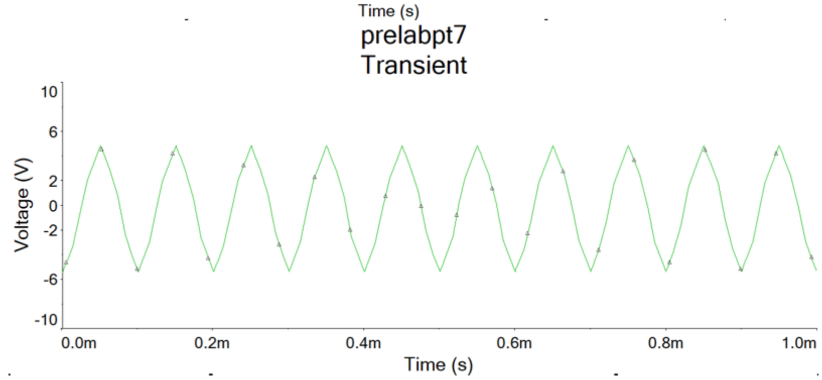
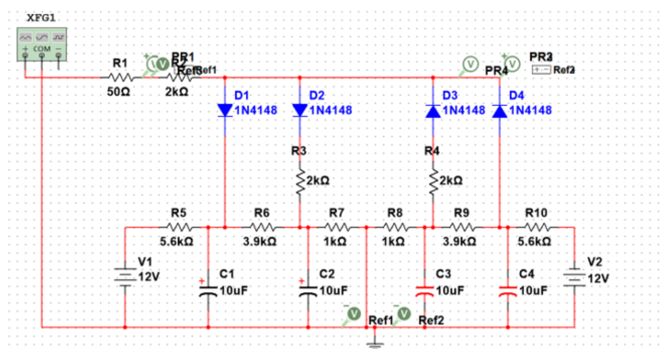
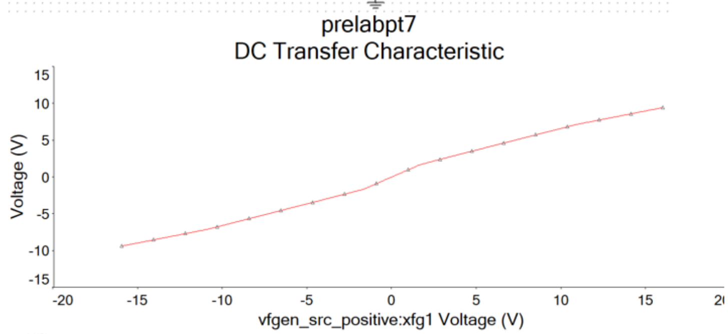
Transient
Voltage (V)
Time (s)


prelabpt7
Transient
Voltage (V)
Time (s)


XFG1
R1
50Ω
2kΩ
D1
1N4148
D2
1N4148
D3
1N4148
D4
1N4148
R3
2kΩ
R4
2kΩ
R5
5.6kΩ
R6
3.9kΩ
R7
1kΩ
R8
1kΩ
R9
3.9kΩ
R10
5.6kΩ
V1
12V
V2
12V
C1
10uF
C2
10uF
C3
10uF
C4
10uF
Ref1
Ref2


prelabpt7
DC Transfer Characteristic
Voltage (V)
vfgen_src_positive:xfg1 Voltage (V)
V(3)

Experiment:

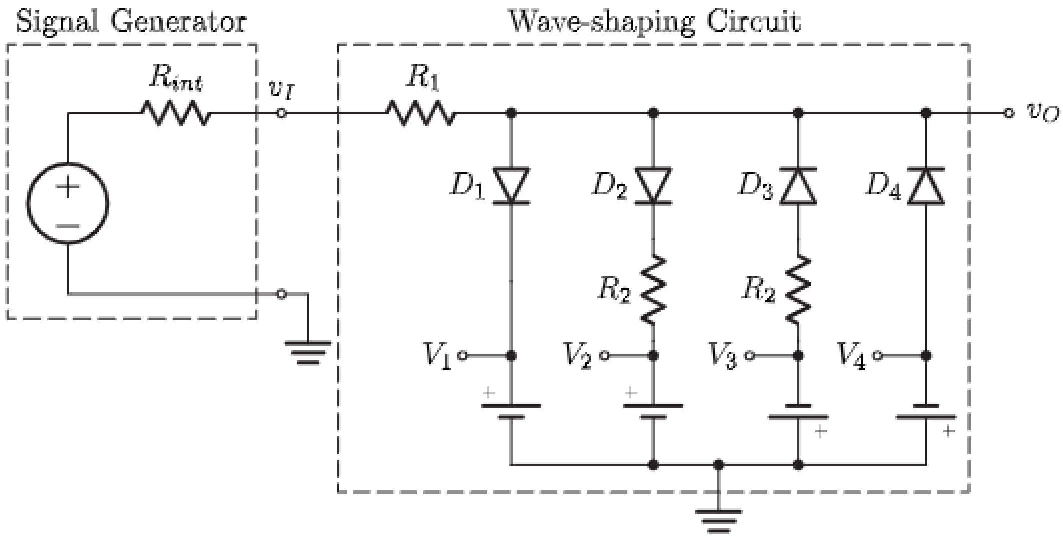


Figure 1. Wave-shaping circuit with multiple DC voltage sources (batteries).

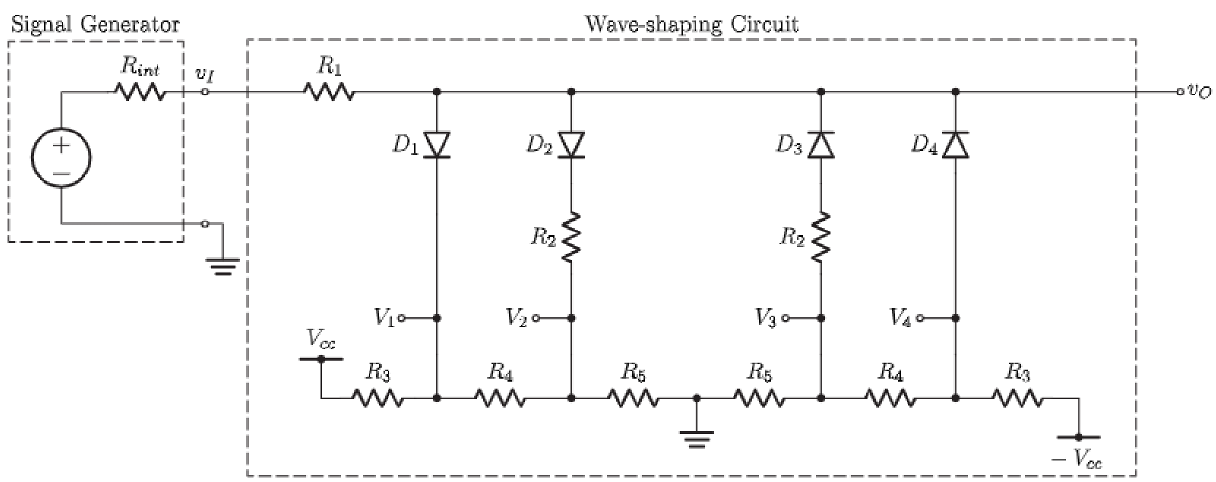


Figure 3. Wave-shaping circuit of Figure 1 in which the DC voltages are obtained from the voltage-dividing network of Figure 2.

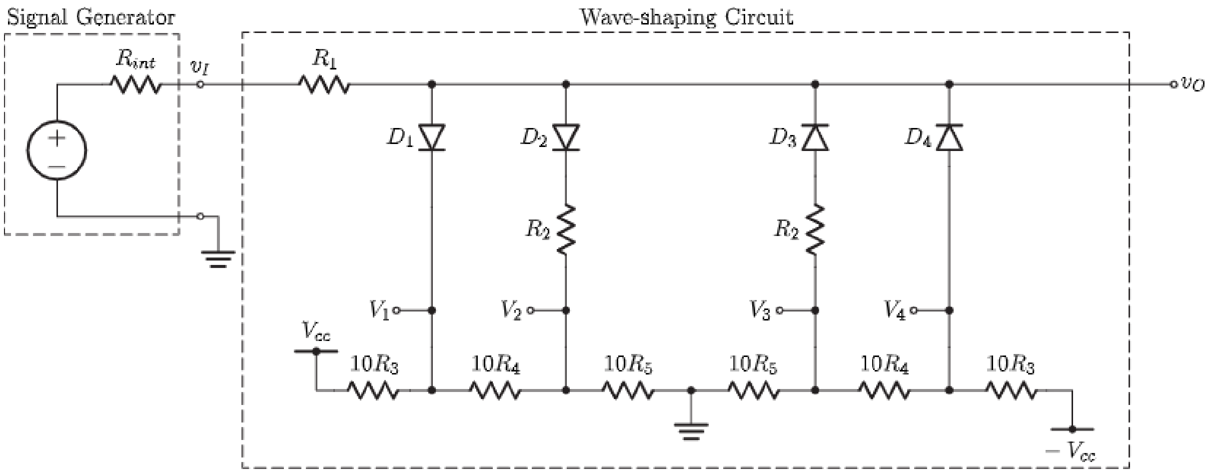


Figure 4. Wave-shaping circuit of Figure 3 in which **R3** through **R5** have been made 10 times larger.

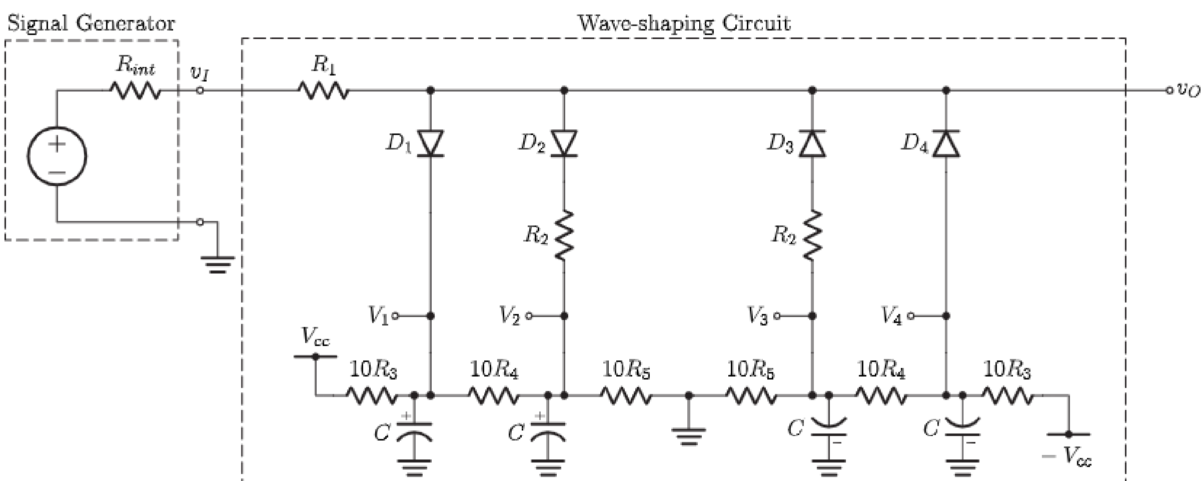
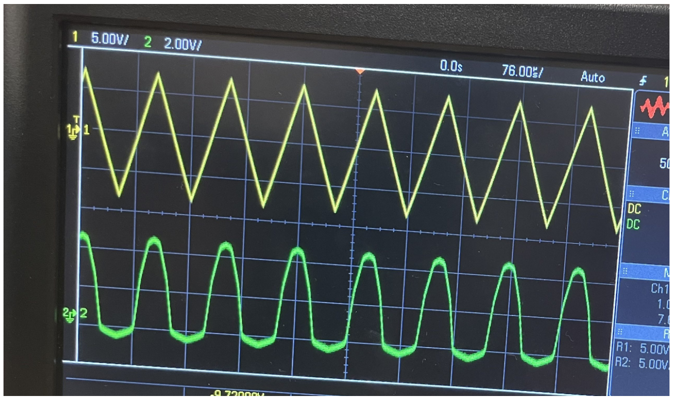
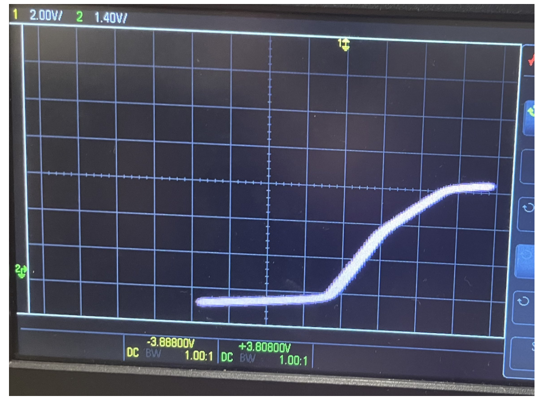


Figure 5. Modified wave-shaping circuit with resistances **R3** through **R5** made 10 times larger and bypassed by electrolytic capacitors

The initial configuration presented in Figure 2 utilizes 1N4148 diodes and a combination of 5 resistors, denoted as R1, R2, R3, R4, and R5. In this setup, the values of R1 and R2 are 3.3kΩ, R3 is 4702Ω, and R4 and R5 are 91Ω. The subsequent circuit depicted in Figure 2 employs the same set of resistors, but with their values increased tenfold for R1 through R5. Finally, the last circuit, illustrated in Figure 4, integrates the components from the previous setup and incorporates bypassed electrolytic capacitors.

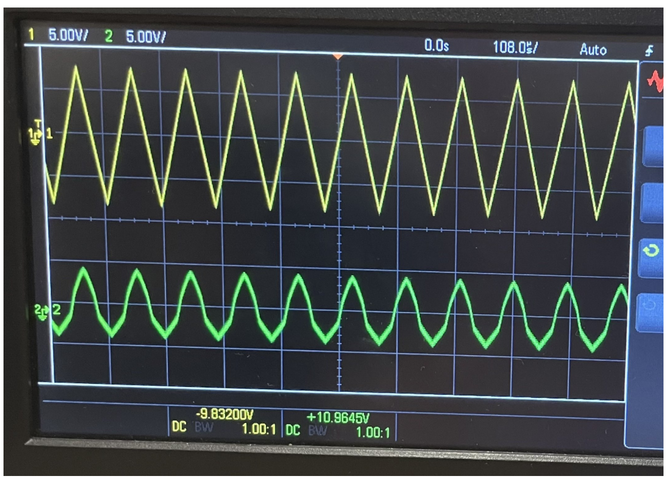
Results:

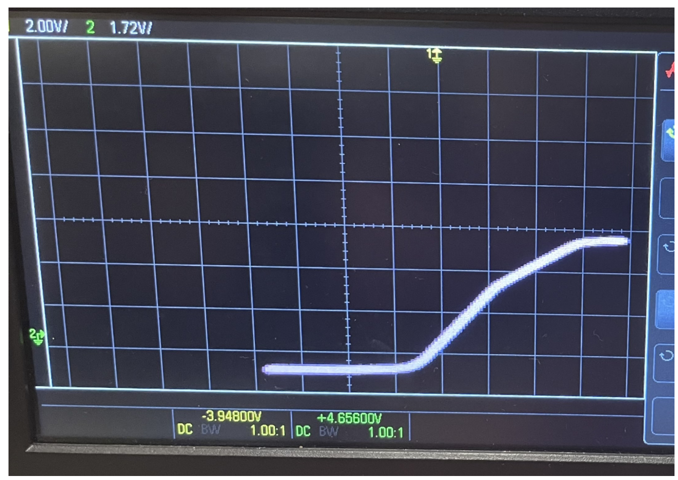




Graph E1A.) **Graph E1B.)**

Graph's E1A and E1B are the results produced by the circuit constructed in fig.3.





Graph E2A.) **Graph E2B.)**

Graph's E2A and E2B are the results produced by the circuit constructed in figure 4.

Graph E3A.) **Graph E3B.)**

Lastly, Graph's E3A and E3B are the results produced by the circuit constructed in figure 5.

Conclusion:

C1:

Based on the transfer characteristics displayed in Graph P3(b), when a symmetrical periodic triangular input voltage is applied to the circuit illustrated in Figure 1, the output voltage will exhibit a symmetrical sinusoidal waveform. However, this waveform is influenced by the presence of diodes configured as voltage clippers.

C2:

The transfer characteristics depicted in Graph P1 and Graph P3(b) can be considered comparable since they utilize a similar ratio of resistors and diodes in their respective circuits. The primary distinction between the two graphs stems from the voltage threshold necessary for the diodes to turn on. However, this discrepancy is insignificant as it does not lead to any contradiction or inconsistency between the two graphs.

C3:

Upon analyzing the transfer characteristics of Graph P1 in comparison to Graphs P5(b) and P6(b), several similarities become apparent. Firstly, all three graphs display a clipper voltage output waveform. Secondly, the slopes of the voltage output in these graphs are comparable. Lastly, in all three cases, the output voltage levels off once it reaches the cut-off point.

C4:

Upon comparing the transfer characteristics of Graph P1, P6(b), and P7(b), it is evident that Graph P7(b) exhibits a more consistent, linear, and higher output voltage in comparison to the other two graphs. This improved performance is attributed to the presence of capacitors in Graph P7(b), which effectively reduce ripple voltages by converting them into a smoother DC voltage flow. In contrast, the absence of capacitors in Graph P6(b) results in lower and less linear output voltage. It is important to note that all three graphs exhibit similar behavior to that of a voltage clipper circuit.

C5:

All of the graphs display a similar overall shape, but the discrepancies between them can be attributed to variations in their saturation points and slopes in the active region. Graphs E1 and P1 have comparable saturation points and slopes since E1 represents a basic and uncomplicated circuit. In contrast, Graphs P1 and E2 exhibit a steeper slope due to increased resistance, resulting in a reduction in oscilloscope noise. Finally, Graphs P1 and E3 differ significantly both in terms of the slope of the graph and the value of their saturation points. The circuit in E3 includes a bypass capacitor that enhances the gain, leading to a steeper slope and a less noisy reading. Additionally, the resistance in this circuit has been increased, resulting in a higher saturation point value.