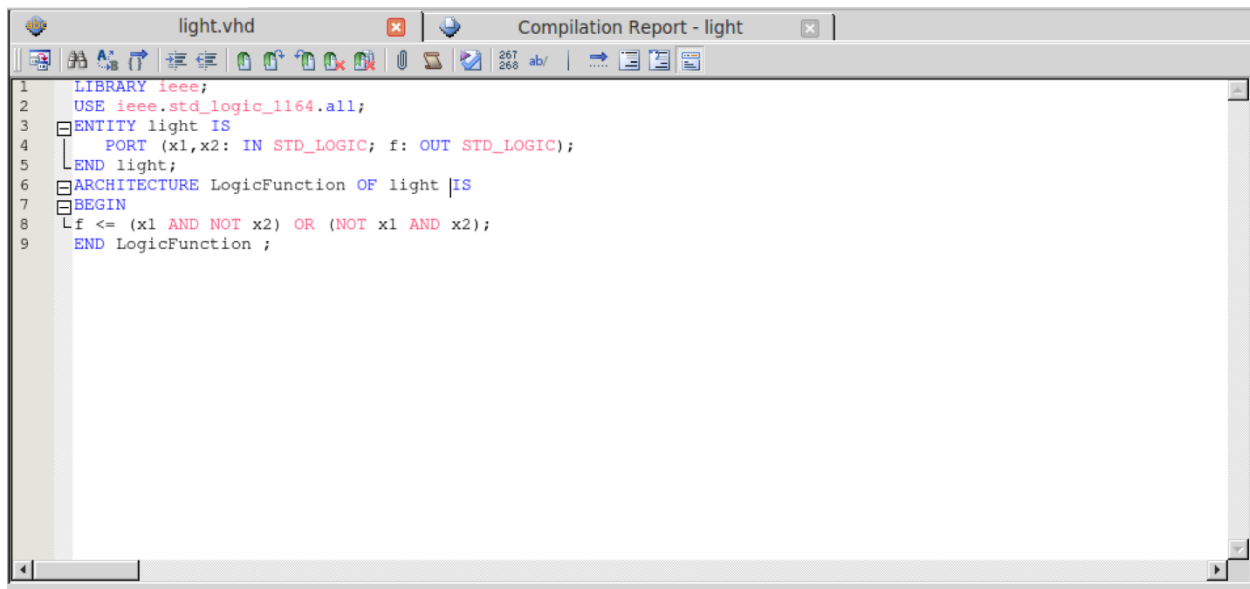


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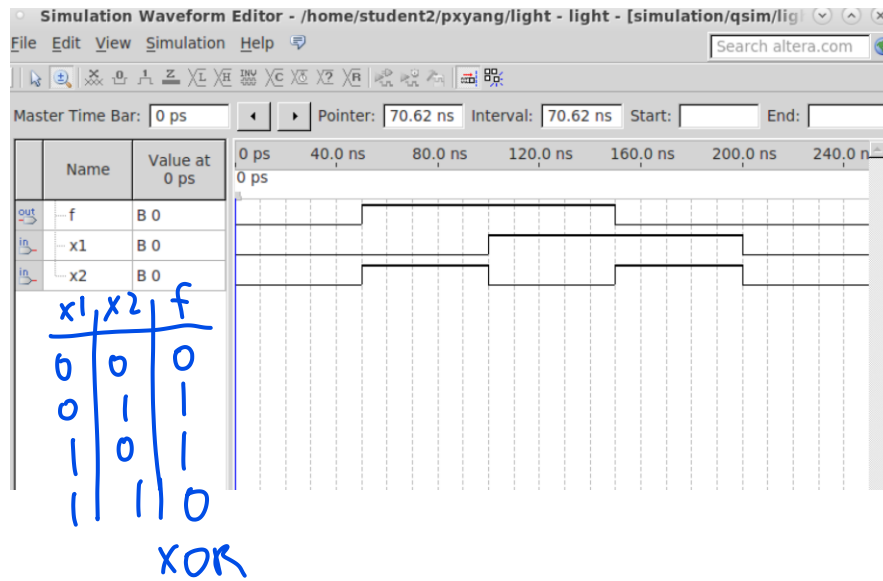
Nini Yang



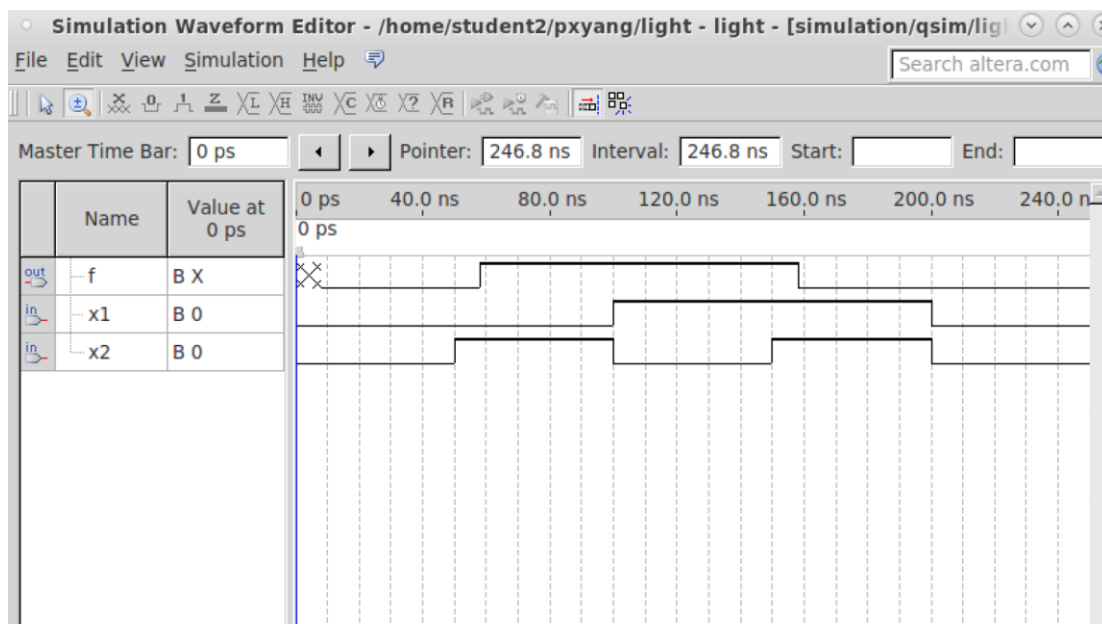
The image shows a screenshot of a VHDL code editor window. The window has a title bar with two tabs: "light.vhd" and "Compilation Report - light". Below the title bar is a toolbar with various icons for file operations, editing, and simulation. The main area of the window displays the following VHDL code:

```
1  LIBRARY ieee;  
2  USE ieee.std_logic_1164.all;  
3  ENTITY light IS  
4  PORT (x1,x2: IN STD_LOGIC; f: OUT STD_LOGIC);  
5  END light;  
6  ARCHITECTURE LogicFunction OF light IS  
7  BEGIN  
8  f <= (x1 AND NOT x2) OR (NOT x1 AND x2);  
9  END LogicFunction ;
```

Functional Simulation



Timing Simulation



The output is slightly delayed due to logic elements and wires in the FPGA device