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Digital Electronics
COE328

Lecture 12

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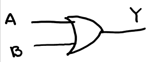
Combinational vs. Sequential Circuit

- Combinational Circuit: output depends on current inputs.

Multiplexer, Decoder, ASU, etc.

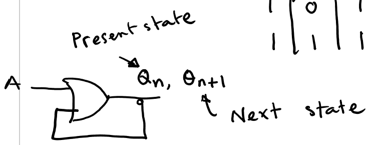
- Sequential Circuit: output depends on current inputs and previous output (memory).

Latch, flip-flop, resister, counter, etc.



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



Truth Table

A	P.S Q_n	N.S Q_{n+1}
0	0	0
1	0	1
1	1	1
0	1	1

Basic Latch

A memory element can be built with NOR gates.

The input (set or reset) is used to change the state Q of the circuit.

Circuit Operation:

Case I:

R=0; S=0;

$$Q_{n+1} = \overline{R + \overline{Q_n}} = \overline{0 + \overline{Q_n}} = Q_n$$
$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{0 + Q_n} = \overline{Q_n}$$

Case II:

R=0; S=1;

$$Q_{n+1} = \overline{R + \overline{Q_n}} = \overline{0 + \overline{Q_n}} = \overline{Q_n}$$
$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{1 + Q_n} = \overline{1} = 0$$

Case III:

R=1; S=0;

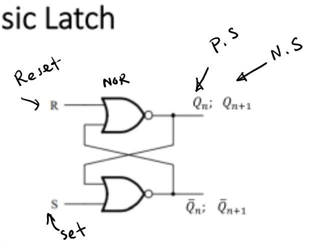
$$Q_{n+1} = \overline{R + \overline{Q_n}} = \overline{1 + \overline{Q_n}} = \overline{1} = 0$$
$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{0 + Q_n} = \overline{Q_n}$$

Case IV:

R=1; S=1;

$$Q_{n+1} = \overline{R + \overline{Q_n}} = \overline{1 + \overline{Q_n}} = \overline{1} = 0$$
$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{1 + Q_n} = \overline{1} = 0$$

Therefore, CASE III is an invalid or not-used case.



R	S	Present State Q_n	Next State Q_{n+1}
0	0	*	$Q_{n+1} = Q_n$ No change
0	1	*	1
1	0	*	0
1	1	*	Invalid

X

Case III

R = 1, S = 0

$$Q_{n+1} = \overline{1 + \bar{Q}_n} = \bar{1} = 0$$

$$\overline{Q_{n+1}} = 1$$

$0 + x = x$

$1 + x = 1$

Case I

R = 0 , S = 0

$$Q_{n+1} = \overline{R + \bar{Q}_n} = \overline{0 + \bar{Q}_n}$$
$$= \bar{\bar{Q}}_n = Q_n$$

No change

$Q_{n+1} = Q_n$ Next state = P.S

$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{0 + Q_n} = \overline{Q_n}$$

$\overline{Q_{n+1}} = \overline{Q_n}$ N.S ⇒ P.S

Case II

R = 0 $\boxed{S = 1}$

$$Q_{n+1} = \overline{R + \bar{Q}_n} = \overline{0 + \bar{Q}_n} = \bar{\bar{Q}}_n = Q_n = 1$$

$$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{1 + Q_n} = \bar{1} = \boxed{0}$$

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$Q_{n+1} = 1 + \bar{Q}_n = 1$

$\overline{Q_{n+1}} = 1$

$\overline{Q_{n+1}} = \overline{S + Q_n} = \overline{1 + Q_n} = \bar{1} = \boxed{0}$

NAND Latch

- A memory element can be built with NAND gates.

The input (set or reset) is used to change the state Q of the circuit.

Circuit Operation:

Case I:

R=0; S=0; $Q_{n+1} = \overline{R.\overline{Q_n}} = \overline{0.\overline{Q_n}} = \bar{0} = 1$ ✓

$\overline{Q_{n+1}} = \overline{S.Q_n} = \overline{0.Q_n} = \bar{0}$=1 } invalid

Therefore, CASE I is an invalid or not-used case.

Case II:

R=0; S=1; $Q_{n+1} = \overline{R.\overline{Q_n}} = \overline{0.\overline{Q_n}} = \bar{0} = 1$ ✓

$\overline{Q_{n+1}} = \overline{S.Q_n} = \overline{1.Q_n} = \overline{Q_n}$ 0

Case III:

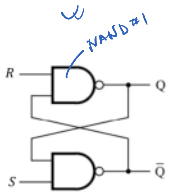
R=1; S=0; $Q_{n+1} = \overline{R.\overline{Q_n}} = \overline{1.\overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$ 0

$\overline{Q_{n+1}} = \overline{S.Q_n} = \overline{0.Q_n} = \bar{0}$=1

Case IV:

R=1; S=1; $Q_{n+1} = \overline{R.\overline{Q_n}} = \overline{1.\overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$

$\overline{Q_{n+1}} = \overline{S.Q_n} = \overline{1.Q_n} = \overline{Q_n}$



R	S	Present State Q_n	Next State Q_{n+1}
0	0	*	Invalid
0	1	*	1
1	0	*	0
1	1	*	$Q_{n+1} = Q_n$ No change

R' S'

$Q_{n+1} = Q_n$

$\overline{Q_{n+1}} = \overline{Q_n}$ } No change

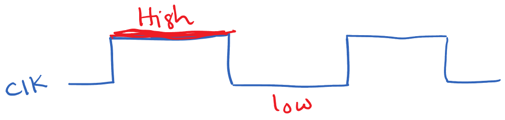
Case IV

R=1, S=1

$Q_{n+1} = \overline{R + \bar{Q}_n} = \bar{1} = 0$ ✓

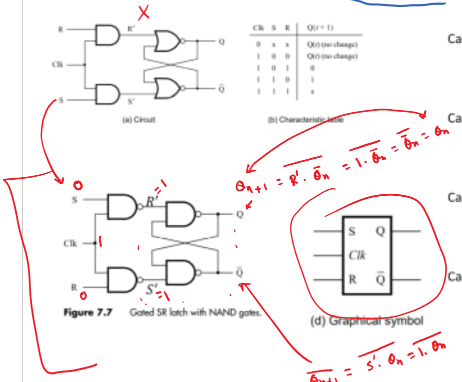
$\overline{Q_{n+1}} = \overline{S + Q_n} = \bar{1} = 0$ ✓

$Q_{n+1} = \overline{Q_{n+1}}$ invalid



Gated SR Latch

← clock



(a) Circuit

Clk	S	R	Q(t + 1)
0	x	x	Q(t) (no change)
1	0	0	Q(t) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

(b) Characteristic table

Figure 7.7 Gated SR latch with NAND gates.

(d) Graphical symbol

$Q_{n+1} = \overline{R'.\bar{Q}_n} = \overline{1.\bar{Q}_n} = \bar{\bar{Q}}_n = Q_n$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{1.Q_n} = \bar{Q}_n$

Case I: Clk=1; S=0; R=0; will give R'=1; S'=1;

$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{1.\overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{1.Q_n} = \overline{Q_n}$

Case II: Clk=1; S=0; R=1; will give R'=1; S'=0;

$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{1.\overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{0.Q_n} = \bar{0} = 1$

Case III: Clk=1; S=1; R=0; will give R'=0; S'=1;

$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{0.\overline{Q_n}} = \bar{0} = 1$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{1.Q_n} = \overline{Q_n}$

Case III: Clk=1; S=1; R=1; will give R'=0; S'=0;

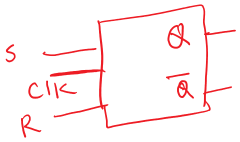
$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{0.\overline{Q_n}} = \bar{0} = 1$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{0.Q_n} = \bar{0} = 1$

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Clk	R	S	P.S Q_n	N.S Q_{n+1}
0	X	X	X	No change
1	0	0	X	NC
1	0	1	X	1
1	1	0	X	0
1	1	1	X	Invalid



Gated D-Latch

Case I: Clk=1; D=0

S=0; R=1; will give R'=1; S'=0;

$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{1.\overline{Q_n}} = \overline{\overline{Q_n}} = Q_n$

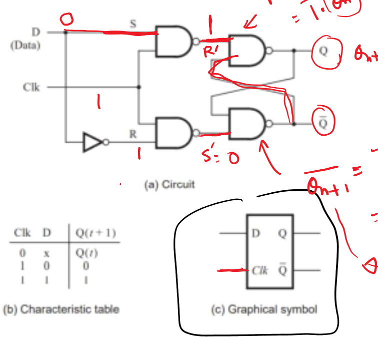
$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{0.Q_n} = \bar{0} = 1$

Case III: Clk=1; D=1;

S=1; R=0; will give R'=0; S'=1;

$Q_{n+1} = \overline{R'.\overline{Q_n}} = \overline{0.\overline{Q_n}} = \bar{0} = 1$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{1.Q_n} = \overline{Q_n}$



$\overline{R'.\bar{Q}_n} = \overline{1.\bar{Q}_n} = \bar{Q}_n = Q_n = 0$

$\overline{Q_{n+1}} = \overline{S'.Q_n} = \overline{0.Q_n} = \bar{0}$

Q = 1

(a) Circuit

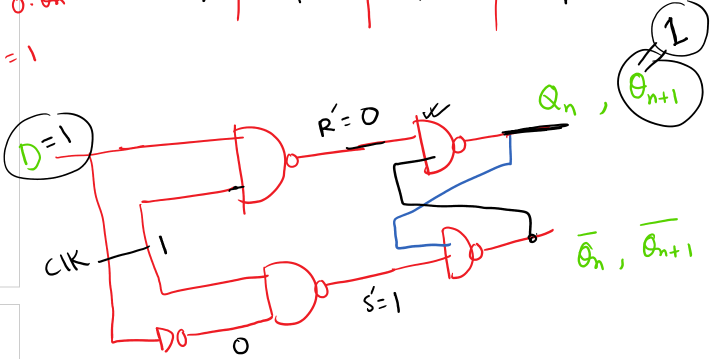
Clk	D	Q(t + 1)
0	x	Q(t)
1	0	0
1	1	1

(b) Characteristic table

(c) Graphical symbol

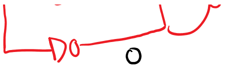
Data

Clk	D	P.S Q_n	N.S Q_{n+1}
0	X	X	NC
1	0	X	0
1	1	X	1



$Q_{n+1} = \overline{R'.\bar{Q}_n} = \overline{0.\bar{Q}_n} = \bar{0} = 1$

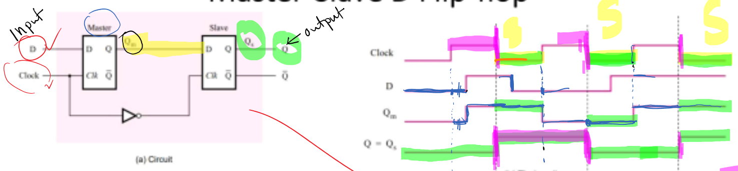
Clk D o/p
1 0 0
1 1 NC



S=1

Clk	D	Qk
1	0	0
1	1	1
0	X	NC

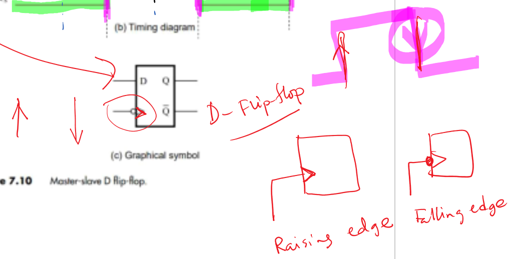
Master-Slave D Flip-flop



(a) Circuit

(b) Timing diagram

Two gated D-latch
The first gate (master) changes its state when Clk=1
The second gate (slave) changes its state when Clk=0
The overall output change happens at the falling edge of the clock.
This is called a master-slave D flip-flop.
The term flip-flop denotes a storage element that changes its output state at the edge of a controlling clock signal.



(c) Graphical symbol

Figure 7.10 Master-slave D flip-flop.

Edge Triggered D Flip-Flop

Case I: Clk=0 makes $P_1 = 1; P_2 = 1$ so the output is Q_n and $\bar{Q}_n$

$$P_4 = \overline{D.P_2} = \overline{D.1} = \bar{D}$$

$$P_3 = \overline{P_4.P_1} = \overline{\bar{D}.1} = \bar{\bar{D}} = D$$

Case II: Clk=1 gives $P_1 = \overline{1.P_3} = \bar{D};$

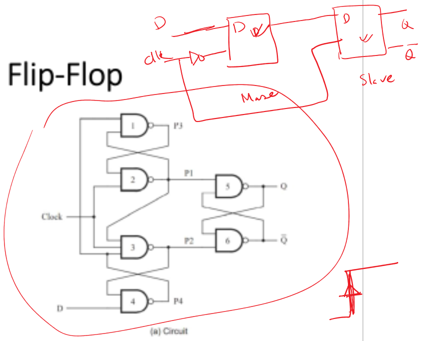
$$P_2 = \overline{P_1.1.P_4} = \bar{\bar{D}} = D$$

so the output is

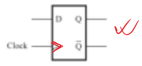
$$Q_{n+1} = \overline{P_1.\bar{Q}_n} = \overline{\bar{D}.\bar{Q}_n}\text{=D}$$

And

$$\bar{Q}_{n+1} = \overline{P_2.Q_n} = \overline{D.Q_n} = \bar{D}$$



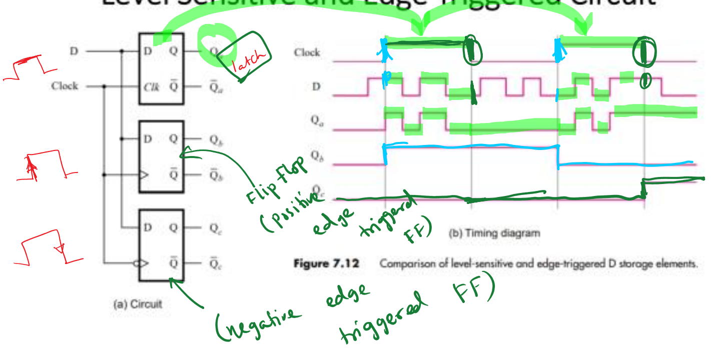
(a) Circuit



(b) Graphical symbol

Figure 7.11 A positive-edge-triggered D flip-flop.

Level Sensitive and Edge Triggered Circuit



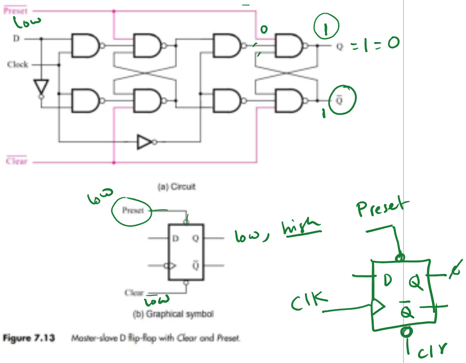
(a) Circuit

(b) Timing diagram

Figure 7.12 Comparison of level-sensitive and edge-triggered D storage elements.

D Flip-Flops with CLEAR and PRESET

Placing a 0 on the Clear input will force the flip-flop into the state Q = 0.
If Clear = 1, then this input will have no effect on the NAND gates.
Similarly, Preset = 0 forces the flip-flop into the state Q = 1, while Preset = 1 has no effect.
To denote that the Clear and Preset inputs are active when their value is 0, we placed an overbar on the names in the figure.
We should note that the circuit that uses this flip-flop should not try to force both Clear and Preset to 0 at the same time.
A graphical symbol for this flip-flop is shown in Figure 7.13b.

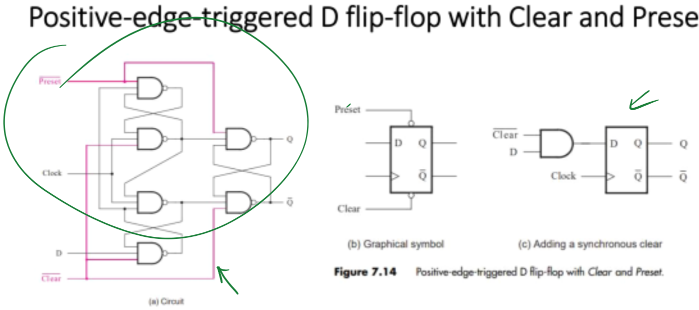


(a) Circuit

(b) Graphical symbol

Figure 7.13 Master-slave D flip-flop with Clear and Preset.

Positive-edge-triggered D flip-flop with Clear and Preset


$\overline{\text{Preset}}$
Clock
D
$\overline{\text{Clear}}$
Q
$\bar{Q}$
Preset
D Q
$\bar{Q}$
Clear
$\overline{\text{Clear}}$
D
Clock
D Q
$\bar{Q}$
Q
$\bar{Q}$

(a) Circuit

(b) Graphical symbol

(c) Adding a synchronous clear

Figure 7.14 Positive-edge-triggered D flip-flop with Clear and Preset.

Symbols , Truth Table , Characteristic table

excitation table

T Flip-Flop

Logic function for $D = \bar{T}Q + T\bar{Q}$

Case 1:

T=0; Q(t)=1; $\bar{Q}(t) = 0$; D=1.1+0.0=1 ; Q(t+1)=1 i.e. Q(t+1)=Q(t)

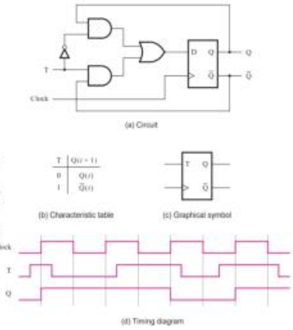
T=0; Q(t)=0; $\bar{Q}(t) = 1$; D=0.0+0.1=0 ; Q(t+1)=0 i.e. Q(t+1)=Q(t)

Case 2:

T=1; Q(t)=1; $\bar{Q}(t) = 0$; D=0.1+1.0=0 ; Q(t+1)=0 i.e. Q(t+1)=$\overline{Q(t)}$

T=1; Q(t)=0; $\bar{Q}(t) = 1$; D=0.0+1.1=1 ; Q(t+1)=1 i.e. Q(t+1)= $\overline{Q(t)}$

T flip-flop derives from the behavior of the circuit, which “toggles” its state when T = 1. The toggle feature makes the T flip-flop a useful element for building counter circuits.



(a) Circuit

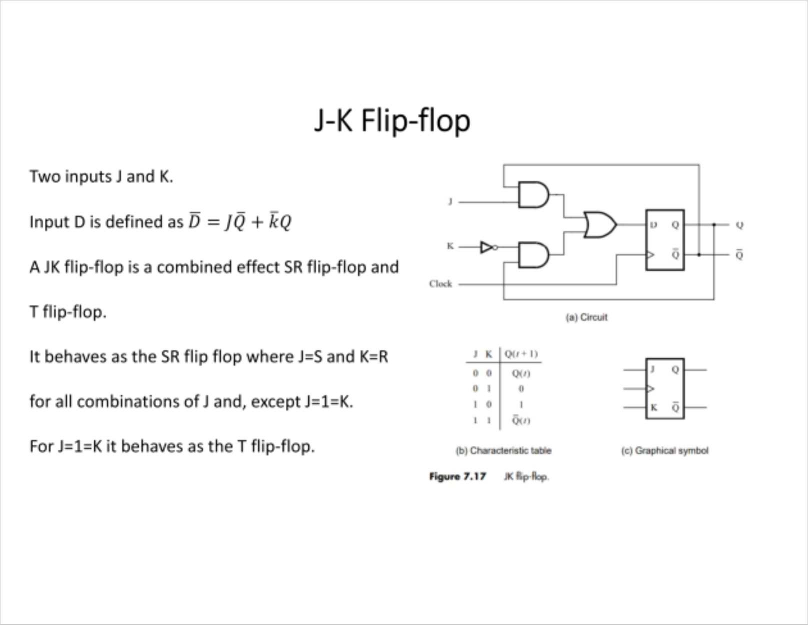
T	Q(t + 1)
0	Q(t)
1	$\bar{Q}(t)$

(b) Characteristic table

(c) Graphical symbol

(d) Timing diagram

Figure 7.16 T flip-flop.



J-K Flip-flop

Two inputs J and K.

Input D is defined as $\overline{D} = J\bar{Q} + \bar{k}Q$

A JK flip-flop is a combined effect SR flip-flop and

T flip-flop.

It behaves as the SR flip flop where J=S and K=R

for all combinations of J and, except J=1=K.

For J=1=K it behaves as the T flip-flop.

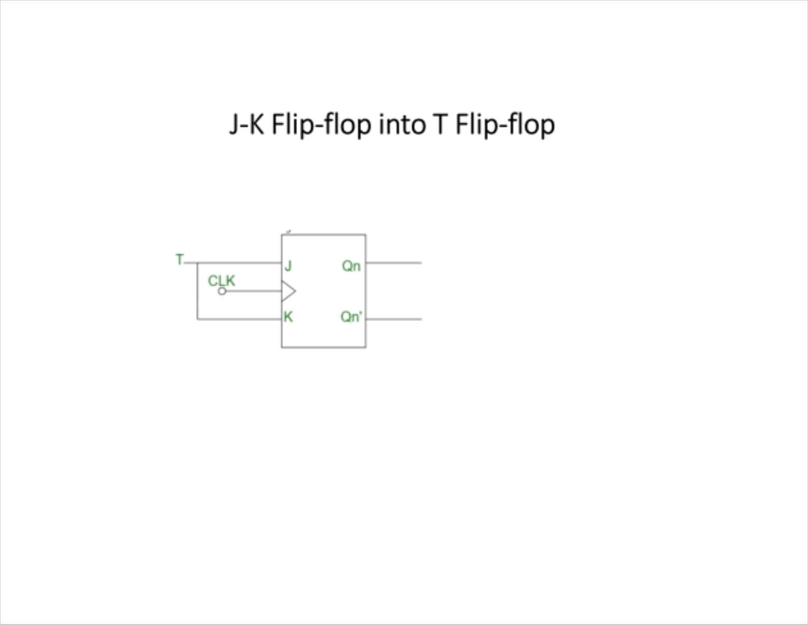
(a) Circuit

J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$\bar{Q}(t)$

(b) Characteristic table

(c) Graphical symbol

Figure 7.17 JK flip-flop.



J-K Flip-flop into T Flip-flop