ELE 202
Laboratory #4

Circuit Theorems and the Superposition Principle

1.0 INTRODUCTION

A complex linear circuit network often consists of combinations of linear elements, linear dependent sources and linear independent sources. Circuit theorems (and related procedures) can be used to reduce such complex circuits to simpler ones, thereby making the circuit analysis that much simpler using *nodal* voltage or *mesh* current techniques.

- **Thevenin's** and **Norton's** theorems allow the isolation of a portion of a circuit network while the remaining portion of the network is replaced by an equivalent network. Related to these theorems is the ***Source Transformation*** technique for simplifying circuits, which is the process of replacing a voltage source in series with a resistor, by a current source in parallel with a resistor, and *vice versa*.

- **Maximum Power Transfer** theorem states that the maximum power gets delivered (by the source) to the load when the load resistance ($\mathbf{R_L}$) equals the Thevenin's resistance ($\mathbf{R_{Th}}$) as seen at the terminal of the load.

The ***Principle of Superposition*** is a conceptual aid that can be very useful in visualizing the behavior of a circuit or network system containing multiple sources. This principle states that when a number of independent input sources are applied simultaneously to a linear network, the response is the sum of the responses due to *each* input acting alone. Hence, the Superposition principle helps simplify the analysis of circuits with multiple independent sources by allowing the voltage across (or current through) any element to be obtained by adding algebraically all the individual voltages (or currents) caused by *each* independent source acting *alone*, with all other independent voltage sources replaced by *short-circuits* and all other independent current sources replaced by *open-circuits*.

Note: A ***two-terminal network*** is defined when interconnections of circuit elements *inside a box* have only two accessible terminals for connection to other networks.

References: (i) Course Textbook: "*Fundamentals of Electric Circuits*" by C. K. Alexander and M. N. O. Sadiku; and (ii) "*Linear Circuit Analysis*" by R. A. DeCarlo and P-M. Lin.

2.0 OBJECTIVES

- To analyze and examine the *Thevenin*'s equivalent circuit of a *two-terminal* source network, and verify the *maximum power transfer* theorem; and
- To analyze and experimentally verify the *Superposition Principle*.

3.0 REQUIRED LAB EQUIPMENT & PARTS

- Digital Multimeter (DMM) and Power Supply
- ELE202 Lab Kit:- various components, breadboard, wires and jumpers.

4.0 PRE-LAB: ASSIGNMENT

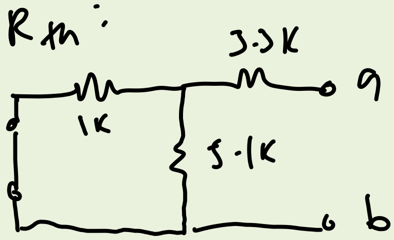
(a) *Thevenin Equivalent Circuit*

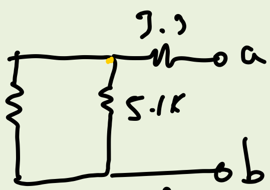
(i) For the circuit shown in **Figures 2.0a** and **2.0b**, consider the input D.C. source voltage, **E = 10 V**. **(1)** Determine the Thevenin's equivalent circuit of the two-terminal source network in **Figure 2.0a** by finding the Thevenin voltage, $\mathbf{V_{Th}}$ and the Thevenin resistor, $\mathbf{R_{Th}}$ as shown in **Figure 2.0c**; **(2)** referring to circuits in **Figure 2.0b**, use either nodal-voltage or mesh-current technique to find the respective open-circuit voltage, $\mathbf{V_{OC}}$ and short-circuit current, $\mathbf{I_{SC}}$; and **(3)** use the Thevenin equivalent circuit model in **Figure 2.0c** to show that $\mathbf{V_{Th}} = \mathbf{V_{OC}}$, and $\mathbf{R_{Th}} = \mathbf{V_{OC}}/\mathbf{I_{SC}}$. Show all your analysis below, and record your results in **Table 2.0**.

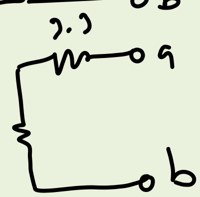
Pre-Lab workspace

1)

R_{th}:



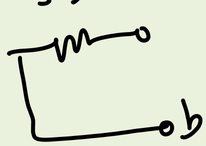




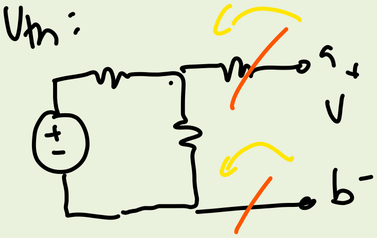
$\dfrac{1}{\frac{1}{1K}+\frac{1}{5.1K}} = R_{eq}$

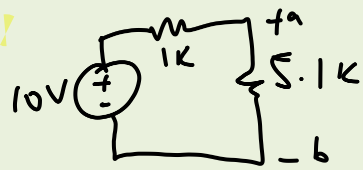
$\dfrac{1}{1+\frac{1}{5.1}} = 0.836$

$3.3 + 0.836 = 4.136\,K\Omega$



V_{th}:



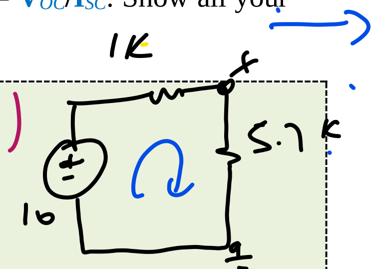


$V = \dfrac{R_{5.1}}{R_T}\,V$

$= \dfrac{5.1K}{6.1K}\,10V$

$V_{th} = 8.36\,V$

2)



$-10V + 1K\,i_1 + 5.1K\,i_1$

$10V = 6.1K\,i_1$

$\dfrac{10}{6.1} = i_1$

$i_1 = 1.639$

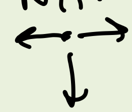
$V = i_1 R_1$

$= 1.639(5.1)$

$V = 8.36\,V$

$I = \dfrac{Vx}{R_3}$

NA:



$i = \dfrac{6.67\,V}{3.3}$

$= 2.021$

3)

$V_{th} = V_{oc}$ from q2.

$R_{th} = \dfrac{V_{oc}}{I_{oc}}$

$4.136 = \dfrac{8.36}{2.02}$

$4.13 = 4.13$

(ii) Construct the circuits of **Figure 2.0b** in MultiSIM, and measure corresponding open-circuit voltage, V_{OC} and short-circuit current, I_{SC}; and then determine V_{Th} and R_{Th} from these values. Record your results in **Table 2.0**.

- Copy and paste a screenshot showing one MultiSIM readings on the circuit. Include the MultiSIM circuit file (**.ms14**) in your Pre-Lab submission.
- All screenshots should show your name printed on the center-top of the MultiSIM screen and the timestamp at the bottom-lower corner.

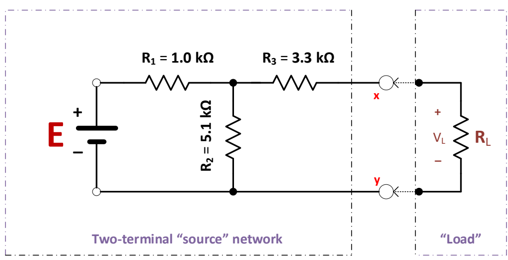


Figure 2.0a: Original Circuit

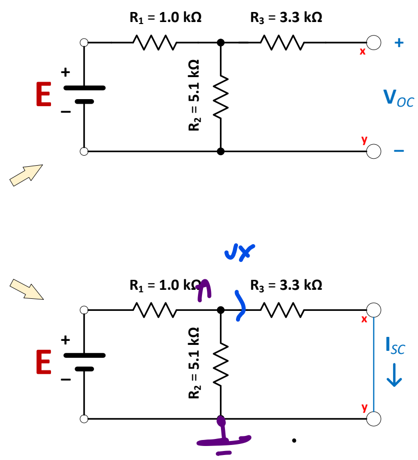


Figure 2.0b: In-circuit measurements for V_{Th} and R_{Th}

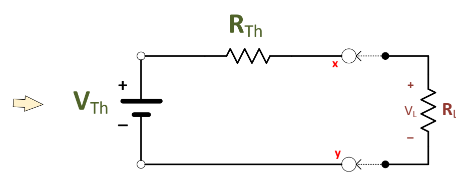


Figure 2.0c: Thevenin Equivalent Circuit

	V_{Th}	R_{Th}	V_{OC}		I_{SC}		$V_{Th} = V_{OC}$		$R_{Th} = V_{OC}/I_{SC}$	
E	Theory (volts)	Theory (kΩ)	Theory (volts)	MultiSIM (volts)	Theory (mA)	MultiSIM (mA)	Theory (volts)	MultiSIM (volts)	Theory (kΩ)	MultiSIM (kΩ)
10 (volts)	8.36	4.14	8.36	8.361	2.021	2.021	8.36	8.361	4.14	4.136

Table 2.0: Theoretical and MultiSIM results of the Figure 2.0 circuits

Compare the MutliSIM simulation results with the calculated theoretical values in **Table 2.0**. Comment on the results, and on any discrepancies.

Pre-Lab workspace

The values are the same

(b) *Maximum Power Transfer*

Consider the circuit in **Figure 2.0c**.

(i) Show that the power, $\mathbf{P_L}$ delivered to the load, $\mathbf{R_L}$ can be expressed as: -

$$\mathbf{P_L} = \left[\frac{\mathbf{V_{Th}}}{\mathbf{R_{Th}} + \mathbf{R_L}}\right]^2 \mathbf{R_L}$$ Show your analysis below.

(ii) Show that the maximum power transfer takes place when the load resistance, $\mathbf{R_L} = \mathbf{R_{Th}}$, with the load voltage, $\mathbf{V_L} = \mathbf{V_{Th}}/2$. Show your analysis below.

Pre-Lab workspace

i) $P = Vi$

$i = \frac{V}{R}$

$i = \frac{V_{th}}{R_{th} + R_L}$

$P = \left(\frac{V_{th}}{R_{th} + R_L}\right)^2 R_L$

ii) $V = \frac{V_t}{R_T + R_L}$

$\frac{V_L}{R} = \frac{V_{th}}{(2R_{Th})}$

$V_L = \frac{1}{2} V_{th}$

$P = \left(\frac{V_t}{R_t + R_L}\right)^2 R_L$

max: $P' = 0$

$P' = \frac{V_{th}^2 (R_{th} + R_L)^2 - R_L \cdot 2(R_{th} + R_L)}{(R_t + R_L)^4}$

$0 = (R_T + R_L)^2 - 2R_L(R_T + R_L)$

$0 = (R_T - R_L)$

$R_T = R_L$

when $P' = 0$ (max), $R_T = R_L$

(iii) Construct the circuit of **Figure 2.0a** in MultiSIM but use the **5** kΩ potentiometer, $\mathbf{R_P}$ as the <u>variable load</u> resistance, $\mathbf{R_L}$ illustrated below in **Figure 2.0d**. Set the input D.C. source voltage, **E** to **10V**. Monitor the load voltage, $\mathbf{V_L}$ across $\mathbf{R_P}$ with the DMM Voltmeter. Adjust the potentiometer until this output voltage, $\mathbf{V_L} = \mathbf{V_{Th}}/2$, at which point theoretically the maximum power transfer should occur per the theorem (<u>note</u>: refer your earlier Pre-Lab analysis for the $\mathbf{V_{Th}}$ value). Record your measured values of $\mathbf{V_L}$ and $\mathbf{R_L}$ in **Table 3.0**.

- Copy and paste a screenshot showing one MultiSIM readings on the circuit. Include the MultiSIM circuit file (**.ms14**) in your Pre-Lab submission.
- All screenshots should show your name printed on the center-top of the MultiSIM screen

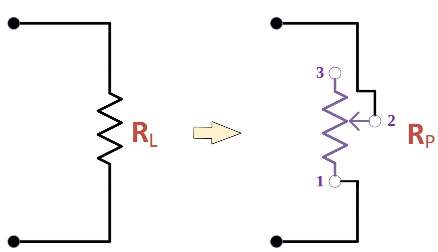


Figure 2.0d: Load, R_L replaced with potentiometer, R_P

Input Source, E	Thevenin voltage, V_{TH} (volts)	Measured load voltage, V_L (volts)	Load resistance R_L per resultant potentiometer, R_P reading. (kΩ)
	From **Table 2.0**	MultiSIM	MultiSIM
10 (volts)	8.36	4.18V	4.136KΩ

Table 3.0: MultiSIM results at the Maximum Power Transfer for the Figure 2.0 circuit.

Compare the above MutliSIM simulation results in **Table 3.0** with your calculated theoretical values in **Table 2.0**. Was the maximum power transfer theorem verified? Explain, and comment on any discrepancies.

Pre-Lab workspace

The measured V_L was 4.18V, which is $V_{TH}/2$.

(c) *Superposition Principle*

(i) For the circuit shown in **Figures 3.0**, consider the input D.C. source voltages, E_1 **= 10V** and E_2 = **4V** (*note the polarities of each source!*). Determine the values of voltage, V_X and current, I_X using either the ***nodal-voltage*** or the ***mesh-current*** analysis technique. Show your analysis below, and record your results in **Table 4.0**.

Pre-Lab workspace

M1:

$0 = -10 + 2.2(i_1) + 3.3(i_1 - i_2) - 4$

$14 = 2.2i_1 + 3.3i_1 - 3.3i_2$

$14 = 5.5i_1 - 3.3i_2$

M2:

$0 = 4 + 3.3(i_2 - i_1) + 2(i_2)$

$-4 = 3.3i_2 - 3.3i_1 + 2i_2$

$-4 = 5.3i_2 - 3.3i_1$

$14 = 5.5i_1 - 3.3i_2$

$-4 = 3.3i_1 + 5.3i_2$

$\rightarrow 46.2 = 18.15i_1 - 10.89i_2$

$-22 = 18.15i_1 + 29.15i_2$

$68.2 = 0 - 40.04i_2$

$-1.7 = i_2$

$V_x = I_2 \cdot R$

$= -1.7(2)$

$= -3.4$

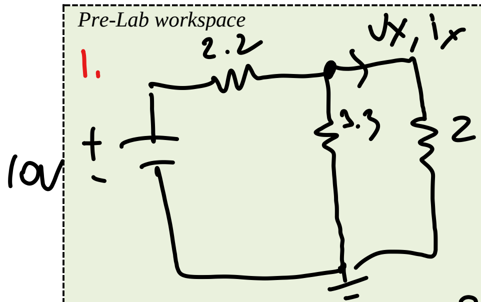
(ii) For the same circuit shown in **Figures 3.0** with the input D.C. source voltages, E_1 **= 10V** and E_2 = **4V**, apply the Superposition Principle technique as follows:-

1. <u>Remove</u> input source, E_2 and <u>replace</u> it with a short-circuit by connecting a wire between "**c**" and "**d**". Determine the resultant voltage, V_{X1} across R_3 and current, I_{X1} through R_3. Show your analysis below, and record the results in **Table 4.0**.

2. <u>Connect</u> input source, E_2 in its original place between "**c**" and "**d**". Be mindful of the polarity connections. Then <u>remove</u> input source, E_1 and <u>replace</u> it with a short-circuit by connecting a wire between "**a**" and "**b**". Determine the resultant voltage, V_{X2} across R_3 and current, I_{X2} through R_3. Show your analysis below, and record the results in **Table 4.0**.

Pre-Lab workspace

1.



$0 = \frac{Vx-0}{3.3} + \frac{Vx-0}{2} + \frac{Vx-10}{2.2}$

$\frac{10}{2.2} = Vx\left(\frac{1}{3.3} + \frac{1}{2} + \frac{1}{2.2}\right)$

$3.6 = Vx_1$

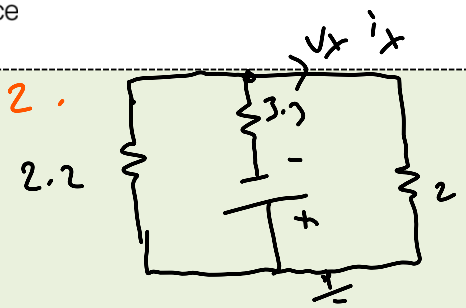
$V = IR$

$I = \frac{V}{R}$

$ix_1 = \frac{3.6}{2}$

$ix_1 = 1.8$

2.



$0 = \frac{Vx-0}{2} + \frac{Vx-4}{3.3} + \frac{Vx-0}{2.2}$

$\frac{4}{3.3} = 1.257\,Vx$

$-0.96 = Vx_2$

$ix_2 = \frac{Vx_2}{R}$

$= \frac{-0.96}{2}$

$ix_2 = -0.48$

$i_T = 1.3$

$V_T = 2.6$

(iii) Construct the circuit of **Figure 3.0** in MultiSIM, and repeat the above circuit-procedures (i) and (ii) to measure V_X, I_X, V_{X1}, I_{X1}, V_{X2} and I_{X2}. Record the results in **Table 4.0**.

- Copy and paste a screenshot showing one MultiSIM readings on the circuit. Include the MultiSIM circuit file (**.ms14**) in your Pre-Lab submission.
- All screenshots should show your name printed on the center-top of the MultiSIM screen

From your results in **Table 4.0**, was the Superposition Principle technique verified using the expressions $V_X = V_{X1} + V_{X2}$ and $I_X = I_{X1} + I_{X2}$? Explain why, and comment on any discrepancies. Does the Superposition Principle make it easier to analyze circuits with multiple power sources? Why?

Pre-Lab workspace

Yes, superposition was verified via multisim, however the mesh analysis values aren't verified, due to calculation errors. In my opinion, superpos makes it easier to analyze with 2 power sources since it cuts down the amount you work with at a time.

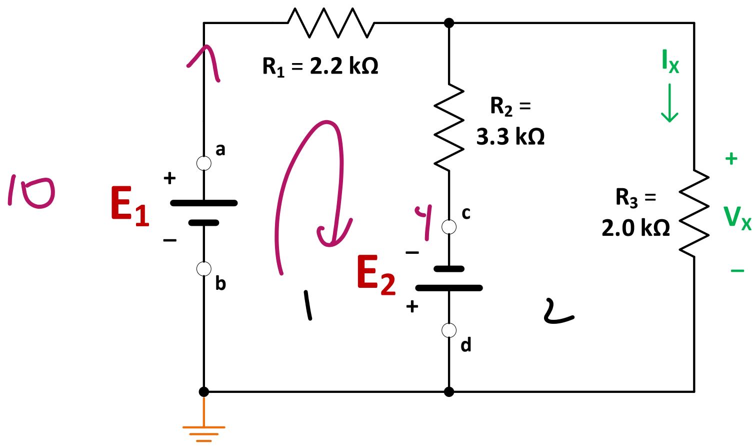


Figure 3.0: Circuit with multiple voltage sources

V_X (volts)		I_X (mA)		V_{X1} (volts)		I_{X1} (mA)		V_{X2} (volts)		I_{X2} (mA)		$V_X = V_{X1} + V_{X2}$		$I_X = I_{X1} + I_{X2}$	
Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.	Th.	MS.
2.6	2.6	1.3	1.3	3.6	3.6	1.8	1.8	-0.96	-0.9	-0.48	-0.48	2.6	2.6	1.3	1.3

Table 4.0: Theoretical (Th.) and MultiSIM (MS.) results of the Figure 3.0 circuits

5.0 IN-LAB Experiment: IMPEMENTATION & MEASUREMENTS

(a) *Thevenin Equivalent Circuit*

Implement the respective circuits in **Figure 2.0b** on your breadboard using the resistor values as shown. Set the input D.C. source voltage, **E** to **10V**. Turn OFF the power supply.

1. Turn ON the power supply.
2. For the circuit at the top in **Figure 2.0b**, use the DMM Voltmeter to measure the open-circuit voltage, V_{OC} between the open-circuit terminals "x" and "y". Record your result in **Table 5.0** below.
3. For the circuit at the bottom in **Figure 2.0b**, use the DMM Ammeter to measure the short-circuit current, I_{SC} through the short-circuit wire between terminals "x" and "y". Record your result in **Table 5.0** below.
4. Turn OFF the power supply.

E	V_{OC} Measured Result (volts)	I_{SC} Measured Value (mA)	$V_{Th} = V_{OC}$ (volts)	$R_{Th} = V_{OC}/I_{SC}$ (kΩ)
10 (volts)	8.367	2.07	8.367	4.04

Table 5.0: Experimental results of the Figure 2.0b circuits

$$R_{th} = \frac{8.367}{2.07} = 4.04$$

(b) *Maximum Power Transfer*

Implement the circuit of **Figure 2.0a** in MultiSIM; set the input D.C. source voltage, **E** to **10V**, and use a potentiometer as the variable load resistance, R_L.

1. Turn OFF the power supply.
2. Locate a **5kΩ potentiometer** (R_P) in your Kit and connect it as illustrated in **Figure 2.0d** and keep track of the potentiometer terminals as wired to the circuit.
3. Turn ON the power supply.
4. Monitor the load voltage, V_L across the variable load, R_P using the DMM Voltmeter.
5. Adjust the potentiometer until the output voltage, V_L is equal to $V_{Th}/2$. Refer to your Pre-Lab analysis for the V_{Th} value to use. Record the value of the output voltage, V_L in **Table 6.0** below.
6. Turn OFF the power supply.
7. Remove the potentiometer off the breadboard, and use the DMM to measure the resultant resistance value between potentiometer terminal "1" and "2" (per **Figure 2.0d**). Record this resistance value as R_L in **Table 6.0** below.
8. Turn OFF the power supply.

Input Source, E	Thevenin voltage, V_{TH} (volts)	Measured load voltage, V_L (volts)	Load resistance R_L per resultant potentiometer, R_P reading. (kΩ)
	From Pre-Lab	Measured Result	Measured Result
10 (volts)	8.36	4.18	4.023

~4k

Table 6.0: Experimental results at the Maximum Power Transfer point for the Figure 2.0 circuit.

(c) *Superposition Principle*

Implement the circuit in **Figure 3.0** on your breadboard using the resistor values as shown. Set the input D.C. voltage sources, E_1 = **10V** and E_2 = **4V** on each respective power-supply. Turn OFF both power supplies. (**Note:** the positive terminal of the power supply E_2 is connected to your ***common ground*** reference point on your breadboard to which the negative terminal of power supply E_1 is also connected).
Setup and connect the DMM **Voltmeter** to monitor the voltage across resistor, R_3; and the DMM **Ammeter** to monitor the current through resistor, R_3.

1. Investigates direct contributions of E_1 and E_2 to V_X and I_X

1. Turn ON both power supplies.
2. Record the readings of the voltage, V_X across resistor, R_3 and the current, I_X through resistor, R_3 in **Table 7.0** below.
3. Turn OFF both power supplies.

2. Investigates contribution of only E_1 to V_X and I_X

1. Remove voltage source, E_2 connections from your breadboard circuit, and replace it with a wire between "**c**" and "**d**" to create a short-circuit.
2. Turn ON the E_1 power supply.
3. Record the readings of the voltage, V_{X1} across resistor, R_3 and the current, I_{X1} through resistor, R_3 in **Table 7.0** below.
4. Turn OFF the E_1 power supply.

3. Investigates contribution of only E_2 to V_X and I_X

1. Remove voltage source, E_1 connections from your breadboard circuit, and replace it with a wire between "**a**" and "**b**" to create a short-circuit.
2. Reconnect input source, E_2 back to its original place between "**c**" and "**d**", and make sure the positive terminal of E_2 power supply is connected to your *common ground* reference point on the breadboard.
3. Turn ON the E_2 power supply, and verify the voltage is still at the original setting of **4V**.
4. Record the readings of the voltage, V_{X2} across resistor, R_3 and the current, I_{X2} through resistor, R_3 in **Table 7.0** below.
5. Turn OFF the E_2 power supply.

V_X (volts)	I_X (mA)	V_{X1} (volts)	I_{X1} (mA)	V_{X2} (volts)	I_{X2} (mA)	$V_X = V_{X1} + V_{X2}$	$I_X = I_{X1} + I_{X2}$
Measured Result	Measured Result	Measured Result	Measured Result	Measured Result	Measured Result	From measured results	From measured results
2.64	1.3	3.6	1.8	-0.967	-0.49[illegible]	2.6	1.3

Table 7.0: Experimental results from the Figure 3.0 related circuit.

6.0 POST-LAB: OBSERVATIONS AND ANALYSIS OF RESULTS

(a) *Thevenin Equivalent Circuit*

Workspace

- From your observations of the results in **Table 5.0**, compare these results to their corresponding values in **Table 2.0** obtained from the Pre-Lab exercise? Explain possible causes of any discrepancies.

yes, table 5 & 2 are the same.

- Was the concept of Thevenin's equivalent circuit verified? Explain.

Thevenin's equivalent was verified, since the values calculated from the lab using real life circuitry equalled to those found in the theoretical calculations

(b) *Maximum Power Transfer*

Workspace

- Explain how your experiment results of V_L and R_L in **Table 6.0** compare to the corresponding values in **Table 3.0**? Comment on any discrepancies.

The V_L values are the same, however the R_L values differ ~0.1, which could be the result of inaccurately measuring the real life circuit

- Did the experiment results verify the maximum power transfer theorem? Explain.

yes, the results verified Pmax theorem, since the theoretical and experimental values are reasonably close to each other.

(c) *Superposition Principle*

Workspace

- From your observation of the experiment results in **Table 7.0**, were $V_X = V_{X1} + V_{X2}$ and $I_X = I_{X1} + I_{X2}$ relationships satisfied per the Superposition Principle? Explain.

Yes, Vx & ix equations were satisfied in the experimental results. The sum of the experimental Vx1 & Vx2 equalled Vx, same for ix1 & ix2 equalling ix. Since these values were calculted through the shorting of V sources, the superposition principle was followed and therefore validates the equation.

- How do the results in **Table 7.0** compare to those in **Table 4.0**? Comment on any discrepancies.

The values are the same.

- What have you discovered about the Superposition Principle?

I discovered that superposition makes it way easier to create & calculate V & i for circuts with a lot of v sources.

7.0 LAB REPORT REQUIREMENTS & GUIDELINES

Lab reporting is to be completed and submitted separately as **Part I** and **Part II**, noted below:

Part I (**Pre-Lab Work**) => represents **40%** of the pre-assigned Lab weight.

Pre-Lab Work (assignment) of **Section 4.0** that includes handwritten calculations, MultiSIM results, and analysis is to be completed and submitted **prior to the start** of your scheduled lab. *The grading is commensurate with completeness and accuracy of your handwritten calculations, analysis and MultiSIM simulation circuits/plots.*

Note the following requirements for the document submission for Part I:

- A completed and signed "COVER PAGE – **Part I**" has to be included with your submission, a copy of which is available on D2L. The report will not be graded if the signed cover page is not included.
- Your completed handwritten pages of **Section 4.0** should be scanned (via a scanner or phone images), together with the required MultiSIM images. **Note:** *MultiSIM results must be generated using the Department's licensed version of MultiSIM, and the captured screenshots should show your name (at the center-top) and the timestamp (at the bottom-right corner of your screen).*
- Collate and create a .pdf or .docx file of the above, and upload it via D2L **any time prior to the start of your scheduled lab**. Upload instructions are provided on D2L.

Zero marks will be assigned for the entire lab if this Part I is not submitted prior to your scheduled lab.

Part II (**In-Lab Work** and **Post-Lab Work**) => represents **60%** of the pre-assigned Lab weight.

In-Lab Work (**Section 5.0**) and **Post-Lab Work** (**Section 6.0**) that include in-lab results, handwritten analysis and observations are to be completed and submitted **by 11.59 p.m.** of the same day as your scheduled lab. *The grading is commensurate with: - completeness, correctness and collection of all experimental results (data and waveforms); merits of observation of the correlations between the experimental and pre-lab assignment results; and reasonableness of the answers to questions posed.*

Note the following requirements for the document submission for Part II:

- A completed and signed "COVER PAGE – **Part II**" has to be included with your submission, a copy of which is available on D2L. The report will not be graded if the signed cover page is not included.
- Scan your completed pages of **Section 5.0** and **Section 6.0** (via a scanner or phone images), together with any required In-Lab Oscilloscope screen-shot images.
- Collate and create a .pdf or .docx file of the above, and upload it via D2L **by 11.59 p.m. on the same day** your lab is scheduled. Late submissions will not be graded.