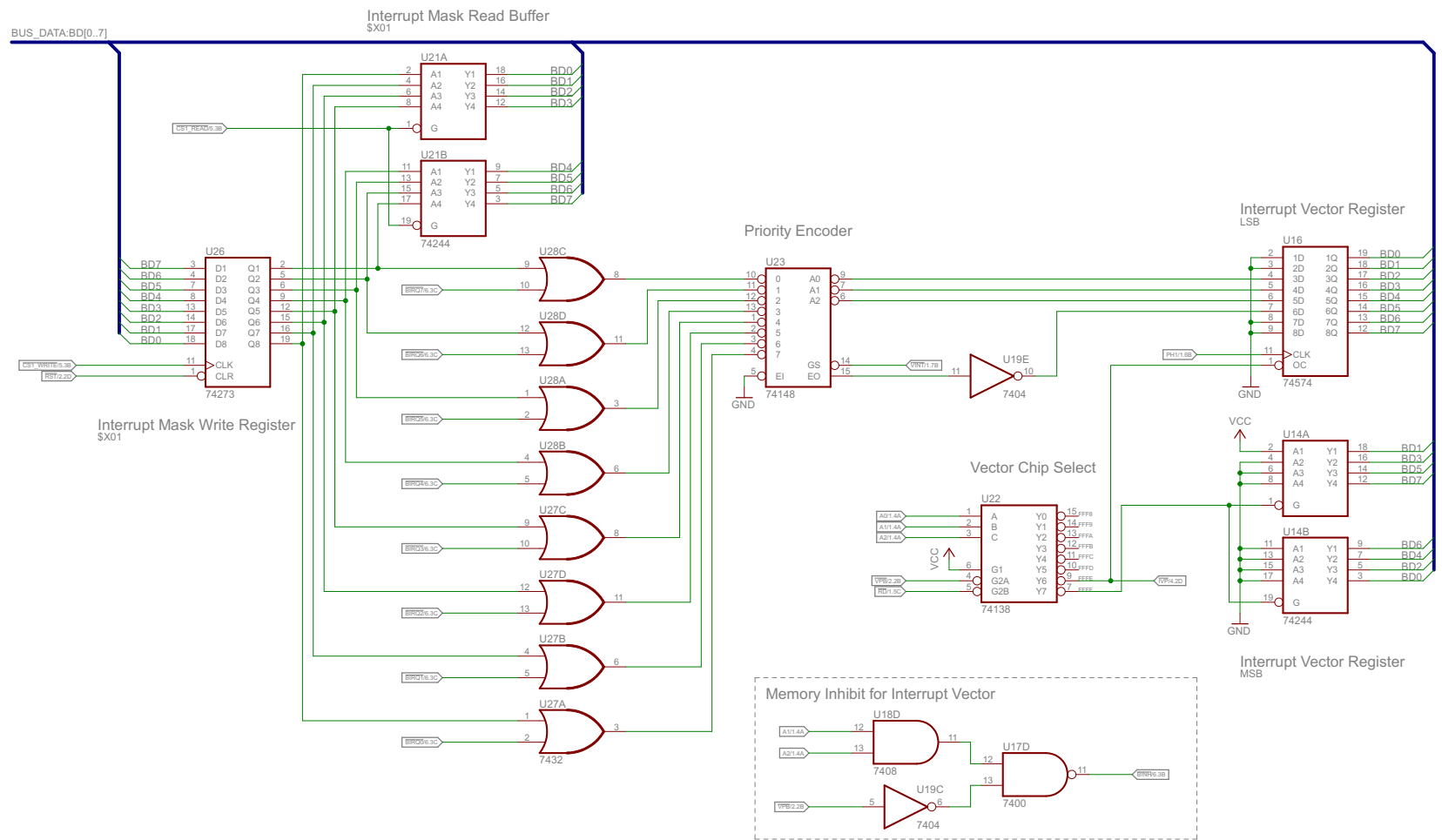


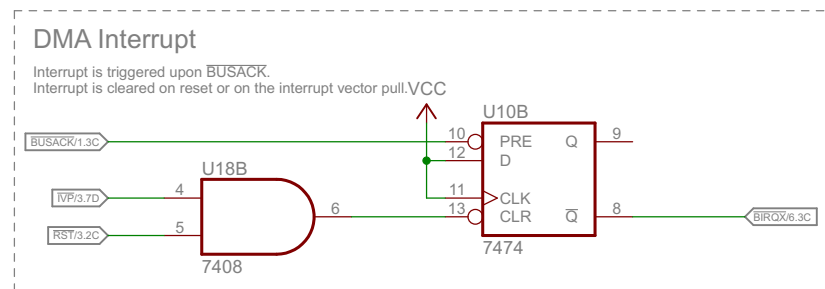
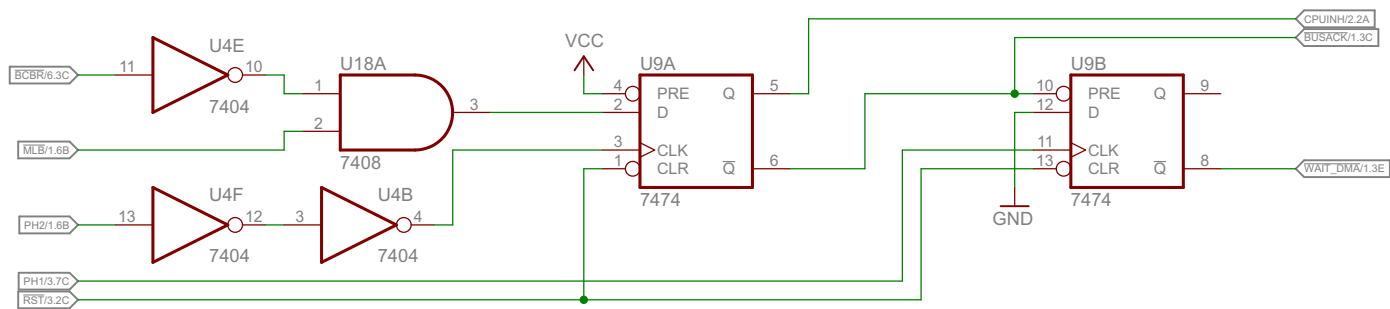
Bank Switcher	
Generates address bits A19-A15 based on current CPU address and the bank register.	
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Interrupt Vector Generator

Takes individual card-specific interrupt requests and generates a prioritized interrupt vector. Individual IRQ lines can be masked with \$X01

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DMA System

Stops CPU operation on request and releases the bus when safe, then acknowledges the request. An interrupt is triggered for each request.

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V2.1

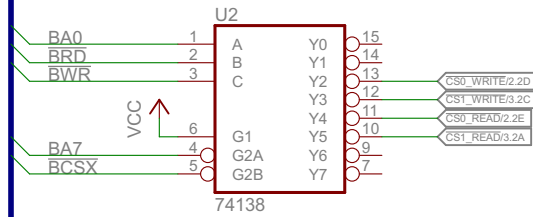
3/24/2019 11:04:00 AM

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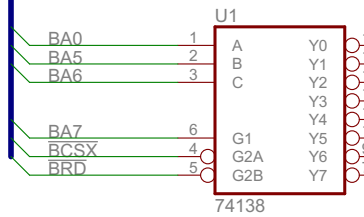
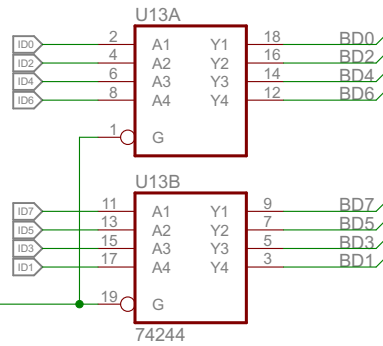
INTERNAL_ADDRESS:A[0..15]

BUS_DATA:BD[0..7]

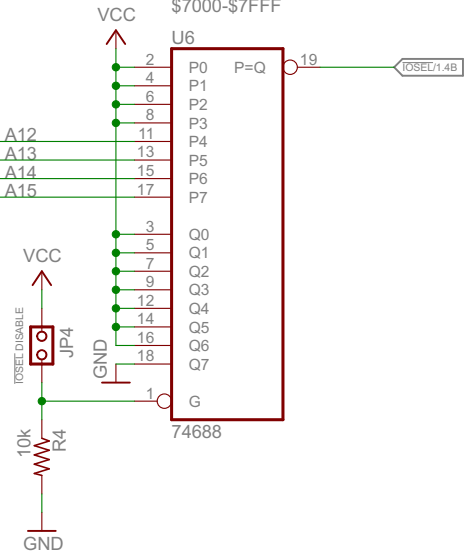
BUS_ADDRESS:BA[0..19],BRD,BWR,BCSX



Card ID Register
\$XFF



IO Comparator
\$7000-\$7FFF



Chip Selects

Generates chip select signals for onboard registers.
IO Comparator generates I/O Select signal.

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