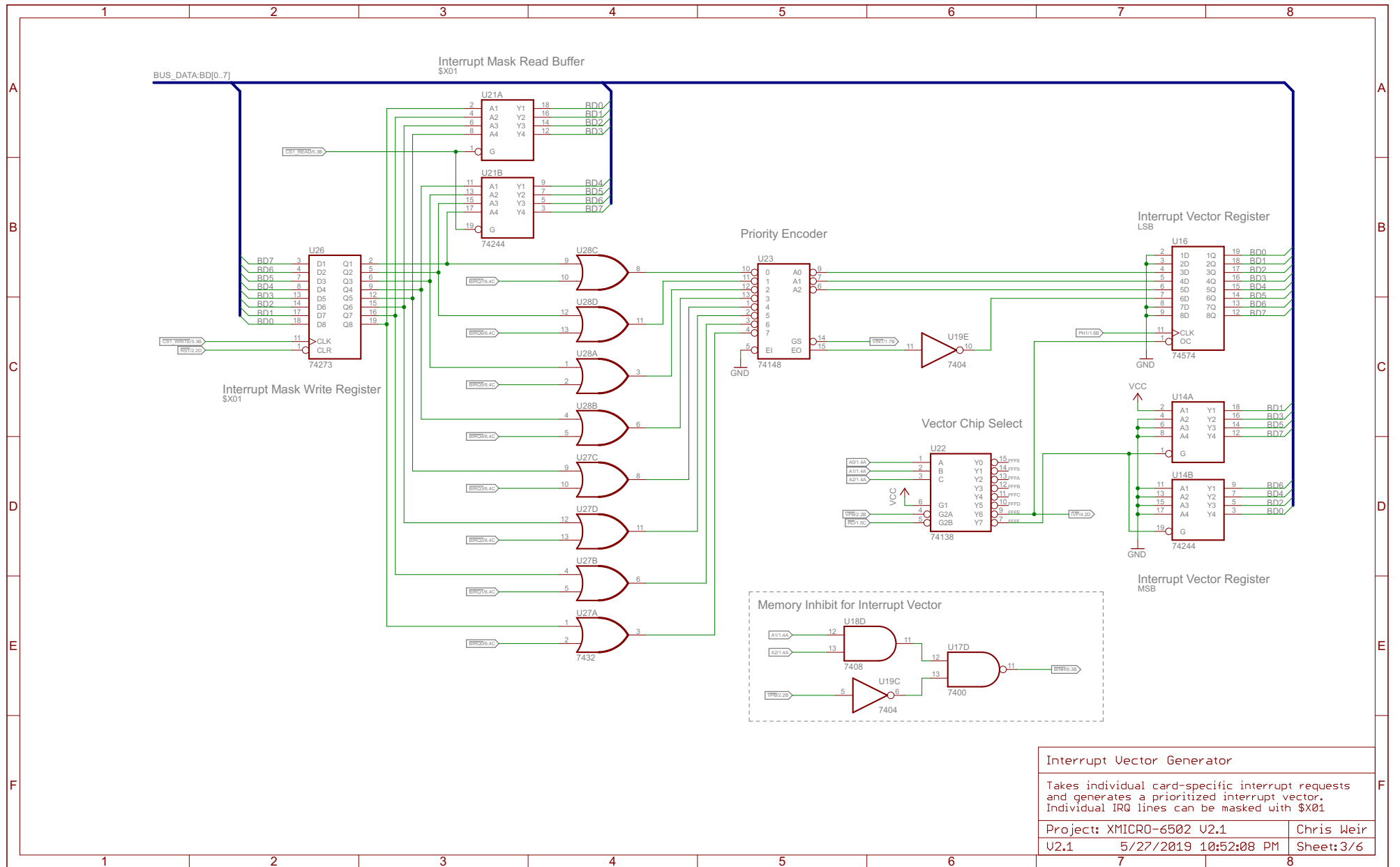
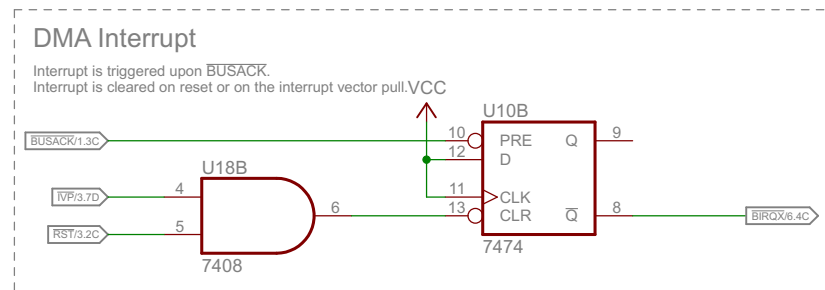
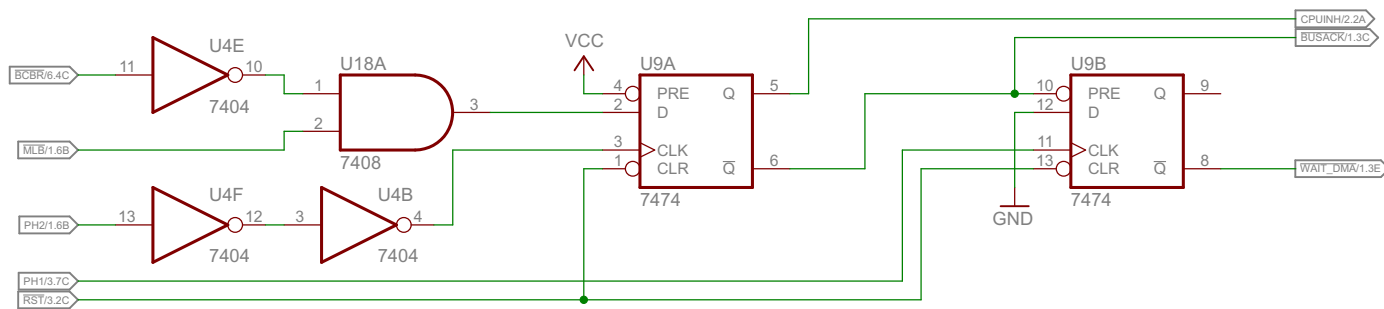


CPU		
W65C02S CPU, clock, signal buffers, and control logic		
Project: XMICRO-6502 U2.1	Chris Weir	
U2.1	5/27/2019 10:52:08 PM	Sheet:1/6





DMA System

Stops CPU operation on request and releases the bus when safe, then acknowledges the request. An interrupt is triggered for each request.

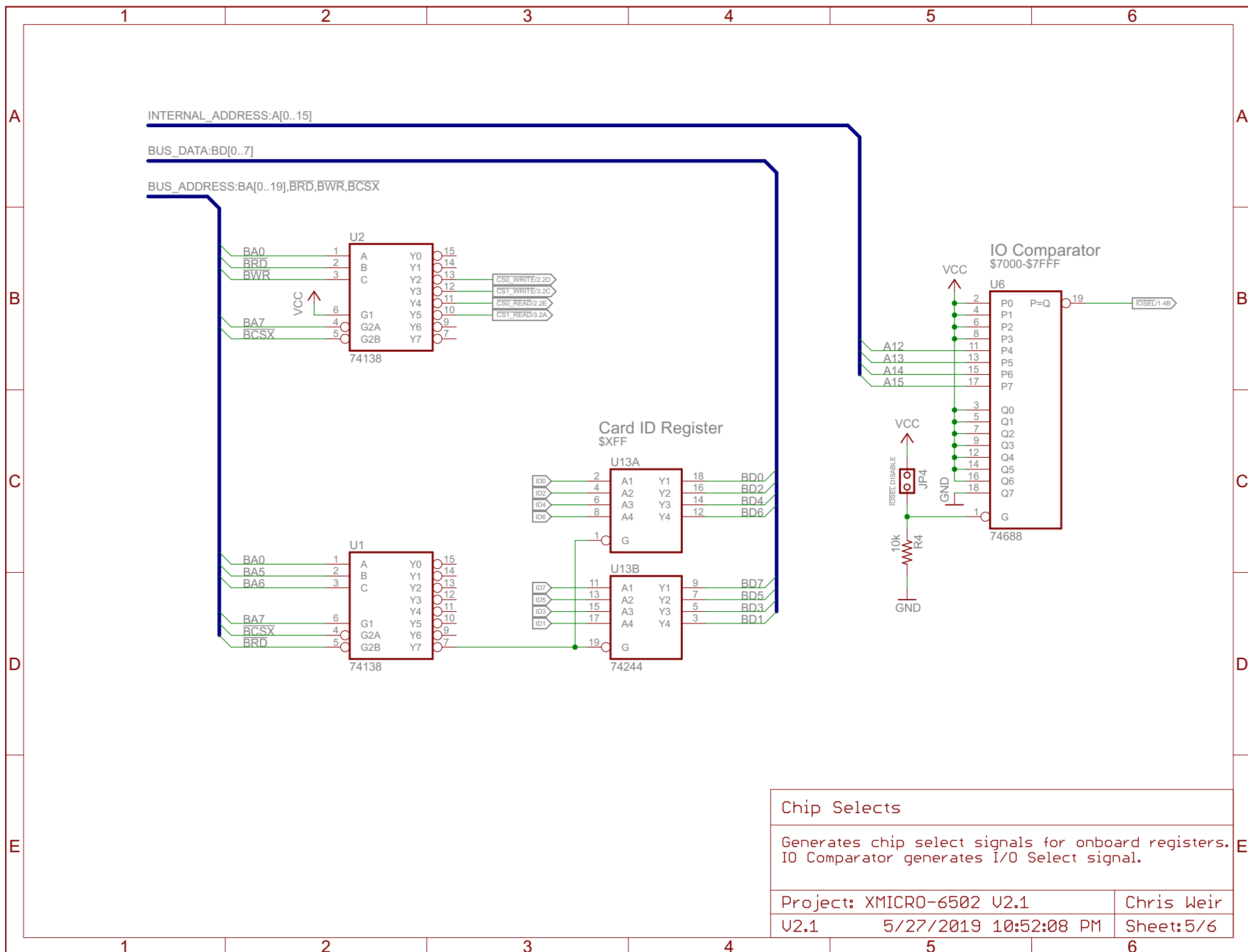
Project: XMICRO-6502 V2.1

Chris Weir

V2.1

5/27/2019 10:52:08 PM

Sheet: 4/6



Chip Selects		
Generates chip select signals for onboard registers. IO Comparator generates I/O Select signal.		
Project: XMICRO-6502 V2.1	Chris Weir	
V2.1	5/27/2019 10:52:08 PM	Sheet: 5/6

