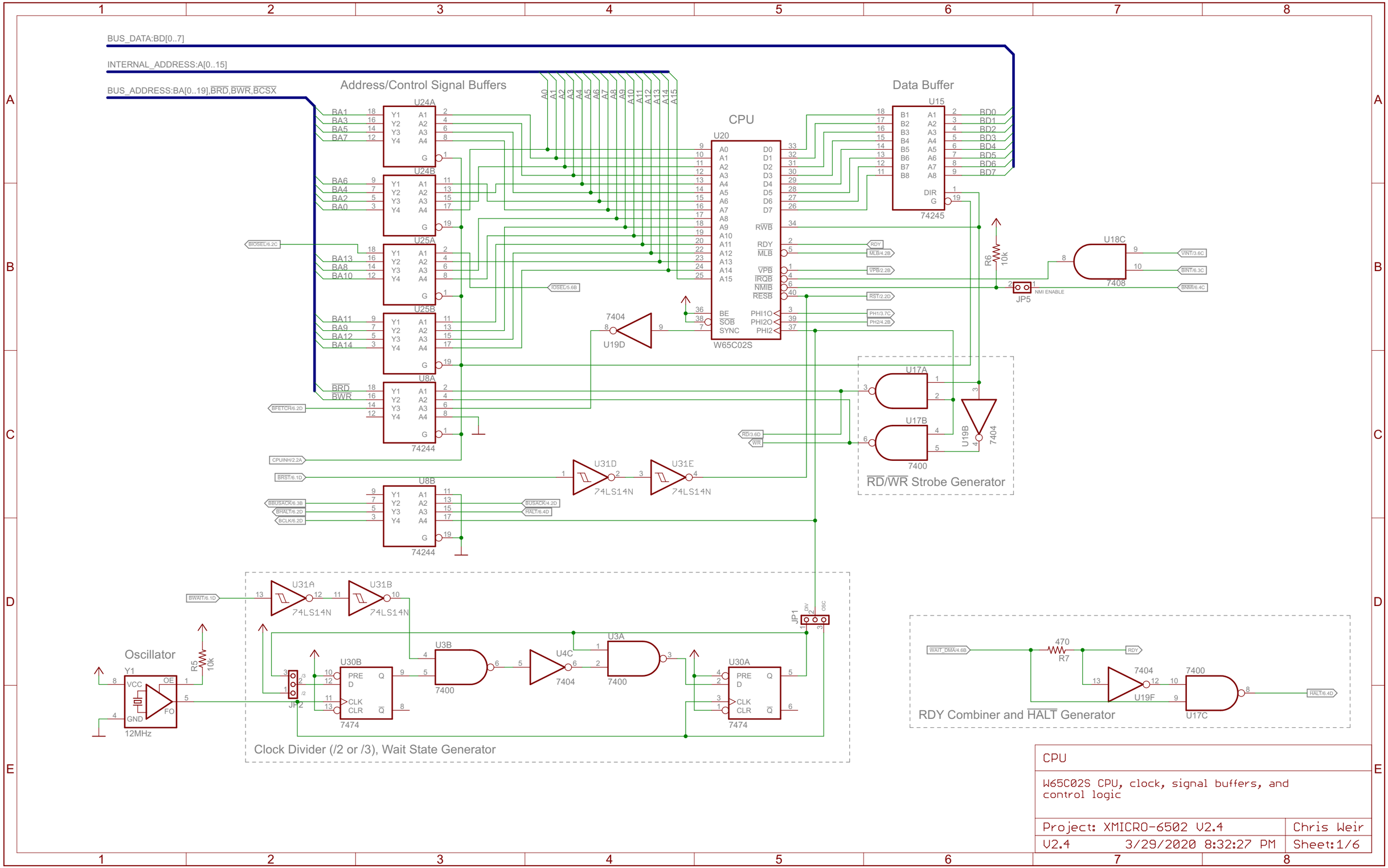
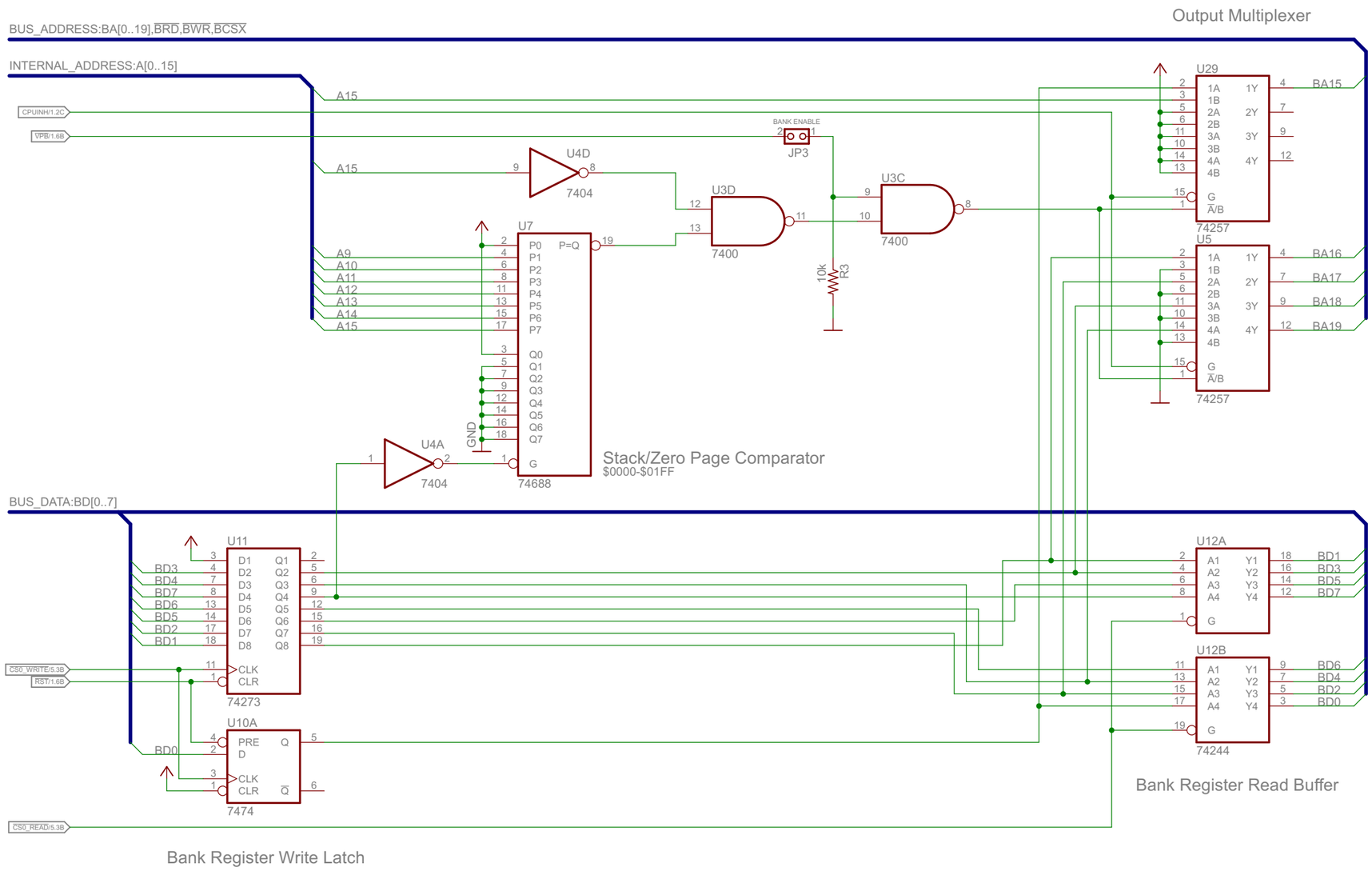

BUS_DATA:BD[0..7]
INTERNAL_ADDRESS:A[0..15]
BUS_ADDRESS:BA[0..19],BRD,BWR,BCSX
Address/Control Signal Buffers
U24A
U24B
U25A
U25B
U8A
U8B
74244
CPU
U20
W65C02S
Data Buffer
U15
74245
U18C
7408
JP5
NMI ENABLE
R6
10k
U19D
7404
U17A
U17B
7400
U19B
RD/WR Strobe Generator
U31D
U31E
74LS14N
U31A
U31B
JP1
JP2
Oscillator
Y1
12MHz
R5
10k
U30B
U30A
7474
U3B
U3A
U4C
Clock Divider (/2 or /3), Wait State Generator
470
R7
U19F
U17C
RDY Combiner and HALT Generator
CPU
W65C02S CPU, clock, signal buffers, and control logic
Project: XMICRO-6502 V2.4
Chris Weir
V2.4
3/29/2020 8:32:27 PM
Sheet:1/6



Bank Switcher

Generates address bits A19-A15 based on current CPU address and the bank register.

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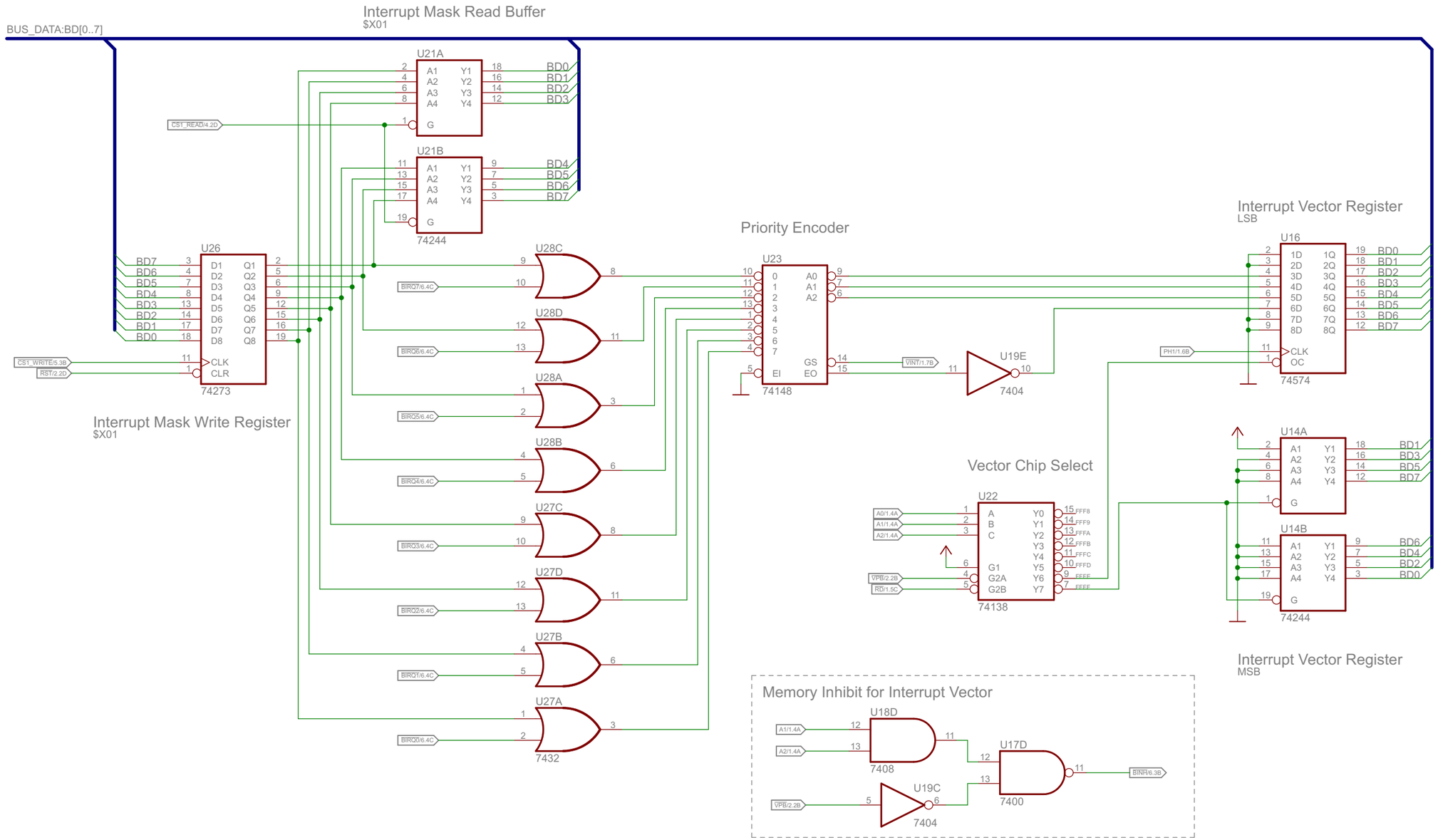
V2.4 3/29/2020 8:32:27 PM	Sheet:2/6



Interrupt Vector Generator

Takes individual card-specific interrupt requests and generates a prioritized interrupt vector. Individual IRQ lines can be masked with $X01

Project: XMICRO-6502 V2.4	Chris Weir
V2.4 3/29/2020 8:32:27 PM	Sheet:3/6