XMICRO BUS

Technical Specifications

V0.1 2018-10-08

Features:

8-bit Data Field Width
1 Megabyte Memory Address Range
Memory-mapped I/O
Asynchronous Data Transfer
Multiple Masters
Position Independence of Cards in Backplane
Automatic position-based Resource Allocation
Hardware Self-Discovery and Configuration
Main Memory Inhibit Signal
CPU Architecture Independence
ATX Power Supply Compatibility
Standard 62-pin Card Edge Connector
Fully Open-source

Functional Description

Elements of a System

An XMICRO system consists of the following elements:

- Backplane
- Primary Master
- Secondary Masters
- Slaves

An XMICRO *Backplane* is the basis of any system. In its simplest form, the backplane handles power and signal distribution, and card-specific signal routing. Typically it should also include address-based card selection, signal combination circuitry for $\overline{\text{CINH}}$ and $\overline{\text{CBR}}$, and a power-on reset circuit. More complex implementations may add significantly more functionality, including peripherals or an onboard primary master. When a primary master is built into a backplane, it should be referred to as a motherboard.

A *Primary Master* is a card or motherboard which acts as the default system controller. Typically this will be the main "CPU" card. In the context of this document, the "system controller" is the device driving the A<19..0>, $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{FETCH}}$ signals. Primary masters must default to this operation unless the bus is requested by another device. Only primary masters handle interrupt signals and bus requests.

A *Secondary Master* is a card with the ability to act as a temporary system controller. This is generally used for DMA operations by the secondary master, independent of the primary master.

A *Slave* is a card with no ability to control the system. Slaves are only capable of reading/writing data under the command of a master.

Note: The master/slave designation is somewhat loose and is used only as a broad classification of the functionality of a device. It may be used to refer to either a discrete subsystem or a card as a whole.

Signal Lines

Power Supply Rails (+12V, +5V, +5VSB +3.3V, GND, -12V)

These lines supply power to the bus. Current capacity is defined by the backplane's specifications, however it is not recomended to exceed 1.5A per card on any rail. If more current is required, an external power connection should be added to the card. Voltage tolerances match the ATX standard. It is recommended that a standard ATX power supply be used.

Address Lines (A<19..0>)

Twenty unidirectional lines driven by the master to specify a memory location.

Data Lines (D<7..0>)

Eight bi-directional lines which carry information between master and slave devices.

Read Strobe ($\overline{\text{RD}}$)

Asserted by the master to indicate that the addressed slave device may place data on the data lines.

Write Strobe ($\overline{\text{WR}}$)

Asserted by the master to indicate that it has placed data on the data lines.

Reset ($\overline{\text{RST}}$)

This open-collector signal resets the system into a known state. During the power-on sequence, this signal should be asserted by the backplane until at least 250ms after all power supply rails have stabilized.

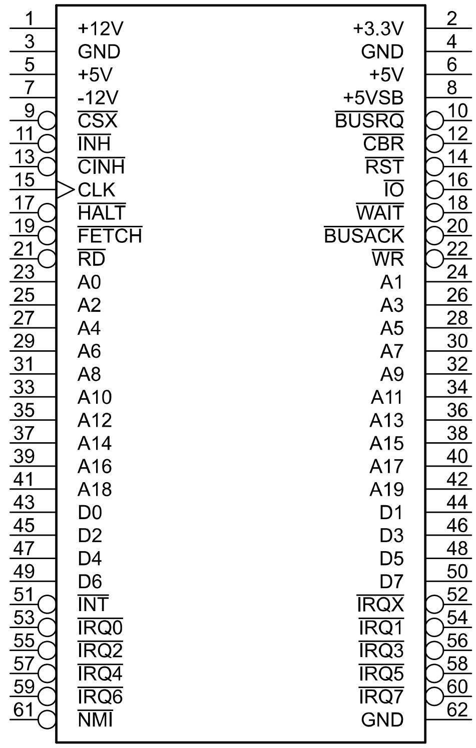


Figure 1: Bus Connector Pinout

System Clock (CLK)

This signal is the main system clock. Care should be taken to ensure it is a clean square wave with a 50% duty cycle. Its frequency is undefined. The primary master should typically provide this signal, however it may optionally be provided by another card such as a video card. It is recommended that primary masters do not require externally generated clock signals to function.

I/O Request ($\overline{\text{IO}}$)

Asserted by the master to address the backplane's card I/O space.

Wait ($\overline{\text{WAIT}}$)

This open-collector line is asserted to inform the master that the current data operation is not yet ready for completion. The master should wait until this signal is released to continue. Not to be confused with $\overline{\text{HALT}}$.

Halt ($\overline{\text{HALT}}$)

This line is asserted by the primary master to indicate to that it is in a halted state and waiting for an interrupt. Not to be confused with $\overline{\text{WAIT}}$.

Instruction Fetch ($\overline{\text{FETCH}}$)

This signal is asserted by the primary master when the current data transfer operation is an instruction fetch.

Main Memory Inhibit ($\overline{\text{INH}}$)

This slot-independent line is used to inhibit general-purpose main memory. When $\overline{\text{INH}}$ is asserted, main memory must be prevented from reading or writing data, or driving the bus. This precludes the need for special hardware configuration when using devices requiring additional address space.

Bus Request ($\overline{\text{BUSRQ}}$)

This slot-independent line is driven by a secondary master to request control of the bus. When the primary master is ready to release control of the bus, it will assert $\overline{\text{BUSACK}}$.

Bus Acknowledge ($\overline{\text{BUSACK}}$)
This signal is held low by the primary master to indicate that it has released the bus for control by a secondary master. The secondary master may only control the bus while this signal is asserted.

Card Select X ($\overline{\text{CSX}}$)
This slot-specific signal is driven by the backplane to indicate that the current address is within the range of the slot's allocated address space. While this signal is asserted, A<19..8> may be ignored by the card because their state is known.

Interrupt Request X ($\overline{\text{IRQX}}$)
This slot-specific line is driven by a card to indicate that it requires the primary master's attention. It is routed to the appropriate input by the backplane. This allows for interrupt vectoring and prioritization based on card position. This is a level-triggered interrupt signal.

Interrupt Request ($\overline{\text{IRQ}}$<7..0>)
These eight lines are driven by cards through the IRQX line. They are used by the primary master for interrupt prioritization and vectoring. Under no circumstances are these lines to be driven directly by a card.

Interrupt ($\overline{\text{INT}}$)
This open-collector signal is used for special purposes where it is necessary to bypass a primary master's onboard interrupt handling circuitry. Typically this is only used to expand interrupt vectoring capabilities on backplanes with more than eight slots. Primary masters must accept this signal, either by including it in their interrupt handling scheme or combining it with the CPU's raw interrupt input. This is a level-triggered interrupt signal.

Non-maskable Interrupt ($\overline{\text{NMI}}$)
Open-collector edge-triggered interrupt signal. Its use is unusual, so it is recommended that this signal be optional on any card using it. This should only be used for emergency signals requiring the immediate attention of the primary master, such as memory errors or power failure. The use of this signal for video timing is discouraged due to compatibiltiy concerns. When possible, primary masters should give this signal an immediate priority override of in-progress interrupts and DMA transfers.

Combined Signals ($\overline{\text{CINH}}$, $\overline{\text{CBR}}$)
These two lines are the combined output of the each slot's $\overline{\text{INH}}$ and $\overline{\text{BUSRQ}}$ signals respectively. In testing it was found that open-collector signals did not exhibit fast enough performance to be used for the memory inhibit function. Instead, each card's $\overline{\text{INH}}$ line is combined on the backplane using a high-speed AND to form the $\overline{\text{CINH}}$ signal. The same is true of the $\overline{\text{BUSRQ}}$ lines to form $\overline{\text{CBR}}$. The result is that the combined signal is asserted if any of the constituent signals is asserted. These signals are only used by devices *accepting* the $\overline{\text{INH}}$ or $\overline{\text{BUSRQ}}$ signals, such as memory cards or primary masters and shound only be driven by the combining circuit.

Signalling

Bus Arbitration

In the system's default state, a primary master takes full control of the system bus. By asserting the $\overline{\text{BUSRQ}}$ line, a secondary master may request to temporarily take over control of some of the bus signals in order to directly access memory. When $\overline{\text{BUSRQ}}$ is asserted, the primary master gracefully pauses operation

The $\overline{\text{BUSACK}}$ signal indicates that the primary master has placed the following signals in a high-impedance state:

- A<19..0>
- D<7..0>
- $\overline{\text{RD}}$
- $\overline{\text{WR}}$

These signals may be driven by a secondary master only while $\overline{\text{BUSACK}}$ is asserted.

If the $\overline{\text{BUSACK}}$ signal is de-asserted before the secondary master de-asserts $\overline{\text{BUSRQ}}$, the secondary master must release the bus signals and wait until $\overline{\text{BUSACK}}$ is once again asserted to continue the operation. The secondary master may terminate the operation early.

In order to prevent bus contention, secondary masters should wait for a command from the primary master before initiating a bus request, and must not initiate a bus request until the $\overline{\text{BUSRQ}}$ **(and $\overline{\textbf{BUSACK}}$?)** signals are no longer asserted.

Electrical Specifications

Power Supply Characteristics

- A backplane must supply cards with the following voltages: +3.3V, +5V, +12V, -12V, +5VSB.
- Specifications of the power supply are to match the ATX standard.
- The use of an ATX power supply is recommended.
- Cards requiring significant supply current may also use standard 4-pin male Molex 8981 connectors to supplement the +5V and +12V rails. Unless isolated, these must be supplied by the same power supply system and must not conflict with the backplane's supply rails.

Signal Characteristics

- A receiver must recognize a voltage of ≤ 0.8V as a logic 0, and a voltage of ≥ 2.0V as a logic 1.
- The minimum sink current capability of any driver on any line must be 24mA at 0.5V. Further, it is recommended that drivers with minimum source capability of 24mA at 2.4V be used.
- The minimum rise and fall transition times (10%-90%) of any line driving device must be > 5ns when driving a capacitive load of 45pF.

Connectors

- The average current on any connector pin must not exceed 1A.

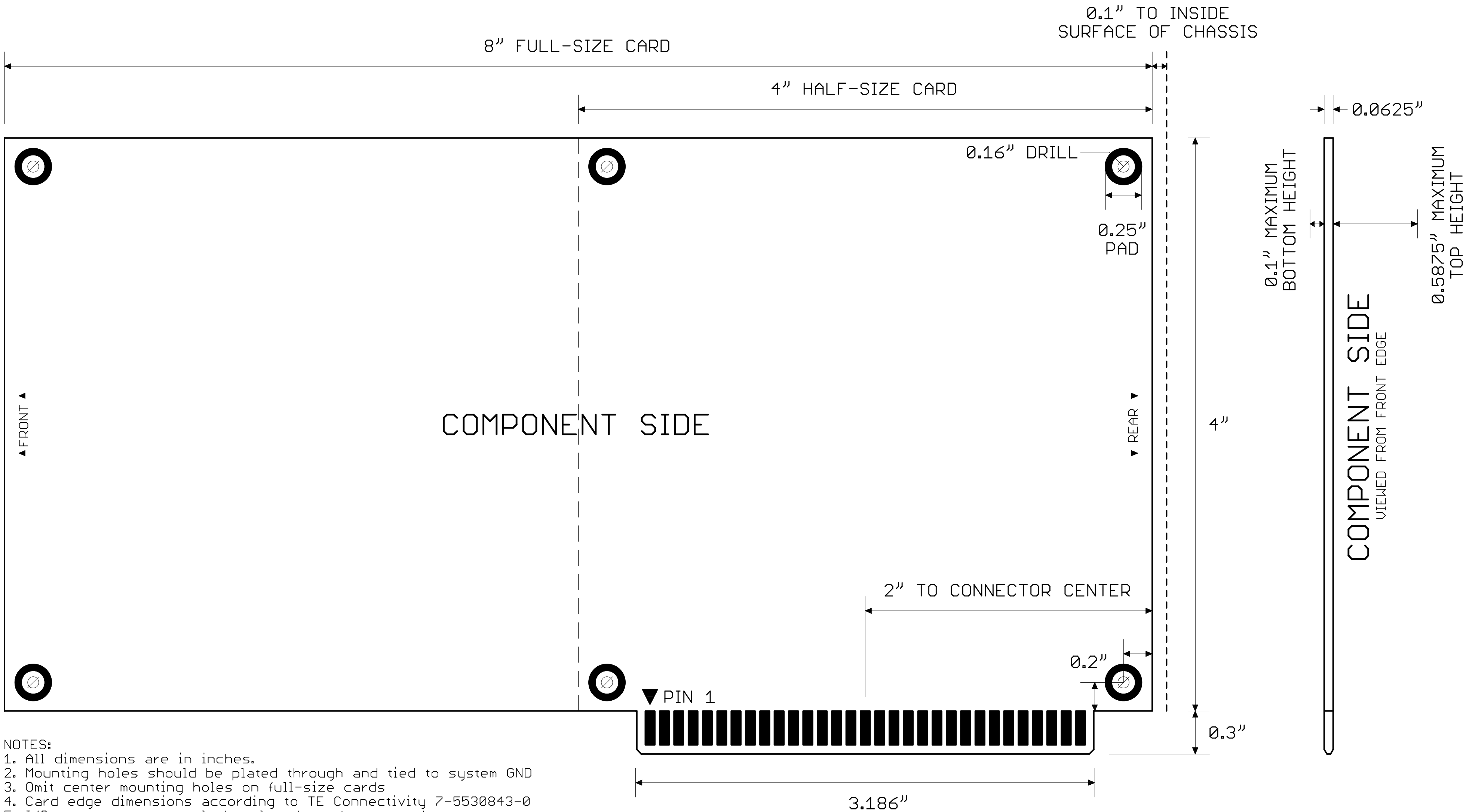
Physical Specifications

Cards

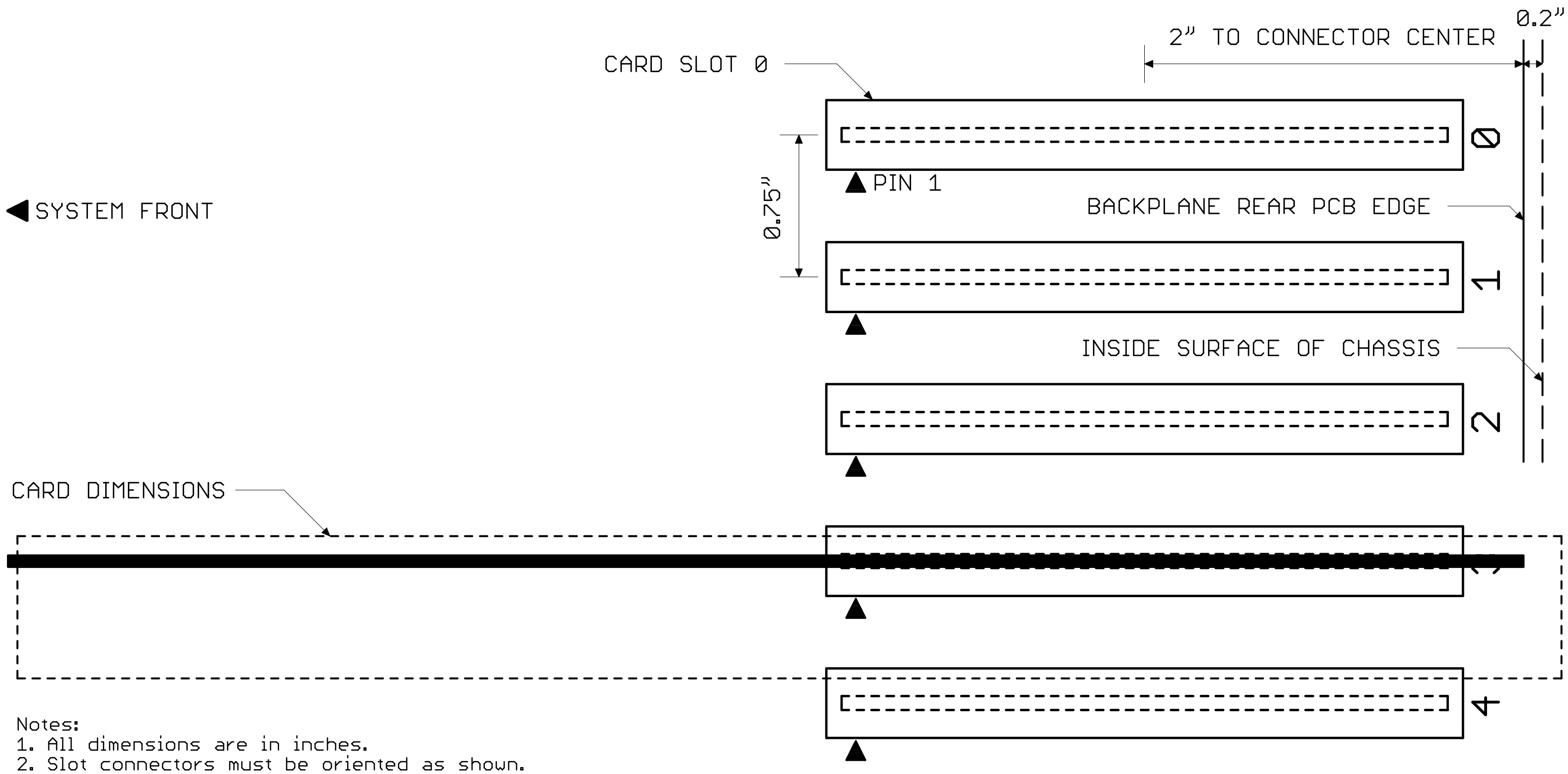
- Cards must connect to the backplane using a 62-pin 0.1 inch pitch card edge connector.
- Card edges must be 3.186" ±0.014" in length and 0.3" in height.
- Card edges should be gold-plated for better reliability. HASL or similar surface finishes are discouraged.
- Card edges should be chamfered for easier insertion.
- A card's dimensions must not exceed the overall dimensions shown in FIGURE X
- The use of standard "full-size" and "half-size" card form-factors is encouraged but not required.

Backplanes

-



NOTES:
1. All dimensions are in inches.
2. Mounting holes should be plated through and tied to system GND
3. Omit center mounting holes on full-size cards
4. Card edge dimensions according to TE Connectivity 7-5530843-0
5. I/O connectors may only be placed on the rear edge.
6. Other edges require 0.05” component clearence.



Notes:
1. All dimensions are in inches.
2. Slot connectors must be oriented as shown.
3. Pin 1 must be marked on at least one slot.
4. Each slot number must be indicated on the PCB.
5. All backplane slots must fit full-dimension cards.
6. Maximum component height under cards may not exceed the edge connectors.