XMICRO BUS

Technical Specifications

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1. General Description

1.1 Features

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- CPU Architecture Independence
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- 1 Megabyte Memory Address Range
- Discrete I/O Address Range
- Asynchronous Data Transfer
- Multiple Masters
- Automatic Resource Allocation
- Hardware Self-Discovery
- ATX Power Supply Compatibility
- Fully Open-source

1.2 Overview

The XMICRO Bus is at its core a collection of signals which are used to interconnect many devices to form a microcomputer system. Discrete modules called “cards” communicate with one another through this bus over a backplane. Each card slot on the backplane is assigned a 256 byte address space and an interrupt request line. This uniform resource allocation allows most cards to be installed in the system with little or no special hardware configuration. Another advantage of this is the ability to use multiple identical cards in the same system without conflicts.

An XMICRO system consists of the following elements:

- Backplane
- Primary Master
- Secondary Masters
- Slaves

A *Backplane* is the basis of any system. In its simplest form, the backplane handles power and signal distribution, decodes I/O addresses, and provides a power-on reset signal. Each backplane contains a number of *slots*, into which *cards* may be inserted to build and expand the system. More complex implementations may add significantly more functionality, including peripherals or an onboard CPU.

A *Primary Master* is a device which acts as the default system controller. Typically this will be the main “CPU” card. Primary masters must default to this operation unless the bus is requested by another device. Only primary masters handle interrupt signals and bus requests.

A *Secondary Master* is a device with the ability to act as a temporary system controller. This is used for DMA operations by the secondary master.

A *Slave* is a device with no ability to control the system. Slaves are only capable of reading/writing data under the command of a master.

Note: The master/slave designation is used only as a broad classification of the functionality of a device. It may be used to refer to either a discrete subsystem or a card as a whole.

1.3 Terminology

Backplane: The central component of the system which provides bus power and signals to all devices.

Motherboard: A backplane containing an integrated Primary Master

Slot: A uniquely identified set of resources and position on a backplane where a card may be installed.

Card: A discrete module which interfaces with a backplane through a slot.

Master: The current active system controller. This could be either the Primary Master of a Secondary Master.

1.4 Signal Notation

1) Active-low signals are denoted by an $\overline{\text{OVERLINE}}$.
2) A range of similar signals are referred to collectively using the format A<19..0>. This example is an abbreviation of signals A19 through A0.

1.5 Numerical Notation

1) All hexadecimal numbers have a leading dollar sign ($).
2) All address values are referenced using hexadecimal notation.
3) Memory addresses use a 5-digit hexadecimal value corresponding to the values of A<19..0>. Example: $01234
4) Variable I/O addresses use a two-digit haxadecimal value formatted as $X00, where X indicates a variable slot number.

2. Signaling

2.1 Signal Lines

2.1.1 Address Lines (A<19..0>)

Twenty unidirectional lines driven by the master to specify a memory or I/O location.

2.1.2 Data Lines (D<7..0>)

Eight bi-directional lines which carry information between master and slave devices.

2.1.3 Read Strobe ($\overline{RD}$)

Asserted by the master to indicate that the addressed slave device may place data on the data lines.

2.1.4 Write Strobe ($\overline{WR}$)

Asserted by the master to indicate that it has placed data on the data lines.

2.1.5 I/O Select ($\overline{IOSEL}$)

Asserted by the master to access the backplane's card I/O space. When asserted, A<11..8> determine which backplane slot is being addressed.

2.1.6 Card Select X ($\overline{CSX}$)

This slot-specific signal is driven by the backplane to indicate that the current address is within the range of the slot's allocated address space. While this signal is asserted, A<19..8> may be ignored by the card because their state is known. Note: this is a discreet signal for each card slot, provided by the backplane.

2.1.7 Main Memory Inhibit ($\overline{INH}$)

This slot-independent line is used to inhibit general-purpose main memory. When $\overline{INH}$ is asserted, main memory must be prevented from reading or writing data, or driving the bus. This allows cards to make special-purpose memory available without reconfiguring or replacing the entire memory system.

2.1.8 Wait ($\overline{WAIT}$)

This open-collector line is asserted by a slave device to indicate that a data transaction is not yet ready to be completed. If $\overline{WAIT}$ is asserted concurrently with $\overline{RD}$ or $\overline{WR}$, the master must hold all Group A signals in their current state until after $\overline{WAIT}$ is deasserted.

2.1.9 Reset ($\overline{RST}$)

This open-collector signal resets the system into a known state. During the power-on sequence, this signal should be asserted by the backplane until at least 250ms after all power supply rails have stabilized.

2.1.10 Bus Request ($\overline{BRQ}$)

This open-collector signal is driven by a secondary master to request control of the bus. When the primary master is ready to release control of the bus, it will assert $\overline{ACK}$.

2.1.11 Bus Acknowledge ($\overline{ACK}$)

This signal is held low by the primary master to indicate that it has released the bus for control by a secondary master. The secondary master may only control the bus while this signal is asserted.

2.1.12 Halt ($\overline{\text{HALT}}$)

This status line is asserted by the primary master to indicate to that it is in a halted state and waiting for an interrupt. Not to be confused with $\overline{\text{WAIT}}$.

2.1.13 Instruction Fetch ($\overline{\text{FETCH}}$)

This signal is asserted by the primary master when the current data transfer operation is an instruction fetch.

2.1.14 Interrupt Request X ($\overline{\text{IRQX}}$)

This slot-specific line is driven by a card to indicate that it requires the primary master's attention. It is routed to the appropriate input by the backplane. This allows for interrupt vectoring and prioritization based on card position. This is a level-triggered interrupt signal.

2.1.15 Interrupt Request ($\overline{\text{IRQ}}$<7..0>)

These eight lines are driven by cards 7-0 through the IRQX signal. They are used by the primary master for interrupt prioritization and vectoring. Under no circumstances are these lines to be driven directly by a card.

2.1.16 Interrupt ($\overline{\text{INT}}$)

This open-collector signal is used for special purposes where it is necessary to bypass a primary master's onboard interrupt handling circuitry. Typically this is only used to expand interrupt capabilities on backplanes with more than eight slots. Primary masters must accept this signal, either by including it in their interrupt handling scheme or combining it with the CPU's raw interrupt input. This is a level-triggered interrupt signal.

2.1.17 Non-maskable Interrupt ($\overline{\text{NMI}}$)

Open-collector edge-triggered interrupt signal. Its use is unusual, so it is recommended that this signal be optional on any card using it. $\overline{\text{NMI}}$ should only be used for special signals requiring the immediate attention of the primary master, such as memory errors, power failure, or video timing. When possible, primary masters should give this signal an immediate priority override of in-progress interrupts and DMA transfers.

2.1.18 System Clock (CLK)

This signal is the main system clock. Care should be taken to ensure it is a clean square wave. Its frequency and duty cycle are undefined. The primary master should typically provide this signal, however it may optionally be provided by another card such as a video card. It is recommended that primary masters do not strictly require externally generated clock signals to function. Any card capable of driving this signal must have an option to disable it, to prevent conflicts with other cards.

2.1.19 Unused Pins (NC)

These pins are not currently used and their use is reserved for future revisions of this specification. These should be individually connected and terminated on the backplane similarly to other signals.

2.1.20 Power Supply Rails (+12V, +5V, +5VSB +3.3V, GND, -12V)

These lines supply power to the bus. Current capacity is defined by the individual backplane's specifications, as well as Section *4.1*. If more current is required, an external power connection should be added to the card (See Section *4.1.2*). Voltage tolerances match the ATX standard. It is recommended that a standard ATX power supply be used.

Table 1: Signal Sources

Group	Signal	Driver	Receiver
A *Information*	A<19..0>	Master	Any
	D<7..0>	Master (WR), Slave (RD)	Slave (WR), Master (RD)
	RD	Master	Any
	WR	Master	Any
	IOSEL	Master	Backplane, Memory Systems
	CSX	Backplane	Cards
B *Control*	INH	Any	Memory Systems
	WAIT	Slave	Master
	RST	Any	Any
	BRQ	Secondary Master	Primary Master
C *Status*	ACK	Primary Master	Secondary Master
	HALT	Primary Master	Any
	FETCH	Primary Master	Any
D *Interrupt*	IRQX	Any	Primary Master
	IRQ<7..0>	Backplane	Primary Master
	INT	Backplane	Primary Master
	NMI	Any	Primary Master
E *Utility*	CLK	Master (Typ.)	Any
	NC	None	None
F *Supply*	+12V	Backplane	Any
	+5V	Backplane	Any
	+5VSB	Backplane	Any
	+3.3V	Backplane	Any
	GND	Backplane	Any
	-12V	Backplane	Any

2.2 Address Space Selection

See Section *3.1* for more information on address spaces.

IOSEL is controlled by the master to indicate which address space is being requested. It is effectively an additional address line. Primary masters must be capable of addressing a minimum of 8 slots.

When IOSEL is asserted, backplanes must determine which slot is being addressed, and assert the CSX signal for that slot.

2.3 Bus Arbitration

In the system's default state, a primary master has full control of the system bus. By asserting the BRQ line, a secondary master may request to temporarily take over control of some signals in order to directly access memory or I/O devices. When BRQ is asserted, the primary master gracefully hands over control of Group A signals.

The ACK signal indicates that the primary master has placed its Group A signals in a high-impedance state. These signals may be driven by a secondary master only while ACK is asserted.

In order to prevent bus contention, secondary masters should wait for a command from the primary master before initiating a bus request, and must not initiate a bus request until the BRQ signal is no longer asserted.

3. System Functionality

3.1 Address Spaces

The system is divided into two discrete address spaces – “Memory” and “I/O”.

1) When $\overline{\text{IOSEL}}$ is deasserted, the memory address space is selected and read/write operations apply to memory devices.
2) When $\overline{\text{IOSEL}}$ is asserted, the I/O address space is selected and read/write operations apply to I/O devices.

3.1.1 Memory

Memory address space layout is defined by the primary master. There are two types of memory that can be added to a system:

1) “Main Memory” is memory that is accessible when $\overline{\text{INH}}$ is deasserted. It is recommended that only one device manages main memory in a system.
2) “Override Memory”, when it is addressed, asserts the $\overline{\text{INH}}$ signal to disable main memory devices occupying the desired location. In this way specialized memory devices may be added to a system without the need to reconfigure the main memory system.

3.1.2 I/O

Each card slot on a backplane is assigned 256 bytes of I/O address space, beginning at I/O address $00000. Each 256-byte block of I/O addresses is assigned to a slot number equal to the value of A<19..8>. For example, slot 0 addresses are located from $00000-$000FF, slot 1 from $00100-$001FF, etc.

Although there is no specified limit, typically no more than 16 slots will exist in a system. I/O addresses are therefore shortened to three nybbles and the upper address bits are ignored. A backplane’s I/O decoding logic may ignore any I/O address bits that are not required to access the number of implemented slots.

When a slot’s I/O block is addressed by the master, the backplane must assert that card’s $\overline{\text{CSX}}$ signal.

$\overline{\text{CSX}}$ indicates to a slave that it is being addressed, and that A<7..0> contain the address to be accessed. Slave devices may only use A<7..0> for addressing purposes, and A<19..8> must be ignored by slaves during I/O operations.

3.2 Reserved Addresses

Addresses $XF8-$XFF are reserved for special bus functions. These should not be used except as described in *Table 2*.

Table 2: Reserved Addresses

Address	Purpose
$XF8	Reserved
$XF9	Reserved
$XFA	Reserved
$XFB	Reserved
$XFC	Reserved
$XFD	Expanded Interrupt Vector
$XFE	Card ID (MSB)
$XFF	Card ID (LSB)

3.2.1 Card IDs

Each card should present an identification value at address $XFF which is unique to that type of card in the system. Identical cards should have identical IDs. Cards may be assigned a permanent ID as part of the XMICRO bus specification. Refer to *Appendix A* for Card ID assignments.

An MSB value of $FF must be taken as $00. In practice the MSB may be ignored altogether, as it is not expected that the number of unique XMICRO-compatible devices will exceed the available pool of single-byte IDs.

3.2.2 Expanded Interrupt Vector

In systems with more than eight slots, additional interrupt vectoring may be desired. Address $XFD (Read) may be overridden by the backplane to provide an interrupt vector from 0-254. This value must correspond to the lowest slot number currently asserting $\overline{\text{IRQX}}$. When no cards are asserting $\overline{\text{IRQX}}$, the value must be $FF.

3.3 Direct Memory Access

Placeholder text

3.4 Interrupts

Placeholder text

3.4.1 Vectored

3.4.2 Non-vectored

3.4.3 NMI

4. Electrical Specifications

4.1 Power Supply Characteristics

4.1.1 Main Power Supply

1) A backplane must supply cards with the following voltages: +12V, +5V, +5VSB, GND (0V), -12V.
2) Specifications of the power supply are to match the ATX standard.
3) The use of an ATX power supply is recommended.

4.1.2 Supplemental Power Supplies

Cards may use an additional connector to supplement the +12V, +5V, and GND rails. Where such a connector is used, the following requirements apply:

1) All supplemental power rails must match the potential of the bus rails such that no significant current flows between them.
2) Supplemental power must be delivered using connectors as specified in Section *4.3.2*.

4.2 Signal Characteristics

1) A receiver must recognize a voltage of ≤ 0.8V as a logic 0, and a voltage of ≥ 2.0V as a logic 1.
2) The minimum sink current capability of any driver on any line must be 20mA at 0.5V. Further, it is recommended that drivers with minimum source capability of 20mA at 2.4V be used.
3) Schmitt trigger inputs are required for all open-collector signals.

Table 3: Bus Driver Output Topologies

Signal	Output Device
A<19..0>	Tri-state
D<7..0>	Tri-state
$\overline{RD}$	Tri-state
$\overline{WR}$	Tri-state
$\overline{IOSEL}$	Tri-state
$\overline{CSX}$	Push-pull
$\overline{ACK}$	Push-pull
$\overline{HALT}$	Push-pull
$\overline{FETCH}$	Push-pull
CLK	Push-pull
$\overline{INH}$	Open-collector
$\overline{WAIT}$	Open-collector
$\overline{RST}$	Open-collector
$\overline{BRQ}$	Open-collector
$\overline{IRQX}$	Open-collector
$\overline{IRQ}$<7..0>	Open-collector
$\overline{INT}$	Open-collector
$\overline{NMI}$	Open-collector

4.3 Connectors

4.3.1 Backplane Interconnects

1) Backplanes must be fitted with TE Connectivity 7-5530843-0 or equivalent connectors. Each of these connectors is considered a discrete slot.

2) Cards must be fitted with card-edges compatible with the specified backplane connectors and conforming to physical specifications outlined in Section *5.1*. The average current on any backplane connector pin must not exceed 2A.

3) The recommended maximum current on backplane connectors is 1A for supply pins and 100mA for all other pins.

4) No XMICRO bus signal may be delivered between any two devices except by these backplane interconnects.

Table 4: Backplane Interconnect Pinout

Pin	Signal	Pin	Signal
1	+12V	2	+3.3V
3	GND	4	GND
5	+5V	6	+5V
7	-12V	8	+5VSB
9	$\overline{\text{CSX}}$	10	NC
11	NC	12	$\overline{\text{BRQ}}$
13	$\overline{\text{INH}}$	14	$\overline{\text{RST}}$
15	CLK	16	$\overline{\text{IOSEL}}$
17	$\overline{\text{HALT}}$	18	$\overline{\text{WAIT}}$
19	$\overline{\text{FETCH}}$	20	$\overline{\text{ACK}}$
21	$\overline{\text{RD}}$	22	$\overline{\text{WR}}$
23	A0	24	A1
25	A2	26	A3
27	A4	28	A5
29	A6	30	A7
31	A8	32	A9
33	A10	34	A11
35	A12	36	A13
37	A14	38	A15
39	A16	40	A17
41	A18	42	A19
43	D0	44	D1
45	D2	46	D3
47	D4	48	D5
49	D6	50	D7
51	$\overline{\text{INT}}$	52	$\overline{\text{IRQX}}$
53	$\overline{\text{IRQ0}}$	54	$\overline{\text{IRQ1}}$
55	$\overline{\text{IRQ2}}$	56	$\overline{\text{IRQ3}}$
57	$\overline{\text{IRQ4}}$	58	$\overline{\text{IRQ5}}$
59	$\overline{\text{IRQ6}}$	60	$\overline{\text{IRQ7}}$
61	$\overline{\text{NMI}}$	62	GND

4.3.2 Supplemental Power

TE Connectivity 174804-1 (Male) or equivalent installed on cards. Pinout and current limits match the ATX standard for peripheral connectors.

Table 5: Supplemental Power Connector Pinout

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

4.4 Grounding

4.4.1 Signal Ground

The GND supply rail serves as the 0V reference and return path for all bus signal and supply rails.

4.4.2 Chassis Ground

1) A separate chassis ground must be maintained for conductive chassis members. The purpose of the chassis ground is to provide a safe return path for ESD and electrical faults, as well as to avoid stray ground paths between cards which could result in unpredictable operation.
2) Where mechanical mounting holes in cards can be used to make an electrical connection to chassis components or other cards, those holes must be isolated from the signal ground. They are not required to be tied together on the PCB.
3) Where connectors have a separate shield conductor that is not used as a signal ground, the shield should be tied to chassis ground.
4) Chassis ground should be tied to the signal ground at the backplane.

5. Physical Specifications

5.1 Cards

1) A card's dimensions must not exceed the overall dimensions shown in *Figure 5-1*.
2) Card edge connectors must match the dimensions shown in *Figure 5-1*.
3) Pin 1 of the edge connector must be indicated on the card.
4) Card edges should be gold-plated for reliability. HASL or similar surface finishes are discouraged.
5) Card edges should be chamfered for easier insertion.
6) The use of standard "full-size" and "half-size" card form-factors shown in *Figure 5-1* is strongly encouraged.
7) Standard card mounting holes should be isolated from the backplane's GND pins and treated as a discreet chassis ground if conductive.
8) I/O connectors may only be placed on the rear edge. Other edges require 0.05" component clearance.

5.2 Backplanes

1) Backplanes must conform to the measurements and orientation shown in *Figure 5-2*.
2) Pin 1 must be indicated on at least one slot.
3) Each slot number must be indicated on the PCB
4) Maximum component height under cards may not exceed the edge connectors
5) All backplane slots must be capable of receiving full-dimension cards

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Figure 5-1: Card Physical Dimensions

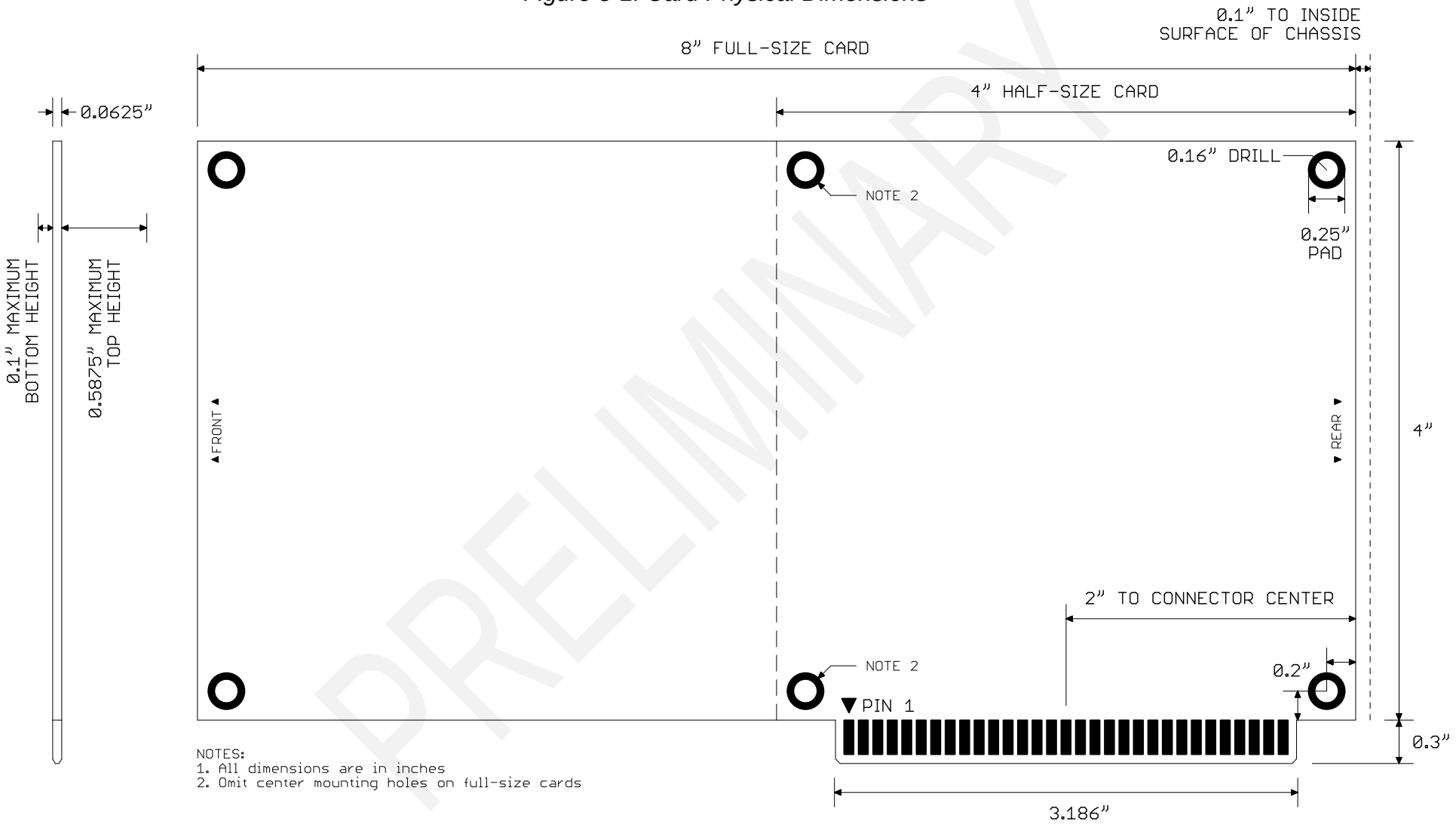

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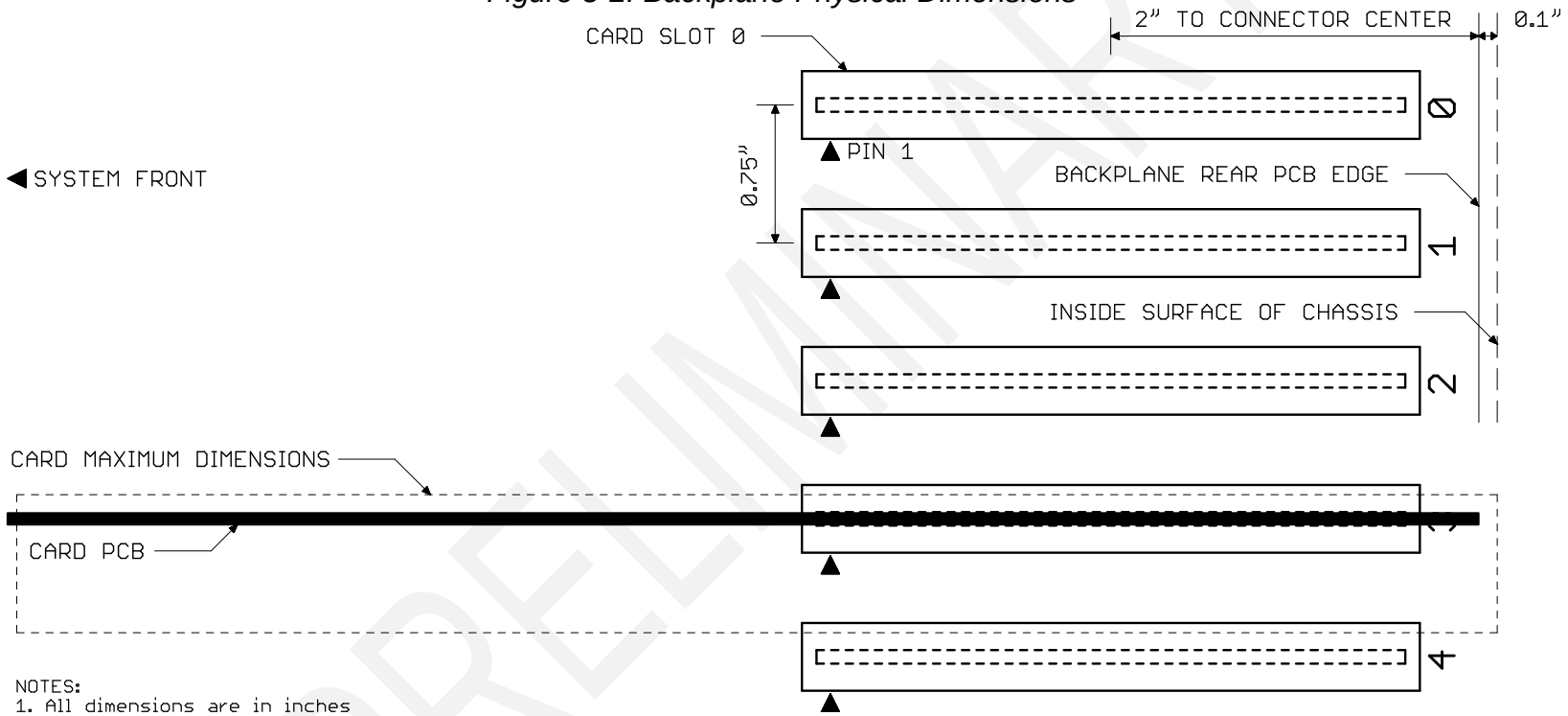
Figure 5-2: Backplane Physical Dimensions



Appendix A Card IDs

IDs $0000 and $00FF are reserved to indicate that no card is installed in the addressed slot.

IDs $00E0-$00FE will not be assigned to any specific devices and may be used for any device that has not been granted a permanent ID.

Any ID not shown in Table *A-1* is not currently assigned and may not be used.

Table A-1: Card ID Assignments

Value	Device
$0000	Reserved (No card)
$0001	XMICRO-6502
$0002	XMICRO-MEMORY
$0003	XMICRO-7SEG
$0004	XMICRO-SERIAL
$0005	XMICRO-VDP
$00E0-$00FE	Open for any use
$00FF	Reserved (No card)