XMICRO BUS

Technical Specifications

V0.2 2020-07-05

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- Standard 62-pin Card Edge Connector
- Fully Open-source

1.2 Elements of a System

An XMICRO system consists of the following elements:

- Backplane
- Primary Master
- Secondary Masters
- Slaves

An XMICRO *Backplane* is the basis of any system. In its simplest form, the backplane handles power and signal distribution, and card-specific signal routing. Typically it should also include an I/O address decoder, and a power-on reset circuit. More complex implementations may add significantly more functionality, including peripherals or an onboard CPU. When a primary master is built into a backplane, it should be referred to as a motherboard.

A *Primary Master* is a card or motherboard which acts as the default system controller. Typically this will be the main “CPU” card. In the context of this document, the “system controller” is the device driving the A<19..0>, $\overline{RD}$, $\overline{WR}$, and $\overline{FETCH}$ signals. Primary masters must default to this operation unless the bus is requested by another device. Only primary masters handle interrupt signals and bus requests.

A *Secondary Master* is a card with the ability to act as a temporary system controller. This is generally used for DMA operations by the secondary master, independent of the primary master.

A *Slave* is a card with no ability to control the system. Slaves are only capable of reading/writing data under the command of a master.

Note: The master/slave designation is somewhat loose and is used only as a broad classification of the functionality of a device. It may be used to refer to either a discrete subsystem or a card as a whole.

2. Signalling

2.1 Signal Lines

2.1.1 Power Supply Rails (+12V, +5V, +5VSB +3.3V, GND, -12V)

These lines supply power to the bus. Current capacity is defined by the individual backplane's specifications, as well as Section 4.1. If more current is required, an external power connection should be added to the card (See Section 4.1.2). Voltage tolerances match the ATX standard. It is recommended that a standard ATX power supply be used.

2.1.2 Address Lines (A<19..0>)

Twenty unidirectional lines driven by the master to specify a memory or I/O location.

2.1.3 Data Lines (D<7..0>)

Eight bi-directional lines which carry information between master and slave devices.

2.1.4 Read Strobe (RD)

Asserted by the master to indicate that the addressed slave device may place data on the data lines.

2.1.5 Write Strobe ($\overline{\text{WR}}$)

Asserted by the master to indicate that it has placed data on the data lines.

2.1.6 I/O Select ($\overline{\text{IOSEL}}$)

Asserted by the master to access the backplane's card I/O space. When asserted, A<11..8> determine which backplane slot is being addressed.

2.1.7 Reset ($\overline{\text{RST}}$)

This open-collector signal resets the system into a known state. During the power-on sequence, this signal should be asserted by the backplane until at least 250ms after all power supply rails have stabilized.

2.1.8 System Clock (CLK)

This signal is the main system clock. Care should be taken to ensure it is a clean square wave. Its frequency and duty cycle are undefined. The primary master should typically provide this signal, however it may optionally be provided by another card such as a video card. It is recommended that primary masters do not strictly require externally generated clock signals to function.

2.1.9 Wait ($\overline{\text{WAIT}}$)

This open-collector line is asserted to inform the master that the current data operation is not yet ready for completion. The master should wait until this signal is released to continue. Not to be confused with $\overline{\text{HALT}}$.

2.1.10 Halt ($\overline{\text{HALT}}$)

This line is asserted by the primary master to indicate to that it is in a halted state and waiting for an interrupt. Not to be confused with $\overline{\text{WAIT}}$.

2.1.11 Instruction Fetch ($\overline{\text{FETCH}}$)

This signal is asserted by the primary master when the current data transfer operation is an instruction fetch.

2.1.12 Main Memory Inhibit (INH)

This slot-independent line is used to inhibit general-purpose main memory. When INH is asserted, main memory must be prevented from reading or writing data, or driving the bus. This precludes the need for special hardware configuration when using devices requiring additional address space.

2.1.13 Bus Request (BRQ)

This slot-independent line is driven by a secondary master to request control of the bus. When the primary master is ready to release control of the bus, it will assert ACK.

2.1.14 Bus Acknowledge (ACK)

This signal is held low by the primary master to indicate that it has released the bus for control by a secondary master. The secondary master may only control the bus while this signal is asserted.

2.1.15 Card Select X (CSX)

This slot-specific signal is driven by the backplane to indicate that the current address is within the range of the slot's allocated address space. While this signal is asserted, A<19..8> may be ignored by the card because their state is known. Note: this is a discreet signal for each card slot, provided by the backplane.

2.1.16 Interrupt Request X (IRQX)

This slot-specific line is driven by a card to indicate that it requires the primary master's attention. It is routed to the appropriate input by the backplane. This allows for interrupt vectoring and prioritization based on card position. This is a level-triggered interrupt signal.

2.1.17 Interrupt Request (IRQ<7..0>)

These eight lines are driven by cards 7-0 through the IRQX signal. They are used by the primary master for interrupt prioritization and vectoring. Under no circumstances are these lines to be driven directly by a card.

2.1.18 Interrupt (INT)

This open-collector signal is used for special purposes where it is necessary to bypass a primary master's onboard interrupt handling circuitry. Typically this is only used to expand interrupt capabilities on backplanes with more than eight slots. Primary masters must accept this signal, either by including it in their interrupt handling scheme or combining it with the CPU's raw interrupt input. This is a level-triggered interrupt signal.

2.1.19 Non-maskable Interrupt (NMI)

Open-collector edge-triggered interrupt signal. Its use is unusual, so it is recommended that this signal be optional on any card using it. NMI should only be used for special signals requiring the immediate attention of the primary master, such as memory errors, power failure, or video timing. When possible, primary masters should give this signal an immediate priority override of in-progress interrupts and DMA transfers.

2.1.20 Unused Pins (NC)

These pins are not currently used and their use is reserved for future revisions of this specification. These should be individually connected and terminated on the backplane similarly to other signals.

Table 1: Signal Sources

Signal	Driver	Receiver
A<19..0>	Master	Any
D<7..0>	Master (WR), Slave (RD)	Slave (WR), Master (RD)
RD	Master	Any
WR	Master	Any
IOSEL	Master	Backplane, Memory Systems
CLK	Master (Typ.)	Any
HALT	Master	Any
FETCH	Master	Any
ACK	Master	Secondary Master
CSX	Backplane	Cards
RST	Any	Any
WAIT	Any	Master
INH	Any	Memory Systems
BRQ	Secondary Master	Primary Master
IRQX	Any	Primary Master
IRQ<7..0>	Backplane	Primary Master
INT	Backplane	Primary Master
NMI	Any	Primary Master
NC	None	None

2.2 IOSEL

Placeholder Text See section 3.1 for more information on address spaces.

2.3 WAIT

The WAIT signal is asserted by a slave device to indicate that a data transaction is not yet ready to be completed. If RD or WR is asserted while WAIT is asserted, the master must hold the following signals in their current state until after WAIT is deasserted:

- A<19..0>
- D<7..0>
- RD
- WR
- IOSEL

2.4 Bus Arbitration

In the system's default state, a primary master takes full control of the system bus. By asserting the BRQ line, a secondary master may request to temporarily take over control of some of the bus signals in order to directly access memory. When BRQ is asserted, the primary master gracefully pauses operation

The ACK signal indicates that the primary master has placed the following signals in a high-impedance state:

- A<19..0>
- D<7..0>
- RD
- WR
- IOSEL

These signals may be driven by a secondary master only while ACK is asserted.

If the $\overline{\text{ACK}}$ signal is de-asserted before the secondary master de-asserts $\overline{\text{BRQ}}$, the secondary master must immediately release the bus signals and wait until $\overline{\text{ACK}}$ is once again asserted to continue the operation.

In order to prevent bus contention, secondary masters should wait for a command from the primary master before initiating a bus request, and must not initiate a bus request until the $\overline{\text{BRQ}}$ signal is no longer asserted.

3. System Functionality

3.1 Address Spaces

The system is divided into two discrete address spaces – “memory” and “I/O”. When the $\overline{\text{IOSEL}}$ signal is asserted, the I/O memory space is selected and read/write operations

3.1.1 Memory

Placeholder text

3.1.2 I/O

Placeholder text

3.2 Direct Memory Access

Placeholder text

3.3 Interrupts

Placeholder text

3.4 Reserved Addresses

Placeholder text

3.4.1 Card IDs

Placeholder text

4. Electrical Specifications

4.1 Power Supply Characteristics

4.1.1 Main Power Supply

- A backplane must supply cards with the following voltages: +3.3V, +5V, +12V, -12V, +5VSB.
- Specifications of the power supply are to match the ATX standard.
- The use of an ATX power supply is recommended.

4.1.2 Supplemental Power Supplies

Cards may use an additional connector to supplement the +5V, +12V, and GND rails. Where such a connector is used, the following requirements apply:

- All supplemental power rails must match the potential of the bus rails such that no significant current is drawn by conflicting supplies.
- Supplemental power must be delivered using connectors as specified in section 4.3.2.

4.2 Signal Characteristics

- A receiver must recognize a voltage of ≤ 0.8V as a logic 0, and a voltage of ≥ 2.0V as a logic 1.
- The minimum sink current capability of any driver on any line must be 24mA at 0.5V. Further, it is recommended that drivers with minimum source capability of 24mA at 2.4V be used.
- Schmitt-trigger inputs must be used for all open-collector signals

Table 2: Bus Driver Output Topologies

Signal	Output Device
A<19..0>	Tri-state
D<7..0>	Tri-state
$\overline{RD}$	Tri-state
$\overline{WR}$	Tri-state
$\overline{IOSEL}$	Tri-state
CLK	Push-pull
$\overline{HALT}$	Push-pull
$\overline{FETCH}$	Push-pull
$\overline{ACK}$	Push-pull
$\overline{CSX}$	Push-pull
$\overline{RST}$	Open-collector
$\overline{WAIT}$	Open-collector
$\overline{INH}$	Open-collector
$\overline{BRQ}$	Open-collector
$\overline{IRQX}$	Open-collector
$\overline{IRQ}$<7..0>	Open-collector
$\overline{INT}$	Open-collector
$\overline{NMI}$	Open-collector

4.3 Connectors

4.3.1 Backplane Interconnects

Backplanes must be fitted with TE Connectivity 7-5530843-0 or equivalent connectors.

Cards must be fitted with card-edges compatible with the specified backplane connectors and conforming to physical specifications outlined in section 5.1. The average current on any backplane connector pin must not exceed 1A.

Table 3: Backplane Interconnect Pinout

Pin	Signal	Pin	Signal
1	+12V	2	+3.3V
3	GND	4	GND
5	+5V	6	+5V
7	-12V	8	+5VSB
9	$\overline{\text{CSX}}$	10	NC
11	NC	12	$\overline{\text{BRQ}}$
13	$\overline{\text{INH}}$	14	$\overline{\text{RST}}$
15	CLK	16	$\overline{\text{IOSEL}}$
17	$\overline{\text{HALT}}$	18	$\overline{\text{WAIT}}$
19	$\overline{\text{FETCH}}$	20	$\overline{\text{ACK}}$
21	$\overline{\text{RD}}$	22	$\overline{\text{WR}}$
23	A0	24	A1
25	A2	26	A3
27	A4	28	A5
29	A6	30	A7
31	A8	32	A9
33	A10	34	A11
35	A12	36	A13
37	A14	38	A15
39	A16	40	A17
41	A18	42	A19
43	D0	44	D1
45	D2	46	D3
47	D4	48	D5
49	D6	50	D7
51	$\overline{\text{INT}}$	52	$\overline{\text{IRQX}}$
53	$\overline{\text{IRQ0}}$	54	$\overline{\text{IRQ1}}$
55	$\overline{\text{IRQ2}}$	56	$\overline{\text{IRQ3}}$
57	$\overline{\text{IRQ4}}$	58	$\overline{\text{IRQ5}}$
59	$\overline{\text{IRQ6}}$	60	$\overline{\text{IRQ7}}$
61	$\overline{\text{NMI}}$	62	GND

4.3.2 Supplemental Power

TE Connectivity 174804-1 (Male) or equivalent installed on cards. Pinout matches the ATX standard for peripheral connectors.

Table 4: Supplemental Power Connector Pinout

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

4.4 Grounding

4.4.1 System Ground

Placeholder Text

4.4.2 Chassis Ground

Placeholder Text

5. Physical Specifications

5.1 Cards

- A card’s dimensions must not exceed the overall dimensions shown in Illustration 1.
- Card edge connectors must match the dimensions shown in Illustration 1.
- Pin 1 of the edge connector must be indicated on the card.
- Card edges should be gold-plated for better reliability. HASL or similar surface finishes are discouraged.
- Card edges should be chamfered for easier insertion.
- The use of standard “full-size” and “half-size” card form-factors is strongly encouraged.
- Standard card mounting holes should be isolated from the backplane’s GND pins and treated as a discreet chassis ground if conductive.
- I/O connectors may only be placed on the rear edge. Other edges require 0.05" component clearence

5.2 Backplanes

- Card slots must have a minimum 0.75” center-to-center spacing.
- Pin 1 must be indicated on at least one slot.
- Each slot number must be indicated on the PCB
- Maximum component height under cards may not exceed the edge connectors
- All backplane slots must be capable of receiving full-dimension cards

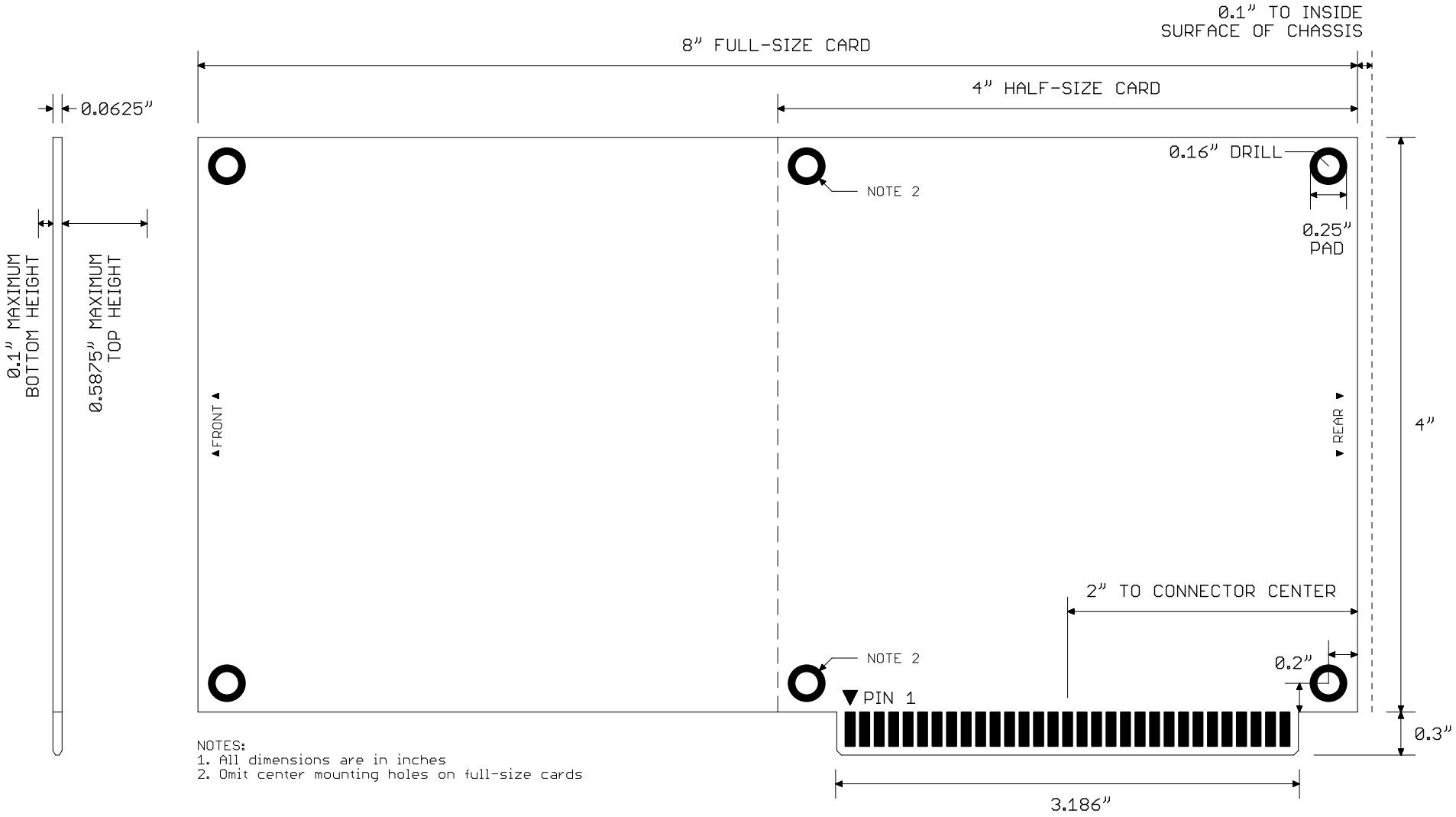

Illustration 1: Card Physical Dimensions

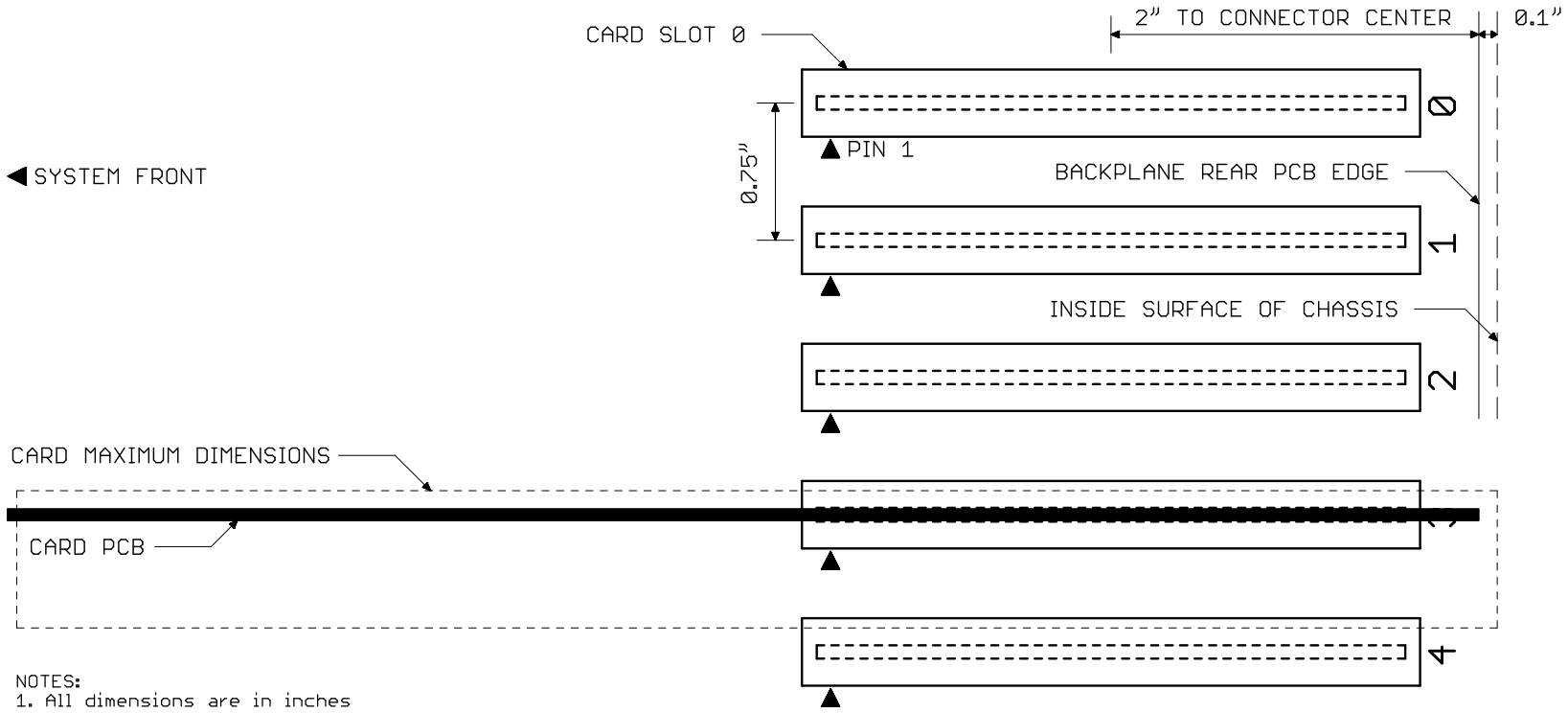

Illustration 2: Backplane Physical Dimensions