XMICRO-MEMORY

Technical Manual

V1.0 2018-06-03
Applies to hardware V1

Features:

- 1MB static RAM
- 32kB EEPROM
- Configurable ROM size, location, and page
- CompactFlash interface
- Real-time clock with programmable interrupts
- Optional battery-backup for lower 512kB of RAM
- Optional system watchdog timer
- Card ID register for system self-configuration
- Fully open-source

Functional Description:

The XMICRO-MEMORY is an XMICRO slave card which provides a system with several main-memory resources and is designed to be suitable for nearly any system. Its 1MB of SRAM fills the entire address range of the XMICRO bus. A 32kB EEPROM is provided for system programs, and is highly configurable to maintain compatibility across a wide range of microprocessor architectures. The onboard CompactFlash interface allows for extremely high-capacity storage on widely supported portable media. The card also has a versatile real-time clock IC with programmable date and time, interrupts, and an optional system watchdog timer.

Tables of Information

Table 1 – Card Memory Map

Address Range	Function
$X00-$X07	CompactFlash Card
$X10-$X1F	RTC Registers
$XD0	Card Status Register
$XFF	Card ID Register

Table 2 – Card Configuration

Setting	Function
JP1	RTC Watchdog Enable
JP2	RTC Reset Enable
JP3	RTC Interrupt Enable
JP4	CompactFlash IORDY Enable
JP5	CompactFlash Interrupt Enable
JP6/7	RAM Power Supply
JP8/9	ROM A12 Automatic/Manual
JP10/11	ROM A13 Automatic/Manual
JP12/13	ROM A14 Automatic/Manual
JP14	RTC Power Supply
S1	ROM Base Address A<19..12>
S2	ROM Page Selection

Table 4 – CompactFlash Registers

Address	Register
$X00	Data
$X01	Error (Read), Feature (Write)
$X02	Sector Count
$X03	Sector Number (LBA 7-0)
$X04	Cylinder Low (LBA 15-8)
$X05	Cylinder High (LBA 23-16)
$X06	Drive/Head (LBA 27-24)
$X07	Status

Table 5 – RTC Registers

Address	Register
$X10	Seconds
$X11	Seconds Alarm
$X12	Minutes
$X13	Minutes Alarm
$X14	Hours
$X15	Hours Alarm
$X16	Day
$X17	Day Alarm
$X18	Day-of-week
$X19	Month
$X1A	Year
$X1B	Programmable Rates
$X1C	Interrupt Enables
$X1D	Flags
$X1E	Control

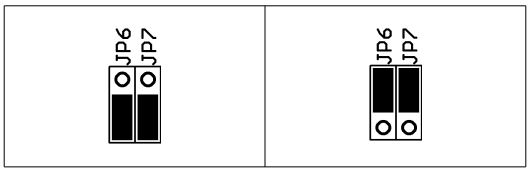
Table 3 – Card Registers

Address	D7	D6	D5	D4	D3	D2	D1	D0
$XD0	N/A				CF CD2	CF CD1	RTC IRQ	CF IRQ
$XFF	Card ID							

RAM

The card provides 1MB of static RAM to fill the entire addressable memory space of the XMICRO bus. As it is considered general-purpose memory, the RAM is inhibited by the $\overline{\text{INH}}$ signal on the bus. This function allows other devices to occupy areas of memory where the RAM is not wanted.

The lower 512kB may optionally be battery-backed to prevent data loss when powered off. This requires a battery to be installed in the RTC and jumper settings shown in Figure 1. This is not recommended for long-term storage, as battery failure will eventually cause data loss.



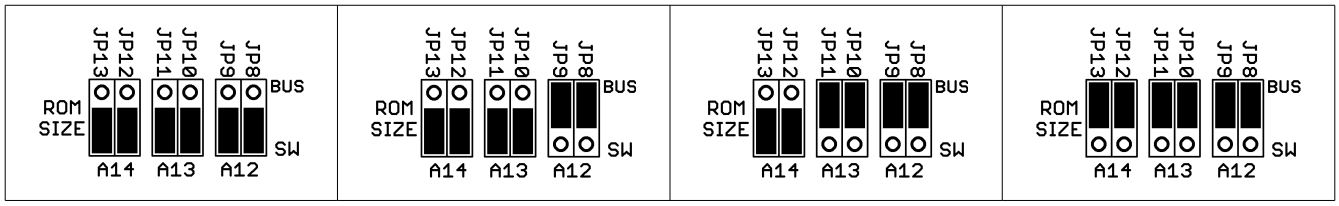
Volatile (Default) Non-Volatile

Figure 1 – Lower RAM Power Source

ROM

The 32KB EEPROM allows for non-volatile permanent program/data storage. It is not writable by the system, but may be removed and reprogrammed externally. During development, use of a zero insertion-force socket is recommended. Typically the ROM is used for the system's initial startup program. It has several configurable parameters to meet the needs of nearly any microprocessor or application. The ROM is also inhibited by the $\overline{\text{INH}}$ signal.

The size of the ROM can be configured by JP8-JP13 as shown in Figure 2. The position of these jumpers determines whether the A<14..12> pins on U1 are driven by the bus address lines or the DIP switch S2. This allows the user to select between multiple ROM pages and store several programs on the card without the need to replace U1. Figure 2 also shows the number of available pages in different configurations.



4K x 8 8K x 4 16K x 2 32K x 1

Figure 2 – ROM Size

The ROM's location can be configured using S1. This DIP switch configures the values of A<19..12> used by the ROM's chip select circuit. The switch value can be determined by A<19..12> of the desired start address of the ROM. Note that A<14..12> on S1 will be ignored if the corresponding bit is set to the "SW" position on JP8-JP13.

The ROM may be disabled all together by removing U5. This prevents the chip from being selected and also prevents the RAM from being inhibited in the configured address range.

CompactFlash Interface

The CompactFlash interface provides removable high-capacity storage to the system using widely available and well-supported CompactFlash cards. This allows for data to be transferred between XMICRO systems, PCs, and other compatible devices. The full detail of how to communicate with CF cards is out of the scope of this document. Refer to the CompactFlash specification for more information.

The XMICRO-MEMORY's CompactFlash interface is implemented as 8-bit IDE mode. The card must be initialized in 8-bit mode to work properly. Native DMA is therefore not implemented, as it is a purely 16-bit function. The base address of the onboard registers is that of the XMICRO-MEMORY card as seen in Table 4. A "busy" indicator D2 is illuminated by the CompactFlash card during read/write operations.

The XMICRO-MEMORY's Card Status Register ($XD0) bits D<3..2> indicate that a CompactFlash card is present in the system when both bits are 0. Bit D0 indicates an interrupt actively being generated by the CompactFlash card when it is 0.

The CompactFlash card's interrupt signal may be enabled by shorting JP5. Similarly, JP4 connects the card's $\overline{\text{IORDY}}$ signal to the bus $\overline{\text{WAIT}}$ line. Unless these signals are required, JP4 and JP5 should be left open.

Real-Time Clock

The BQ4845 Real-Time Clock (RTC) IC integrates several useful functions. The full list of features and how to program the BQ4845 is beyond the scope of this document. Refer to the BQ4845 datasheet for more information on this device.

JP2 connects the RTC's reset pin to the system $\overline{\text{RESET}}$ line. When the chip's supply voltage enters an acceptable range, $\overline{\text{RESET}}$ is asserted for 200ms. The RTC includes a system watchdog timer which can be enabled by shorting both JP1 and JP2. This watchdog monitors A0 for activity. If no activity is detected within the programmed time, the RTC will cause a system reset to recover from the condition. Naturally, this feature is not suitable if the system may be in a halted state for extended periods.

The main power supply rail for the RTC can be selected between +5V and +5VSB using JP14 as seen in Figure 3. It must be noted that the power-on reset function of the power-on reset function of this chip will not work if the supply is set to +5VSB. Using +5VSB may be preferable in some cases to extend the longevity of the RTC's battery cell. Note however, that when the RTC is powered by +5VSB, it doesn't typically see power loss and thus will not reset itself. It can then cause undesired interrupts in the next power cycle if they have been enabled. It is therefore recommended to mask RTC interrupts until it has been initialized. The battery may be replaced with a standard CR2032 cell.

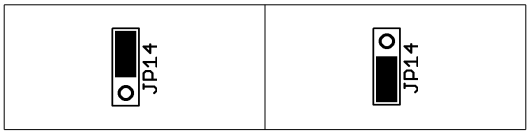


Figure 3 – RTC Power Supply Rail

Card Status Register

A status register is available at $XD0 to provide the system with the current status of onboard devices. Bit D0 indicates an active CompactFlash interrupt with a value of 0. Bit D1 indicates an active RTC interrupt with a value of 0. Bits D<3..2> indicate a properly inserted CompactFlash card when both have a value of 0.