1. General Description

The XMICRO-MEMORY is an XMICRO slave card providing 1MB of RAM and an optional relocatable 8KB EEPROM.

1.1 Features

- 1MB SRAM fills all XMICRO bus memory address space
- 8kB EEPROM available to bus

1.2 System Outline

Table 1: Card Memory Map

ADDRESS RANGE	FUNCTION
$XFF	Card ID Register (R)

Table 2: Card Configuration

SETTING	FUNCTION
JP1	Enable wait states for ROM accesses
JP2	Enable ROM
S1	ROM page selection
S2	ROM address selection

Table 3: ROM Address Examples

S2 SETTING	ROM ADDRESS RANGE
0000000	$00000-$01FFF
0000111	$0E000-$0FFFF
0001000	$10000-$11FFF

Table 4: ROM Pages

S1 SETTING	RANGE ON EEPROM
00	$0000-$1FFF
01	$2000-$3FFF
10	$4000-$5FFF
11	$6000-$7FFF

2. RAM

The 1MB SRAM is “Main Memory” as descrived by the XMICRO bus specification. Bus read/write operations will default to this RAM, provided that IOSEL and INH are not asserted. When either IOSEL or INH are asserted, the XMICRO-MEMORY’s RAM is disabled.

3. ROM

The ROM, when enabled, overrides the onboard RAM in the 8kB range specified using switch S2. When bus address bits A<19..13> match the setting on S2, the ROM is selected. See *Table 3* for examples.

The 32kB EEPROM is divided into four pages of 8kB which are selected using switch S1. See *Table 4* for page settings.

As the ROM operates significantly slower than the RAM, it is equipped with a wait state generator to meet timing requirements of high-speed bus masters.

4. Onboard Registers

4.1 Card ID Register ($XFF)

The Card ID Register contains the ID value $02 as assigned in XMICRO Bus specification Appendix A. This register is used by the system to determine card types and locations.

Card ID Register
$XFF, Value $02

U8A
R4 1k
R3 1k
RD/2.3D
CSX
DIR
OE
A=B
74ABT245-SN

DATA:D[0..7]
RN3
10k
U9A
74ABT245-SN
U2C
BINH/2.2D
IOSEL/2.3D
74AHCT132N

RN2A
RN1A
10
10
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7

P1
BUSRQ
BUSAK
INH
IRQX
NMI
SINT
V0
V1
V2
V3
V4
V5
V6
V7
+5V
+3.3V
+5V
+12V
-12V
+5VSB
0V
0V
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
IOSEL
CSX
RD
WR
RST
WAIT
HALT
FETCH
CLK
BRD
BWR
BRST
BWAIT/3.5D

ADDRESS:A[0..19],IOSEL,CSX,RD,WR

U1A
BA0
BA1
BA2
BA3
BIOSEL
BCSX
BRD
BWR
A0
A1
A2
A3
IOSEL
CSX
RD
WR
74ABT245N

U5
BA4
BA5
BA6
BA7
BA8
BA9
BA10
BA11
A4
A5
A6
A7
A8
A9
A10
A11
74ABT245N

U7
BA12
BA13
BA14
BA15
BA16
BA17
BA18
BA19
A12
A13
A14
A15
A16
A17
A18
A19
74ABT245N

74AHCT132N
TP1
BWR
BRD
RWCYCLE/3.3D
U2B

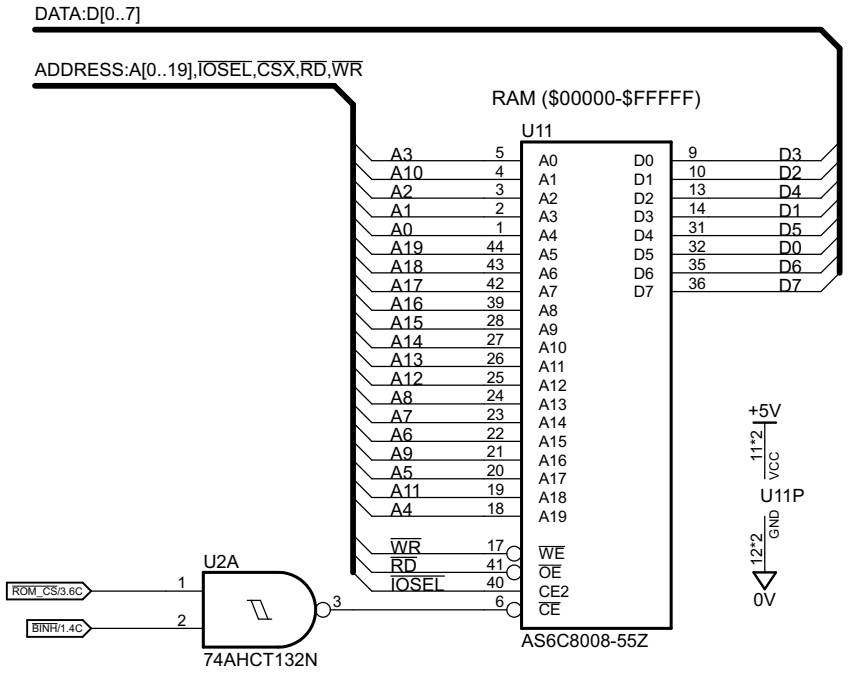
U3C
U3B
74AHCT14N
74AHCT14N
RST/3.3D

U3A
U3D
U3E
U3F
74AHCT14N

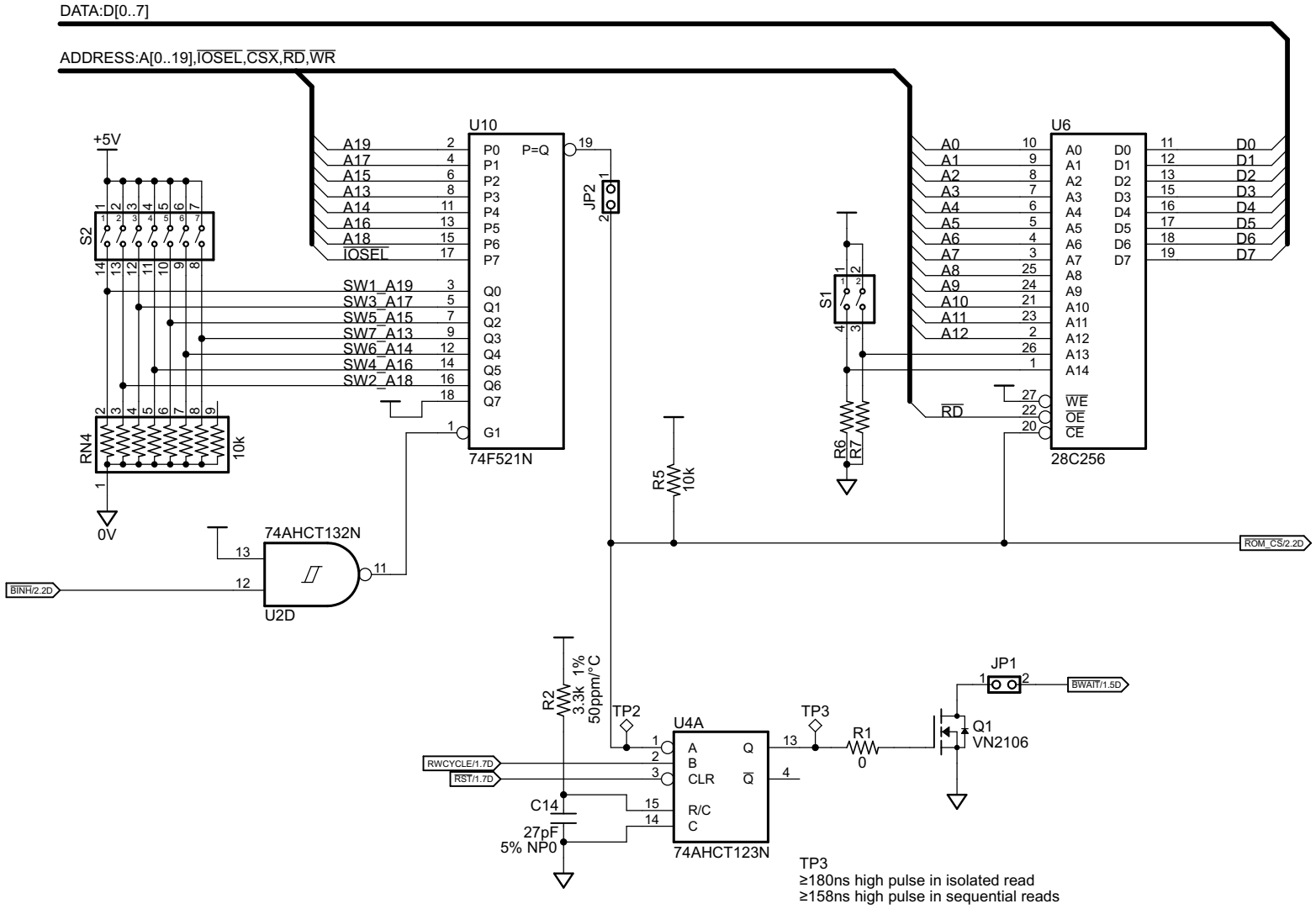
U4B
74AHCT123N

C1 0.1uF
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13 10uF 6.3V

Title: Bus Interface		XMICRO
Project: XMICRO-MEMORY		Revision: 1.0
Drawn by: Chris Weir	2024-04-06 11:47:29	Sheet: 1/3



Title: RAM		XMICRO
Project: XMICRO-MEMORY		Revision: 1.0
Drawn by: Chris Weir	2024-04-06 11:47:29	Sheet: 2/3



Title: ROM		XMICRO
Project: XMICRO-MEMORY		Revision: 1.0
Drawn by: Chris Weir	2024-04-06 11:47:29	Sheet: 3/3