

## General Description

The XMICRO-MEMORY is an XMICRO slave card providing 1MB of RAM and an optional relocatable 8KB EEPROM.

## Features

- 1MB SRAM fills all XMICRO bus memory address space
- 8kB EEPROM available to bus

## Basic Information

Table 1: Card Memory Map

ADDRESS RANGE	FUNCTION
\$XFF	Card ID Register (R)

Table 2: Card Configuration

SETTING	FUNCTION
JP1	Enable wait states for ROM accesses
JP2	Enable ROM
S1	ROM page selection
S2	ROM address selection

Table 3: ROM Address Examples

S2 SETTING	ROM ADDRESS RANGE
0000000	\$00000-\$01FFF
0000111	\$0E000-\$0FFFF
0001000	\$10000-\$11FFF

Table 4: ROM Pages

S1 SETTING	RANGE ON EEPROM
00	\$0000-\$1FFF
01	\$2000-\$3FFF
10	\$4000-\$5FFF
11	\$6000-\$7FFF

## RAM

The 1MB SRAM is “Main Memory” as described by the XMICRO bus specification. Bus read/write operations will default to this RAM, provided that  $\overline{\text{IOSEL}}$  and  $\overline{\text{INH}}$  are not asserted. When either  $\overline{\text{IOSEL}}$  or  $\overline{\text{INH}}$  are asserted, the XMICRO-MEMORY’s RAM is disabled.

## ROM

The ROM, when enabled, overrides the onboard RAM in the 8kB range specified using switch S2. When bus address bits A<19..13> match the setting on S2, the ROM is selected. See Table 3 for examples.

The 32kB EEPROM is divided into four pages of 8kB which are selected using switch S1. See *Table 4* for page settings.

As the ROM operates significantly slower than the RAM, it is equipped with a wait state generator to meet timing requirements of high-speed bus masters.

## **Onboard Registers**

### **Card ID Register (\$XFF)**

The Card ID Register contains the ID value \$02 as assigned in XMICRO Bus specification Appendix A. This register is used by the system to determine card types and locations.





