General SPI Design

For BK3432 FLASH

Approvals

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Revision History

Rev.	Date (YY/MM/DD)	Author(s)	Remark
0.1		Lizhen	Used for BK3432 FLASH of UMC；
0.2			

Content

1. Purpose

We need find a general interface for configuring OTP, EEPROM or FLASH on chip. This interface should have expansibility and can be used by other project or next generation product. This spec is used for the FLASH of grace specially used by BK3432.

2. PIN

There are four pin shared with GPIO. They are SPI_clk, SPI_cs, SPI_mosi, SPI_miso.

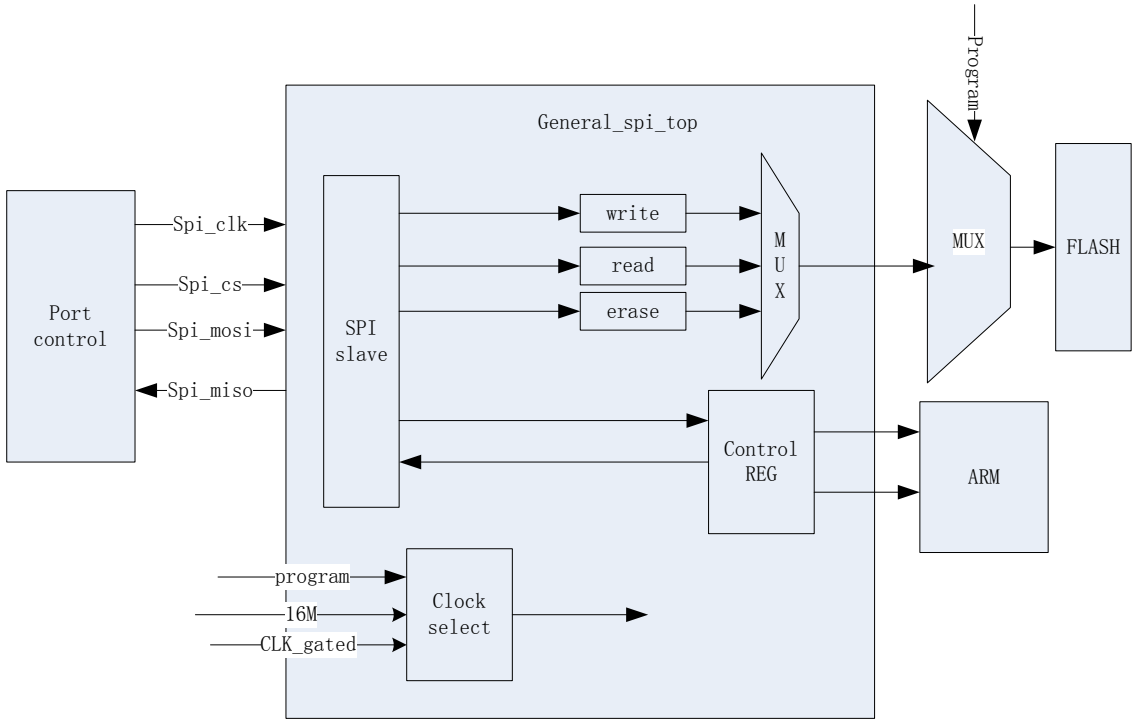
P0.4= SPI_mosi

P0.5= SPI_miso

P0.6= SPI_clk

P0.7= SPI_cs

3. Diagram



4. Interface timing

Read timing

Command (8bits)	Address(8 or 16 bits)	Read back data (8 bits)

Write timing

Command (8bits)	Address(8 or 16 bits)	write data (8 bits)

Pure command

Command (8bits)		

5. Command description

command	operation	description	note
8'h00			Only command
8'h01			Only command
8'h11			
8'h12			
8'h13			
8`b14	Flash CRC check		
8'h21	Write FLASH		16bits address
8'h22	Read FLASH		16bits address
8'h23	erase FLASH sector		Command+address
8'h24	erase FLASH block		Command+address
8'h25	erase whole FLASH		Only command
8'h31	Write reg		
8'h32	Read reg		
8'h41			
8'h42			

6. Register

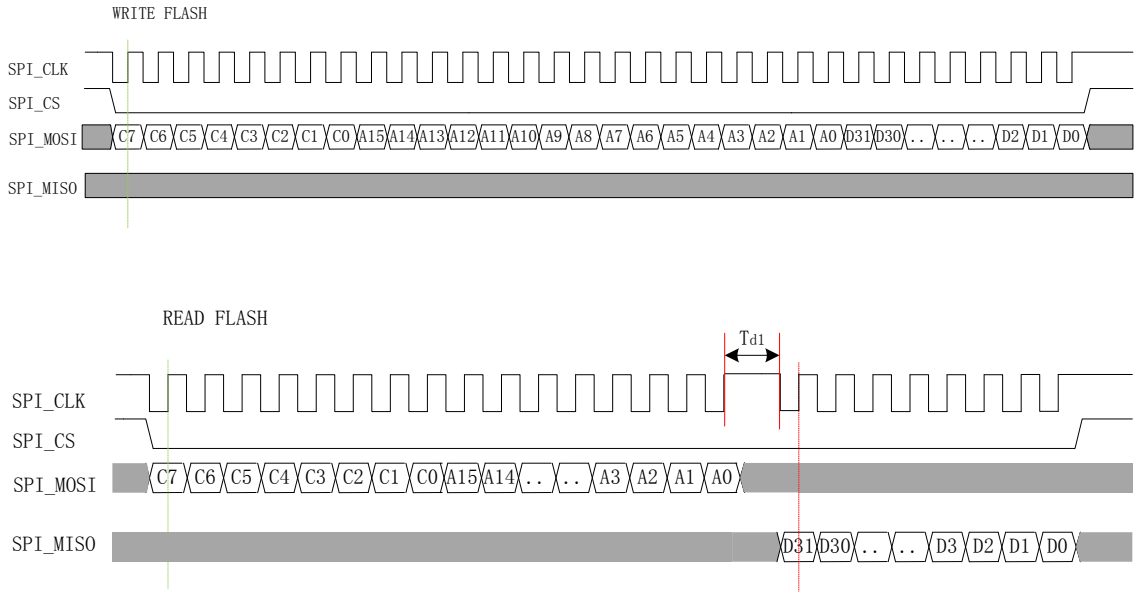
address	name	bit	default	R/W	Definition
8'h05(version)			0x32	R	
8'h04(control register)	ex_vread0	0	0	R/W	Read operation VREAD0 bit
	ex_vread1	1	0	R/W	Read operation VREAD1 bit
	ex_prepgm	2	0	R/W	Write operation support preprogram or not
				R/W	
	Retry_en	4	0	R/W	Erase operation RETRY enable bit
8'h03	Protect word1		0	R/W	Need write as C3 to remove change protect
8'h02	Protect word0		0	R/W	Need write as A5 to remove change protect
8'h01(control register)	Work mode	07:06	0	RW	00: normal work mode
					11:mbist RAM mode
		05:04	0	RW	00:MAIN SPACE
					01:NVR SPACE
					10:RDN SPACE
					11:00

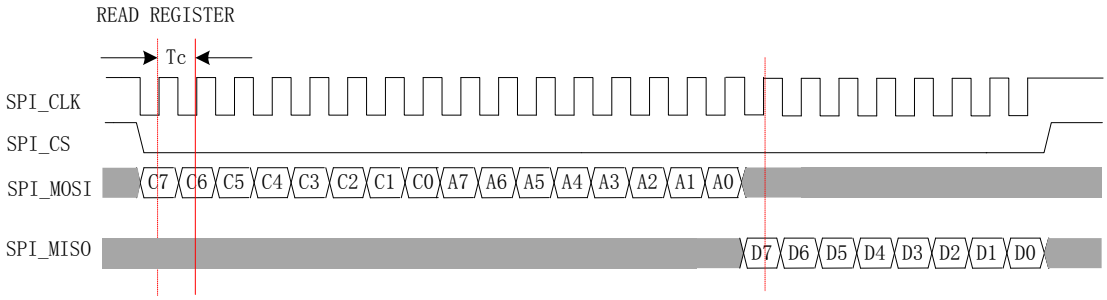
8'h00(status register)		7	0	R	
		6	0	R	
	FLASH_crc_pass	5	0	R	1:FLASH CRC check pass
					0:fail
	FLASH_check_status	4	0	R	1: FLASH check done
					0:not ready
		3			
	RAM check fail	2	0	R	1: RAM check fail 0: not fail
	RAM check pass	1	0	R	1: RAM check pass 0: not pass
	RAM check done	0	0	R	1: RAM check done
					0:not ready

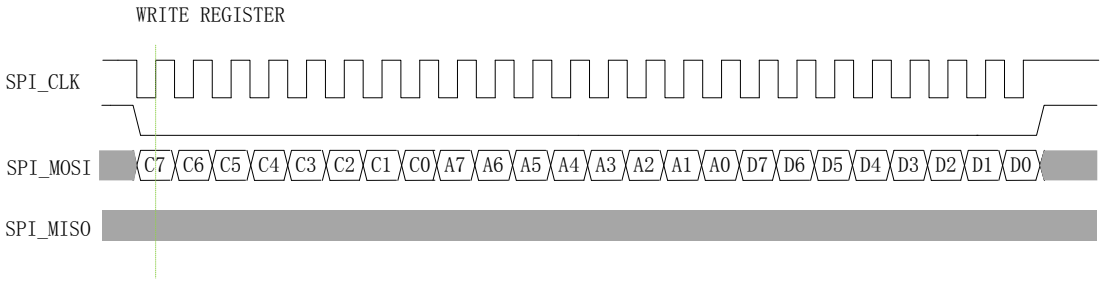
7. Note

- This module can work only in program mode.
- XTAL clock (16M) should be work normally in program mode, and used for SPI operation. (when program=1)
- This module can be reset by POR and reset pin.
- SPI clock <=4Mhz
- One internal address

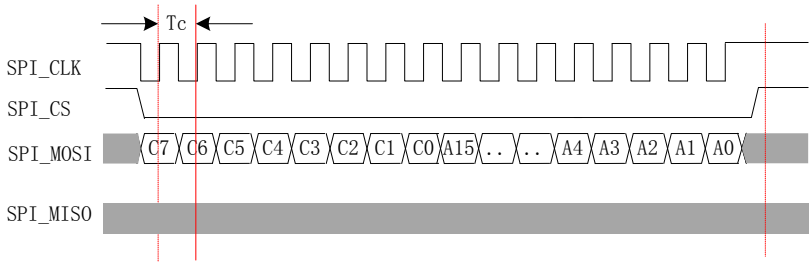
8. SPI timing



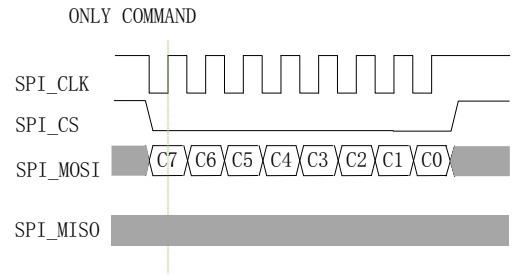


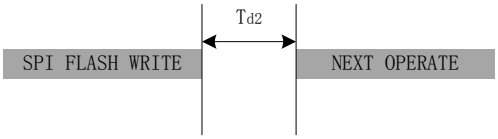


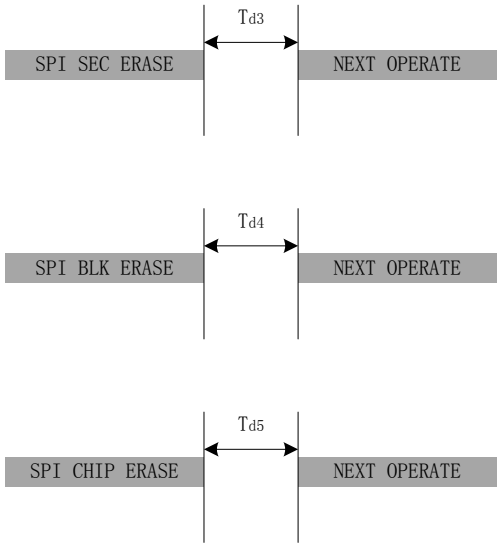
SECTOR/BLOCK ERASE



Erase CHIP







9. Time parameter

Variables	Time (MAX)	Time (MIN)	Def	Note
Td1	-	1.2us/10us		1.2us for normal read; 15us for VREAD read
Td2	-	30us		
Td3	-	4ms		
Td4	-	6ms		
Td5	-	10ms		

10. 空间分布

512Bytes/Sector

8Sectosr/Block

4KBytes/Block

256Sectors/total

32Blocks/total

128KBytes/total

NVR 4 sectors

RND 4 sectors

- Main 访问

第一个 sector，address=16'h0;

第二个 sector，address=16'h80;

第三个 sector，address=16'h100;

第四个 sector，address=16'h180;

....

第一个 Block，address=16'h0;

第二个 Block，address=16'h400;

第三个 Block，address=16'h800;

第四个 Block，address=16'hc00;

....

NVR 和 RDN 空间各有四个，但是此 FLASH 是由两大块 FLASH 组成的，所以选择上以最高地址位进行区分，所以第三个 sector 地址是 0X8000，注意此地址为芯片内部绝对地址（32bits 基准），是要在 spi 总线上送入的地址。

- NVR 访问：

第一个 sector，address=16'h0; 只能读

第二个 sector，address=16'h80;

第三个 sector，address=16'h8000;

第四个 sector，address=16'h8080;

- RDN 访问：

第一个 sector，address=16'h0;

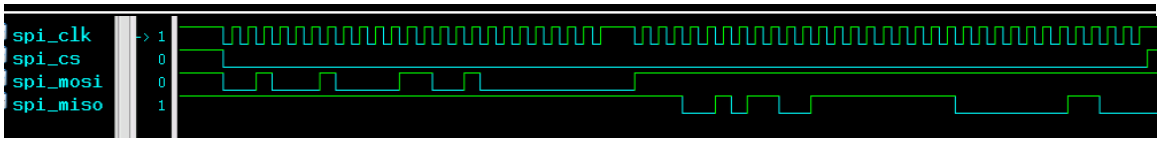
第二个 sector，address=16'h80;

第三个 sector，address=16'h8000;

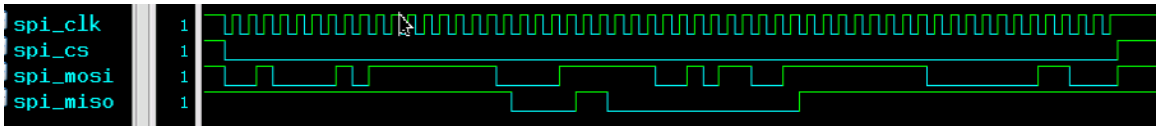
第四个 sector，address=16'h8080;

11. 时序示例

Read



Write



12. Lab 调试软件

Lab 调试软件读取写入的 main 空间地址是以 byte 计的，内部地址是 32bits 计的，所以填入方框的地址软件先除 4 再送入了芯片内部解析。

所以放 CRC 的地址是 27FF8~227FFB, 内部是 9FFE， 放读保护的地址是 27FFC~27FFF，内部是 9FFF。

13. 上电抢下载时序

如果 program pin 有 bonding 出来,则拉高此 pin 进入下载模式。

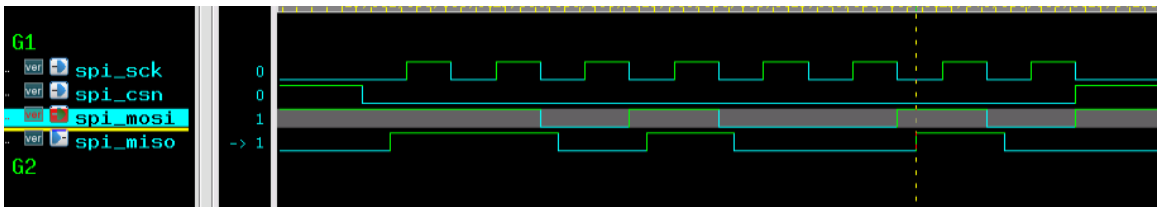
如果没有 program pin ,则进行上电初始化期间抢总线方式进入下载模式。此时最好在上电后拉低 reset 脚，使芯片重新运行，这样防止错过抢总线时间窗口。

下图说明的是进入下载模式的命令，如果在初始化期间收到 D2 命令，回复 D2 命令，并且在初始化完成后的 SPI 发送窗口发送 2D 给外部 MCU，以指示初始化完成，可以进入下载模式。在收到 D2 的情况下，初始化完成后进入下载模式， 如果在初始化期间没有收到 D2 命令，则在初始化完成后进入正常工作模式，此时接口为 JTAG 模式，由软件决定是否切换端口为正常 GPIO。

注意的是 SPI 时钟只有在模式选择期间是打开的，其他期间都是关闭的，防止误触发进入相应的模式。

如果 MCU 在发送 D2 命令后，收到 D2 命令，在一定时间后没有收到 2D 回复， 而是其他数据回复，则需要重启芯片，重复上述模式进入过程。

开始发送 D2 命令和回复 D2 信息。



结束时发送 D2 命令，回复 2D 信息，表示后面进入了下载模式。