Bluetooth 5.2 Dual Mode and Proprietary 2.4 GHz Wireless System on Chip

Specification

Beken Corporation
Building 41, Capital of Tech Leaders, 1387 Zhangdong Road,
Zhangjiang High-Tech Park, Pudong New Area, Shanghai, China
Tel： (86)21 51086811
Fax： (86)21 60871089

Table of Contents

1 General Description 3
1.1 Overview 3
1.2 Features 4
2 Pin Information 6
2.1 QFN32 6
2.2 QFN40 8
2.3 QFN48 10
3 Functional Description 12
3.1 Power Management 12
3.2 GPIO 14
3.3 Timers 15
3.3.1 PWM Timers 15
3.3.2 Watch Dog Timer and RTC Timer 16
3.3.3 Sub-Micro Second Event Timer 16
3.4 ADC 16
3.5 UART, I2C and SPI 17
3.6 USB 17
3.7 True Random Number Generator 17
3.8 I2S Digital Audio 18
3.9 Code Encryption and System Security 18
4 Electrical Specifications 19
5 Package Information 22
5.1 QFN 4x4 32-Pin 22
5.2 QFN 5x5 40-Pin 23
5.3 QFN 6x6 48-Pin 23
6 Solder Reflow Profile 25
7 Ordering Information 27
Revision History 28

1 General Description

1.1 Overview

The BK3633 chip is a highly integrated wireless system on chip, which supports Bluetooth 5.2 Dual Mode and proprietary 2.4 GHz protocols. It integrates a high-performance RF transceiver, baseband, low power processor, rich feature peripheral units, programmable protocol and profile to support a wide range of applications. The Flash program memory makes it suitable for customized applications.

Designed with advanced technology process and integrated with switch DCDC regulator, the BK3633 features ultra-low power consumption and ultra-low leakage power. The embedded high order interference suppression filter and fast automatic gain control logic make it work well in high interference environment.

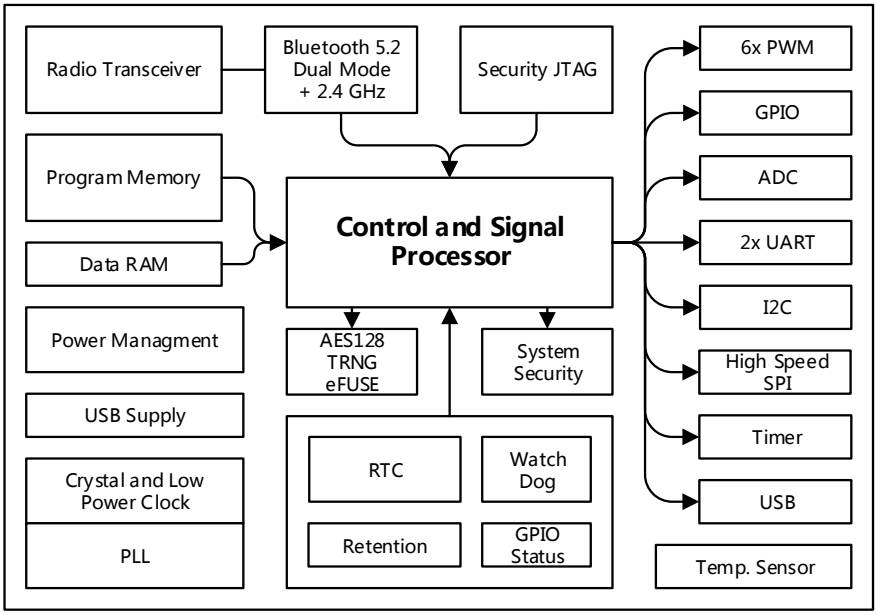


Figure 1 BK3633 Block Diagram

1.2 Features

- Bluetooth 5.2 Dual Mode and proprietary 2.4 GHz protocol
- Around 5 mA full operation current
- Around 1 μA deep sleep current with low power running timer
- Bluetooth Low Energy (LE) 125 kbps, 500 kbps, 1 Mbps and 2 Mbps
- Classic Bluetooth 1 Mbps
- Proprietary 2.4 GHz 250 kbps, 1 Mbps and 2 Mbps
- High output power up to 10 dBm and Bluetooth LE Power Control
- 32-bit RISC Core with 80 KB data memory and up to 64 MHz speed
- 500 KB programmable Flash
- 32-byte eFUSE
- Operating voltage: 0.9 ~ 1.5 V (boost), 2.0 ~ 3.6 V (buck)
- Clock
  - 16 MHz crystal reference clock with internal tuning load capacitance
  - 64 MHz digital PLL clock
  - 32 kHz ring oscillator
  - External 32 kHz crystal oscillator
  - MCU can run with any clock source with internal frequency divider
  - Dedicated audio PLL clock for I2S main clock
- Interface and peripheral units
  - Quad IO FLASH programming
  - I2C interface
  - High-speed SPI interface up to 32 MHz
  - Two UART interfaces, one with UART download support

- Multi-channel high resolution 32-bit PWM with capture mode
- USB Host and Device interface with USB audio capability
- On-chip high accurate temperature sensor
- On-chip 10 bit generic ADC
- GPIOs with multiplexed interface functions
- True random number generator (TRNG)
- AES 128-bit hardware accelerator
- I2S/PCM digital audio interface with master and slave mode
- High quality high speed and low power clock output
- Code encryption and online decryption
- Secure JTAG and system protection

- Typical package type
  - 32-pin QFN 4 mm x 4 mm
  - 40-pin QFN 5 mm x 5 mm
  - 48-pin QFN 6 mm x 6 mm

2 Pin Information

2.1 QFN32

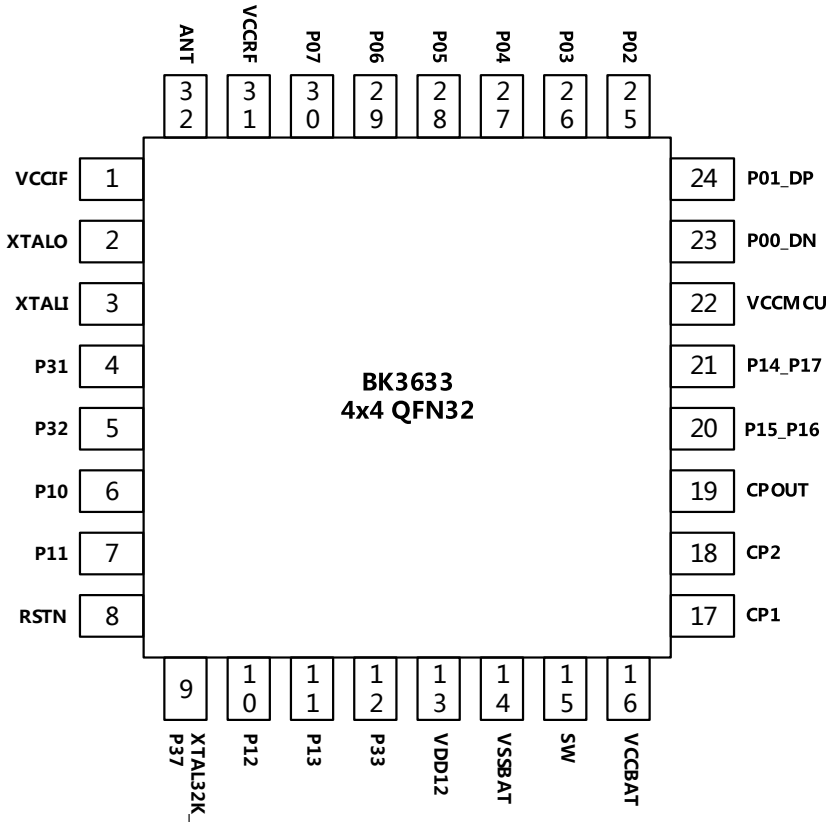


Figure 2 BK3633 QFN32 Pin Assignment

Table 1 BK3633 QFN32 Pin Description

PIN	Name	Pin Function	Description
1	VCCIF	Power	IF power, 1.5 V
2	XTALO	Analog	16 MHz crystal output
3	XTALI	Analog	16 MHz crystal input
4	P31	Digital I/O	General purpose IO
5	P32	Digital I/O	General purpose IO

PIN	Name	Pin Function	Description
6	P10	Digital I/O	General purpose IO
7	P11	Digital I/O	General purpose IO
8	RSTN	Analog	Reset pin of the system, low active
9	XTAL32K _P37	Analog	32 kHz Crystal input, and GPIO P37
10	P12	Digital I/O	General purpose IO
11	P13	Digital I/O	General purpose IO
12	P33	Digital I/O	General purpose IO
13	VDD12	Analog	LDO output, 1.2 V
14	VSSBAT	Ground	Ground
15	SW	Analog	Switch regulator pin for two battery mode
16	VCCBAT	Power	Battery power, 3 V
17	CP1	Analog	Charge pump component for FLASH
18	CP2	Analog	Charge pump component for FLASH
19	CPOUT	Power	Charge pump output voltage for FLASH
20	P15_P16	Digital I/O	General purpose IO
21	P14_P17	Digital I/O	General purpose IO
22	VCCMCU	Power	Power, 1.5 V
23	P00_DN	Digital/ Analog	General purpose IO, USB DN
24	P01_DP	Digital/ Analog	General purpose IO, USB DP
25	P02	Digital I/O	General purpose IO
26	P03	Digital I/O	General purpose IO
27	P04	Digital I/O	General purpose IO
28	P05	Digital I/O	General purpose IO
29	P06	Digital I/O	General purpose IO
30	P07	Digital I/O	General purpose IO
31	VCCRF	Power	RF power, 1.5 V
32	ANT	RF	RF signal port

2.2 QFN40

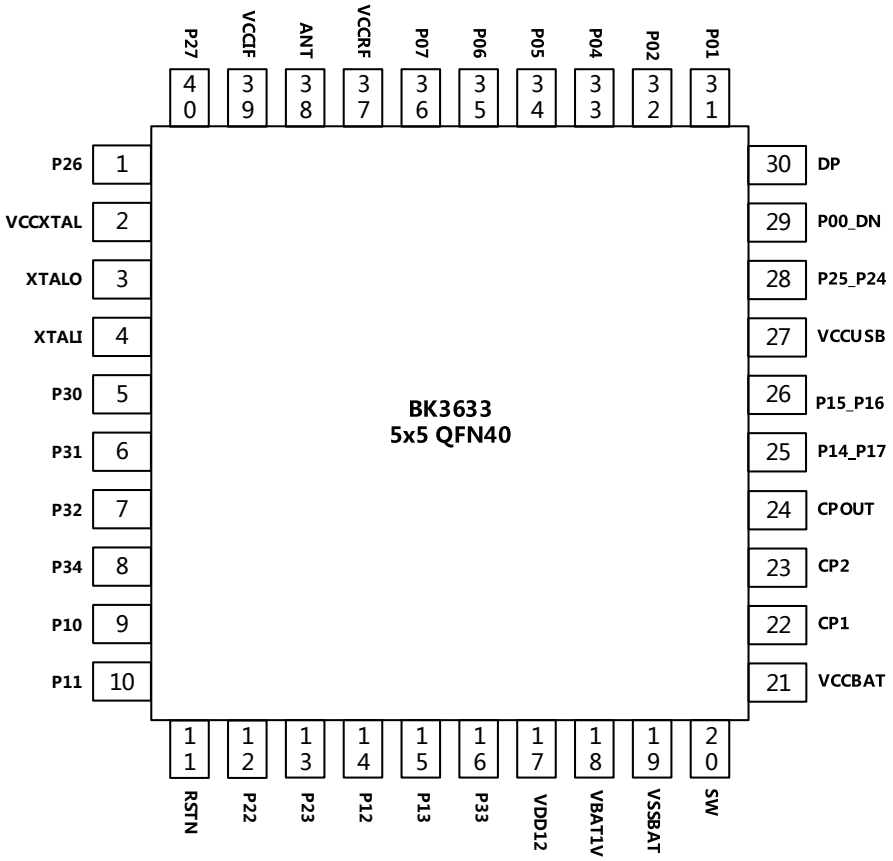


Figure 3 BK3633 QFN40 Pin Assignment

Table 2 BK3633 QFN40 Pin Description

PIN	Name	Pin Function	Description
1	P26	Digital I/O	General purpose IO
2	VCCXTAL	Power	XTAL power
3	XTALO	Analog	16 MHz crystal output
4	XTALI	Analog	16 MHz crystal input
5	P30	Digital I/O	General purpose IO
6	P31	Digital I/O	General purpose IO
7	P32	Digital I/O	General purpose IO

PIN	Name	Pin Function	Description
8	P34	Digital I/O	General purpose IO
9	P10	Digital I/O	General purpose IO
10	P11	Digital I/O	General purpose IO
11	RSTN	Analog	Reset pin of the system, low active
12	P22	Digital I/O	General purpose IO
13	P23	Digital I/O	General purpose IO
14	P12	Digital I/O	General purpose IO
15	P13	Digital I/O	General purpose IO
16	P33	Digital I/O	General purpose IO
17	VDD12	Analog	LDO output, 1.2 V
18	VBAT1V	Analog	One battery mode (battery input) or two battery mode (Ground)
19	VSSBAT	Ground	Ground
20	SW	Analog	Switch regulator pin for two battery mode
21	VCCBAT	Power	Battery power, 3 V
22	CP1	Analog	Charge pump component for FLASH
23	CP2	Analog	Charge pump component for FLASH
24	CPOUT	Power	Charge pump output voltage for FLASH
25	P14_P17	Digital I/O	General purpose IO
26	P15_P16	Digital I/O	General purpose IO
27	VCCUSB	Power	Leave NC without USB
28	P25_P24	Digital I/O	General purpose IO
29	P00_DN	Digital/ Analog	General purpose IO, USB DN
30	DP	Analog	USB DP
31	P01	Digital I/O	General purpose IO
32	P02	Digital I/O	General purpose IO
33	P04	Digital I/O	General purpose IO
34	P05	Digital I/O	General purpose IO
35	P06	Digital I/O	General purpose IO
36	P07	Digital I/O	General purpose IO
37	VCCRF	Power	RF power
38	ANT	RF	RF signal port
39	VCCIF	Power	IF power

PIN	Name	Pin Function	Description
40	P27	Digital I/O	General purpose IO

2.3 QFN48

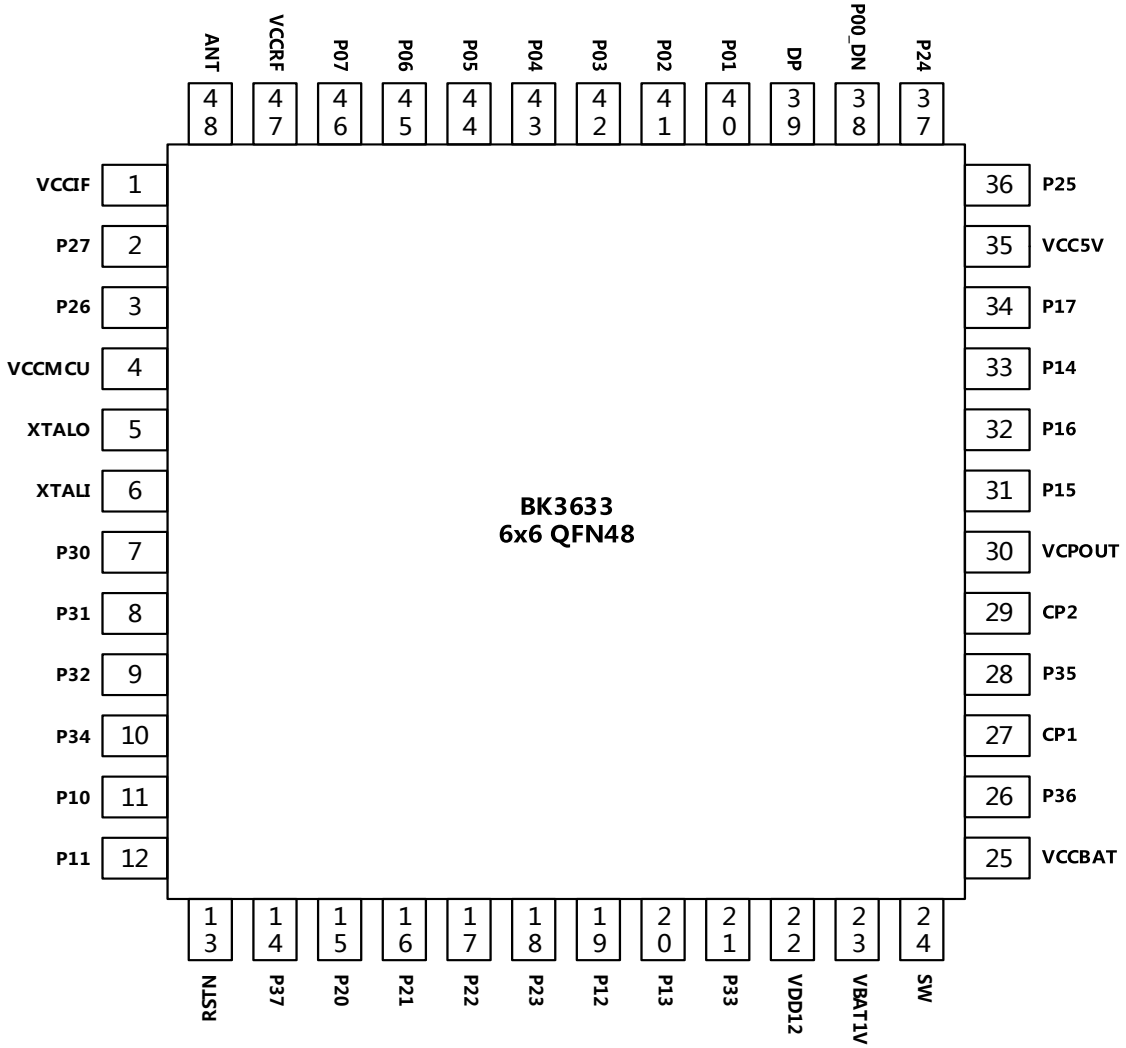


Figure 4 BK3633 QFN48 Pin Assignment

Table 3 BK3633 QFN48 Pin Description

PIN	Name	Pin Function	Description
1	VCCIF	Power	IF power, 1.5 V

PIN	Name	Pin Function	Description
2	P27	Digital I/O	General purpose IO
3	P26	Digital I/O	General purpose IO
4	VCCMCU	Power	Power, 1.5 V
5	XTALO	Analog	16 MHz crystal output
6	XTALI	Analog	16 MHz crystal input
7	P30	Digital I/O	General purpose IO
8	P31	Digital I/O	General purpose IO
9	P32	Digital I/O	General purpose IO
10	P34	Digital I/O	General purpose IO
11	P10	Digital I/O	General purpose IO
12	P11	Digital I/O	General purpose IO
13	RSTN	Analog	Reset pin of the system, low active
14	P37	Digital I/O	General purpose IO
15	P20	Digital I/O	General purpose IO
16	P21	Digital I/O	General purpose IO
17	P22	Digital I/O	General purpose IO
18	P23	Digital I/O	General purpose IO
19	P12	Digital I/O	General purpose IO
20	P13	Digital I/O	General purpose IO
21	P33	Digital I/O	General purpose IO
22	VDD12	Analog	LDO output, 1.2 V
23	VBAT1V	Analog	One battery mode (battery input) or two battery mode (Ground)
24	SW	Analog	Switch regulator pin for two battery mode
25	VCCBAT	Power	Battery power, 3 V
26	P36	Digital I/O	General purpose IO
27	CP1	Analog	Charge pump component for FLASH
28	P35	Digital I/O	General purpose IO
29	CP2	Analog	Charge pump component for FLASH
30	VCPOUT	Power	Charge pump output voltage for FLASH
31	P15	Digital I/O	General purpose IO
32	P16	Digital I/O	General purpose IO
33	P14	Digital I/O	General purpose IO
34	P17	Digital I/O	General purpose IO

PIN	Name	Pin Function	Description
35	VCC5V	Power	5 V power
36	P25	Digital I/O	General purpose IO
37	P24	Digital I/O	General purpose IO
38	P00_DN	Digital/ Analog	General purpose IO, USB DN
39	DP	Analog	USB DP
40	P01	Digital I/O	General purpose IO
41	P02	Digital I/O	General purpose IO
42	P03	Digital I/O	General purpose IO
43	P04	Digital I/O	General purpose IO
44	P05	Digital I/O	General purpose IO
45	P06	Digital I/O	General purpose IO
46	P07	Digital I/O	General purpose IO
47	VCCRF	Power	RF power
48	ANT	RF	RF signal port

3 Functional Description

3.1 Power Management

The power management system on the BK3633 includes a DC-DC converter which can be configured as boost mode or buck mode and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The BK3633 can be powered directly from a 2.0 V to 3.6 V external battery via the VCCBAT pin or a 0.9 V to 1.5 V external battery via the VBAT1V pin.

The BK3633 can operate in buck mode, boost mode or LDO mode. Figure 5 below shows the power supply diagram in buck, LDO and boost modes. When operating in boost and buck mode, most of the modules are powered by the DC-DC converter. When operating in LDO mode, all modules are powered by the SYS LDO regulator. Outputs from the DC-DC

converter and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the BK3633 EVB User Guide and application note for more details about choosing the proper bypass capacitors.

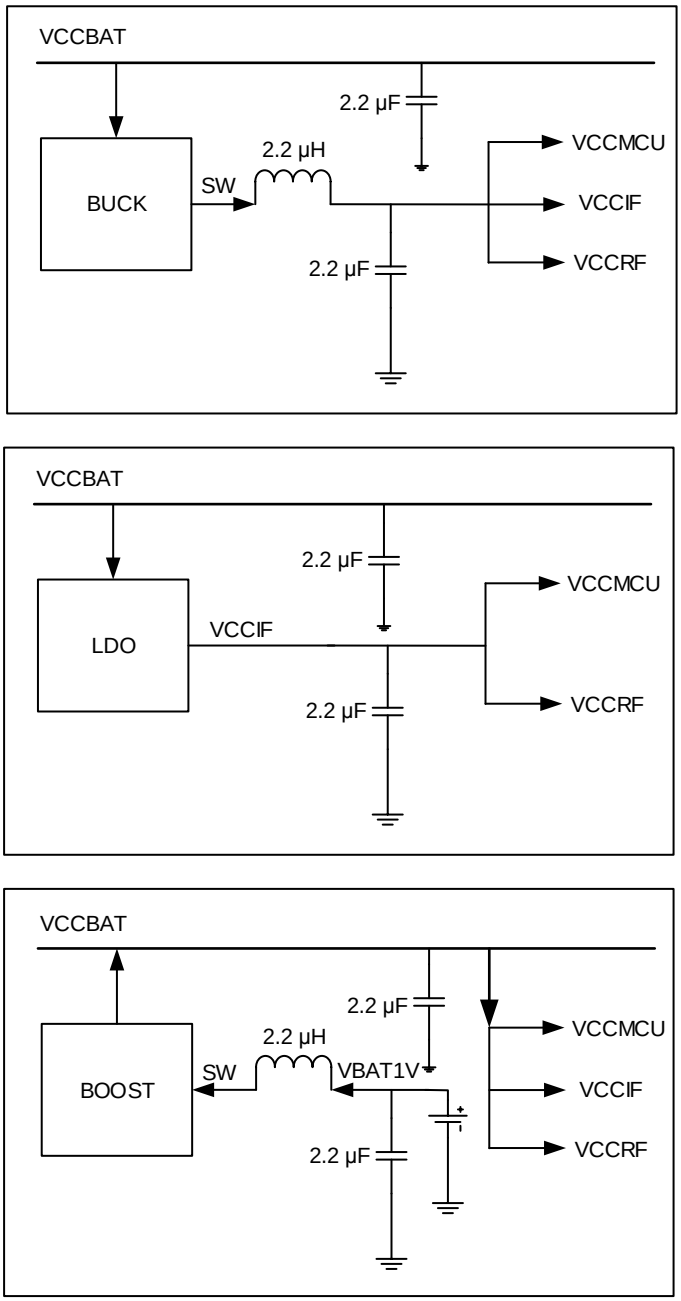


Figure 5 Power Supply in Buck, LDO and Boost Modes

Note: For buck and LDO modes, the VBAT1V pin must be grounded.

The BK3633 can enter deep sleep mode when there is no active connection. The BK3633 can be woken from deep sleep mode by any GPIO signal.

3.2 GPIO

The BK3633 has up to 32 GPIO pins, which can be configured as either input or output. Secondary functions are available for GPIO pins and can be configured via firmware.

At the beginning of the chip start-up, the chip will enter programming mode, JTAG mode or normal according received command from Mode Selecting Pin.

Table 4 BK3633 GPIO Function Mapping

	Description		Program Mode	JATG Mode
P00	UART	UART_TX/SCL	DL_UART_TX	
P01		UART_RX/SDA	DL_UART_RX	
P02	I2C	SCL		
P03		SDA		JTAG_NTRST
P04	SPI	SPI_SCK	SPI_MOSI	JTAG_TDI
P05		SPI_MOSI	SPI_MISO	JTAG_TDO
P06		SPI_MISO/PWM[5]	SPI_SCK	JTAG_TCK
P07		SPI_NSS/PWM[4]	SPI_CS	JTAG_TMS
P10	PWM	PWM[0]		
P11		PWM[1]		
P12		PWM[2]		
P13		PWM[3]		
P14		PWM[4]		
P15		PWM[5]		
P16	UART2	UART2_TX		
P17		UART2_RX		

	Description		Program Mode	JATG Mode
P20				
P21				
P22				
P23				
P24				
P25	PCM/I2S	PCM_BCLK		
P26		PCM_SCLK		
P27		PCM_DOUT		
P30		PCM_DIN		
P31	ADC/Clock Output	Ch1		
P32		Ch2		
P33		Ch3/CLKOUT		
P34		Ch4		
P35		CLKOUT2/Ch5		
P36				
P37				

Each GPIO pin can be the source to wake up MCU from shutdown state. In the shutdown state, any voltage level change on the pre-configured GPIO pin will trigger the wake-up procedure.

3.3 Timers

3.3.1 PWM Timers

There are six 32 bits PWM timers. The clock of PWM timers can be selected as 32 kHz clock or 16 MHz clock by register.

There are four modes of PWM timers. The first mode is the timer mode. The timer mode can generate interrupt to MCU. The second mode is the PWM mode, which can generate PWM waveform and output to GPIO pins to drive external device such as LED. Six GPIO pins can be used to output

PWM waveform separately. The third mode is the capture mode, which can count the clock cycle between either combination of falling edge or rising edge of the signal in the special pin. The fourth mode is the pulse mode, which can count the number of either active high or active low pulse.

3.3.2 Watch Dog Timer and RTC Timer

The watch dog timer and RTC timer run on the always on power domain, whose clock source is 32 kHz clock.

The 16 bits watch dog timer runs with 4 kHz frequency that its period can be up to 16 second. After the watch dog timer is expired, it will reset the whole chip.

The 32 bits RTC timer in always on power domain run with ROSC frequency that its period can be up to one day. After the RTC timer times out, it will wake up the MCU.

3.3.3 Sub-Micro Second Event Timer

There is a sub-micro second resolution timer recording the timing of special event such as the moment of the Bluetooth transmitter first bit of the packet or receiver synchronization word gets matched. Also it can get a shot of the timing of the edge of special GPIO.

3.4 ADC

A 10-bit generic ADC is integrated in BK3633. Totally five external channels and three internal channels can be selected for ADC transfer. It supports both single and continuous modes.

ADC Channel Number	ADC Source
Channel 0	Temperature Sensor

ADC Channel Number	ADC Source
Channel 1	GPIO31
Channel 2	GPIO32
Channel 3	GPIO33
Channel 4	GPIO34
Channel 5	GPIO35
Channel 6	VBAT1V-pin
Channel 7	VCCBAT-pin

3.5 UART, I2C and SPI

There are two UART interfaces, one I2C interface and one SPI interface, which support both master and slave modes.

The UART baud rate can be up to 3.2 MHz, and the SPI clock speed can be up to 32 MHz.

3.6 USB

It integrates USB host and device transceiver and baseband.

The USB interface supports EP0 to EP8. For EP0 there is 64 bytes FIFO each direction. For every channel of EP1 to EP4, there is 256 bytes FIFO each direction. For every channel of EP5 to EP8 there is 64 bytes FIFO in single direction.

3.7 True Random Number Generator

By using device noise variation characteristic, it provides a one bit true random number generator.

3.8 I2S Digital Audio

The I2S audio interface is mapped to GPIO[25,26,27,30], which support arbitrary sample rates from 8 kHz to 96 kHz. When working as master, the main clock can be output from GPIO33.

The I2S interface supports both PCM mono channel mode and I2S stereo channel mode. The data width can be 16, 24 and 32 bit.

3.9 Code Encryption and System Security

There is one time NVM for code encryption and system security. Each unit has different password for code encryption, where hardware will do the decryption automatically.

The download and debug interface can be disabled permanently by the user to keep system security.

The user can also use the NVM for other purposes such as unique ID or MAC address. The NVM used for code encryption can be closed for read and write operation, and other space can be closed for write operation. Once the access right is changed, no roll back is possible to provide permanent security of the system.

4 Electrical Specifications

Table 5 BK3633 DC Characteristics

Name	Parameter (Condition)	Min	Typical	Max	Unit
VCCBAT	Battery Supply	0.9	3.0	3.6	V
TEMP	Temperature	-40	+20	+125	ºC
VIH	High level	VCC-0.3		VCC+0.3	V
VIL	Low level	VSS		VSS+0.3	V
VOH	High level (IOH=-0.25 mA)	VCC- 0.3		VCC	V
VOL	Low level (IOL=0.25 mA)	VSS		VSS+0.3	V
IVDD	Deep sleep (1 kHz Timer)		0.9		μA
IVDD	Shutdown		100		nA
IVDD	Sleep current (RF OFF, 32 kHz clock, DIG Retention)		2		μA
IVDD	Active RX (3.3 V)		5.5		mA
IVDD	Active TX @ 0 dBm (3.3 V)		6.1		mA

Table 6 BK3633 RF Characteristics

FOP	Operating frequency	2402		2480	MHz
FXTAL	Crystal frequency		16		MHz
RFSK	Air data rate	0.125	1	2	Mbps
PRF	Output power	-20	9.5	+10	dBm
BLE 1 Mbps data rate performance					
PBW	Modulation 20 dB bandwidth			1	MHz
PRF1	Out of band emission 2 MHz		-35		dB
PRF2	Out of band emission 3 MHz		-45		dB
Carrier Drift	Maximum carrier drift	-50	5	50	kHz
Drift Rate	Maximum drift rate		2.5	20	kHz/50μs
Δf1avg	Maximum modulation	225	255	275	kHz
Δf2min	Minimum modulation	185	213		kHz
Δf2avg/Δf1avg		0.8	0.92		
Max Input	30.8% PER		0		dBm
RXSENS	30.8% PER sensitivity		-96		dBm

Intermodulation	Pin=-64 dBm; Punwant=-50 dBm; f0=2f1-f2, f2-f1=3 MHz or 4 MHz or 5 MHz		-27	-22	dBm
C/ICO	Co-channel C/I		9		dB
C/I1ST	ACS C/I 1MHz		-3		dB
C/I2ND	ACS C/I 2MHz		-39		dB
C/I3RD	ACS C/I 3MHz		-49		dB
C/I1STI	ACS C/I Image channel		-32		dB
C/I2NDI	ACS C/I Image +1 MHz		-43		dB
Blocking	@ 30 MHz ~ 2 GHz		5		dBm
Blocking	@ 2 GHz ~ 2.399 GHz		-3		dBm
Blocking	@ 2.484 GHz ~ 3 GHz		-2		dBm
Blocking	@ 3 GHz ~ 12.75 GHz		5		dBm
Leakage	Leakage @ < 1 GHz		-71		dBm
Leakage	Leakage @ > 1 GHz		-56		dBm
RSSI	Dynamic range	-97		-62	dBm
RSSI	Resolution		1		dB

Table 7 BK3633 ADC Characteristics

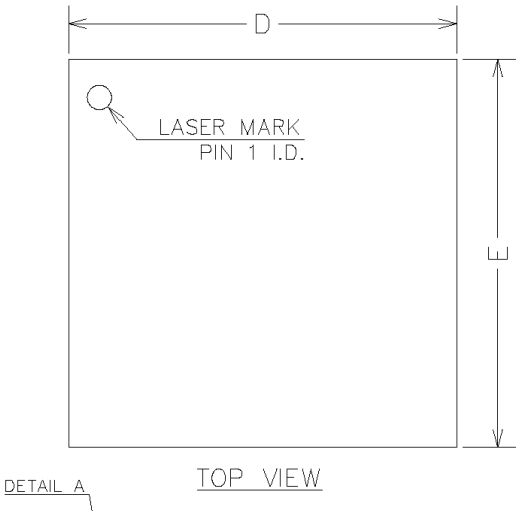
Name	Condition	Min	Typical	Max	Unit
Conversion Clock (Fs)				16	MHz
Conversion Time			16		Cycle
VREF	Internal		0.5		V
Resolution			10		bits
No Missing Code			9		bits
Input Voltage Range		0		ADC_VREF*2	V
Input Impedance			16/(Fs*Cs)		kOhm
Input Capacitance (Cs)			8		pF
Offset		-90		90	mV
DNL			1		bits
INL			2		bits

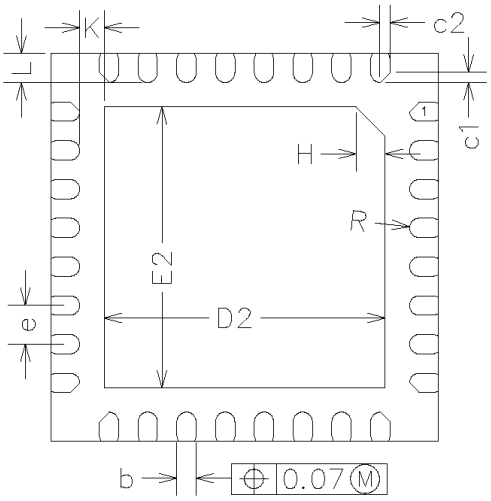
Name	Condition	Min	Typical	Max	Unit
Offset Temperature Drift				0.2	LSB/ºC
Gain Temperature Drift				0.01	%/ºC
SNDR			60		dB
Dynamic Range			64		dB
Tstartup				1	μs
Current Consumption			750		μA

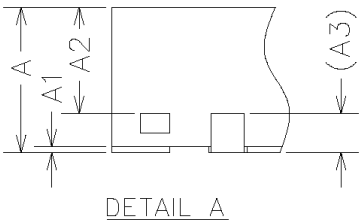
5 Package Information

5.1 QFN 4x4 32-Pin

The BK3633 32-pin uses the 4 mm x 4 mm QFN package.





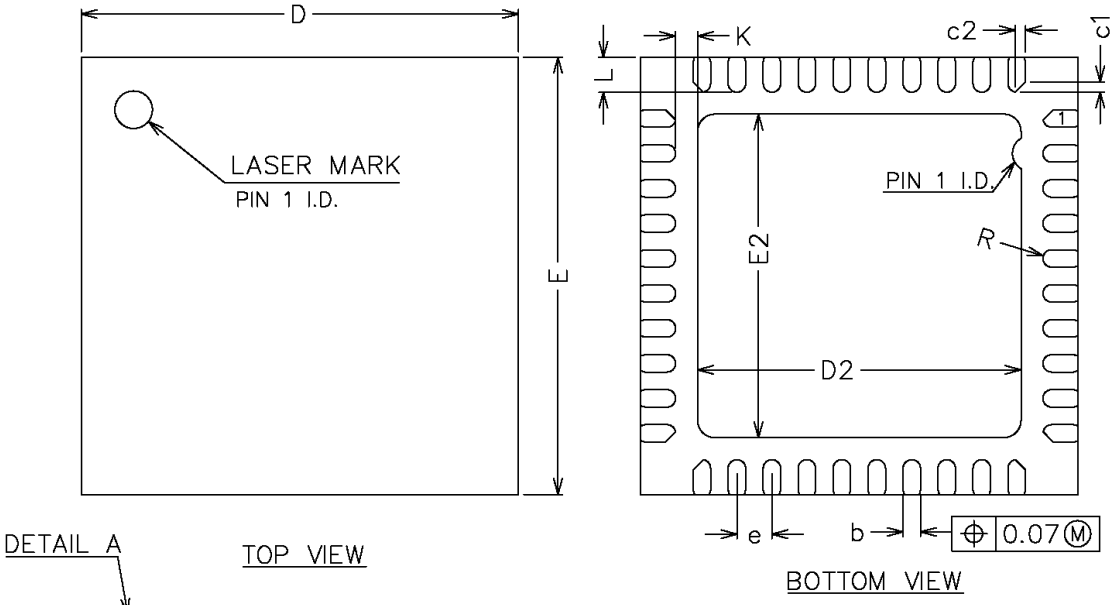


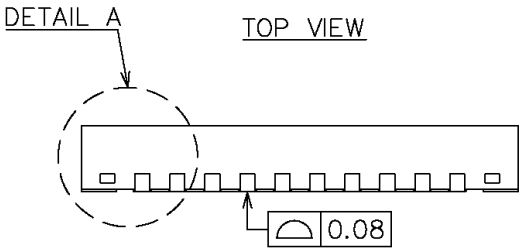
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

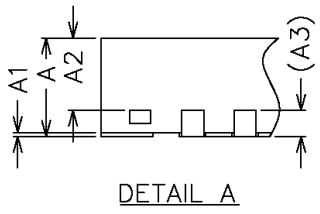
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H		0.30REF	
K		0.25REF	
L	0.25	0.30	0.35
R	0.09	–	–
c1	–	0.10	–
c2	–	0.10	–

5.2 QFN 5x5 40-Pin

The BK3633 40-pin uses the 5 mm x 5 mm QFN package.





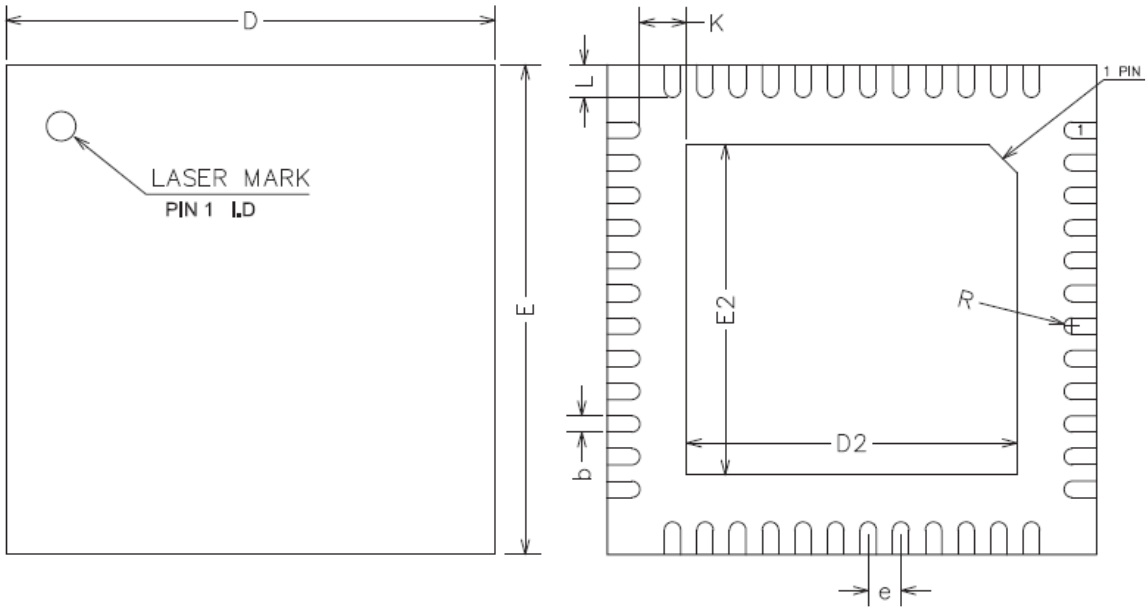


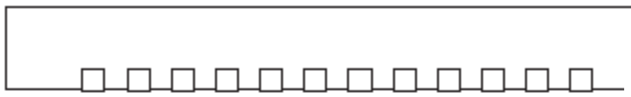
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

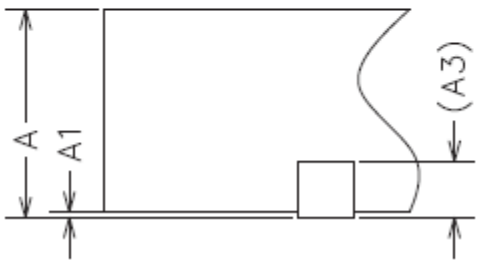
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
c1	–	0.12	–
c2	–	0.12	–

5.3 QFN 6x6 48-Pin

The BK3633 48-pin uses the 6 mm x 6 mm QFN package.



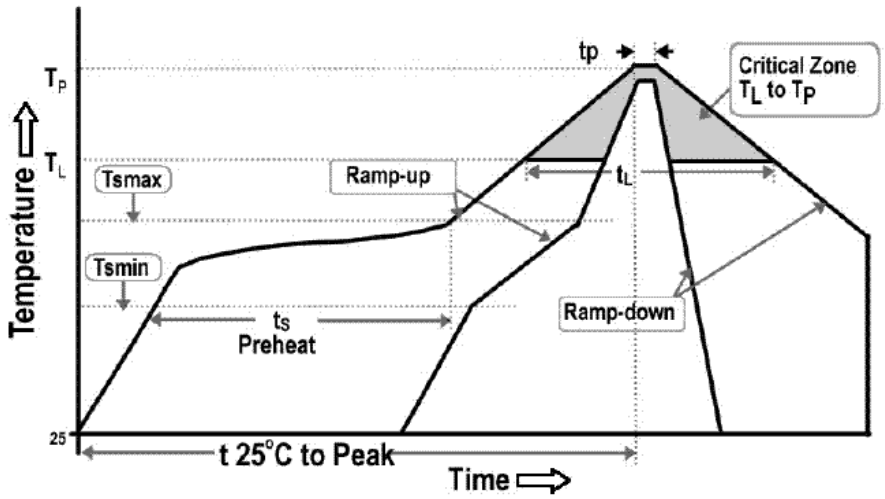




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

6 Solder Reflow Profile



Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC (RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

7 Ordering Information

Part Number	Package	Packing	Minimum Order Quantity
BK3633QN32	QFN 4mmx4mm 32-Pin	Tape Reel	3K
BK3633QN40	QFN 5mmx5mm 40-Pin	Tape Reel	3K
BK3633QN48	QFN 6mmx6mm 48-Pin	Tape Reel	3K

Revision History

Version	Date	Description
0.1	20/02/2020	Initial draft
0.2	07/04/2020	Updated some information of package
0.3	19/05/2020	Updated some information of PIN
0.4	30/06/2020	Updated flash information
0.5	09/09/2020	Updated Section 2 Pin Information and Section 4 Electrical Specifications, added Section 6 Solder Reflow Profile
0.6	19/10/20	Updated the GADC information and QFN package of QFN 6X6 48PIN
0.7	27/10/20	Updated the description of RSTN pin
0.8	16/12/20	Updated the information of QFN48 package
0.9	13/04/21	Updated Figure 3 BK3633 QFN40 Pin Assignment and Figure 4 BK3633 QFN48 Pin Assignment
1.0	11/10/21	• General wording fix • Section 1.2 Features: Revised deep sleep current with low power running timer, added 2.4 GHz proprietary 250 kbps, eFUSE and AES support and removed IrDA support • Revised the maximum SPI clock speed in Section 1.2 Features and Section 3.5 UART, I2C and SPI • Updated Table 2 BK3633 QFN40 Pin Description and Table 3 BK3633 QFN48 Pin Description • Added Section 3.1 Power Management • Updated Table 4 BK3633 GPIO Function Mapping • Updated the channel number and source for ADC in Section 3.4 ADC
1.1	22/12/21	• Revised the maximum output power in Section 1.2 Features and Table 6 BK3633 RF Characteristics • Removed AoA/AoD feature from Section 1.2 Features and original Section 3.10 • Removed output power with PA from Table 6 BK3633 RF Characteristics

Version	Date	Description
		• Removed external reference voltage for ADC from Table 7 BK3633 ADC Characteristics
1.2	23/03/06	• Updated dimensions of A, A1 and A2 for QFN32 package in Section 5.1 QFN 4x4 32-Pin • Updated dimensions of A, A1 and A2 for QFN40 package in Section 5.2 QFN 5x5 40-Pin
1.3	23/03/24	Updated the maximum MCU frequency and the digital PLL frequency in Section 1.2 Features