The stage delays are 35, 40, 28, 42, 30, and 38 nanoseconds, and the latch delay in each stage is 5 nanoseconds. Total delay = (35+5) + (40+5) + (28+5) + (42+5) + (30+5) + (38+5)

Total delay = 243 nanoseconds.

The clock period is the inverse of the clock frequency.

Therefore, we can calculate the maximum clock frequency as follows: Maximum clock frequency = 1 / (Total delay) Maximum clock frequency = 1 / (243 nanoseconds) Maximum clock frequency = 4.12 MHz.

The maximum clock frequency at which the pipeline can operate is = 4.12 MHz.

2. a) For the wireless sensor nodes scenario, using a microcontroller would be the most appropriate choice. This is because the task involves low-power sensors that will be turned off most of the time and only wake up when a vibration sensor is triggered. A microcontroller can handle low-power operations and can be programmed to control the sensor nodes' power states. Additionally, microcontrollers are cheaper and easier to program than FPGAs or ASICs. The sensors' relatively simple data collection and processing requirements do not necessitate the use of FPGAs or ASICs.

b) For the scanning tunneling electron microscope control scenario, an FPGA would be the most suitable choice. The device requires high-speed data acquisition, processing, and output, with multiple I2C and SPI streams. FPGAs can handle high-speed parallel processing of data and are highly customizable for specific applications, making them well-suited for handling the wide variety of sensors required by the microscope. Additionally, FPGAs can be programmed for real-time processing, which is crucial for the microscope's control system. ASICs could also be used, but they are less flexible than FPGAs, and require a significant investment in upfront design costs. Microcontrollers, on the other hand, would not be able to handle the high-speed processing requirements of this scenario