计算机组织与结构双语-开发区

考试时间：2022-12-26 08:00~2022-12-26 10:00 答题时长：100 分钟

四道大题 共 2 页 满分 100 分

一、单项选择题（每题 2 分，共 20 分）

1. Which capacity is the largest?
   A. Register
   B. Cache
   C. Memory
   D. Disk
2. Which is **not** the functionality of the compiler?
   A. Preprocessing
   B. Translation
   C. Compilation
   D. Linking
3. Which of the followings do we need to use logic shift operation?
   A. Left shift for an unsigned number
   B. Left shift for a signed number
   C. Right shift for an unsigned number
   D. Right shift for a signed number
4. Which of the following is **not** true?
   A. $|Tmin| = Tmax + 1$
   B. $Umax = 2 * Tmax + 1$
   C. $Umax = 2^{w-1} - 1$
   D. $Umin = 0$
5. Which of the following cannot be the operand of an instruction?
   A. Memory
   B. Immediate
   C. Register
   D. Cache
6. Which instruction can cause pipeline hazards?
   A. Add
   B. Call
   C. Ret
   D. Mov
7. At which stage will the processor access the value of registers?
   A. Fetch
   B. Decode
   C. Memory
   D. Execute
8. Which is **not** the characteristic of CU?
   A. Define the basic elements of the processor
   B. Describe the micro-operations that the processor performs
   C. Use signals to control the micro-operations
   D. Execute logic and arithmetic calculations

9. In a micro-programmed control unit, which is **not** correct?
   A. The control memory specifies the sequencing
   B. The control word can indicate whether a signal is ON or OFF
   C. The resulting control signals will cause one or more micro-operations to be performed
   D. If the condition indicated by the condition bits is true, the CU will execute the next microinstruction in sequence
10. Which description of interrupt is true?
   A. It is composed of both hardware and software operations
   B. The main program will be suspended and recovered after completing the interrupt routine
   C. The program status word will be stacked in the memory
   D. The interrupt routine of DMA is to use the cycle stealing process to accelerate

二、简答题（每题 5 分，共 20 分）

1. List the differences between SRAM and DRAM.
2. List the main components of disk access time. Which is the longest? Explain how to calculate each of them.
3. Describe the details for reading a sector from a Disk.
4. List three mechanisms for dealing with Bus Conflict. Describe the details for each of them.

三、分析题（4 小题，共 35 分）

1. （10 分）Can we directly connect the peripherals to the system bus? Explain the reason.
2. （10 分）How many different type of misses of cache? Give an example for each of them.
3. （10 分）TLB can be used to speed up address translation. Explain following issues.
   （1）（5 分）What is a TLB? Explain its usage.
   （2）（5 分）Describe the details of the TLB hit and TLB miss.
4. （5 分）List all micro-operations of the interrupt cycle.

四、计算题（2 小题，共 25 分）

1. （15 分）Given a number A = 2023.125
   （1）（5 分）Compute the 32-bit floating representation.
   （2）（5 分）Store A in a big endian machine with an entrance 0x2000. Draw a figure to illustrate the byte representation.
   （3）（5 分）After A is transferred to a 64-bit X86 machine with a memory entrance 0x8000, please draw a figure to illustrate the new byte representation.
2. （10 分）In a computer, four SDRAMs are used. In each SDRAM, D0~D15 are used as the data buses, A0~A15 are row address buses, and A0~A10 are multiplexed (复用) as column address buses. BA0, BA1 and BA2 are used for chip selection. Please compute the overall capacity in MB.