DIGITAL DESIGN

LAB1　USING VIVADO + EGO1

2021 SUMMER TERM

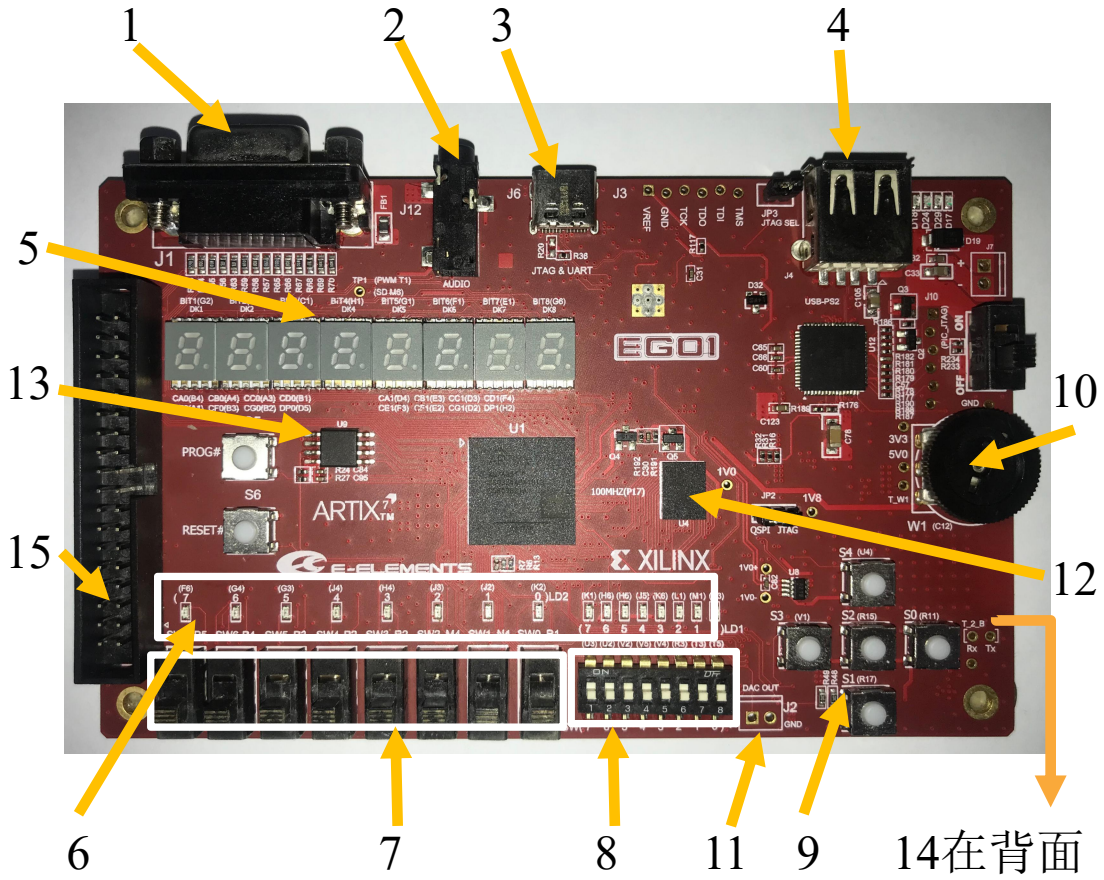
- Sakai site:
  - CS211-M21
- E-mail
  - wangq9@mail.sustech.edu.cn
- Office Hour
  - Friday, 14:30~17:00; Room 110, South Tower, College of Engineering
- Lab Grading Criteria
    - 20% class performance + 30% practice + 50% project
    - Class performance: attendance; question & answer
    - Practice: 1 or 2 practices in class (*1.0 if completed in class; *0.8 if completed in 1 week; *0.5 if completed in 2 weeks; *0.2 if completed over 2 weeks)
    - Project: a whole digital system run on EGO1 board

EXPERIMENTAL SUITE: VIVADO 2017 + EGO1

- vivado 2017 :
  - Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.
  - Vivado enables developers to synthesize (compile) their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.
  - The version we choose is vivado 2017

- Installation of vivado (20 G free hard disk space above is suggested)
  - Attention: the name of the directory which includes installation package MUST NOT containing Chinese character !

EGO1

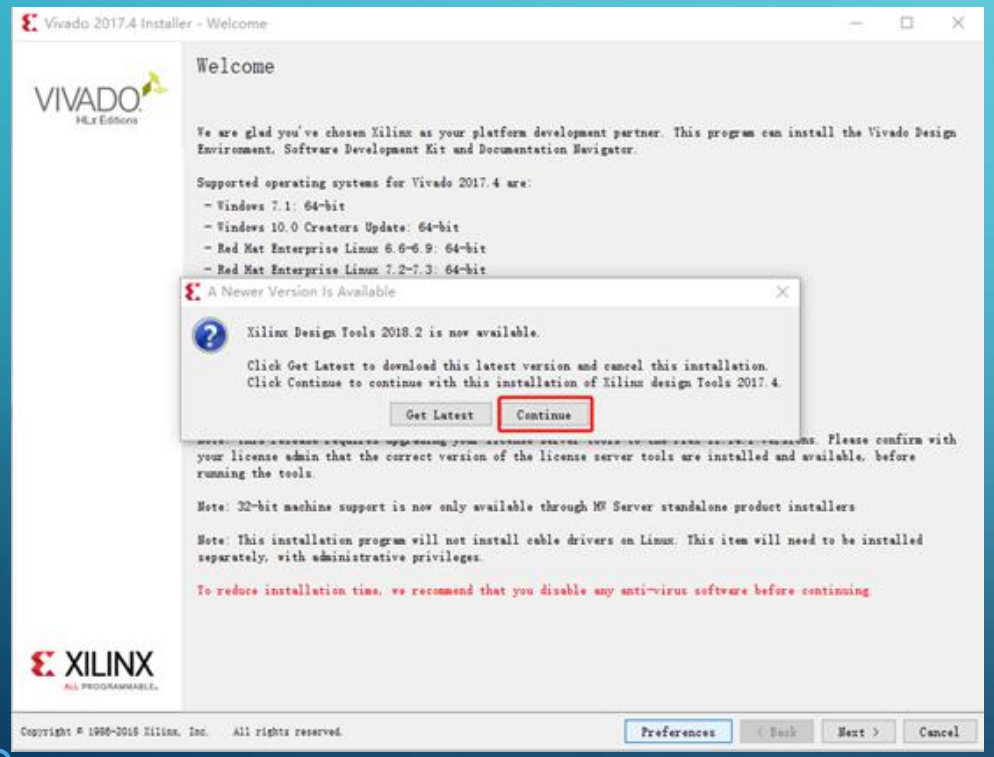


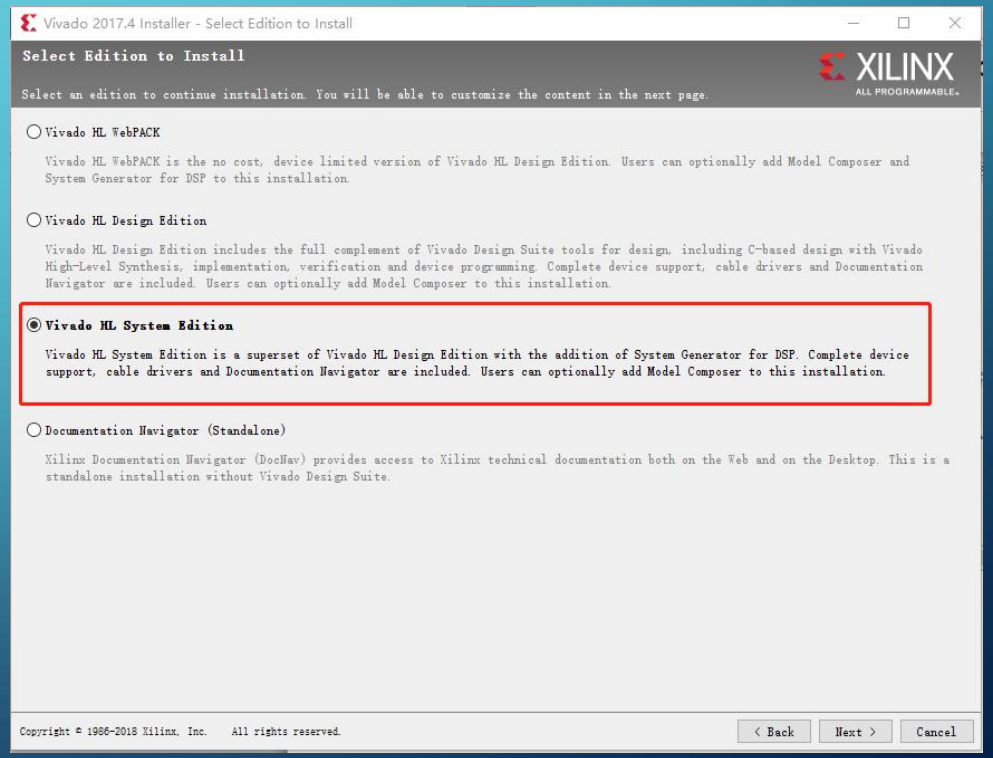
编号	描述	编号	描述
1	VGA接口	9	5个按键
2	音频接口	10	1个模拟电压输入
3	USB转Type-C接口	11	1个DAC输出接口
4	USB接口	12	SRAM存储器
5	2个4位数码管	13	SPI FLASH存储器
6	16个LED灯	14	蓝牙模块
7	8个拔码开关	15	通用扩展接口
8	1个8位DIP开关		

VIVADO(2017.4) INSTALLATION （TIPS1）

ftp://10.20.118.226/ account: ftp-d-logic password: ggsddu

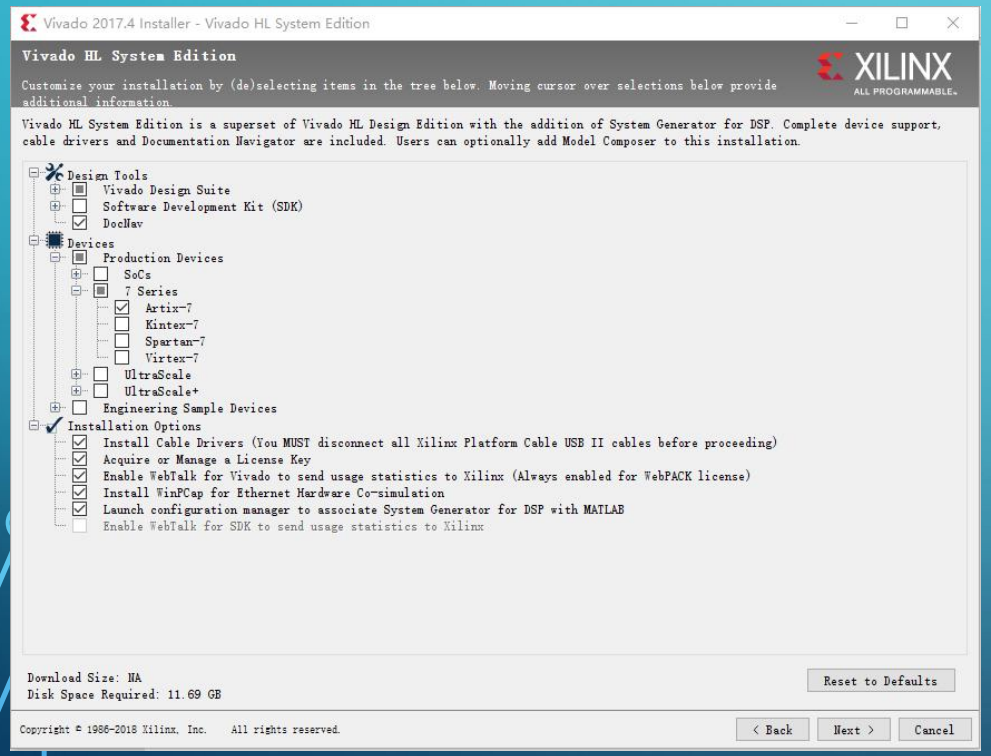
xsetup



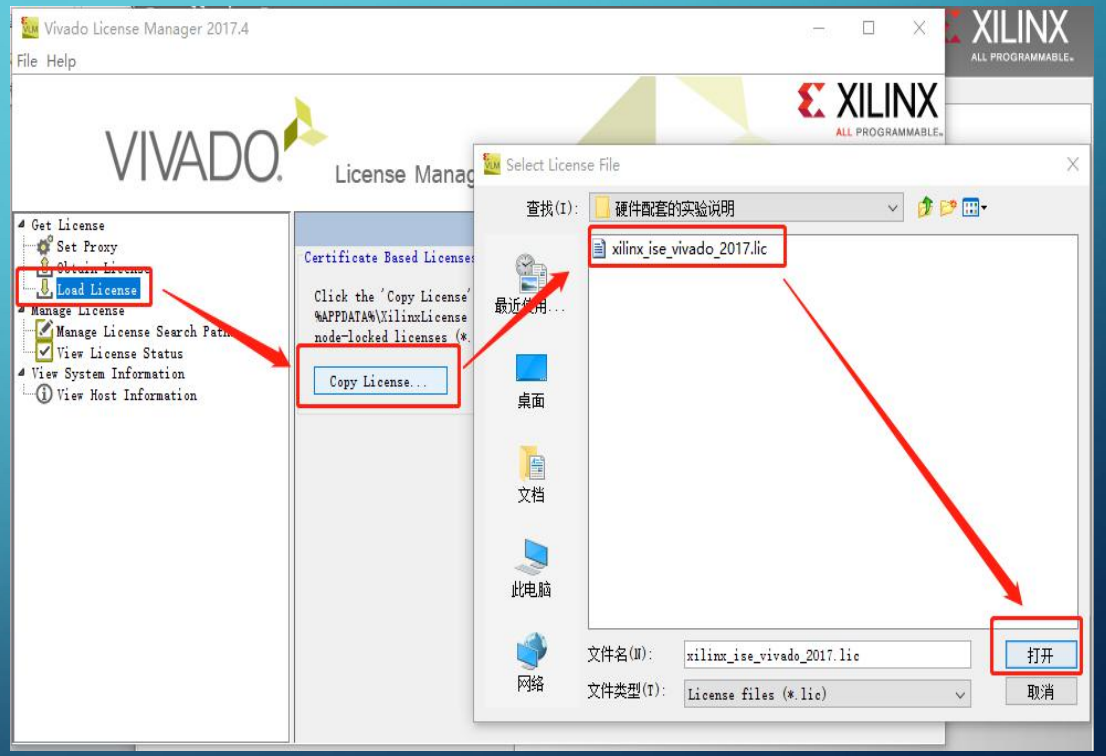


VIVADO INSTALLING （TIPS2）

Select only what is needed

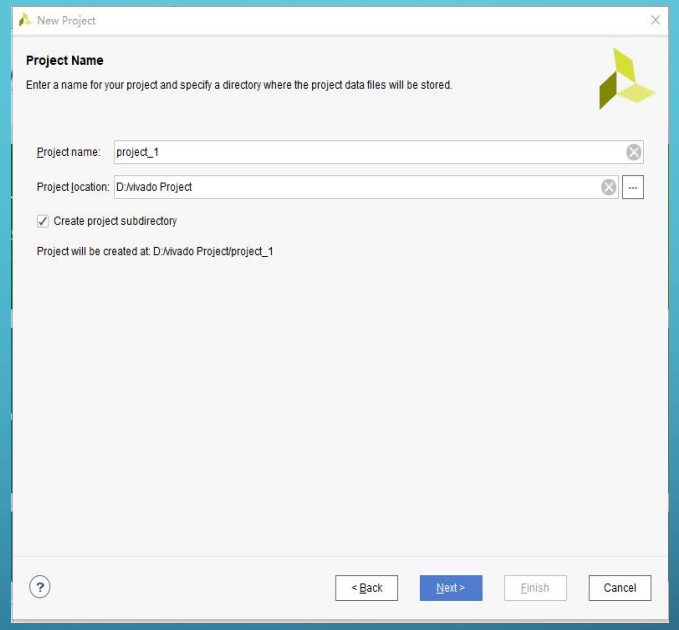


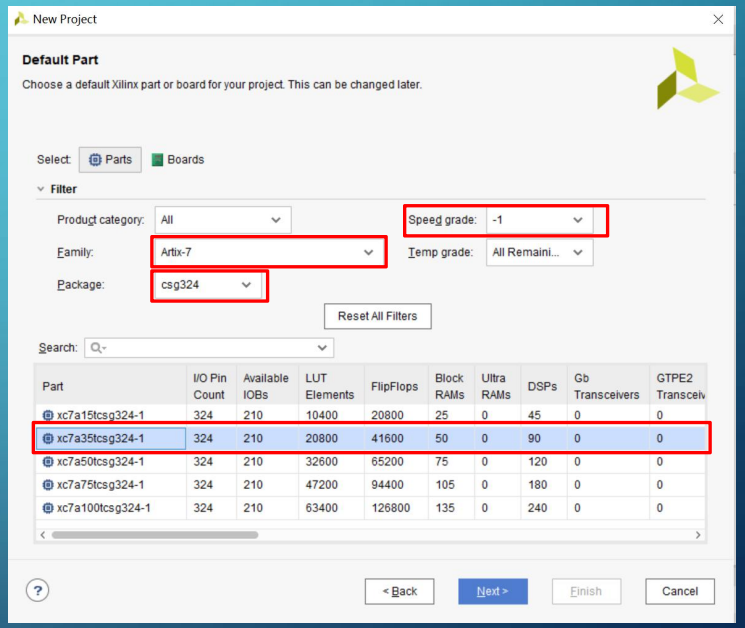
At the end of installing, load license



LAB1 USING VIVADO + EGO1

1. Create project , select “rtl type” , select the corresponding FPGA chip name





tips: FPGA Chip(Artix 7 xc7a35t-1CSG324-1) is embedded in EGO1 board

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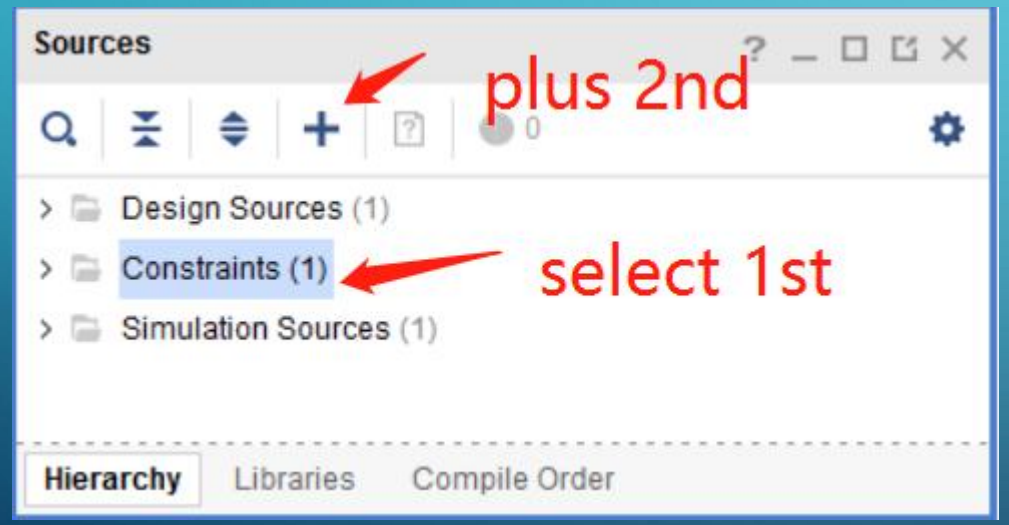
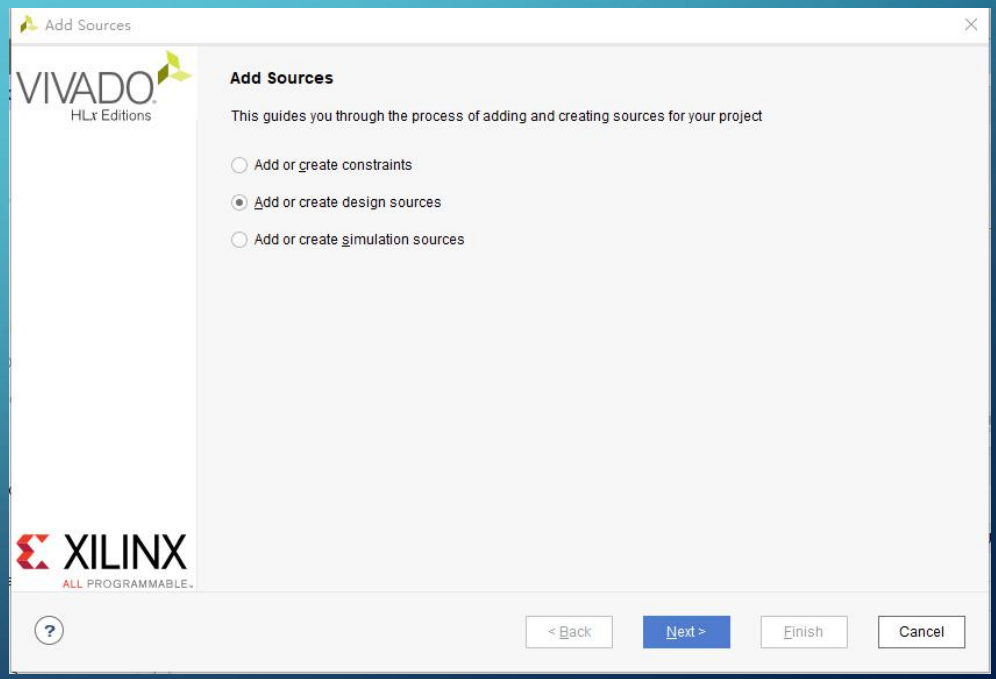
2. Add source file, simulation file and constraints file





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- 3.Following the steps to verify the function and generate bitstream file which is used to program FPGA chip
  - 1）Do the simulation to verify the function of the designed Circuit
  - 2）After simulation ,there will be a waveform which records the states of circuit's input and output signals
  - 3）if the function of circuit is ok , run synthesis ,then run implements
  - 4) after implementation is finished, Generate Bitstream , there will be a .bit file which will be used to program device

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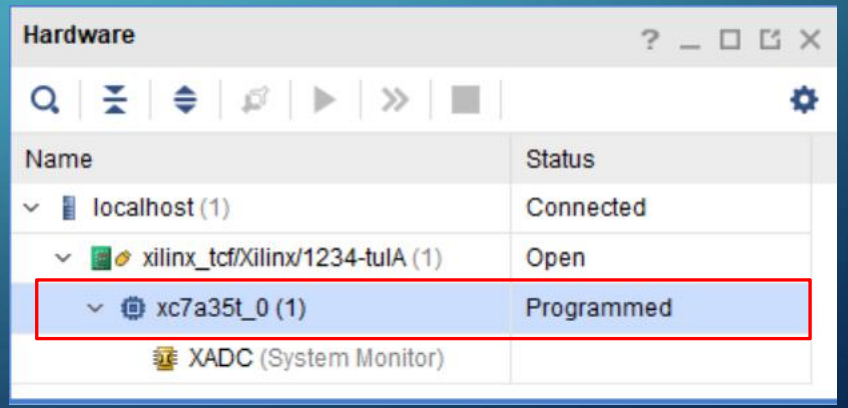
- 4. Connect EGO1 board with PC
  - USB typeC interface
- 5. Turn on the EGO1 board
- 6. Use the “open target ” to connect the vivado project with EGO1 board



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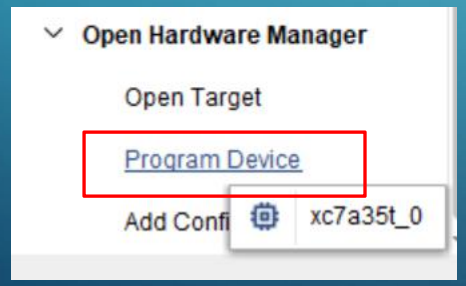
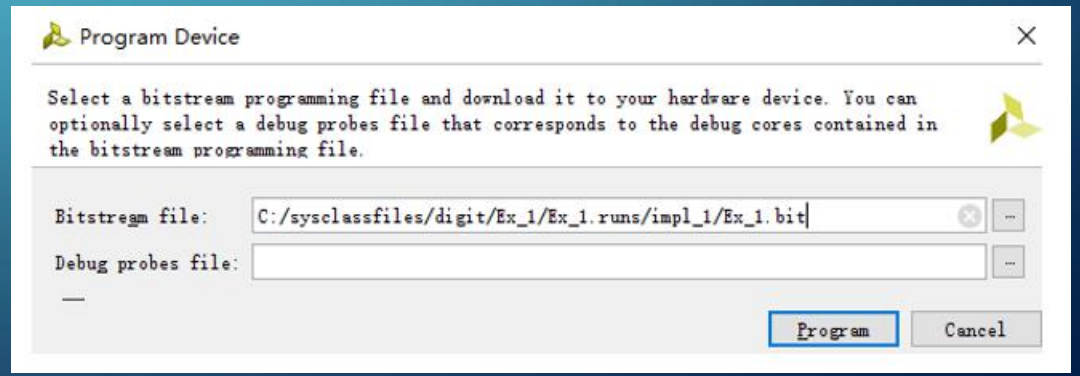
- 7. Right click “program device”, then choose the device name.
- 8. Select the bitstream file, and click “program” button.
- 9. While the the led on EGO1 flashes, it means the bit file has been written into the device.
- 10. Do the testing on the EGO1 board.





PRACTICE 1

- Design a circuit run on EGO1 board, using 16 switches to control the display of 16 leds, led turns light when the corresponding switch is 1.
  1. Use two ways to append source file into project: add file, and create file
  2. Use two ways to append simulation file into project: add file, and create file
  3. Use three ways to append constraints file into project: add file, create file, and I/O planning (As there can only be one constraints file in one project, please remove the current constraints file before appending another constraints file)
  4. Generate bitstream and program EGO1 board
- Tips: the files are in sakai site https://sakai.sustech.edu.cn/portal/site/794e0078-07c8-4f26-9342-ef09b4b77f90/tool/6a25f6d7-c4a5-450c-844a-93c817aa1830?panel=Main#/group/794e0078-07c8-4f26-9342-ef09b4b77f90/Labs/srcs/lab1/