Homework 4 Solution

Problem 1. (25 points)

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

(1) What is the cache block size (in words)? (2 points)

Answer: Offset: 5 bits, thus the block size is $2^5 = 32$ bytes = 8 words

(2) How many entries does the cache have? (2 points)

Answer: Index: 5 bits, thus number of entries = $2^5 = 32$

Starting from power on, the following byte-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

(3) Fill in blanks (show index and tag in decimal, and indicate replace using Y/N) (12 points, 1 point per column)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index	0	0	0	4	7	5	0	0	4	0	5	4
Tag	0	0	0	0	0	0	1	0	0	3	0	2
Hit/Miss	M	H	H	M	M	M	M	M	H	M	H	M
Replace	N	N	N	N	N	N	Y	Y	N	Y	N	Y

Index=number of block in cache
=[block address/block size] mod (number of entries)

Tag = [block address/block size] /(number of entries)

(4) What is the hit ratio? (3 points)

Answer: Hit ratio = 4/12=0.33

(5) List the final state of the cache, with each valid entry represented as a

record of <index, tag, data>. (6 points, 2 points per column)

Answer:

<index	tag	data>
$<00000_2$	00000000000000000011_2	Mem[3072]>
$<00100_2$	00000000000000000010_2	Mem[2176]>
$<00101_2$	00000000000000000000_2	Mem[160]>
$<00111_2$	00000000000000000000_2	Mem[224]>

或者:

<index	tag	data>
< 0	3	Mem[3072]-Mem[3103]>
< 4	2	Mem[2176]-Mem[2207]>
< 5	0	Mem[160]-Mem[191]>
< 7	0	Mem[224] -Mem[255]>

Index、Tag 用十进制或者二进制均可，data 段用 Mem[起始地址]或者 Mem[起始地址]到 Mem[终止地址]一整段表示均可。

Problem 2. (35 points)

For a 2-way set associative cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-11	10-4	3-0

the following byte-addressed cache references are recorded.

Address											
17	32	2	2059	4124	65	2067	2200	30	0	4102	360

Assume that the cache is initially empty. Using LRU replacement policy, answer questions below.

(1) Fill in the blanks (show index and tag in decimal, and indicate replace using Y/N): (24 points, 2 points per column)

Address	17	32	2	2059	4124	65	2067	2200	30	0	4102	360
Index	1	2	0	0	1	4	1	9	1	0	0	22
Tag0	0	0	0	0	0	0	1	1	1	0	0	0
Tag1				1	2		2		0	1	2	
Hit/Miss	M	M	M	M	M	M	M	M	M	H	M	M
Replace	N	N	N	N	N	N	Y	N	Y	N	Y	N

(2) Calculate the cache size. (6 points)

Answer: Number of entries = $2^n = 2^7 = 128$ … (2 points)

考虑 dirty bit、reference bit、valid bit，再加上 tag 和 data:

Size of cache $= 2^n \times \left((2^m \times 32 + (32 - n - m - 2) + 3) \times 2\right)$

$$= 128 \times (4 \times 32 \times 2 + 21 \times 2 + 6)$$
$$= 38912\ bits = 4864\ bytes = 1216\ words$$

或者只考虑 valid bit、tag 和 data：

Size of cache $= 2^n \times \left((2^m \times 32 + (32 - n - m - 2) + 1) \times 2\right)$

$$= 128 \times (4 \times 32 \times 2 + 21 \times 2 + 2)$$
$$= 38400\ bits = 4800\ bytes = 1200\ words$$

…公式列对 2 分，结果算对 2 分

两种结果都算对，结果用 bits、bytes、words 表示均可，无单位扣 1 分，若转化错误扣 1 分

(3) List the final state of the cache (in decimal): (5 points)

Index	Tag	Data	Tag	Data
0	0	Mem[0]	2	Mem[4096]
1	1	Mem[2064]	0	Mem[16]
2	0	Mem[32]		
4	0	Mem[64]		
9	1	Mem[2192]		
22	0	Mem[352]		

或者：

Index	Tag	Data	Tag	Data
0	0	Mem[0]-Mem[15]	2	Mem[4096]-Mem[4111]
1	1	Mem[2064]-Mem[2079]	0	Mem[16]-Mem[31]
2	0	Mem[32]-Mem[47]		
4	0	Mem[64]-Mem[79]		
9	1	Mem[2192]-Mem[2207]		
22	0	Mem[352]-Mem[367]		

Problem 3. (10 points)

The following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
43	16 GiB	4 KiB	4

(1) For a single-level page table, how many page table entries (PTEs) are needed? (6 points)

Answer: Page Size = 4KiB, so there are $log_2 4096 = 12\ bits$ page offset. …(2 points)

For a single-level page table, there will be 43-12=31 bits virtual page number. …(2 points)

So page table entries $= 2^{31}$ …(2 points)

(2) How much physical memory is needed for storing the page table? (4 points)

Answer: PTE Size =4 Bytes. We need $2^{31} \times 4\ bytes = 2^{33}\ Bytes = 8G\ Bytes$ physical memory.

Problem 4. (30 points)

This Exercise examines the single error correcting, double error detecting (SEC/DED) Hamming code.

(1) What is the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code? (10 points)

Answer: Assume that number of parity bit = p, and number of data bits = d.

So there are $p + d$ bit word.

$$2^p \geq p + d + 1$$

and we get $p \geq 8$, we need 8 bits parity bit for single error correcting.

… (5 points)

Considering double error detecting, we need another parity bit for checking all bits. Therefore, the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code is 8+1=9.

… (5 points)

(2) Consider a SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x5C6, is there an error? If so, correct the error. (20 points)

Answer: 0x5C6 = 0101 1100 0110

Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded date bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverate	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

Position 1 checks bits 1, 3, 5, 7 ,9, 11

Position 2 checks bits 2, 3, 6, 7 ,10, 11

Position 4 checks bits 4, 5, 6, 7 ,12

Position 8 checks bits 8, 9, 10, 11, 12

$$p_1 = XOR(0,0,1,0,0,1) = 0$$
$$p_2 = XOR(1,0,1,0,1,1) = 0$$

$$p_4 = XOR(1,1,1,0,0) = 1$$
$$p_8 = XOR(0,0,1,1,0) = 0$$

…(10 points)

C=0100, there is a single error in bit 4. …(5 points)

Corrected value = 0100 1100 0110 = 0x4C6 …(5 points)

二进制表示、十六进制表示均可