

## CS202H Computer Organization HW#4

### Problem 1.

For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

(1) What is the cache block size (in words)?

(2) How many entries does the cache have?

Starting from power on, the following byte-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

(3) Fill in blanks (show index and tag in decimal, and indicate replace using Y/N)

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180
Index												
Tag												
Hit/Miss												
Replace												

(4) What is the hit ratio?

(5) List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

### Problem 2.

For a 2-way set associative cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-11	10-4	3-0

the following byte-addressed cache references are recorded.

Address											
17	32	2	2059	4124	65	2067	2200	30	0	4102	360

Assume that the cache is initially empty. Using LRU replacement policy, answer questions below.

(1) Fill in the blanks (show index and tag in decimal, and indicate replace using Y/N):

Address	17	32	2	2059	4124	65	2067	2200	30	0	4102	360
Index												
Tag0												
Tag1												
Hit/Miss												
Replace												

(2) Calculate the cache size.

(3) List the final state of the cache (in decimal):

Index	Tag	Data	Tag	Data
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### Problem 3.

The following list provides parameters of a virtual memory system.

Virtual Address (bits)	Physical DRAM Installed	Page Size	PTE Size (byte)
43	16 GiB	4 KiB	4

- (1) For a single-level page table, how many page table entries (PTEs) are needed?
- (2) How much physical memory is needed for storing the page table?

### Problem 4.

This Exercise examines the single error correcting, double error detecting (SEC/DED) Hamming code.

- (1) What is the minimum number of parity bits required to protect a 128-bit word using the SEC/DED code?
- (2) Consider a SEC code that protects 8 bit words with 4 parity bits. If we read the value 0x5C6, is there an error? If so, correct the error.