**ECE4612–Fall 2023**

**Homework #1 –Chapter 1**

**Due: 09/12/2024 by 5pm**

**1.4** Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.

***1.4.1*** *What is the minimum size in bytes of the frame buffer to store a frame*

Number of Pixels = P = 1280 \* 1024

Number of Bytes Per Pixel = B = 8 \* 3 / 8

Minimum Bytes = P \* B = 1280 \* 1024 \* 3 = **3932160**

***1.4.2*** *How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?*

Number of Mbit = N = 3932160 \* 8 / 1000000

Seconds = N / 100 = .**3145728 seconds**

**1.5** Consider three different processors P1, P2, and P3 executing the same instruction set.

P1 has a 3 GHz clock rate and a CPI of 1.5

P2 has a 2.5 GHz clock rate and a CPI of 1.0

P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

***1.5.1*** *Which processor has the highest performance expressed in instructions per second?*

***P2 is the fastest***

***1.5.2*** *If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.*

***1.5.3.*** *We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?*

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**1.6** Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D).

* P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and
* P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows:

* 10% class A,
* 20% class B,
* 50% class C, and
* 20% class D
  + 1. *Which implementation is faster?*

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* + 1. *What is the global CPI for each implementation?*

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* + 1. *Find the clock cycles required in both cases.*

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**1.8** The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

* + 1. *For each processor find the average capacitive loads.*

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* + 1. *Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.*

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* 1. Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E9 arithmetic instructions, 1.28E9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency.

Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 x p (where p is the number of processors) but the number of branch instructions per processor remains the same.

***1.9.1*** *Find the total execution time for this program on 1, 2, 4, and 8 processors, and show the relative speedup of the 2, 4, and 8 processor result relative to the single processor result.*

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**1.9.2** *If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors?*

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***1.9.3*** *To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values?*

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**1.12** Section 1.10 cites as a pitfall the utilization of a subset of the performance equation as a performance metric. To illustrate this, consider the following two processors. P1 has a clock rate of 4 GHz, average CPI of 0.9, and requires the execution of 5.0E9 instructions. P2 has a clock rate of 3 GHz, an average CPI of 0.75, and requires the execution of 1.0E9 instructions.

***1.12.1*** *One usual fallacy is to consider the computer with the largest clock rate as having the largest performance. Check if this is true for P1 and P2.*

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***1.12.2*** *Another fallacy is to consider that the processor executing the largest number of instructions will need a larger CPU time. Considering that processor P1 is executing a sequence of 1.0E9 instructions and that the CPI of processors P1 and P2 do not change, determine the number of instructions that P2 can execute in the same time that P1 needs to execute 1.0E9 instructions.*

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***1.12.3*** *A common fallacy is to use MIPS (millions of instructions per second) to compare the performance of two different processors and consider that the processor with the largest MIPS has the largest performance. Check if this is true for P1 and P2.*

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**1.13** Another pitfall cited in Section 1.10 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. Consider a computer runing a program that requires 250s, with 70s spent executing FP instructions, 85s executed L/S instructions, and 40s spent executing branch instructions.

***1.13.1*** *By how much is the total time reduced if the time for FP operations is reduced by 20%?*

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***1.13.2*** *By how much is the time for INT operations reduced if the total time is reduced by 20%?*

*INT = 55*

*55 \* (.2) = 11*

*Int speeds up by 11 seconds.*

***1.13.3*** *Can the total time be reduced by 20% by reducing only the time for branch instructions?*

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