Name	Interface	Slave Segment	Master Base Address	Range	Master High Address
Network 0					
/axi_vdma_0					
/axi_vdma_0/Data_MM2S (32 address bits : 4G)					
/zynq/S_AXI_HP0	S_AXI_HP0	HP0_DDR_LOWOCM	0x0000_0000	512M	0x1FFF_FFFF
/axi_vdma_0/Data_S2MM (32 address bits : 4G)					
/zynq/S_AXI_HP0	S_AXI_HP0	HP0_DDR_LOWOCM	0x0000_0000	512M	0x1FFF_FFFF
Network 1					
/zynq					
/zynq/Data (32 address bits : 0x40000000 [1G])					
/axi_gpio_0/S_AXI	S_AXI	Reg	0x4120_0000	64K	0x4120_FFFF
/axi_vdma_0/S_AXI_LITE	S_AXI_LITE	Reg	0x4300_0000	64K	0x4300_FFFF
/AXIS2VGA_0/param_AXI	param_AXI	param_AXI_reg	0x43C0_0000	64K	0x43C0_FFFF
/OV7670_decoder_0/S00_AXI	S00_AXI	S00_AXI_reg	0x43C1_0000	64K	0x43C1_FFFF