|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 当前状态 | 指令\控制信号 | **PCWre** | ALUSrcA | ALUSrcB | DBDataSrc | **RegWre** | WrRegDSrc | InsMemRW | RD | **WR** | **IRWre** | ExtSel | PCSrc | RegDst | ALUOp |
| sIF | X | 0 | X | X | X | 0 | X | 1 | X | 1 | 1 | X | X | X | X |
| sID | J | 1 | X | X | X | 0 | X | X | X | 1 | 0 | X | 11 | X | X |
| Jal | 1 | X | X | X | 1 | 0 | X | X | 1 | 0 | X | 11 | 00 | X |
| Jr | 1 | X | X | X | 0 | X | X | X | 1 | 0 | X | 10 | X | X |
| halt | 0 | X | X | X | 0 | X | X | X | 1 | 0 | X | X | X | X |
| EAL | Add | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 000 |
| sub | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 001 |
| Addi | 0 | 0 | 1 | 0 | 0 | X | X | X | 1 | 0 | 1 | X | X | 000 |
| Or | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 101 |
| And | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 110 |
| Ori | 0 | 0 | 1 | 0 | 0 | X | X | X | 1 | 0 | 0 | X | X | 101 |
| Sll | 0 | 1 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 100 |
| Slt | 0 | 0 | 0 | 0 | 0 | X | X | X | 1 | 0 | X | X | X | 011 |
| Slti | 0 | 0 | 1 | 0 | 0 | X | X | X | 1 | 0 | 1 | X | X | 011 |
| ELS | Sw | 0 | 0 | 1 | X | 0 | X | X | X | 1 | 0 | 1 | X | X | 000 |
| Lw | 0 | 0 | 1 | X | 0 | X | X | X | 1 | 0 | 1 | X | X | 000 |
| EBR | Beq（zero=1） | 1 | 0 | 0 | X | 0 | X | X | X | 1 | 0 | 1 | 01  00 | X | 001 |
| (zero=0) |
| Bne(zero=0) | 1 | 0 | 0 | X | 0 | X | X | X | 1 | 0 | 1 | 01  00 | X | 001 |
| (zero=1) |
| Bgtz(zero=0 && sign=0) | 1 | 0 | 0 | X | 0 | X | X | X | 1 | 0 | 1 | 01  00 | X | 001 |
| (zero=1 || sign=1) |
| MLD | Lw | 0 | X | X | 1 | 0 | X | X | 0 | 1 | 0 | X | X | X | X |
| MST | sw | 1 | X | X | X | 0 | X | X | X | 0 | 0 | X | 00 | X | X |
| WLD | Lw | 1 | X | X | X | 1 | 1 | X | X | 1 | 0 | X | 00 | 01 | X |
| WAL | Addi,ori,slti | 1 | X | X | X | 1 | 1 | X | X | 1 | 0 | X | 00 | 01  10 | X |
| Add,sub,or,and,slt,sll |