IERG1810 Electronic Circuit Design Lab

Report on Mini Project

An Electronics Dice

Group: B 16

Members:

BU Liu Shiuan (CUID:1155188577)

YU Mu Quan (CUID:1155191596)

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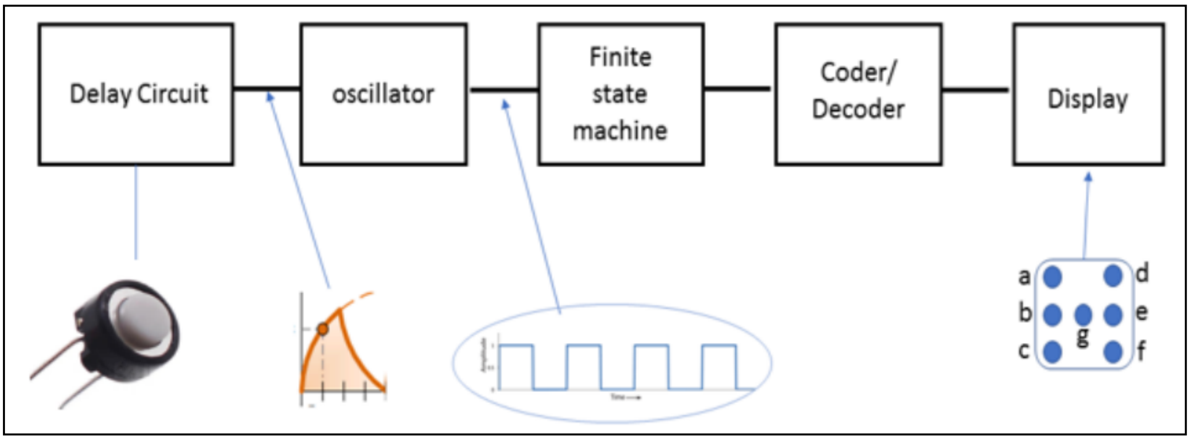
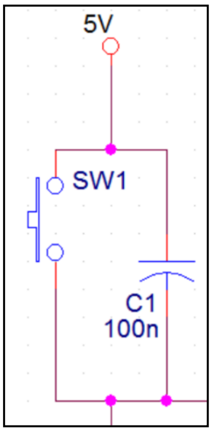
Disclaimer

I declare that the assignment here submitted is original except for source material explicitly acknowledged, and that the same or related material has not been previously submitted for another course. I also acknowledge that I am aware of University policy and regulations on honesty in academic work, and of the disciplinary guidelines and procedures applicable to breaches of such policy and regulations, as contained in the website http://www.cuhk.edu.hk/policy/academichonesty/

BU Liushiuan	BU Liushiuan	28 April 2023
Signature	Name	Date
YU Muquan	YU Muquan	28 April 2023
Signature	Name	Date

I. Introduction to each function block of the whole circuit

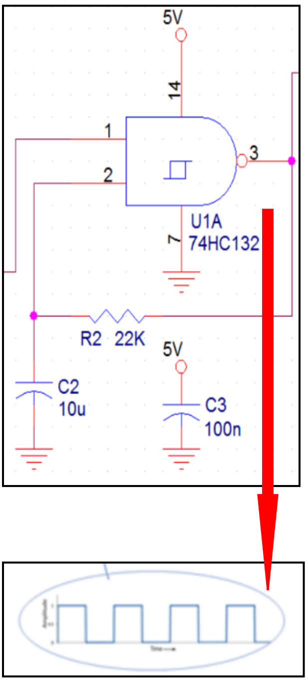




1. Delay circuit: keeps the oscillator oscillating for a short time.

Theory Used: When the button is pressed, the Vcc will only go through the branch of the button. When the button is off, the capacitor starts to discharge, and the display will still change order in a “delay time”.

In this following chapter, we will mention which component will affect the delay time, and what the relation between (i.e., equation) capacitance and the delay time is.

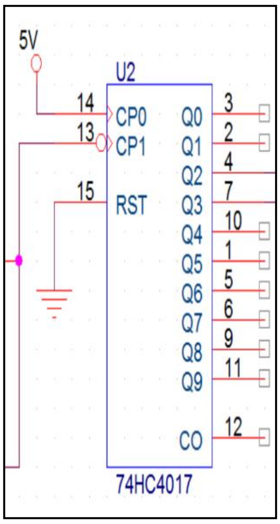


2. Oscillator: generates a clock signal for the dice rolling.

Theory Used: 74HC132 actually serves as “NAND gates”. When input-1 receives high-voltage, the inputs will become (1,0), and output-3 will result in high-voltage(1), passing the signal to the input-2. The following inputs will change into (1,1), and output-3 will result in low-voltage(0), passing the signal to the input-2.

It is like a routine that results in output-3 can generate a “clock signal”.

In this following chapter, we will mention which component will affect the oscillator frequency, and what the relation between (i.e., equation) components and the delay time is.

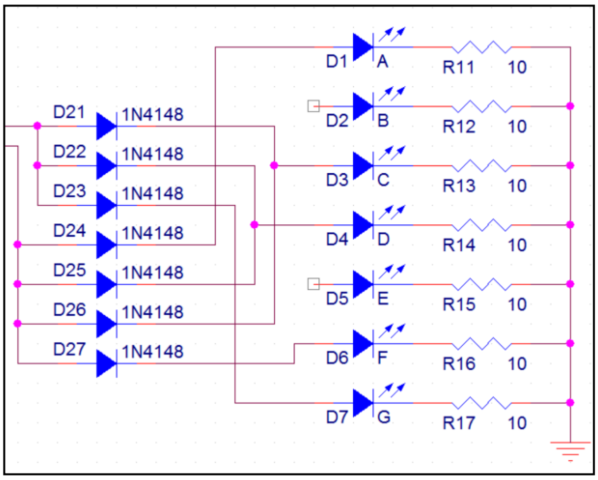


3. Finite State Machine: changes the state by the clock signal.

Functions Used: Receiving signal form 74HC132.

- **Receive signal (1) first time: output high voltage from Q0.**
- **Receive (0): no output.**
- **Again receive signal (1) first time: output high voltage from Q1.**
- **Receive (0): no output.**
- **Again receive signal (1) first time: output high voltage from Q2.**
- **…,**
- **we can also use RESET to determine how many times in a routine we need to use.**

In this following chapter, we will mention how we design the circuit.



4. Decoder: converts status to the display part.

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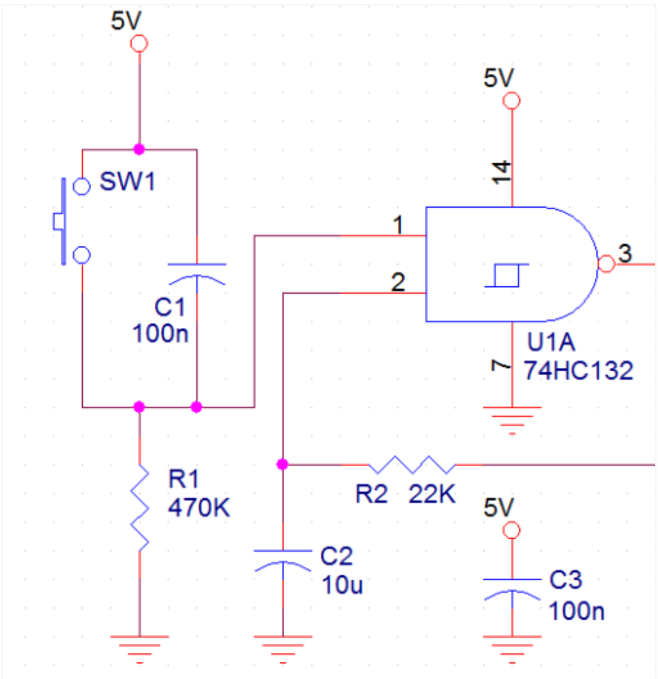
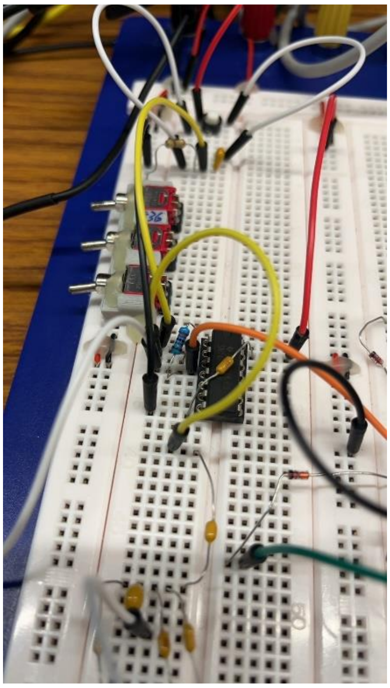
5. Display: a group of LEDs shows dice patterns.

In this following chapter, we will mention how we design the circuit.

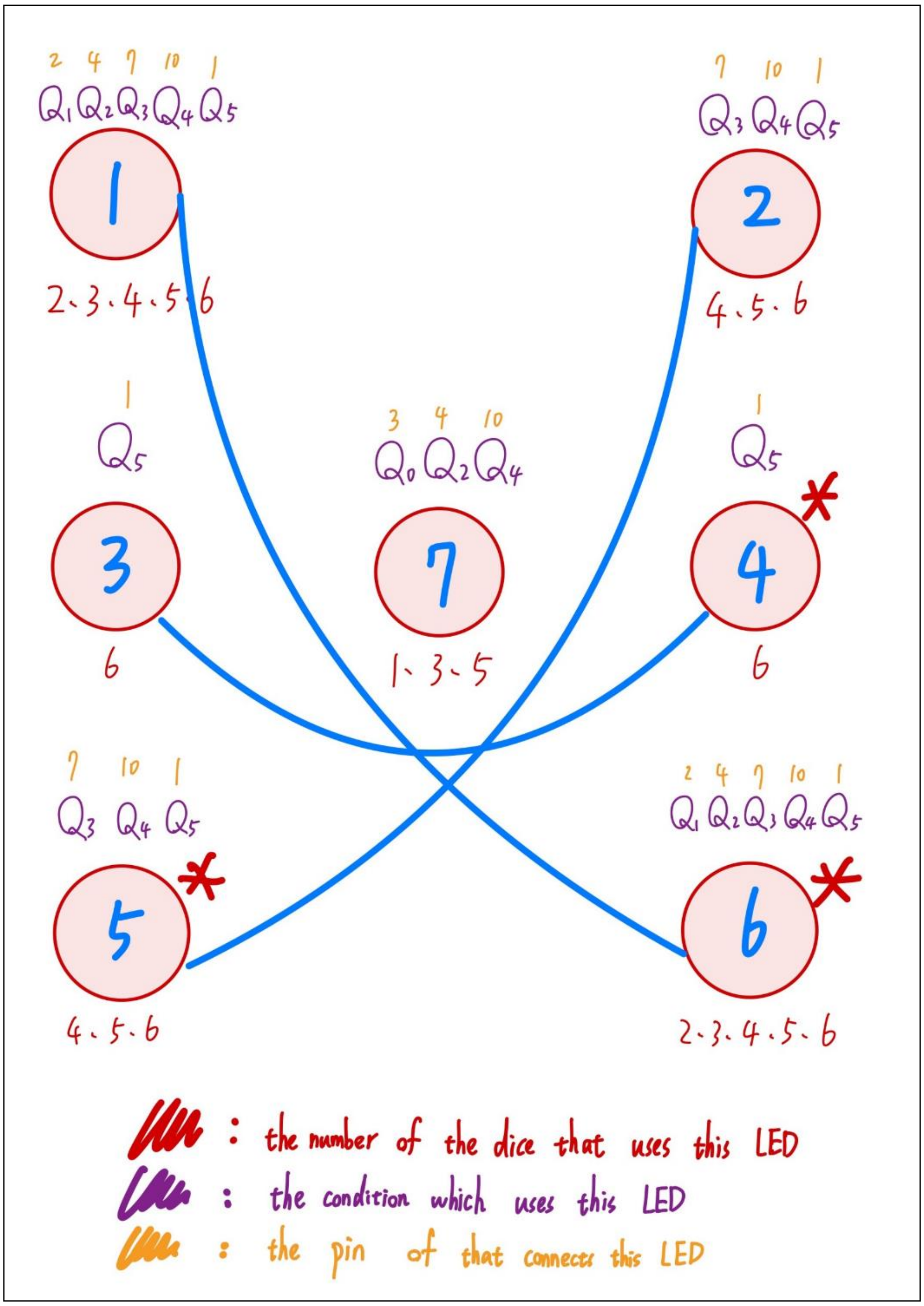
II. Designing and building process

1. Build up the delay circuit and the oscillator as the below.





2. We built up the display of LED lights first. We decided to start from the display, simplify the wires there and eventuallly connect those to the finite state machine.



This is the result of the 74HC4017 pin connection after simplifying.

During the siplification, We noticed that light 4, 5, 6 can be connect to Light 3, 2, 7, respectively. Thus, We only have to connect the wires between light 1, 2, 3, 7 to their corresponding 74HC4017 pins.

Noted: Each LED must be with a resistor.

3. Setting up 74HC4017

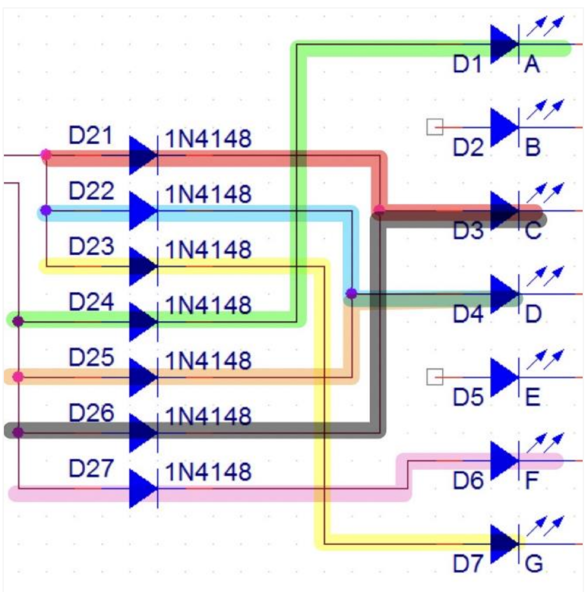
- Pin 16 & Pin 14: Connect to Vcc.
- Pin 15: Connect to Pin 5 (Condition Q6).

  We only need 6 conditions (Q0~Q5). **Letting Pin 5 connect to Pin 15 will "RESET" the counter, leading to start from Q0 after next clock signal high-peak.**

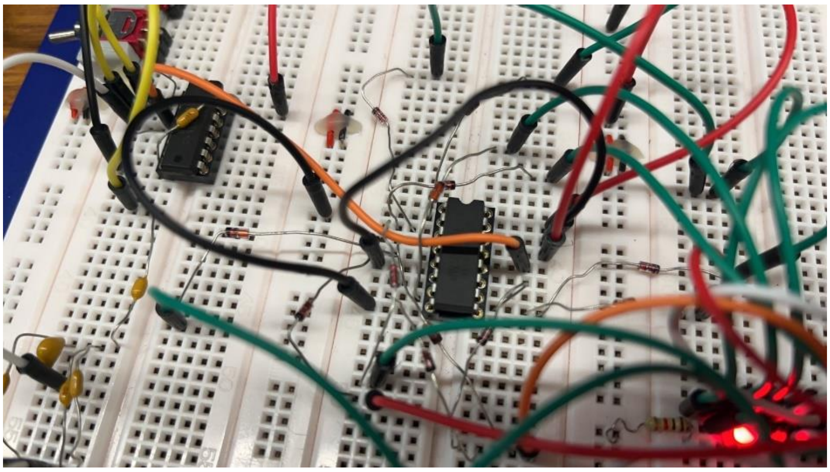
- Pin 13: Connect to the oscillator.

4. Testing and problem fixing

When we were building the circuit, we did notice that usege of diodes in the the circuit, **which prevent signals in one condition to affect other conditions. That is, without diodes, high-voltage may go through every wires and let other LED lights in other conditions turn on.** Still we didn't understand it completely. At first, we connected all the diodes to each LED light, which means that we only use 7 diodes in our circuits. After studying, we discovered that:

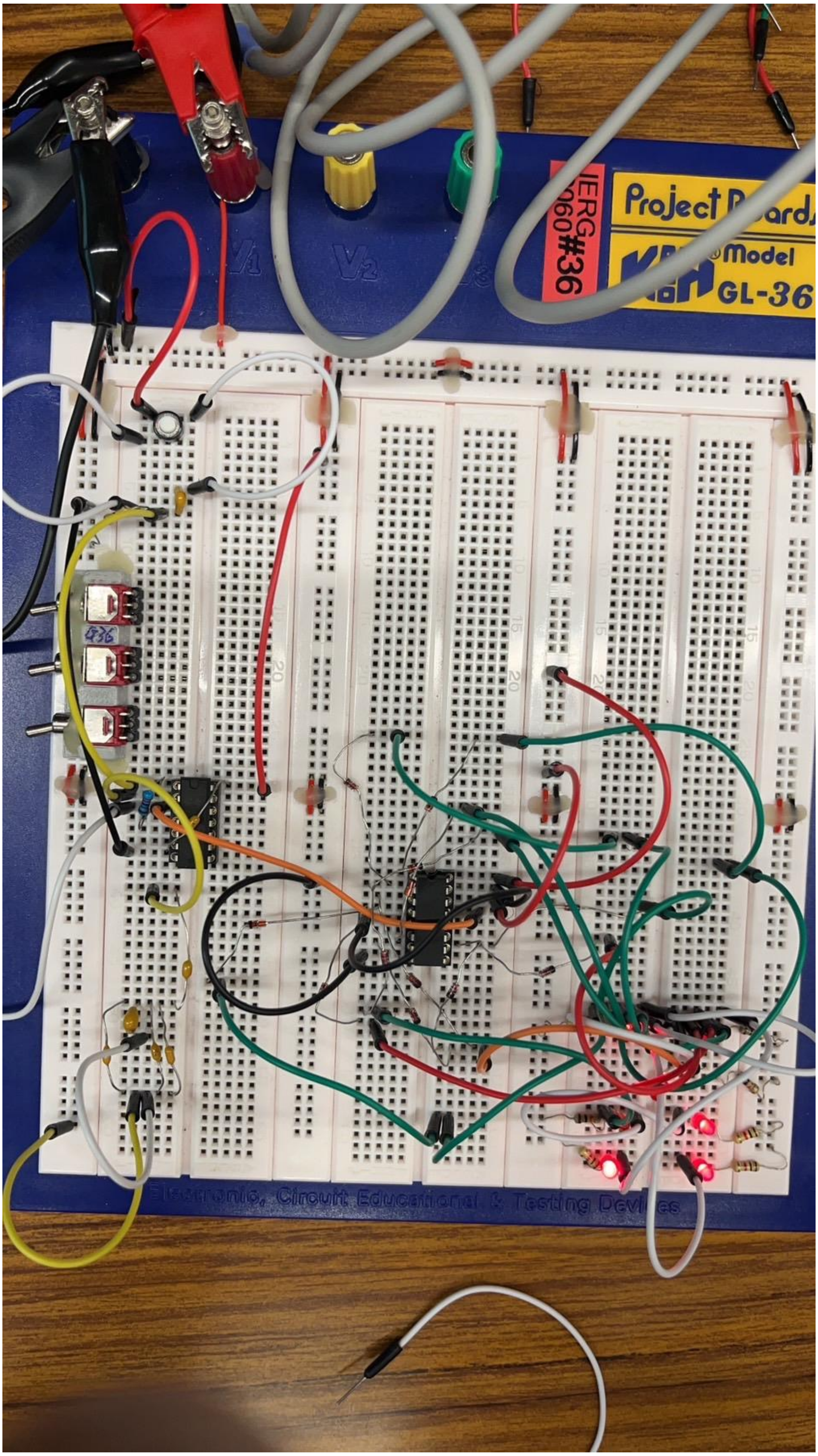


We define the line with highlight a “branch”. A branch must contains a diode. We analyzed how many branches we had and add diodes on them.



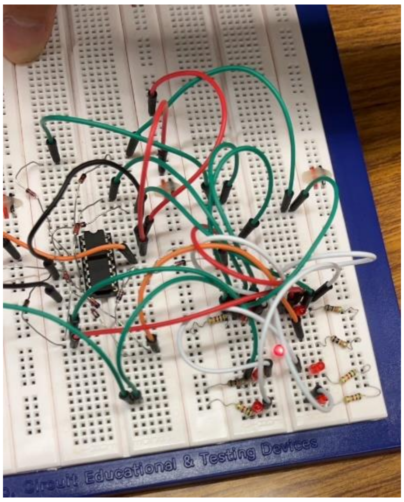
Eventually, it ran correctly.

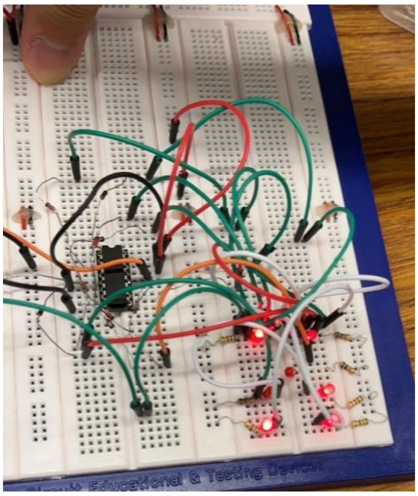
The whole circuit:



1:

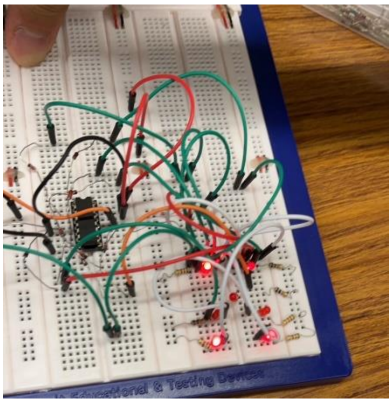
6:

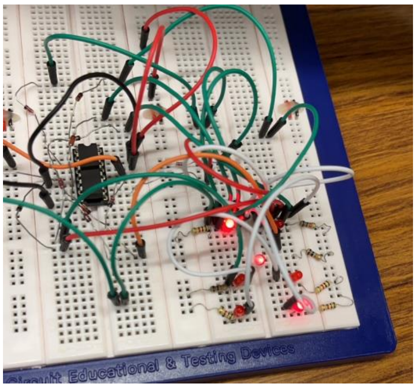




4:

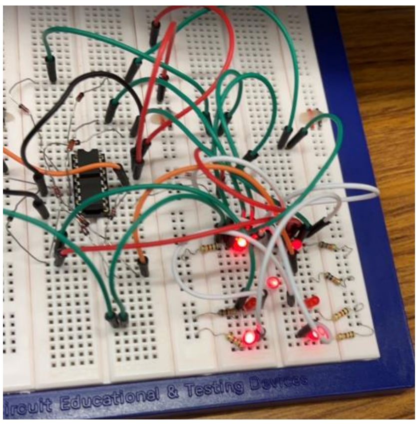
3:

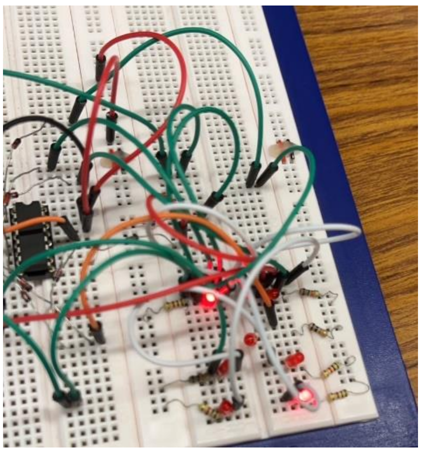




5.

2.





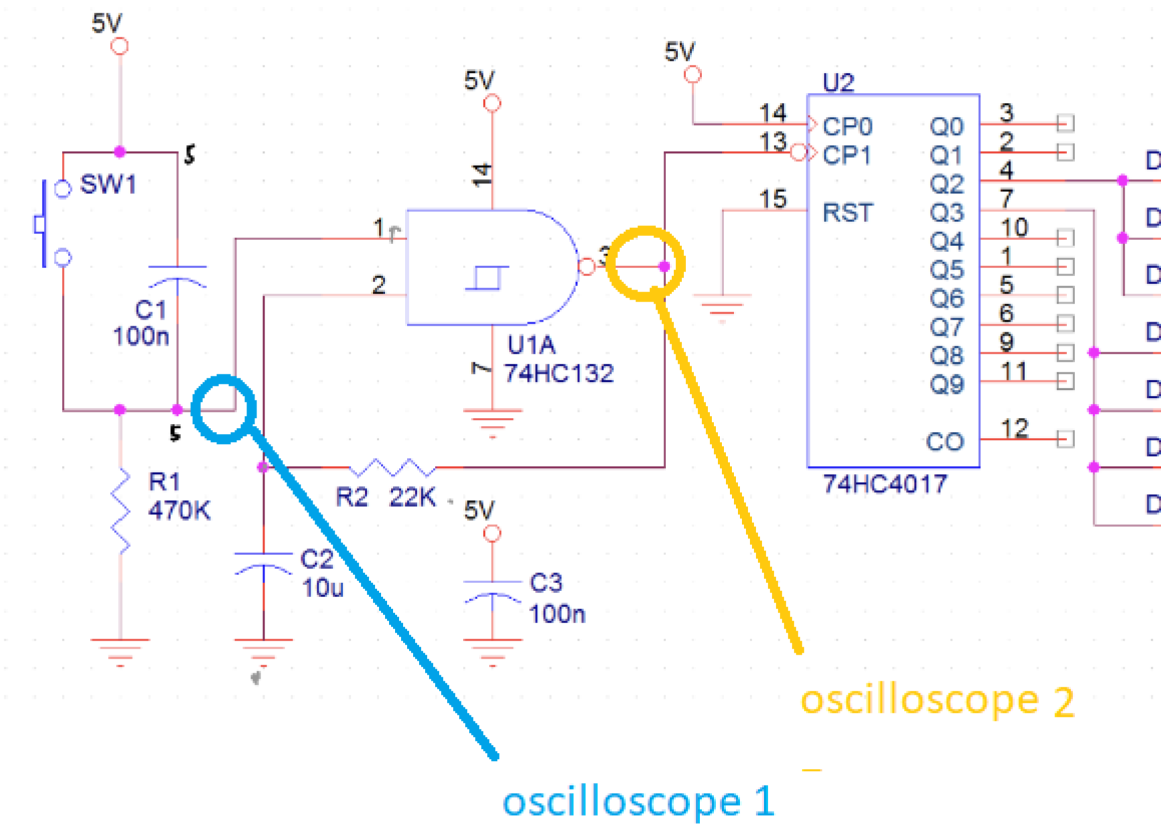
(Our order: 164352)

III. Measuring the circuit

1. Measuring the delay (calculating is in section IV)

In order to make the dice act more randomly, we have to ways to modify the circuit. The first way is to make the delay time between the moment we let our hands of the button and the dice ends rolling. First we need to measure the delay time.

1.1 Basic theorum



We set 2 oscilloscope pins 1, 2 (blue and yelow) at the 2 positions above. When we let off the button, there will be a voltage drop at the position 1. After the delay, the voltage of position 3 will stop oscillatiing and remain stable. When the frequency of position 3 is high, we can just measure the time difference between the drop moment of the oscilloscope 1 and the moment when position 2 stops to oscillate.

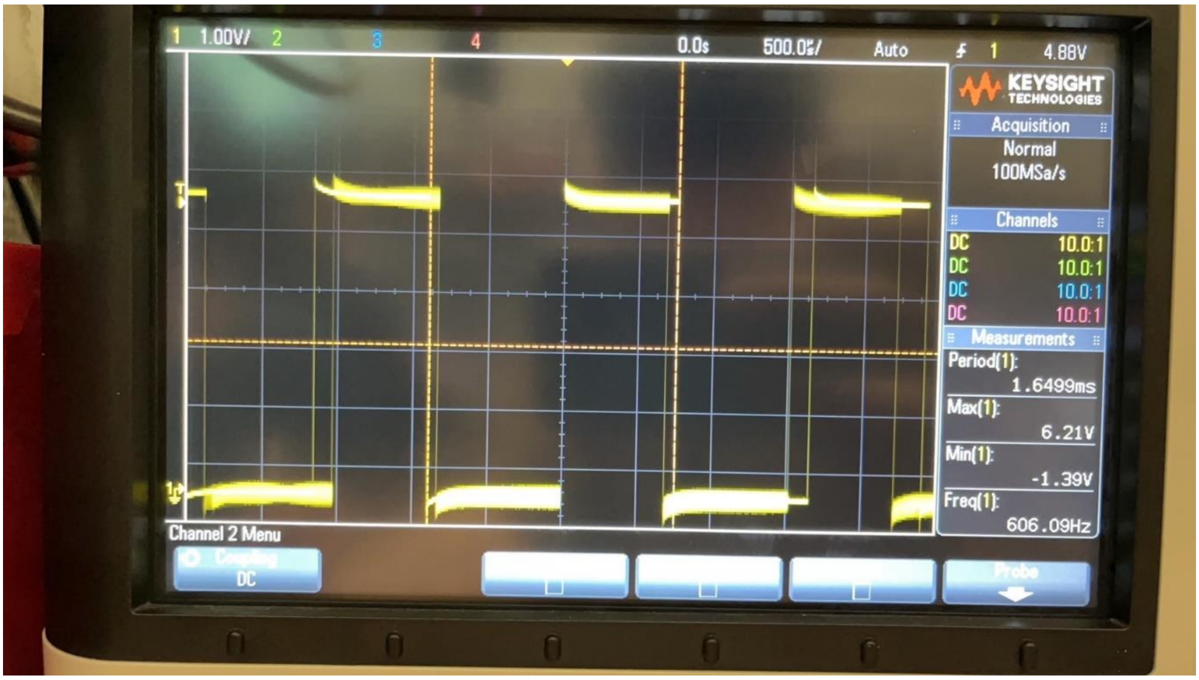
1.2 Measurement

Use the trigger function of the oscilloscope and single run to capture the snapshot of the falling edge of the position 1 (blue voltage) and the graph is shown above. Use the cursor function to find the time difference between the 2 moments and we get the time difference of the 2 points which is the delay. In our case, the delay time is 52 ms.

2. Measure the oscilator frequency (calculating is in section IV)

The other way to make the circuit act randomly is to make the frequency high so that raw eye cannot detect the change in digits their sequence.

To measure the frequency, we use an osciloscope to measure the voltage frequency of psition 2 and it is the oscillator frequency.

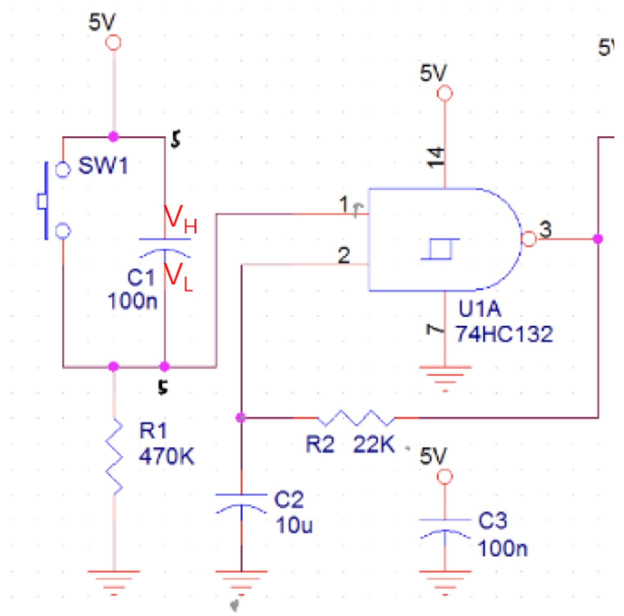


In our case, the frequency of the oscillator is 606.09 Hz.

IV. Optimizing the circuit

1. Modifying the delay

We look at the delay circuit.



When we press the button, $V_H = V_L = 5V$, the capacitor is not charged, and the NAND gate oscillator starts to oscillate. The moment we release the switch, V_L gradually decreases to 0, in the process, the current flow from capacitor to ground, while charging the capacitor. When V_L is lower than the low level threshold voltage, the NAND gate stops to oscillate and the delay stops.

So to modify the circuit, to modify the delay, we can either make changes on C_1 or R_1.

1.1 Change C_1

To make the delay longer, we want the voltage drop slower, which means that with the same amount of charge flowing into the capacitor, the voltage drop should be less. With the formula

$$\Delta V = \frac{\Delta Q}{C}$$

We know that we should make the capacitance larger.

In contrary, to make the delay shorter, we should make the capacitance smaller.

1.2 Change R_1

To make the delay longer, we should make the current small so that the voltage drop won't be to quick. With Ohm's law

$$I = \frac{V}{R}$$

We know that the resistance should be bigger.

In contrary, to make the delay time shorter, we need to make the resistance smaller.

1.3 Alternative: analysing the delay with detailed calculation

According to the capacitor discharging formula:

$$V(t) = Vm\, e^{-\frac{t}{R1C1}}$$

So in the discharging process we have:

$$V = Vm\, e^{-\frac{t}{R1C1}}$$

Where V is the threshold voltage where the oscillator stops to oscillate.

From our measurement, V = 1.488 V (the orange figure at right down)

Vm = Vcc = 5V

By calculation we get

$$t = 1.212 R_1 C_1$$

So to increase the delay, increase R1 or C1,

To decrease the delay, decrease R1 or C1.

Which is the same result we get from above.

2. Modifying the frequency

In the experiment, we should modify the frequency to the last three digits of our student SID. In our case, the frequency is 596 Hz.

2.1 Basic Theory

In one period of oscillation, when we look at the pin 1 of the NAND gate, we can separate the period to 2 process:

(1) V_1 increases from low level threshold voltage V_N to high level threshold voltage V_P
(2) V_1 decreases form high level threshold voltage V_P to low level threshold voltage V_N

Checking the manual of M74HC, we know that the delay time of the status changing is in nanoseconds, so we ignore the calculation of delay time.

With the formula of capacitor

$$V(t) = Vs + (Vo - Vs)\, e^{-\frac{t}{\tau}}$$

(1) Decrease process lasts for t_1:

$$V_N = V_{OL} + (V_P - V_{OL})e^{-\frac{t_1}{RC}}$$

(2) Increase process lasts for t_2:

$$V_P = V_{OH} + (V_N - V_{OH})e^{-\frac{t_2}{RC}}$$

(3) Frequency:

$$f = \frac{1}{t_1 + t_2}$$

Where V_{OL} is the low level output threshold voltage

V_{OH} is the high level output threshold voltage

R is the resistance of R2

C is the capacitance of C2

By calculation we get

$$f = \frac{1}{0.6931RC}$$

So if we want to increase f, we need to decrease R2 or C2

In contrary, if we want to decrease f, we need to increase R2 or C2

Table 6. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_P	High level threshold voltage	2.0		1.0	1.25	1.5	1.0	1.5	1.0	1.5	V
		4.5		2.3	2.7	3.15	2.3	3.15	2.3	3.15	
		6.0		3.0	3.5	4.2	3.0	4.2	3.0	4.2	
V_N	Low level threshold voltage	2.0		0.3	0.65	0.9	0.3	0.9	0.3	0.9	V
		4.5		1.13	1.6	2.0	1.13	2.0	1.13	2.0	
		6.0		1.5	2.3	2.6	1.5	2.6	1.5	2.6	
V_H	Hysteresis voltage	2.0		0.3	0.6	1.0	0.3	1.0	0.3	1.0	V
		4.5		0.6	1.1	1.4	0.6	1.4	0.6	1.4	
		6.0		0.8	1.2	1.4	0.8	1.7	0.8	1.7	
V_{OH}	High level output voltage	2.0	I_O = -20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O = -20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O = -20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O = -4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O = -5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low level output voltage	2.0	I_O = -20 µA			0.1		0.1		0.1	V
		4.5	I_O = -20 µA			0.1		0.1		0.1	
		6.0	I_O = -20 µA			0.1		0.1		0.1	
		4.5	I_O = -4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O = -5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input leakage current	6.0	$V_I = V_{CC}$ or GND			±0.1		±1		±1	µA
I_{CC}	Quiescent supply current	6.0	$V_I = V_{CC}$ or GND			1		10		20	µA

Checking the manual we have in experiment condition, we let

V_N = 1.8V V_P = 3V

V_{OL} = 0V V_{OH} = 5V

f = 596Hz

We get

$$RC = 2.421 \times 10^{-3}$$

We want to keep the original R2 and modify C2, so

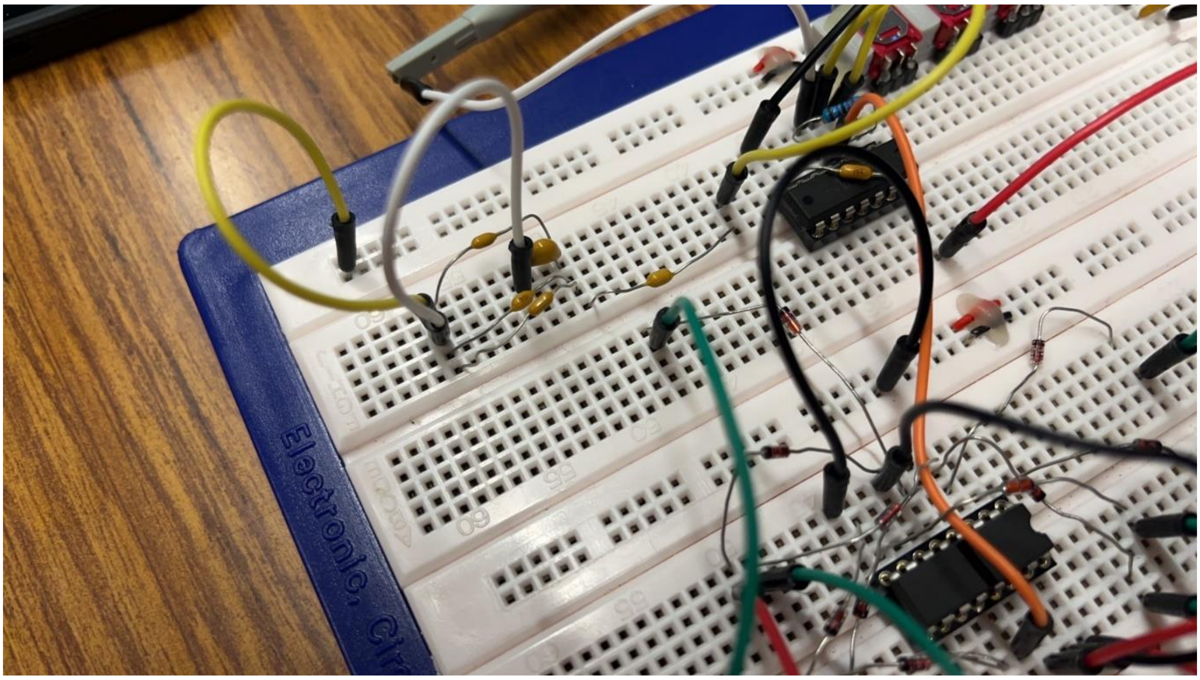
R2 = 22 KΩ

C2 = 110 nF

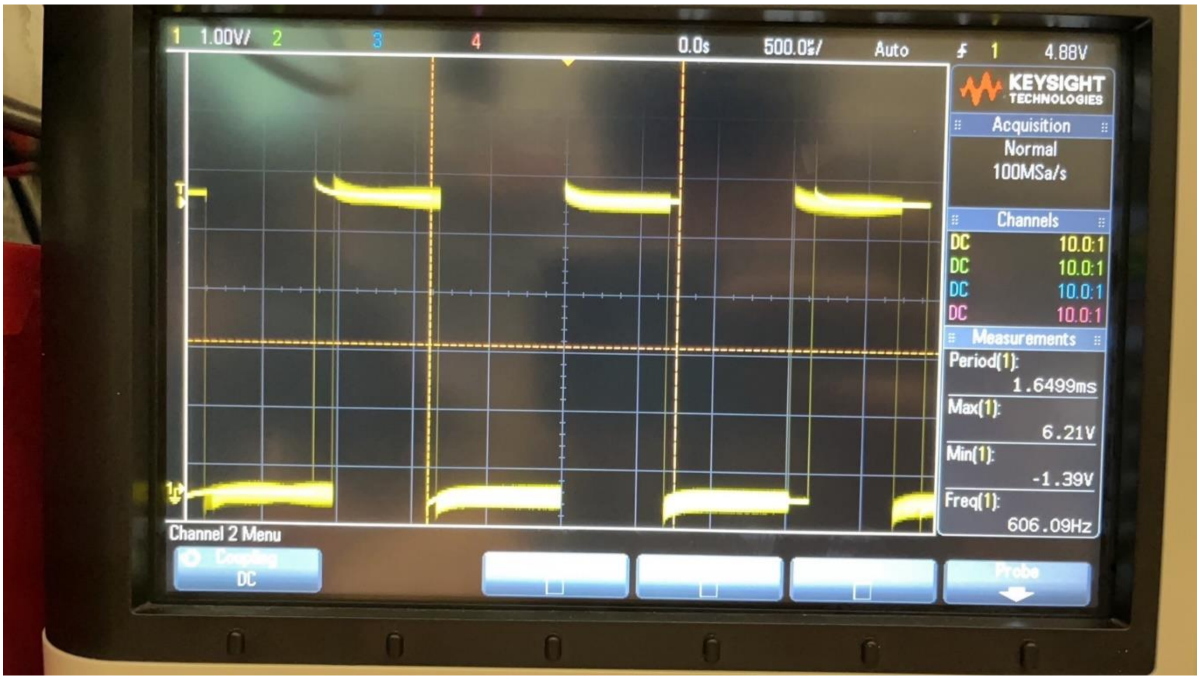
2.2 Circuit modification

We change C2 to 100nF, but the frequency is around 460 Hz, which means that C2 is to big.

So we add 4 100 nF capacitor in parallel then in series with the original capacitor,



Which makes C2 400nF // 100nF = 80nF,
And the frequency becomes 606.09Hz, which is in range.



2.3 Modifying the state, pattern, display sequence

Each state and display sequence is controlled by the finite state machine, and when the CP0 pin gets a pulse the state will change from Q_n to Q_{n+1} (or to Q_0 if a period finishes).

Each pattern is controlled by the circuit we designed to connect the LEDs.

They are discussed in detail in section I, II.

V. Summary

In summary, during the mini project, we built a electronics dice using the components and theory we learnt in IERG 1810 and IERG 2060.

We used a delay circuit to generate a delay when we release the button, and we uses a feed back NAND gate to generate an oscillation to trigger the finite state machine. Then we used a finite state machine to generate six different status in the dice. Finally we designed our own LED connection to make six different LED patterns to represent number 1~6.

In this project we learnt how to build and design complex circuits, how to use measure equipment like DMM and oscillators to measure the data, and how to apply theoretical analysis to real circuit to modify some parameters to make the work more humanized.

VI. DIVISION OF WORK

For experiments with delay circuit and oscillator, BU worked on the experiment and YU put down the data and took photos, and for experiments with finite state machine and LED display, the roles are exchanged.

For the lab report, BU did I II YU did III and IV.

VII. REFERENCES

1. M74HC132 datasheet.