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Version History

Historical Version	Modified content	Version Date
REV 1.0	Initial Version	2018-05-05
REV 1.1	1. Add user configuration area, P15~P18 2. Add the description of encryption area, P18~P19	2018-09-03
REV 1.2	1. Remove the external crystal	2018-10-24
REV 1.3	1. Add section 9 Product naming rules 2. Chapter 5 description update 3, QC3.0 characteristic RDM pull-down resistor resistance update	2019-02-13
REV 1.4	1. Modify DAC DNL, INL characteristics, P36 2. Revision of clerical errors, P5, P15 3. QFN24 package thickness modification, P40 4. Add burn mode encryption address and description in encryption area, P20	2019-04-02
REV 1.5	1. QFN24 package thickness modification, P40 2, QFN32 package parameter description modification, P41 3. Increase comparator response time, P37 4. Update the typical application diagram, P30	2019-08-08

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1 Product Overview

1.1 Function Description

The CS32G020 series is a USB Type-C controller that supports USB Type-C and PD3.0 protocols and can be used in PC power adapters, cell phone chargers, mobile power supplies, car chargers, HUBs, etc. The CS32G020 has a n embedded ARM® Cortex™-M0 core with a maximum main frequency of 48MHz and can support a wide range of industrial control applications and applications requiring high performance CPU. The CS32G020 is available in 64K bytes program flash, 4K bytes LDROM, and 8K bytes SRAM.

1.2 Main Features

Type-C and USB PD support

- Support USB PD3.0 protocol, support PPS
- CC port configurable RP and RD
- Supports 2 Type-C ports for independent PD communication
- CC port supports 21V withstand voltage
- Built-in 2 high voltage (21V) control ports
- Support for Fast Role Exchange (FRS)

other protocols

- Supports QC4.0+, SCP, FCP, AFC protocols
- Support BC1.2, Apple 2.4A
- Supports all configurations on DP, DM
- Supports a variety of fast charging protocol input

peripherals such as FCP, AFC, etc.

- Up to 27 general purpose (GPIO) pins
- 3 16-bit timers, 8-bit prescale
- 1 group UART
- 1 group SPI
- 1 group I2C (master-slave mode supported)
- 2 analog comparators
- 12-bit analog-to-digital converter (ADC)
- 11-bit digital-to-analog converter (DAC)
- Brown-out detection (BOD)

32-bit MCU

- Core ARM®Cortex™-M0 core at up to 48MHz
- 60K Flash memory for application programs (APROM)
- Configurable data flash (Data Flash)
- 4KB boot code space (LDROM)
- Embedded 8KB SRAM
- System boot interval is configurable and can be booted from APROM, LDROM or SRAM

Clocks and Crystals

- 24/8MHz internal oscillator (HSI) (25°C, 5V, 1% error)
- 10 KHz internal low-power oscillator (LSI)

operating mode (low-power mode, multi-clock low-power strategy)

- Normal mode , operating current 10mA@5V.

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Gathering the core of a

25℃
- Sleep mode, operating current 2mA@5V, 25℃
- Deep-Sleep1 mode , operating current 100uA@5V, 25℃
- Deep-Sleep2 mode, operating current 12uA@5V, 25℃
- Deep Power-Down mode, operating current 2.5uA@5V, 25℃

Chip Security

- Provides multi-level security policy for Flash memory
- Provides CRC-32 calculation unit with polynomial 0x4C11DB7 (same as Ethernet standard)
- Internal SRAM supports parity check

operating conditions

- Working temperature:-40℃~85℃
- Operating voltage:2.5V~5.5V

package

- QFN24
- QFN32

Applications

- Adapter
- Mobile Power
- car charger
- HUB

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1.3 Selection table

Model	Flash	SRAM	IO	CC port	PD Modules	Dead battery Function	QC PHY	Timer	ADC	DAC	Package
CS32G020K8U6	64K	8K	27	2 groups	2	Support	2 Roads	3*16bit	24 Tong Road	11bit	QFN32
CS32G020E8U6	64K	8K	19	2 groups	2	Not supported	2 Roads	3*16bit	20 pass Road	11bit	QFN24

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2 Block Diagram

2.1 Block diagram of functional modules

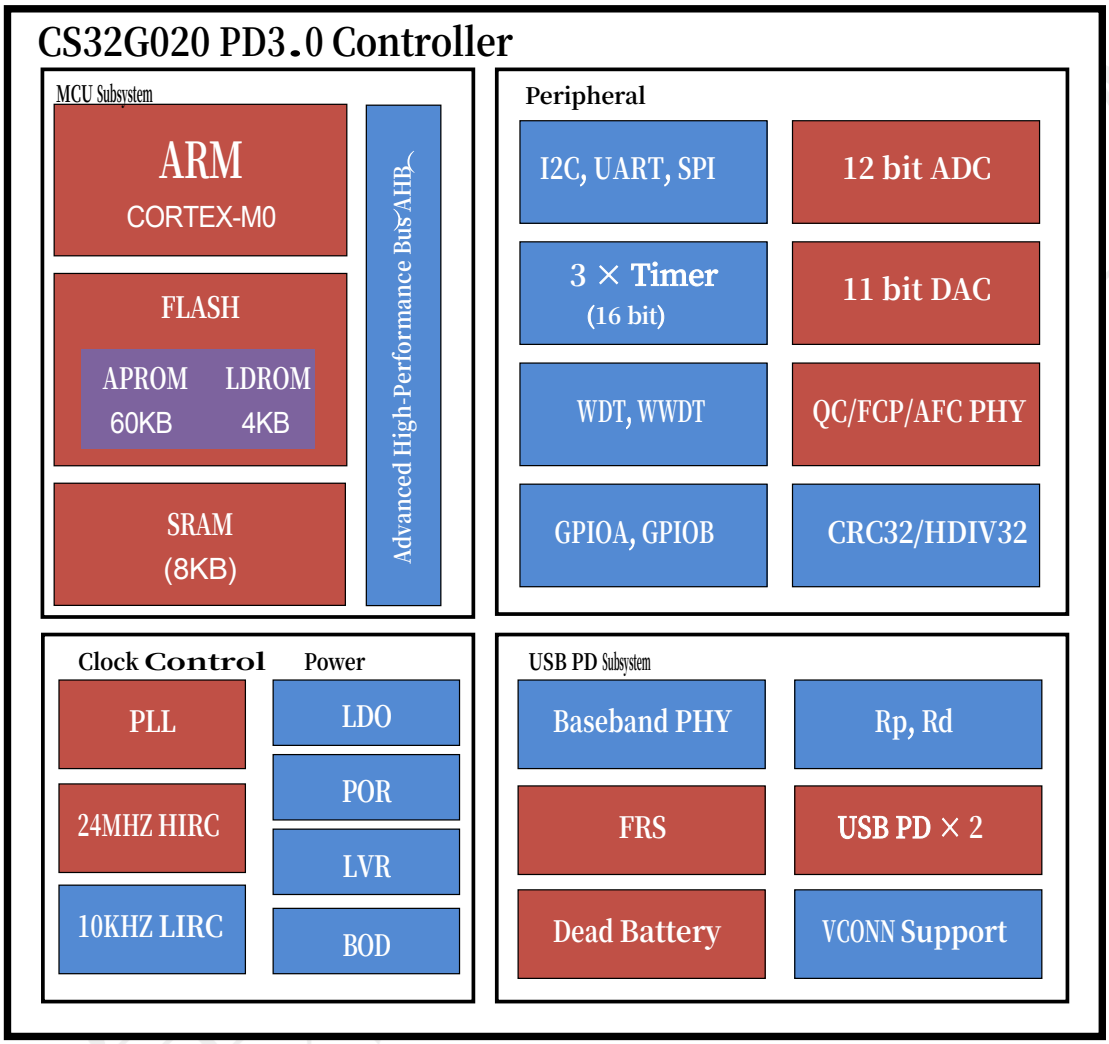

Figure 1 CS32G020 system block diagram

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2.2 Internal circuit block diagram

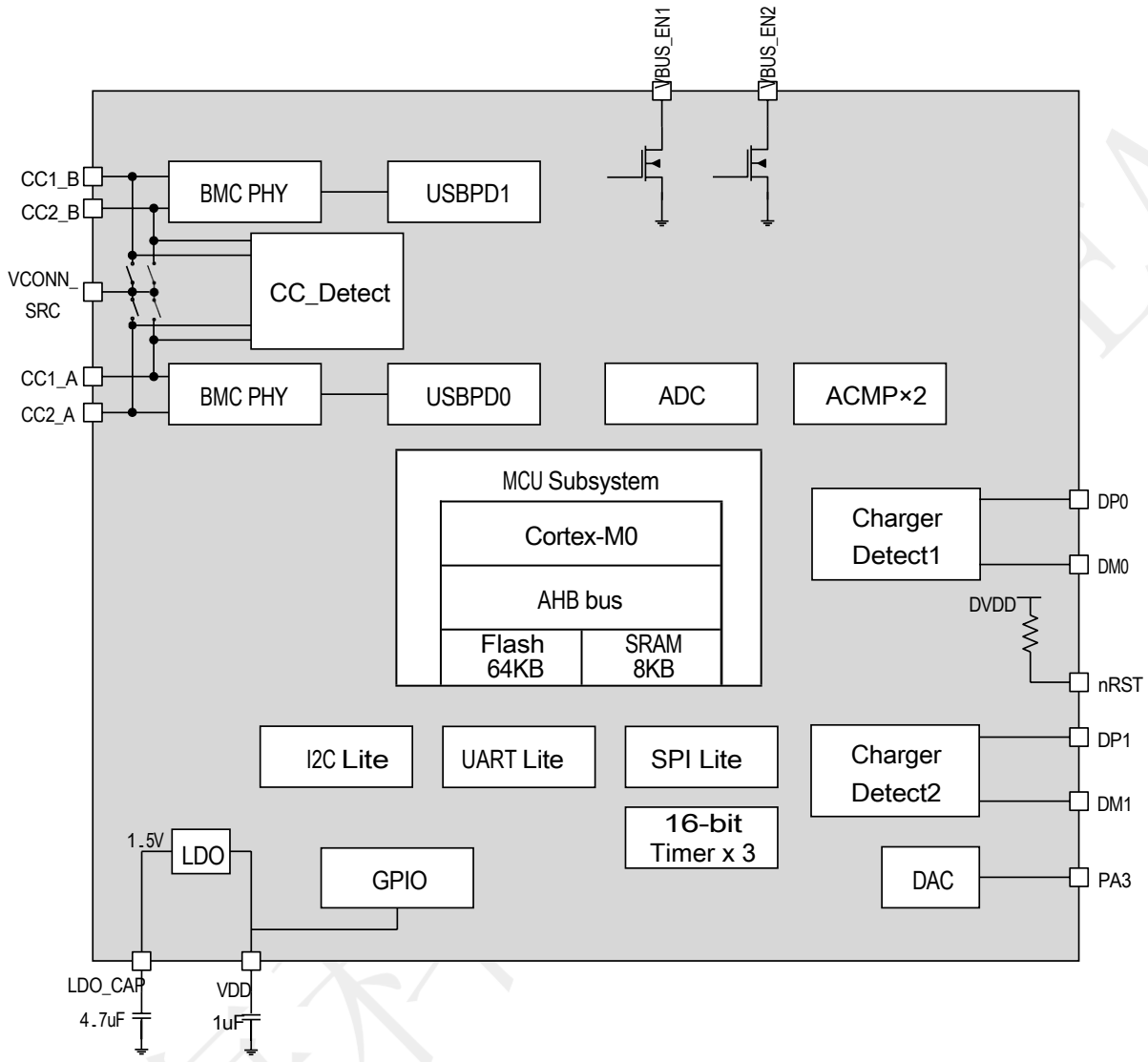

Figure 2 Internal circuit block diagram

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3 Pin diagram

3.1 QFN24

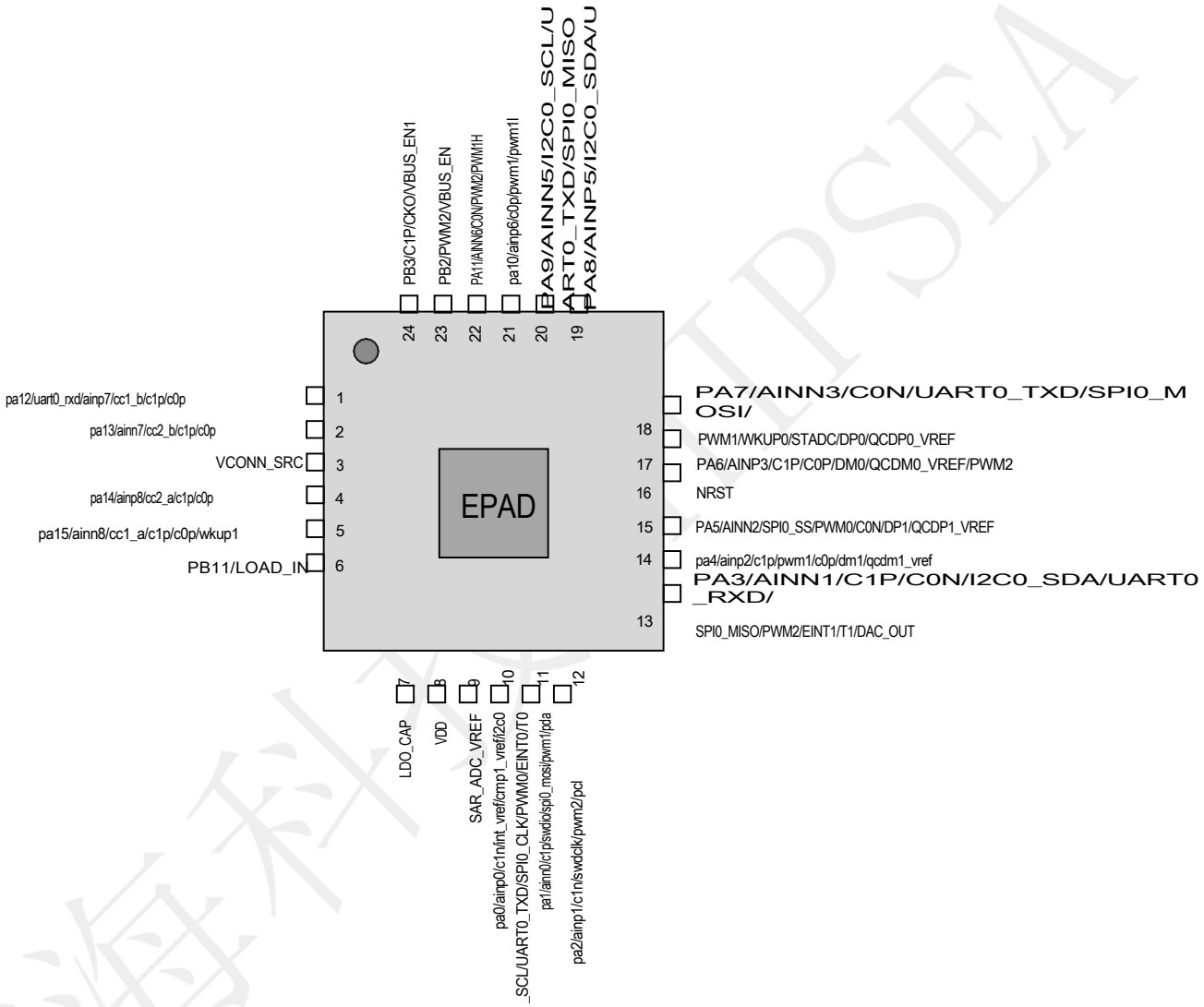

Figure 3 QFN24 Pinout Diagram (Top View)

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3.2 QFN32

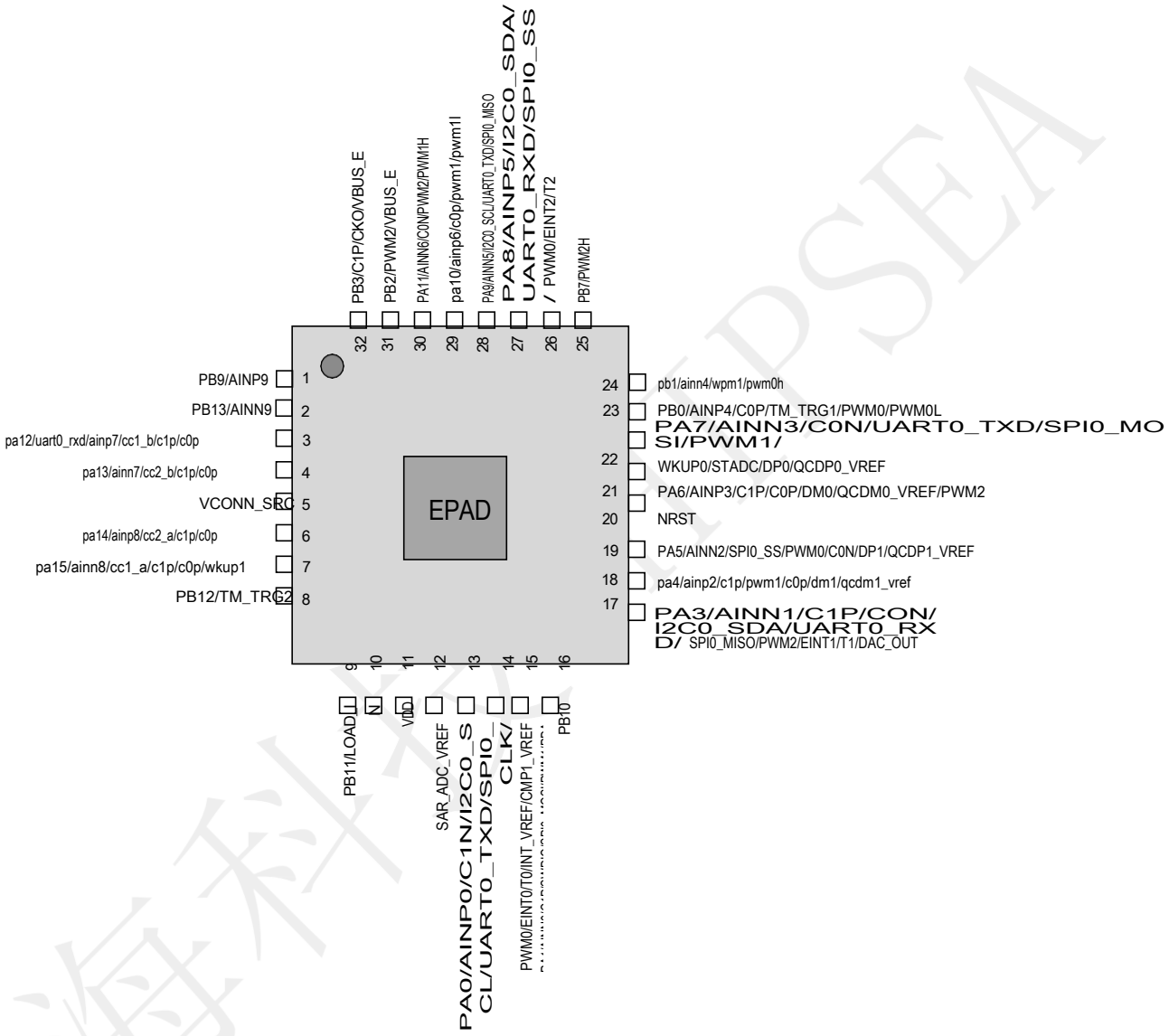

Figure 4 QFN32 Pinout Diagram (Top View)

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3.3 Pin Description

Pin Type
Abbreviation
Description I : Digital Input
Port O : Digital Output Port
I/O: Digital input and output port AI: Analog input port AO: Analog output port
P: Power supply

Table 3-1 Pin Description Table

QFN32 -PIN	QFN24 -PIN	Pin Name	Pin	Description
1		PB9	I/O	General purpose input/output pins
		AINP9	AI	AINP9 Input
2		PB13	I/O	General purpose input/output pins
		AINN9	AI	AINN9 Input
3	1	PA12	I/O	General purpose input/output pins
		UART0_RXD	I	UART0 Receive signal
		AINP7	AI	AINP7 Input
		CC1_B	I/O	USB PD1 CC1 end
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
4	2	PA13	I/O	General purpose input/output pins
		AINN7	AI	AINN7 Input
		CC2_B	I/O	USB PD1 CC2 end
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
5	3	VCONN_SRC	P	VCONN power input, 4.5V to 5.5V input required
6	4	PA14	I/O	General purpose input/output pins
		AINP8	AI	AINP8 Input
		CC2_A	I/O	USB PD0 CC2 end
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
7	5	PA15	I/O	General purpose input/output pins
		AINN8	AI	AINN8 Input
		CC1_A	I/O	USB PD0 CC1 end
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
		WKUP1	I	Power-down mode wake-up pin, active high
8		PB12	I/O	General purpose input/output pins
		TM_TRG2	I	Timer external trigger input 2
		PB11	I/O	General purpose input/output pins

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		LOAD_IN	I	Universal input/output pins and support for 800K pull-down resistors
10	7	LDO_CAP	AO	LDO output pin, 4.7uF capacitor required
11	8	VDD	P	IO power supply (1.8V~5.5V)
12	9	SAR_ADC_VREF	AO	SAR_ADC reference voltage output, requires external 1uF capacitor
13	10	**PA0**	**I/O**	**General purpose input/output pins**
		AINP0	AI	AINP0 Input
		C1N	AI	Comparator 1 negative input
		I2C0_SCL	I/O	I2C0 clock signal
		UART0_TXD	0	UART0 Send signal
		SPI0_CLK	I/O	SPI0 clock signal
		PWM0	0	PWM0 Output
		EINT0	I	EINT0 Input
		T0	I	Timer 0 input
		INT_VREF	AO	Internal reference voltage output
		CMP1_VREF	AI	Comparator 1 reference voltage output
14	11	**PA1**	**I/O**	**General purpose input/output pins**
		AINN0	AI	AINN0 Input
		C1P	AI	Comparator 1 positive input
		SWDIO	I/O	SWD data signal
		SPI0_MOSI	I/O	SPI0 Host output/slave input signal
		PWM1	0	PWM1 Output
		PDA	I/O	Burning data port
15	12	**PA2**	**I/O**	**General purpose input/output pins**
		AINP1	AI	AINP1 input
		C1N	AI	Comparator 1 negative input
		SWDCLK	I	SWD Clock signal
		PWM2	0	PWM2 output
		PCL	I	Burning clock port
16		**PB10**	**I/O**	**General purpose input/output pins**
17	13	**PA3**	**I/O**	**General purpose input/output pins**
		AINN1	AI	AINN1 Input
		C1P	AI	Comparator 1 positive input
		C0N	AI	Comparator 0 Negative input
		I2C0_SDA	I/O	I2C0 data signal
		UART0_RXD	I	UART0 Receive signal
		SPI0_MISO	I/O	SPI0 Host input/slave output signal
		PWM2	0	PWM2 output
		EINT1	I	EINT1 Input
		T1	I	Timer 1 input
		DAC_OUT	AO	DAC Output
18	14	**PA4**	**I/O**	**General purpose input/output pins**
		AINP2	AI	AINP2 input
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
		PWM1	0	PWM1 Output

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		DM1	AI	QC Port Group 1 Negative Input
		QCDM1_VREF	AO	QCDM1_VREF Voltage Output
19	15	**PA5**	**I/O**	**General purpose input/output pins**
		AINN2	AI	AINN2 Input
		C0N	AI	Comparator 0 Negative input
		SPI0_SS	I/O	SPI0 chip select signal
		PWM0	O	PWM0 Output
		DP1	AI	QC Port Group 1 Positive Input
		QCDP1_VREF	AO	QCDP1_VREF Voltage Output
20	16	NRST	I	Reset pin input, with pull-up resistor 40K by default
21	17	**PA6**	**I/O**	**General purpose input/output pins**
		AINP3	AI	AINP3 Input
		C1P	AI	Comparator 1 positive input
		C0P	AI	Comparator 0 Positive input
		PWM2	O	PWM2 output
		DM0	AI	QC Port Group 0 Negative Input
		QCDM0_VREF	AO	QCDM0_VREF Voltage Output
22	18	**PA7**	**I/O**	**General purpose input/output pins**
		AINN3	AI	AINN3 Input
		UART0_TXD	O	UART0 Send signal
		SPI0_MOSI	I/O	SPI0 Host output/slave input signal
		PWM1	O	PWM1 Output
		WKUP0	I	Power-down mode wake-up pin, active high
		STADC	I	ADC trigger input pins
		C0N	AI	Comparator 0 Negative input
		DP0	AI	QC Port Group 0 Positive Input
		QCDP0_VREF	AO	QCDP0_VREF Voltage Output
23		**PB0**	**I/O**	**General purpose input/output pins**
		AINP4	AI	AINP4 input
		COP	AI	Comparator 0 Positive input
		TM_TRG1	I	Timer external trigger input 1
		PWM0	O	PWM0 Output
		PWM0L	O	Complementary PWM0L Output
24		**PB1**	**I/O**	**General purpose input/output pins**
		AINN4	AI	AINN4 Input
		PWM1	O	PWM1 Output
		PWM0H	O	Complementary PWM0H Output
25		**PB7**	**I/O**	**General purpose input/output pins**
		PWM2H	O	Complementary PWM2H Output
26		**PB8**	**I/O**	**General purpose input/output pins**
		PWM2L	O	Complementary PWM2L Output
27	19	**PA8**	**I/O**	**General purpose input/output pins**
		AINP5	AI	AINP5 Input
		I2C0_SDA	I/O	I2C0 data signal
		UART0_RXD	I	UART0 Receive signal
		SPI0_SS	I/O	SPI0 chip select signal

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		PWM0	O	PWM0 Output
		EINT2	I	EINT2 Input
		T2	I	Timer 2 Input
28	20	PA9	I/O	General purpose input/output pins
		AINN5	AI	AINN5 Input
		I2C0_SCL	I/O	I2C0 clock signal
		UART0_TXD	O	UART0 Send signal
		SPI0_MISO	I/O	SPI0 Host input/slave output signal
29	21	PA10	I/O	General purpose input/output pins
		AINP6	AI	AINP6 Input
		C0P	AI	Comparator 0 Positive input
		PWM1	O	PWM1 Output
		PWM1L	O	Complementary PWM1L Output
30	22	PA11	I/O	General purpose input/output pins
		AINN6	AI	AINN6 Input
		C0N	AI	Comparator 0 Negative input
		PWM2	O	PWM2 output
		PWM1H	O	Complementary PWM1H output
31	23	PB2	I/O	General purpose input/open drain output pins
		PWM2	O	PWM2 output
		VBUS_EN2	O	High voltage control switch, open drain output
32	24	PB3	I/O	General purpose input/open drain output pins
		VBUS_EN1	I/O	High voltage control switch, open drain output
		C1P	AI	Comparator 1 positive input
		CKO	O	Frequency divider output
–	–	EPAD	GND	Ground

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4 Function Introduction

4.1 MCU Subsystem

MCU subsystem features are as follows

- The CS32G020 series are 32-bit microprocessors with embedded ARM® Cortex™-M0 cores
- Can be used for industrial control and applications requiring high performance and low power consumption.
- Kernel includes serial debugging interface (SWD) for development debugging and application burn-in
- Supports 4 breakpoints and 2 watchpoints.

4.2 Flash

The CS32G020 is embedded with 60K bytes of on-chip flash, which is used as application program memory (APROM), and the flash controller features are as follows

- Zero-wait sequential address read access up to 24MHz
- 60KB of application storage (APROM)
- 4
- (
- A
- S (IAP) for updating the on-chip

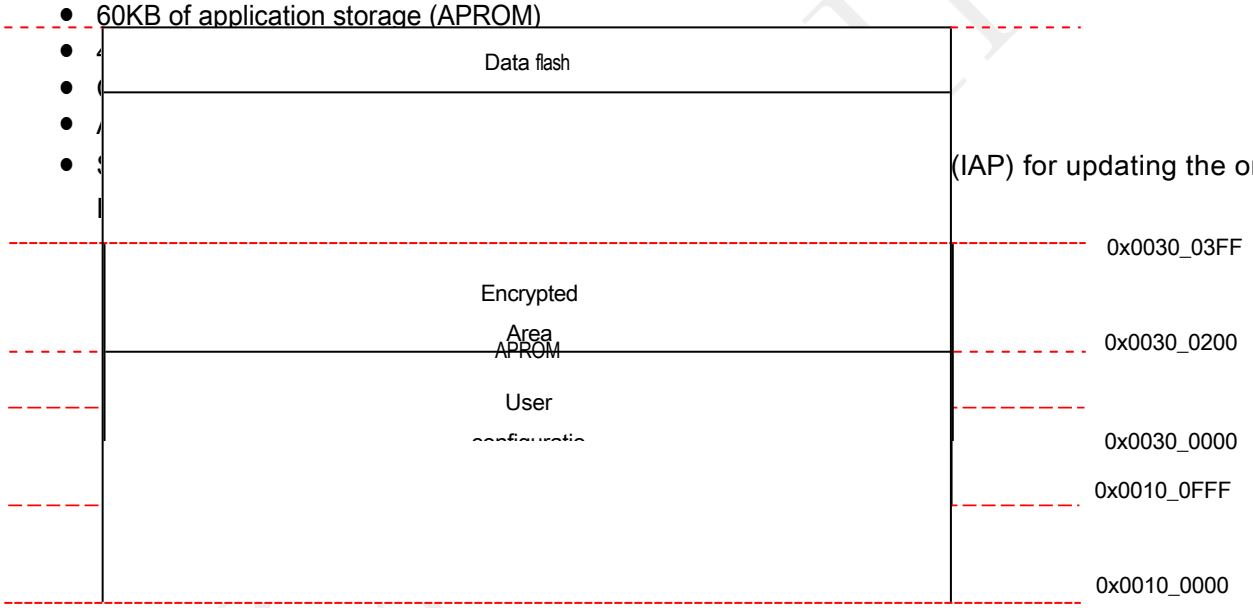

Figure 4-1 Flash memory controller block diagram

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4.3 LDROM

LDROM is used to store the bootloader, CS32G020 has 4K bytes of bootloader space. The user cannot modify the LDROM interval program.

4.4 User configuration area

The user configuration area is an internally programmable configuration area. The user configuration area is addressed in Flash memory as 0x0030_0000, 0x0030_0004, 0x0030_0008, 0x0030_000C for a total of 4 words. Its content is used to configure some peripheral registers at system boot time. The lower half word is the user configuration bit and the higher bit is the inverse of the user configuration bit.

CONFIG0 (address = 0x0030_0000)

31	30	29	28	27	26	25	24
~CWDTEN	~CLIRC_EN	Reserved		~CDELAY[1:0]		~XT_SEL	~HIRC_SEL
23	22	21	20	19	18	17	16
~CBODEN	~CBOV[2:0]			~CBORST	~CHVRST	Reserved	Reserved
15	14	13	12	11	10	9	8
CWDTEN	CLIRC_EN	Res		CDELAY[1:0]		XT_SEL	HIRC_SEL

Table 4-1

Bits	Description	
31:16	Reserved	Inverse code of the lower 16 bits
15	CWDTEN	**Watchdog enable control** 0 = Enable watchdog timer after chip power up. 1 = Watchdog off by default at power-up.
14	CLIRC_EN	**LIRC Enable Control** 0 = LIRC's 10K clock source is always enabled and cannot be turned off by software. 1 = 10K clock source for LIRC controlled by LIRC_EN (CLKCON[3])
13:12	Reserved	Reserved
11:10	CDELAY[1:0]	**Reset delay time selection** 00 = 20ms 01 = 40ms 10 = 60ms 11 = 98ms CDELAY[1:0] is the delay selection bit, valid when the delay selection bit is inverted with the parity bit, other cases Both use a maximum delay time of 98ms.
9	Reserved	Reserved

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8	HIRC_SEL	**Internal high-speed oscillator frequency selection** 1 = 24MHz 0 = 8MHz
7	CBODEN	**Undervoltage detection enable** 0= Enable undervoltage detection after power-up 1= Disable undervoltage detection after power-up Note: When under-voltage detection is enabled, it also enables 6.5V high voltage detection; when disabled, it also disables
		6.5V high voltage detection.
6:4	CBOV [2:0]	**Undervoltage voltage selection** 000 = 1.8V 001 = 2.0V 010 = 2.4V 011 = 2.7V 100 = 3.0V 101 = 3.6V 110 = 4.0V 111 = 4.0V
3	CBORST	**Undervoltage reset enable** 0 = Enable undervoltage reset after power-up 1 = Disable undervoltage reset after power-up
2	CHVRST	**6.5V High Voltage Reset Enable** 0 = Enables 6.5V high voltage reset after power up 1 = 6.5V high voltage reset disabled after power up
1:0	Reserved	Reserved

CONFIG1 (address = 0x0030_0004)

31	30	29	28	27	26	25	24
~CWDTSEN	Reserved	~CWDTSIS[2:0]			~FRD_CFG[2:0]		
23	22	21	20	19	18	17	16
~CBS[1:0]		Reserved					~DFEN
15	14	13	12	11	10	9	8
CWDTSEN	Reserved	CWDTSIS[2:0]			FRD_CFG[2:0]		

Table 4-2

Bits	Description	
31:16	Reserved	Inverse code of the lower 16 bits
15	CWDTSEN	**Lite Watchdog Enable Control** 0 = Enable watchdog timer after chip power up. 1 = Watchdog off by default at power-up.
14	Reserved	Reserved

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13:11	CWDTSIS[2:0]	**Selects the timeout interval for the lite version of the watchdog timer.** Reset Delay CDELAY[1:0]=00 or 01 000 = 2^{13}*T$_{LIRC}$ 001 = 2^{14} * T$_{LIRC}$ 010 = 2^{15} * T$_{LIRC}$ 011 = 2^{16} * T$_{LIRC}$ 100 = 2^{12} * T$_{LIRC}$ 101 = 2^{11} * T$_{LIRC}$ 110 = 2^{10} * T$_{LIRC}$ 111 = 2^{9} * T$_{LIRC}$ Reset delay CDELAY[1:0]=10 or 11 000 = 2^{13}*T$_{LIRC}$ 001 = 2^{14} * T$_{LIRC}$ 010 = 2^{15} * T$_{LIRC}$ 011 = 2^{16} * T$_{LIRC}$ 100 = 2^{13}*T$_{LIRC}$ 101 = 2^{14} * T$_{LIRC}$ 110 = 2^{15} * T$_{LIRC}$ 111 = 2^{16} * T$_{LIRC}$
10:8	FRD_CFG[2:0]	Flash fetch finger configuration during normal operation These 3 bits must be configured to 000
7:6	CBS[1:0]	**Chip start-up options** CBS [1] Description 0 Chip booting from APROM 0 LDROM start-up CBS[0] Description 1 No IAP functionality 0 IAP Function Enable
5:1	Reserved	Reserved
0	DFEN	**Data Flash Enable** 0 = enable data flash 1 = Disable data flash

CONFIG2 (address = 0x0030_0008)

31	30	29	28	27	26	25	24
~DFBADR [15:8]							
23	22	21	20	19	18	17	16
~DFBADR[7:0]							
15	14	13	12	11	10	9	8
DFBADR [15:8]							
7	6	5	4	3	2	1	0

Table 4-3

Bits	Description	
31:16	~DFBADR[15:0]	Inverse code of the lower 16 bits

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15:0	DFBADR[15:0]	**Data Flash Base Address** The data flash base address is defined by the user. Because the on-chip flash erase unit is 512 bytes, it is forced to keep bit 8-0 as 0 DFBA[15:0] value is minimum 200h, if it is less than 200h, it is equal to 200h, i.e. APROM space Minimum 0.5KB

CONFIG3 (address = 0x0030_000C)

31	30	29	28	27	26	25	24
~SWD_EN[7:0]							
23	22	21	20	19	18	17	16

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Reserved							
15	14	13	12	11	10	9	8
SWD_EN[7:0]							
7	6	5	4	3	2	1	0
Reserved							

Table 4-4

Bits	Description	
31:24	~SWD_EN[7:0]	SWD_EN[7:0] Invert bits
23:16	Reserved	Must be 0xFF
15:8	SWD_EN[7:0]	SWD Debug Enable Bit 0x55: Disable SWD debug function Other: Enables SWD debugging function
7:0	Reserved	Must be 0x00

4.5 Encrypted Area

Table 4-5

Serial number	Address	Description
1	0x0030_0200	Read enable configuration for the **first** 32KB of the main area of the Flash **in user mode** Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, it is encrypted by default. Bit15: 1 indicates 2KB (0x0000_7800~0x0000_7FFF) read enable 0 indicates 2KB (0x0000_7800~0x0000_7FFF) read disable ... bit 1: 1 indicates 2KB (0x0000_0800~0x0000_0FFF) read enable 0 indicates 2KB (0x0000_0800~0x0000_0FFF) read forbidden bit 0: 1 indicates 2KB (0x0000_0000~0x0000_07FF) read enable 0 indicates 2KB (0x0000_0000~0x0000_07FF) read disable
2	0x0030_0204	Read enable configuration for 32KB home area after Flash **in user mode** Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, the encryption is defaulted. Bit15: 1 indicates 2KB (0x0000_F800~0x0000_FFFF) read enable 0 indicates 2KB (0x0000_F800~0x0000_FFFF) read disable ... bit 1: 1 indicates 2KB (0x0000_8800~0x0000_8FFF) read enable 0 indicates 2KB (0x0000_8800~0x0000_8FFF) read disable bit 0: 1 indicates 2KB (0x0000_8000~0x0000_87FF) read enable 0 indicates 2KB (0x0000_8000~0x0000_87FF) read disable

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3	0x0030_0208	**User Mode** Flash Front 32KB Home Area Write Enable Configuration Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, it is encrypted by default. Bit15: 1 indicates 2KB (0x0000_7800~0x0000_7FFF) write enable 0 indicates 2KB (0x0000_7800~0x0000_7FFF) write disable ...

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		bit 1: 1 indicates 2KB (0x0000_0800~0x0000_0FFF) write enable 0 indicates 2KB (0x0000_0800~0x0000_0FFF) write disable bit 0: 1 indicates 2KB (0x0000_0000~0x0000_07FF) write enable 0 indicates 2KB (0x0000_0000~0x0000_07FF) write forbidden
4	0x0030_020C	**User Mode** Flash Back 32KB Home Area Write Enable Configuration Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, it is encrypted by default. Bit15: 1 indicates 2KB (0x0000_F800~0x0000_FFFF) write enable 0 indicates 2KB (0x0000_F800~0x0000_FFFF) write disable ... bit 1: 1 indicates 2KB (0x0000_8800~0x0000_8FFF) write enable 0 indicates 2KB (0x0000_8800~0x0000_8FFF) write disable bit 0: 1 indicates 2KB (0x0000_8000~0x0000_87FF) write enable 0 indicates 2KB (0x0000_8000~0x0000_87FF) write disable
5	0x0030_0210	**User mode** Flash front 32KB main area erase enable configuration Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, it is encrypted by default. bit 15: 1 indicates 2KB (0x0000_7800~0x0000_7FFF) erase enable 0 indicates 2KB (0x0000_7800~0x0000_7FFF) Erase Disable ... bit 1: 1 indicates 2KB (0x0000_0800~0x0000_0FFF) erase enable 0 indicates 2KB (0x0000_0800~0x0000_0FFF) Erase Disable bit 0: 1 indicates 2KB (0x0000_0000~0x0000_07FF) erase enable 0 indicates 2KB (0x0000_0000~0x0000_07FF) Erase Disable
6	0x0030_0214	**User mode** Flash back 32KB home erase enable configuration Bit 31~16: The inverse of the lower 16 bits is used for checksumming. If the checksum fails, it is encrypted by default. bit 15: 1 indicates 2KB (0x0000_7800~0x0000_7FFF) erase enable 0 indicates 2KB (0x0000_7800~0x0000_7FFF) Erase Disable ... bit 1: 1 indicates 2KB (0x0000_8800~0x0000_8FFF) erase enable 0 indicates 2KB (0x0000_8800~0x0000_8FFF) Erase Disable bit 0: 1 indicates 2KB (0x0000_8000~0x0000_87FF) erase enable 0 indicates 2KB (0x0000_8000~0x0000_87FF) Erase Disable
7	0x0030_0214~ 0x0030_021C	**Reserved**
8	0x0030_0220	Flash64KB main area read enable configuration **in burn mode** Bit31: 1 indicates 2KB (0x0000_F800~0x0000_FFFF) read enable 0 indicates 2KB (0x0000_F800~0x0000_FFFF) read disable ... bit 1: 1 indicates 2KB (0x0000_0800~0x0000_0FFF) read enable 0 indicates 2KB (0x0000_0800~0x0000_0FFF) read forbidden bit 0: 1 indicates 2KB (0x0000_0000~0x0000_07FF) read

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		enable 0 indicates 2KB (0x0000_0000~0x0000_07FF) read disable

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4.6 USB PD

CS32G020 supports 2 groups of Type-C ports, and the Type-C port features are as follows

- Individually configurable 5.1K pull-down resistors and 80/180/330uA current sources per CC port
- Support dead battery detection function
- CC port device access automatic detection, the user can directly query the detection results
- Support fast role exchange detection
- Support automatic wake-up for device access in low-power mode

The USB PD module supports USB PD3.0 protocol, and the 2 sets of CC ports

can communicate independently without affecting each other. USBPD Physical

Layer

The USB PD physical layer consists of a transmitter and a receiver, based on the PD3.0 protocol, using BMC encoded data via

CC port communication. All communication is half-duplex. The physical layer or PHY layer incorporates a conflict avoidance mechanism to minimize communication errors on the channel. the USB-PD module contains $_{RP}$ and $_{RD}$, $_{which\ are}$ used for connection detection, port initialization, and USB DFP/UFP identification. The $_{RP}$ resistor is implemented with a pull-up current source.

According to the USB Type-C protocol specification, a Type-C controller must have a fixed resistor on the CC port when it is not powered up, depending on its power role. When a mobile power supply is doing Sink, it must have $_{RD\ connected\ to\ the\ CC\ port;}$ while as a power adapter, both CC ports must be left hanging. To accommodate this application, the CS32G020 can be configured with dead battery resistor $_{RD\ on\ the\ CC}$ port when not powered up. the QFN32 package CC port will have dead battery detection and the QFN24 package CC port will not have dead battery detection.

4.7 VBUS PFE control port

The CS32G020 integrates 2 PFET control outputs to drive VBUS control switches. They are VBUS_EN1 (PB3) and VBUS_EN2 (PB2) ports, which are open-drain outputs and only support low output or high resistance input, high output requires external pull-up resistors.

4.8 ADC

The CS32G020 contains a 20+4 channel 12-bit SAR type analog-to-digital converter (SAR A/D converter). The main features are as follows:

- Analog input voltage range：0 to VDD
- 12-bit resolution
- Up to 10 pairs of differential input channels
- Up to 20+4 single-ended analog input channels
- Up to 200KHz SPS sampling rate
- 5 modes of operation
  - Single conversion mode: A/D completes one conversion in the specified channel
  - Burst mode: A/D conversion is performed continuously on a specified single channel, and the results are stored sequentially in the data register
  - Single-cycle scan mode: A/D conversion is done once for all specified channels (from low to high serial numbered channels)
  - Limited cycle scan mode: each channel conversion specified number of times after switching the next channel, can be configured to discard the previous specified number of conversion results calculation, can be configured to remove the maximum and

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minimum value calculation

- Continuous scan mode: A/D conversion continuously performs single-cycle scan mode until software stops A/D conversion

- The conversion result for each channel is stored in the corresponding data register with valid and overflow flags

The SAR_ADC VREF port is an internal reference voltage output that must be connected to a 1uF capacitor.
The CS32G020 supports up to 10 pairs of differential input channels and can also be configured in single-ended mode.

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4.9 DAC

The CS32G020 has a built-in 11-bit voltage-output digital-to-analog converter with a maximum conversion rate of 200KHz SPS and a choice of internal 2V, 3V, and 4V reference voltages.

4.10 Analog Comparator

The CS32G020 has up to 2 comparators that can be used in different configurations. When the positive input is greater than the negative input, the comparator outputs a logic "1", otherwise it outputs "0". Each comparator can be configured to generate an interrupt when the comparator output value changes. The main features of the analog comparators are as follows:

- Analog input voltage range: 0~VDD
- Hysteresis support
- Supports 8-step output filtering function
- Support output reversal function
- Optional input internal reference voltage for each analog comparator positive/negative side
- Support out-of-range voltage calibration function
- Each comparator supports one interrupt vector

4.11 GPIO

The CS32G020 has up to 27 general-purpose I/O pins that are shared with other functions. 27 pins are divided into 2 ports named PA, PB, each with up to 16 pins. Each pin is independent and has a corresponding register to control the pin operation mode and data.

The I/O type of each pin can be independently configured by software as input, output, and open-drain. The main features are as follows:

- 3 I/O modes.
  - Input mode with high resistance
  - Push-pull output
  - Open Drain Output
- Schmitt trigger input mode is selected by Px_TYPEn[15:0] to enable or disable
- Each I/O pin can be used as an interrupt source, supporting edge/level triggering
- When the pin interrupt function is enabled, the wake-up function of the pin will also be enabled
- Each I/O can be configured as a pull-up or pull-down function

4.12 Communication Interface

The CS32G020 supports 3 general-purpose communication interfaces, they are I2C, SPI, and UART.

4.12.1 I2C

I2C is a 2-wire, bi-directional serial bus that provides a simple and efficient method of communicating data between devices. the I2C standard is a multi-host bus and includes conflict detection and arbitration mechanisms to prevent data conflicts when two or more hosts attempt to control the bus at the same time.

The I2C bus transmits data between devices connected to the bus via two lines (SDA and SCL), and the main features of the bus include

- Supports host and slave modes
- Bidirectional data transfer between host and slave
- Multi-host bus (no central host)

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- Multiple hosts send data simultaneously for arbitration, serial data on the bus is not corrupted
- Supports 7-bit addressing mode
- Support fast mode and standard mode

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- Programmable clock for different rate control
- Independent transmit-receive cache, 8 levels each

4.12.2 SPI

The CS32G020 supports 1 lite SPI interface, including master and slave modes.

The SPI interface allows the MCU to communicate with other SPI interface devices in full-duplex, synchronous, serial communication in two modes: master and slave modes. MISO. When two SPI devices communicate, one as the host and one as the slave, communication between SPI interfaces is initiated by the host, and the host sends the clock (SPICLK) and the slave select signal (SPISS) controls the data exchange, and the host and slave can send and receive data simultaneously.

4.12.3 UART

The CS32G020 primarily provides a programmable full duplex serial communication interface. This interface is capable of transmitting and receiving data simultaneously. The main features of the UART are as follows:

- 1 group UART
- Support for simultaneous sending and receiving of data;
- Baud rate can be matched
- Support auto baud rate
- Receive and transmit have 8 levels of FIFO, RX_FIFO(8*9Bit), TX_FIFO(8*9Bit)
- Receive interrupts support off-air interrupts and receive waterline interrupts
- Send interrupts support send air interrupts and send waterline interrupts
- Supports 8/9-bit data transmission and reception

4.13 Timer

The timer controller includes 3 sets of 16-bit timers, TIMER0~TIMER2, for user-friendly timing control applications. The timer module can support functions such as time counting, external hardware triggering, clock generation, PWM output and complementary PWM output.

The main features of the timer are as follows

- 3 groups of 16-bit timers with 16-bit up counter and a 4-bit prescaler
- Support counting function
- Supports PWM function
- Supports complementary PWM output with adjustable deadband
- Supports up to 96MHz clock counting

4.14 Watchdog Timer

The watchdog timer is used to perform the system reset function when the software runs to an unknown state. In addition to preventing the system from hanging indefinitely, the watchdog timer can also wake up the CPU from idle/sleep mode.The CS32G020 has 3 built-in watchdog counters, they are Watchdog Timer (WDT), Window Watchdog (WWDT), and Lite Watchdog (WDT Lite).

4.14.1 WDT

WDT module enablement is controlled by code options only, once configured as enable, the software can not be turned off, only clear the dog. the main features of WDT are

Down

- 18-bit free-running counter for watchdog timeout interval.
- Timeout interval optional (^{24} ~ ^{218}) WDT_CLK cycle, timeout time range 104 ms ~ 26.3168 s (If WDT_CLK

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= 10 KHz).

- Support watchdog reset delay, reset delay time can be selected 3/18/130/1026 * WDT_CLK.

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- Power-up enable watchdog is supported when the CWDTEN (CONFIG[31] watchdog enable bit) bit is equal to 0.
- The watchdog timeout wake-up function is supported if 10 kHz is selected for the watchdog clock source.
- The watchdog timeout wake-up function is supported if the 32.768 kHz external low-speed crystal is selected as the watchdog clock source.

4.14.2 WWDT

The window watchdog timer is used to implement a system reset in a specified window period to avoid the software from entering an uncontrollable state indefinitely. The main features are as follows

- 6-bit down counter current value (WWDTCVAL) and 6-bit comparison window value (WINCMP) make WWDT timeout window period more flexible
- Supports 4-bit values, programmed WWDT counters up to 11-bit prescaled counter cycles

4.14.3 WDT Lite

This WDT is mainly used for Powerdown mode wake-up, other modes, WDT Lite is not effective. The main features are as follows

- Operates on 5V domain power, power down mode still works
- Clock source is LIRC 10KHz
- Supports wake-up CPU function only in power-down mode

4.15 Operational units

The CS32G020 hardware supports 3 common operations, they are single cycle multiplier, hardware divider, and CRC32 calculation unit.

4.15.1 Single-cycle multipliers

The multiplier is a 32-bit single-cycle multiplier, which can be used to multiply 32-bit data directly without any register configuration, making it easy to use.

4.15.2 Hardware Divider

The Hardware Divider (HDIV) is used to improve the efficiency of applications. The hardware divider is a signed, integer divider with provider and remainder outputs. The main features of the divider are as follows:

- Signed (2's complement) integer calculations
- 32-bit divisor, 16-bit divisor calculation capability
- 32-bit quotient and 32-bit remainder output (16-bit remainder with sign extension to 32 bits)
- Except 0 warning signs
- Each calculation requires 16 HCLK clock cycles
- Write divisor trigger calculation
- Automatically wait for the calculation to complete when reading the quotient and remainder

4.15.3 CRC32 calculation unit

The CRC calculation unit can be used to quickly calculate the result code of a cyclic redundancy check based on the input data according to a defined polynomial algorithm. In many applications, the technique of cyclic redundancy checks is commonly used to check the integrity of data transmission or storage. In the scope of functional security standards
The CRC calculation unit can calculate software signatures at any time, allowing signature comparisons to be done in situ at the time of communication and storage.

CRC32 calculation unit main features:

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- CRC-32 (same as Ethernet standard) polynomial used 0x4C11DB7
  $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x2 + x + 1$
- Manipulate 8, 16, 32-bit data
- CRC initial value can be preset

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- Single input/output 32-bit data register
- Equipped with an input buffer that does not affect real-time calculations when the bus is stalled
- Each CRC calculation is done in 4 AHB clock cycles (HCLK)
- Equipped with 8-bit registers for general purpose (can be used as temporary storage)
- Reversibility option for providing I/O data

4.16 Power Management

To meet the clock and power requirements of different applications, the CS32G020 provides five operating modes, including normal operating mode, Sleep mode, Deep-Sleep mode 1, Deep-Sleep mode 2, and Power-Down mode. The entry and wake-up modes of these modes are shown in the following table

Table 4-6

Mode	Enter	Awakening	Clock influence	Voltage Impact	Wake-up delay
Sleep mode (SLEEP)	(LPMODE=000)+WFI	Any interruption	CPU clock off, for other clocks and analog Clock has no effect	None (digital circuit power supply primary LDO and secondary LDO on)	M0 kernel intrinsic delay
	(LPMODE=000)+WFE	Wake-up time			M0 kernel intrinsic delay
Deep sleep mode 1 (deepsleep1)	(LPMODE=001)+ WFI or WFE	Any external interrupt, supporting LSE or LSI interrupts (WDT/WWDT). BOD interrupt, comparator interrupt	HSE , HSI Close	Digital circuit power supply primary LDO and secondary LDO Open	HSE or HSI start-up stabilization delay + M0 kernel intrinsic delay
Deep sleep mode 2 (deepsleep2)	(LPMODE=011)+ WFI or WFE			Digital Circuit Power Primary LDO Off, Secondary LDO Open	Main LDO turn-on delay +LDO switching + HSE or HSI Start-up Stability Delay+ M0 kernel intrinsic delay
Powerdown mode	(LPMODE=1x1)+ WFI or WFE	Wake-up pin, NRST reset, POR reset	HSE, HSI, LSE and LSI Close	Digital circuit power supply primary LDO and secondar	Reset delay

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				y LDO Close	

4.16.1 Normal working mode

In normal operation mode, the ARM®Cortex™-M0 core runs instructions normally and the different peripheral clocks can be configured independently or can be disabled or enabled individually. Each analog module can also be disabled or enabled by the enable bit. The normal operating mode has a high power consumption.

4.16.2 Sleep mode

In sleep mode, the ARM Cortex- M0 core's clock stops working, instruction execution is suspended, and each clock oscillator does not stop working. Any interrupt can wake up the sleep mode and enable the core to resume execution of instructions.

In sleep mode, the processor status registers, peripheral registers and internal memory values remain unchanged, the logic levels of the pins remain static, and RESET remains active.

Peripheral functions are not affected, and modules that have enabled enable turned on continue to work in sleep mode. The state of the analog module is determined by the module enable bit.

4.16.3 Deep-Sleep1 mode

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In deep sleep mode 1, the system clock of the ARM Cortex- M0 core stops working and instruction execution is suspended. The internal high-speed oscillator HSI stops working, and the LSI continues to operate if enabled on. Deep-Sleep1 mode can be awakened by an external interrupt or WDT interrupt or reset.

In Deep-Sleep mode, the processor status registers, peripheral registers and internal memory values remain unchanged and the logic levels of the pins remain static. The logic levels of the pins remain static.

As the clock stops and peripherals stop working, to ensure power consumption in deep sleep mode, it is recommended to turn off analog modules such as SAR_ADC, comparators, operational amplifiers, etc. to save power.

In deep sleep mode, the FLASH is in a power-down state to reduce static leakage power consumption, and it takes a long time for the FLASH to restart when waking up.

4.16.4 Deep-Sleep2 mode

In Deep Sleep Mode 2, the system clock of the ARM Cortex- M0 core stops working and instruction execution is suspended. The internal high-speed oscillator HSI stops working, and the LSI continues to operate if enabled on. Deep-Sleep2 mode can be awakened by an external interrupt or WDT interrupt or reset.

Deep-Sleep2 mode consumes less power than Deep-Sleep1 mode. However, the wake-up time is also longer.

In Deep-Sleep mode, the processor status registers, peripheral registers and internal memory values remain unchanged and the logic levels of the pins remain static. The logic levels of the pins remain static.

As the clock stops and peripherals stop working, to ensure power consumption in deep sleep mode, it is recommended to turn off analog modules such as SAR_ADC, comparators, operational amplifiers, etc. to save power.

In deep sleep mode, the FLASH is in a power-down state to reduce static leakage power consumption, and it takes a long time for the FLASH to restart when waking up.

4.16.5 Deep Power-Down Mode

In Deep Power-Down mode, the entire chip power (with the built-in LDO turned off) and clock are off, except for pins WKUP0 and WKUP1, which wake up the chip from Deep Power-Down mode when a rising edge is input to the WKUP0 and WKUP1 pins. When WKUP0 and WKUP1 are enabled, these two pins will force a pull-down resistor on and reset the chip when a rising edge input is detected.

In Deep Power-Down mode, the processor status registers, peripheral registers and internal memory values are no longer held and the RESET pin is disabled

When the chip is woken up from Deep Power-Down mode, the built-in LDO turns on and the chip starts working again.

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5 Application burn-in

The CS32G020 supports three ways to update the application: 1. Burning the application through the serial burn-in interface

2、 Update application via Type-C port firmware update

3、 Burning through SWD interface, this way is only for debugging

Typically, the CS32G020 is burned through the serial burn-in interface. When the product is produced and the application needs to be updated, the serial burn-in interface or the bootloader program can call the Type-C port for the update.

5.1 Flash burning via serial burn port

For mass production, CoreTech will provide a special burn-in tool for burn-in.

The format of the burn file is a hex file, which is generated by the compiler and downloaded and written to Flash by the burner to complete the burn.

The serial burn-in interface is connected as shown in the following diagram during burn-in. The chip is powered by the power supply of the burn-in hardware, which corresponds the burn-in clock, data port, and NRST port one by one.

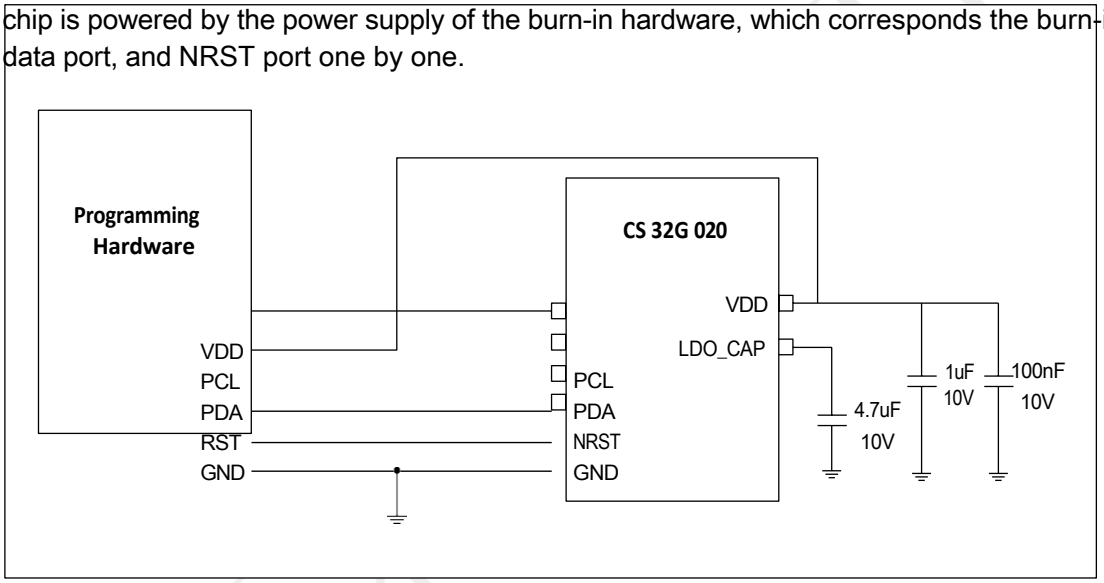

Figure 5-1 Serial burn-in interface to burn CS32G020

5.2 Upgrade applications via Type-C port

The CS32G020 chips are shipped with BoostLoader upgrade program, which supports PD3.0 firmware upgrade function, and the software upgrade can be completed by connecting the supporting firmware upgrade tool via CC data cable.

The format of the burn file is a hex file, which is generated by the compiler and is downloaded and burned to FLASH through the CS32G020 configuration host and firmware upgrade tool via PD3.0 non-block transfer method.

The firmware upgrade tool burn connection is shown in the following figure:

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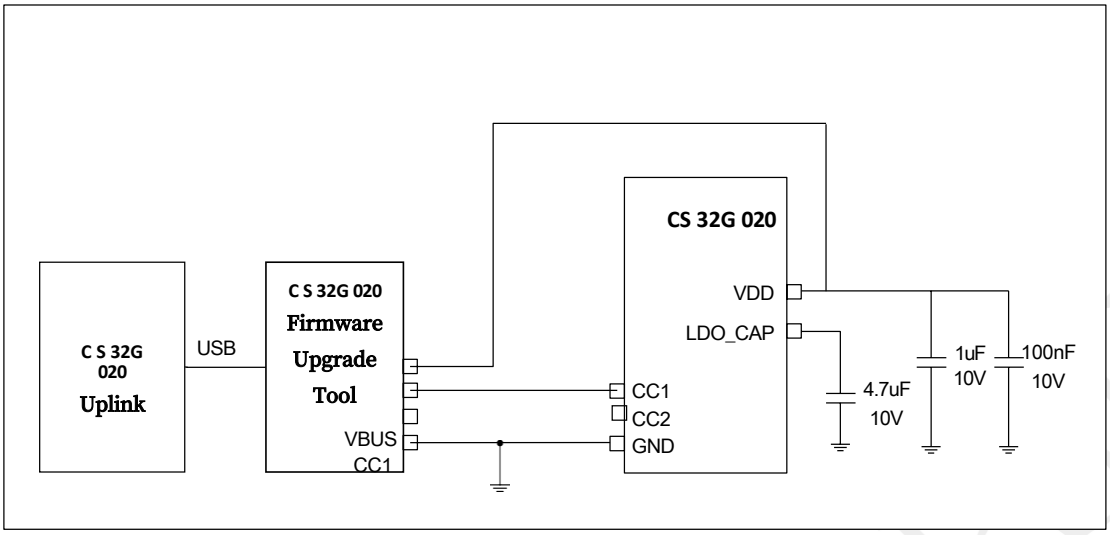

Figure 5-2 Type-C interface burn-in CS32G020

5.3 Burning via SWD port

The CS32G020 supports burn-in debugging via the SWD port when debugging or a small amount of burn-in is performed. The use of the SWD port for debugging assumes that the SWD port of the CS32G020 is not multiplexed as another function port.

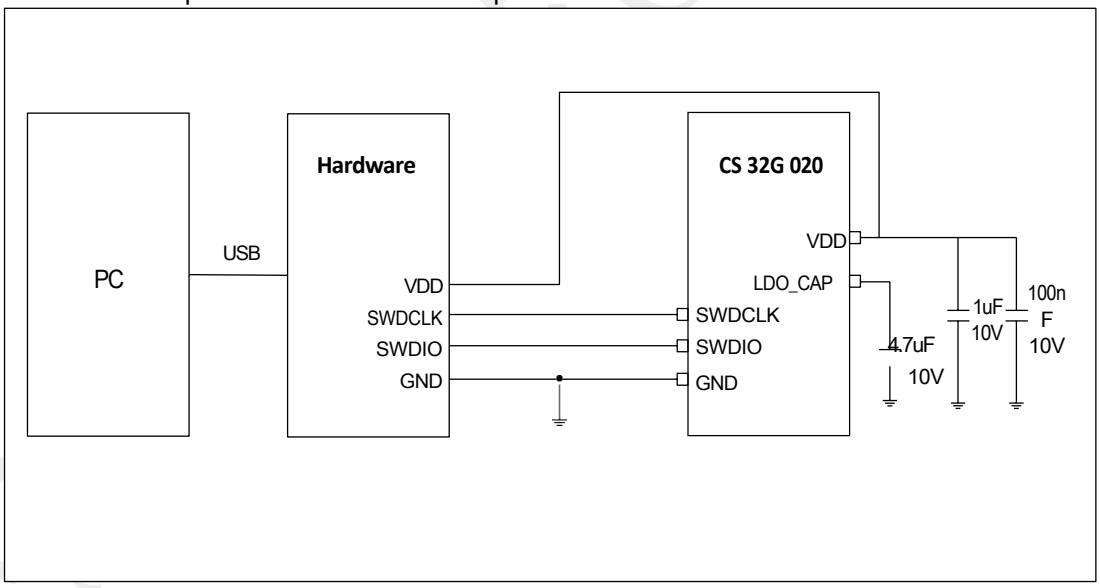

Figure 5-3 SWD port burn-in CS32G020

5.4 Burning method selection

For the chip burning method, there can be different choices depending on the situation.

- When burning the die, you can use a dedicated burner or the SWD port for burning.
- When the chip is already on the board and the burn-in and SWD ports are reserved, you can use a dedicated burner or the SWD port for burning.

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- When the chip is already on the board and has a Type-C port, and supports bootloader upgrade, you can use the bootloader for burning.
- For solution development, SWD can be used for burn-in, which is simple and easy to debug
- For mass production, it is recommended to use a special burner for burning, and we have two types of burners available: one with four burners and a simple burner. The simple burner is for development only and is not recommended for mass production.

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6 Typical applications

6.1 Mobile power typical applications

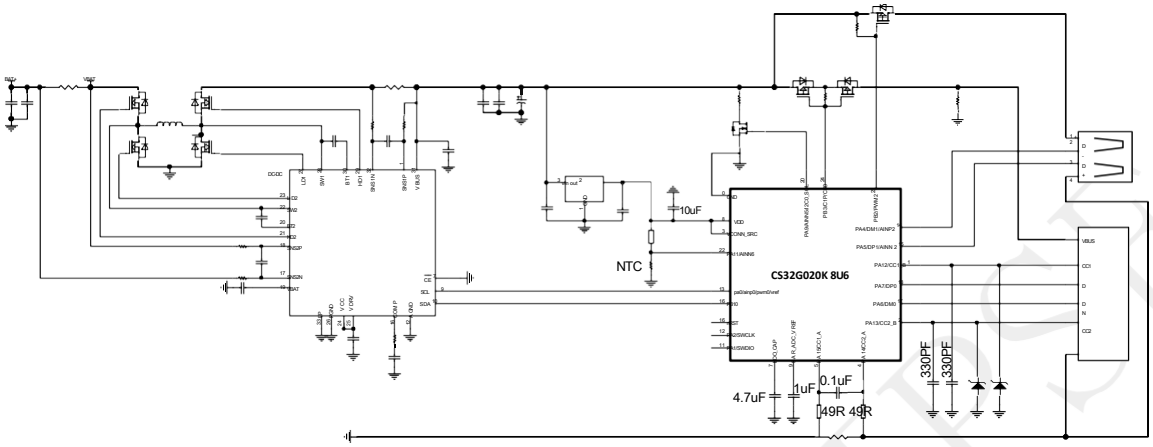

Figure 6-1 Mobile power typical application diagram

6.2 Typical applications for car chargers

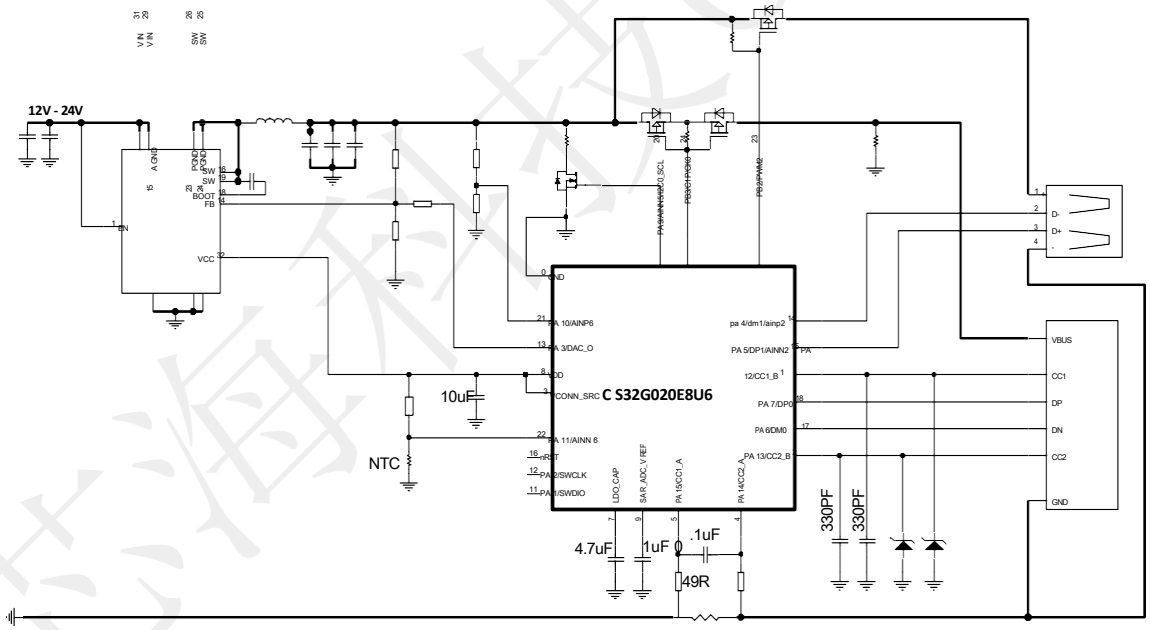

Figure 6-2 Typical application of car charger

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6.3 Power adapter typical applications

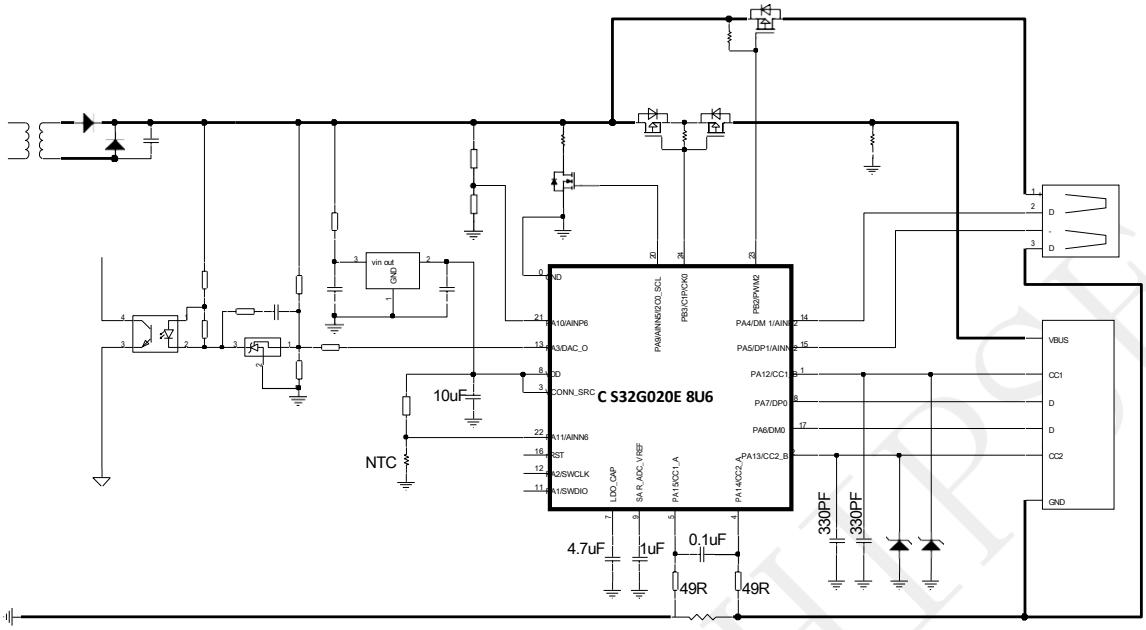

Figure 6-3 Typical Application of Power Adapter

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7 Electrical characteristics

7.1 Limit values

Table 7-1

Symbols	Parameters	Minimum value	Maximum value	Unit
VDD-VAGND	DC supply voltage	-0.3	6.0	V
VIN	Pin Input Voltage	VAGND-0.3	VDD+0.3	V
VCC_PIN	CC port (PA12, PA13, PA14, PA15) transmission Inlet Voltage	-	24	V
VVBUS_ENn	VBUS_EN1 (PB3), VBUS_EN2 (PB2) Port input voltage	-	24	V
TA	Operating temperature	-40	85	ºC
TST	Storage temperature	-55	150	ºC
IVDD	VDD Maximum Inflow Current	-	120	mA
IGND	GND Maximum outflow current	-	120	mA
IIO	Single pin maximum fill current	-	35	mA
	Maximum outflow current from a single pin	-	35	mA
	Sum of the maximum supply current of all pins	-	100	mA
	Total maximum output current of all pins	-	100	mA

7.2 DC gas characteristics

(VDD-VGND=2.5~5.5V, TA=25 ºC)

Table 7-2

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating Voltage	2.5	5	5.5	V	-40 ºC ~+85 ℃,up to 48MHz
VAGND/ AVAGND	Power Ground	-0.3	0	0.3	V	
LDO	Output Voltage	1.35	1.5	1.65	V	VDD≥1.8V
RPH	PA,PB and NRST pull-up resistors		40		kΩ	VDD=5V
			70		kΩ	VDD=3V
RPD	PA, PB and TESTEN Pull Down Resistors		40		kΩ	VDD=5V
			70		kΩ	VDD=3V
ILK	Input leakage of PA,PB Flow	-1	-	1	uA	VDD=5V,0<VIN< VDD Open-drain mode or input mode
	PA,PB input low	-0.3	-	VDD/2	V	VDD=4.5V

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V_{IL1}	(Schmitt input disabled) In)	-0.3	-	VDD/2	V	VDD=3.0V
V_{IH1}	PA,PB input high (Schmitt input disabled) In)	VDD/2	-	VDD+0.3	V	VDD=5.5V
		VDD/2	-	VDD+0.3	V	VDD=3.0V
V_{ILS1}	NRST Negative Threshold Electricity Pressure (Schmitt input)	-0.3	-	$0._{2VDD}$	V	-
V_{IHS1}	NRST Forward Threshold Electricity Pressure (Schmitt input)	$0._{7VDD}$	-	VDD+0.3	V	-
V_{ILS2}	PA,PB Negative Threshold Electricity Pressure (Schmitt input)	-0.3	-	$0._{3VDD}$	V	-
V_{IHS2}	PA,PB Positive threshold voltage (Schmitt input)	$0._{7VDD}$	-	VDD+0.3	V	-
V_{OL1}	PA, PB output low power	-	0	-	V	-
	Flat (except PA12/PA13/PA14/PA15/PB2/PB3)					
V_{OH1}	PA, PB output high (except PA12/PA13/PA14/PA15/PB2/PB3)	-	V_{DD}	-	V	-
V_{OL2}	PA12/PA13/PA14/PA15/PB2/PB3 output Low Level	-	0	-	V	-
V_{OH2}	PA12/PA13/PA14/PA15/PB2/PB3 output high level	-	V_{DD} – 0.7	V_{DD}	V	The output high level is related to the load, if it is a capacitive load, not go current, for VDD, if it is a resistive load, depends on the resistance value of large Jr.
I_{OH0}	PB0/PB1/PB7/PB8/PA10/PA11	-	15	-	mA	VDD=5.0V
I_{OH1}	PA,PB source currents except for the ports in I_{OH0} (push pull output)	-	8	-	mA	VDD=5.0V
I_{OH2}		-	4	-	mA	VDD=3.0V
I_{OL0}	PB0/PB1/PB7/PB8/PA10/PA11	-	21	-	mA	VDD=5.0V
I_{OL1}	The PA,PB irrigation current except for the	-	12	-	mA	VDD=5.0V
I_{OL2}		-	5	-	mA	VDD=3.0V

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	port in IOL0 (push pull output)					
IIDLE1	Operating current in run mode @ IRC 24MHz, HCLK=48MHz	-	10	-	mA	VDD=5.0V, enable all peripherals, enable PLL
IIDLE2		-	8	-	mA	VDD=5.0V, turn off all peripherals, turn off PLL
IIDLE3		-	9	-	mA	VDD=3.3V, enable all peripherals, enable PLL
IIDLE4		-	7	-	mA	VDD=3.3V, turn off all peripherals, enable PLL
IIDLE5	Operating current in run mode @ IRC8MHz, HCLK=8MHz	-	3	-	mA	VDD=5.0V, enable all peripherals, enable PLL
IIDLE6		-	2.5	-	mA	VDD=5.0V, turn off all peripherals, turn off PLL
IIDLE7		-	2.5	-	mA	VDD=3.3V, enable all peripherals, enable PLL
IIDLE8		-	2	-	mA	VDD=3.3V, turn off all peripherals, enable PLL
IIDLE9	Operating current in run mode @ IRC 24MHz, HCLK=24MHz	-	7	-	mA	VDD=5.0V, enable all peripherals, enable PLL
IIDLE10		-	4	-	mA	VDD=5.0V, turn off all peripherals, turn off PLL
IIDLE11		-	6.5	-	mA	VDD=3.3V, enable all peripherals, enable PLL
IIDLE12		-	4	-	mA	VDD=3.3V, turn off all peripherals, enable PLL
IIDLE13	Operating current in operating mode @ IRC 10KHz, HCLK=10KHz	-	110	-	uA	VDD=5.0V, enable all peripherals
IIDLE14		-	105	-	uA	VDD=5.0V, turn off all peripherals
IIDLE15		-	92	-	uA	VDD=3.3V, enable all peripherals
IIDLE16		-	90	-	uA	VDD=3.3V, turn off all peripherals
IPWD1	Standby power in deep sleep mode 2 (not off) LDO)	-	12	-	uA	VDD=5.0V, all oscillators and analog modules Block off, IO not connected to load
IPWD2		-	8	-	uA	VDD=3.3V, all oscillators and analog modes
						Block off, IO not connected to load
IPWD3	Standby current in power-down mode (Turn off LDO)	-	2.5	-	uA	VDD=5.0V, all oscillators and analog modules Block off, IO not connected to load
IPWD4		-	1.5	-	uA	VDD=3.3V, all oscillators and analog modes

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						Block off, IO not connected to load

7.3 AC Electrical Characteristics

7.3.1 Internal 24/8MHz RC oscillator

Table 7-3

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
FHRC	Center Frequency	–	24	–	MHz	TA=25 ºC, VDD=5V
	Center Frequency	–	8	–	MHz	TA=25 ºC, VDD=5V
	After calibration	-1	–	+1	%	TA=25 ºC, VDD=5V
		-2	–	+2	%	TA=-40~85 ℃, VDD=2.5~5.5V
IHRC	Operating current		400		uA	TA=25 ºC, VDD=5V

7.3.2 Internal 10KHz RC oscillator

Table 7-4

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VLRC	Voltage	2.5	–	5.5	V	–
FLRC	Center Frequency	–	10	–	KHz	–
	After calibration	-10	–	+10	%	TA=25 ºC, VDD=5V
		-30	–	+30	%	TA=-40~85 ℃, VDD=2.5~5.5V
ILRC	Operating current	–	2	–	uA	TA=25 ºC, VDD=5V

7.3.3 PLL Features

Table 7-5

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
FPLL_IN	PLL Input Clock	2	6	24	MHz	TA=25 ºC
	PLL Input Clock Duty Cycle	40	–	60	%	TA=25 ºC
FPLL_OUT	PLL multiplier output clock	16	–	48	MHz	TA=25 ºC
TLOCK	PLL Lock Time	–	–	200	us	TA=25 ºC
JitterPLL	Clock jitter	–	–	300	ps	TA=25 ºC

7.3.4 I2C Features

Table 7-6 I2C Characteristics

Symbols	Parameters	Standard Mode		Quick Mode		Unit
		Minimum value	Maximum value	Minimum value	Maximum value	

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Gathering the core of a

V_{DD}	Operating Voltage	1.62	5.5	1.62	5.5	V
F_{SCL}	SCL clock frequency	0	100	0	400	KHz
T_{HD}:STA	Hold time of START condition	4	–	0.6	–	μs
T_{LOW}	Low level pulse width of SCL	4.7	–	1.3	–	μs
T_{HIGH}	High level pulse width of SCL	4	–	0.6	–	μs
T_{SU}:STA	Repeat START signal build time	4.7	–	0.6	–	μs
T_{HD}:DAT	Data hold time for I2C bus devices	0	3.45	0	0.9	μs
	between					
T_{SU}:DAT	Data creation time	250	–	100	–	ns
T_r	Rise time of SCL and SDA signals	–	1000	20+0.^{1Cb2}	300	ns
T_f	SCL and SDA signal fall time	–	300	20+0.1Cb	300	ns
T_{SU}:STO	Establishment time of STOP condition	4	–	0.6	–	μs
T_{BUF}	Between STOP and START conditions of bus idle time	4.7	–	1.3	–	μs
T_{SP}	Burrs that can be filtered out by input filtering Pulse Width	N/A	N/A	0	50	μs

Note 1: The voltage of the pull-up resistor for the I2C bus does not have to be equal to the chip voltage, for example, if the chip power supply voltage is 5V, the I2C bus pull-up resistor voltage can be 1.8V.

Note 2: Cb is the value of all capacitances on a bus in pF.

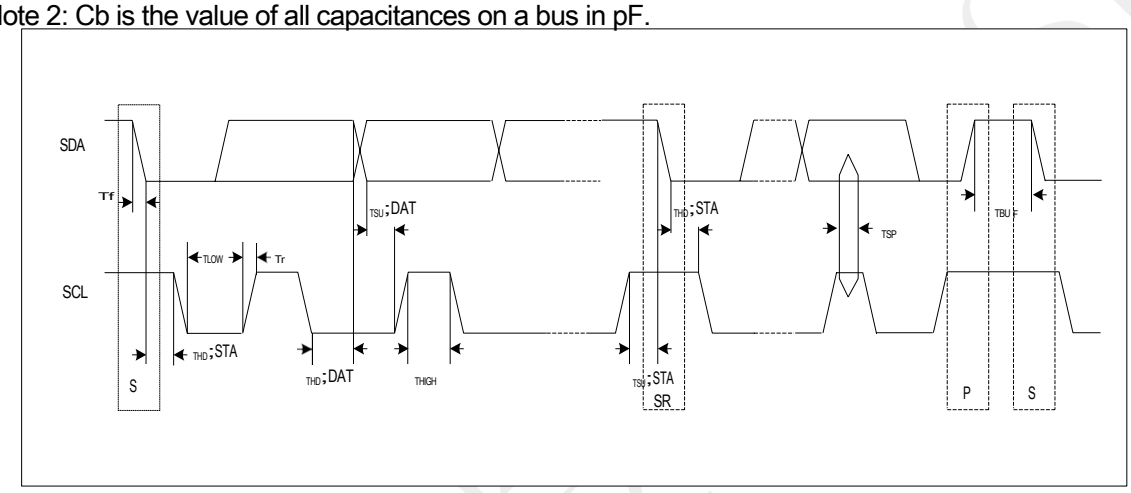

Figure 7-1 I2C Standard and Fast Mode Timing Definitions

7.3.5 Flash

Features Table 7-7

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
T_{ERASE}	Flash Block Erase Time	4	4.5ms	5	ms	-40~85 ºC
T_{WRITE}	Flash Word (32bit) Write time			60	us	-40~85 ºC
T_E	Flash Erase Count			20000	times	-40~85 ºC
T_{DR}	Flash retention	100		–	years	25 ºC

7.4 Analog characteristics

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Table 7-8

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating Voltage	2.5	5	5.5	V	-40~85 ºC
VIN	Analog input range	0	–	VDD	V	–
IADC	ADC Operating Current	–	0.75	–	mA	VDD=5V (VDD as reference voltage)
TCONV	ADC conversion time	5	–	–	us	VDD=5V
DNL	Differential nonlinearity	-2	±1	2	LSB	VDD=5V
INL	Integral nonlinearity (full differential mode)	-3	–	3	LSB	Full differential mode VREF=0.5V@[0-60mV], VDD=5V
		-2	–	2	LSB	Full differential mode VREF=1V@[0-60mV] , VDD=5V
		-4	–	4	LSB	Full differential mode, reference voltage cannot be selected VDD,, VDD=5V
	Integral nonlinearity (single-ended mode)	-7	–	7	LSB	Single-ended mode VREF=0.5V, VDD=5V
		-5	–	5	LSB	Single-ended mode VREF is the other voltage, and VDD=5V
EO	Full Differential Mode Offset Error	–	±2	–	LSB	VDD=5V
	Single Ended Mode Offset Error	–	±3	–	LSB	VDD=5V
EG	Gain error	-4	–	+4	LSB	VDD=5V

Maximum external input impedance calculation formula:

$$Rain < \frac{Ts}{9C_{ADC}} - RADC$$

where RADC=2.3k and CADC=17.5pF refer to the internal sampling resistance and sampling capacitance of the ADC, respectively.

Sampling time Ts/us	2	4	8	16
External	10.5	23.1	48.5	99.3

Note: This table is guaranteed by design and has not been verified by testing. (RADC=3.3k if one of AINP7, AINN7, AINP8, AINN8 is selected for the input port)

7.4.2 11bit DAC

Table 7-9

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating Voltage	2.5	5	5.5	V	-40~85 ºC
IDAC	DAC Operating Current	–	0.75	–	mA	VDD=5V (VDD as reference voltage)
TCONV	DAC Conversion Rate	5	–		us	VDD=5V
RLOAD	Resistive load	5	–		kΩ	Turn on BUFFER
CLOAD	Capacitive load		–	50	pF	Turn on BUFFER
DAC_OUT min	DAC Minimum Output	0.2	–		V	Turn on BUFFER
DAC_OUT max	DAC Maximum Output	–	–	VDD-	V	Turn on BUFFER

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				0.2		
Gathering the core of a						CLOAD≤50pF, RLOAD≥5K
Tsettling	DAC build time	–	3	4	uS	10BIT input code jumps from min. to max. to DAC_OUT stabilized at the final value of ±0.5 1LSB of time
Update rate	Refresh rate	–		200	KS/s	CLOAD≤50pF, RLOAD≥5K Input code change 1LSB, DAC_OUT change
Twakeup	Wake-up time	–	6.5	10	uS	CLOAD≤50pF, RLOAD≥5K DAC from off to output relative to input code Response value
DNL	Differential nonlinearity	-1	–	1	LSB	–
INL	Integral nonlinearity	-4	–	4	LSB	–
EG	Gain error	-0.5	–	-0.5	%	–

7.4.3 Comparator

Table 7-10

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Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VCMP	Operating Voltage	2.5	5	5.5	V	-40 ºC ~+85 ºC
TA	Temperature	-40	25	85	ºC	–
VIN	Input Voltage Range	0	–	VDD	V	–
Icomp	Operating current		60		uA	VDD=2.5V~5V
PSRR	Supply voltage rejection ratio	–	60	–	dB	–
Tresp	Response time	–	–	10	uS	VDD=2.5V~5V
CMRR	Common mode rejection ratio	–	60	–	dB	–
CMP LSB	Minimum Resolution	–	2	–	mV	–
Voffset	Failure to adjust voltage	-2	–	2	mV	2.5V~5.5V，-40 ºC ~+85 ºC

7.4.4 Internal Reference Voltage

Table 7-11

Symbols	Parameters	Minimum value	Typical values	Maximum Value	Single position	Test conditions
VRIN	Internal Reference Voltage	-1%	1.0	+1%	V	VDD=5.0V，TA=25 ºC
		-2%	1.0	-2%	V	VDD=2.5~5.5V，TA=-40~85 ºC
		-1%	2.0	+1%	V	VDD=5.0V，TA=25 ºC
		-2%	2.0	-2%	V	VDD=2.5~5.5V，TA=-40~85 ºC
		-1%	3.0	+1%	V	VDD=5.0V，TA=25 ºC
		-2%	3.0	-2%	V	VDD=3.3~5.5V，TA=-40~85 ºC
		-1%	4.0	+1%	V	VDD=5.0V，TA=25 ºC
		-2%	4.0	-2%	V	VDD=4.3~5.5V，TA=-40~85 ºC
		–	VDD	–	V	VDD=5.0V，TA=25 ºC
CMP0_VREF	Comparator 0 Reference Voltage	0.00	0.00	0.05	V	VDD>2.7V
		0.275	0.325	0.38	V	VDD>2.7V
		0.55	0.60	0.65	V	VDD>2.7V
		0.85	1.00	1.15	V	VDD>2.7V
		1.80	2.00	2.20	V	VDD>2.7V
		2.40	2.70	3.00	V	VDD>3.2V
		2.70	3.00	3.30	V	VDD>3.5V
		3.00	3.30	3.60	V	VDD>3.8V
		1.00	1.20	1.40	V	VDD>2.7V
		2.25	2.40	2.65	V	VDD>2.9V

Note: VDD needs to be 0.5V larger than the reference voltage to ensure the accuracy of the reference voltage.

7.4.5 LDO Specifications and Power Management

Table 7-12

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Input Voltage	2.5	–	5.5	V	–
VLDO	Output Voltage	1.35	1.5	1.65	V	–
TA	Operating temperature	-40	25	85	ºC	–
CLDO	Capacitance	–	4.7	–	uF	RESR<1Ω

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Note: To ensure power supply stability, connect a 4.7uF capacitor between the LDO and the nearest VSS.

7.4.6 Undervoltage reset

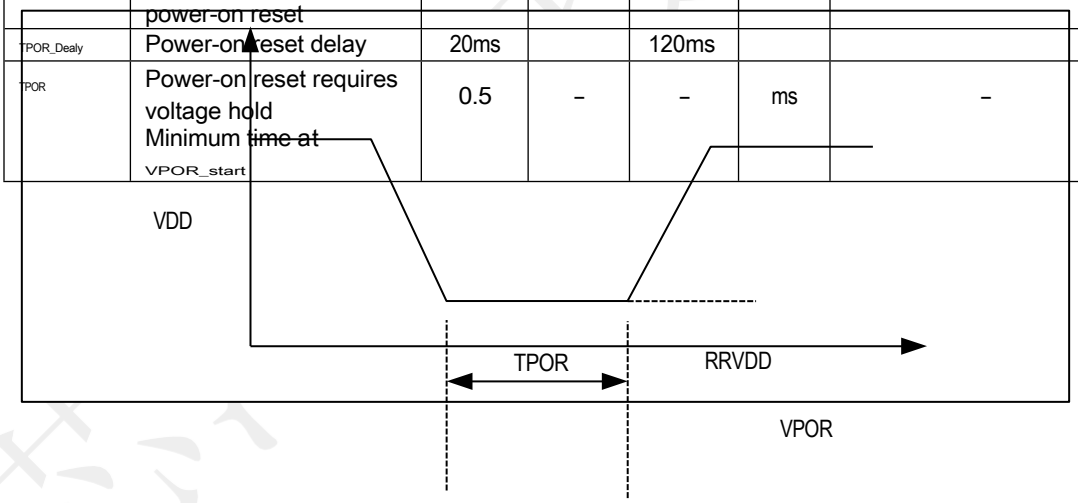
Table 7-13

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating Voltage	0	–	5.5	V	–
TA	Operating temperature	-40	25	85	ºC	–
IBOD	Static current	–	1	140	uA	VDD=5.5V
VBOD	Undervoltage voltage (rising edge)	1.65	1.8	1.95	V	TA = -40~85 ºC
		1.85	2.0	2.15	V	TA = -40~85 ºC
		2.2	2.4	2.6	V	TA = -40~85 ºC
		2.5	2.7	2.9	V	TA = -40~85 ºC
		2.8	3.0	3.2	V	TA = -40~85 ºC
		3.3	3.6	3.9	V	TA = -40~85 ºC
		3.6	4.0	4.4	V	TA = -40~85 ºC
		6.0	6.5	7.0	V	TA = -40~85 ºC
VBOD	Undervoltage voltage (falling edge)	1.65	1.8	1.95	V	TA = -40~85 ºC
		1.85	2.0	2.15	V	TA = -40~85 ºC
		2.2	2.4	2.6	V	TA = -40~85 ºC
		2.5	2.7	2.9	V	TA = -40~85 ºC
		2.8	3.0	3.2	V	TA = -40~85 ºC
		3.3	3.6	3.9	V	TA = -40~85 ºC
		3.6	4.0	4.4	V	TA = -40~85 ºC
		6.0	6.5	7.0	V	TA = -40~85 ºC

7.4.7 Power-on reset

Table 7-14

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
TA	Operating temperature	-40	25	85	ºC	–
VPOR_th	Reset release threshold voltage	–	1.6	–	V	–
VPOR_start	Start-up voltage for power-on reset	–	–	100	mV	–
RRVDD	Voltage rise rate of power-on reset	0.025	–	–	V/ms	–
TPOR_Dealy	Power-on reset delay	20ms		120ms		
TPOR	Power-on reset requires voltage hold Minimum time at VPOR_start	0.5	–	–	ms	–



Features

7.4.8 Type-C

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Figure 7-2

(VDD = 5V, T_A = 25°C, all conditions if not otherwise specified)

Table 7-15

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating voltage range	2.5	5	5.5	V	25 ºC
		2.7	5	5.5	V	-40 ºC ~+85 ºC
Rp	CC1, CC2	73	80	87	uA	VDD>3V
		165	180	195	uA	VDD>3V
		303	330	357	uA	VDD>3V
Rd	Pull Down Resistors	4.6	5.1	5.6	KΩ	VDD=2.7V~5V
Tsettle_pd	The rise of the PD square wave and Descent time	300	–	1300	ns	CC port recommended to connect 330pf capacitor

7.4.9 QC3.0 Features

(VDD = 5V, T_A = 25ºC, all conditions if not otherwise specified)

Table 7-16

Symbols	Parameters	Minimum value	Typical values	Maximum value	Unit	Test conditions
VDD	Operating voltage range	2.5	5	5.5	V	25 ºC
		2.7	5	5.5	V	-40 ºC ~+85 ºC
RDP	DPn pull-down resistor	300	500	1500	KΩ	
RDM	DMn pull-down resistor	16	18	20	KΩ	
	DPn and DMn shorting power obstruction	–	20	40	Ω	

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8 Package information

8.1 QFN24-PIN(4mm*4mm*0.55,e=0.5mm)

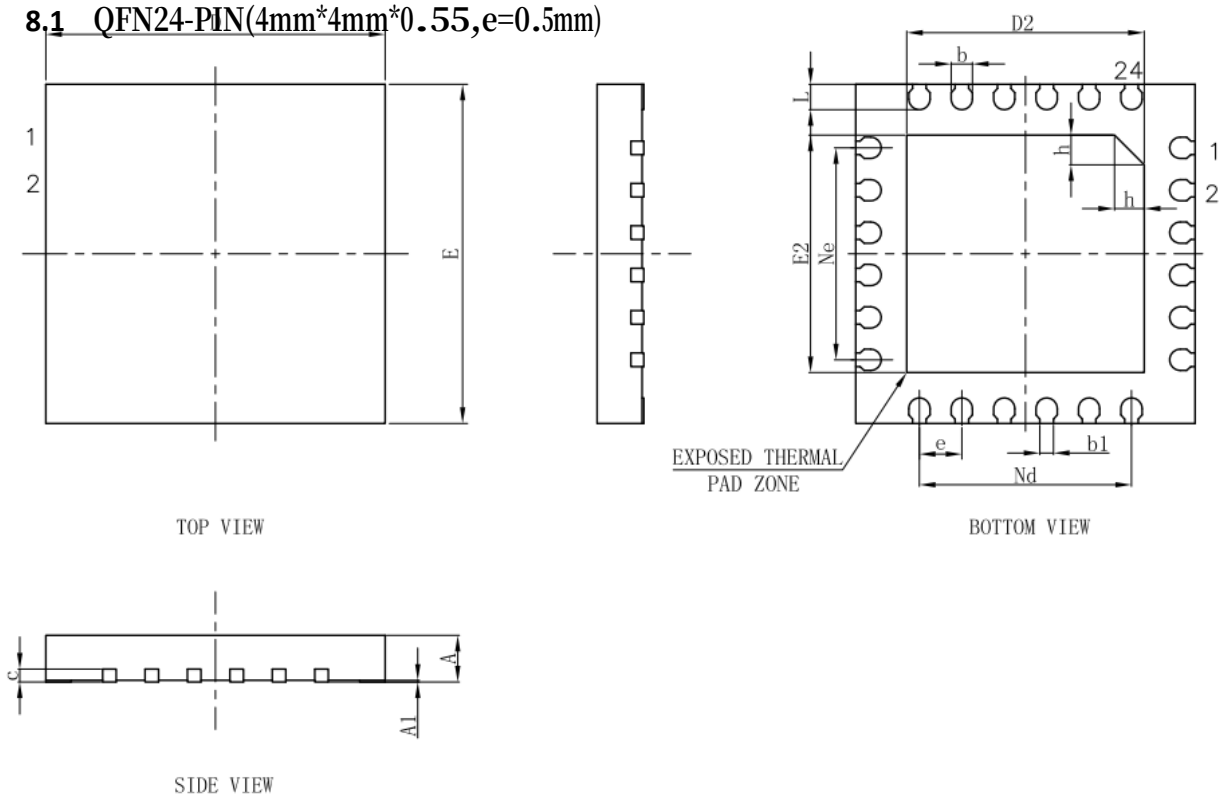

Figure 8-1

Table 8-1

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.35	0.40	0.45
h	0.30	0.35	0.40

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8.2 QFN32(5mm*5mm*0.75mm,e=0.5mm)

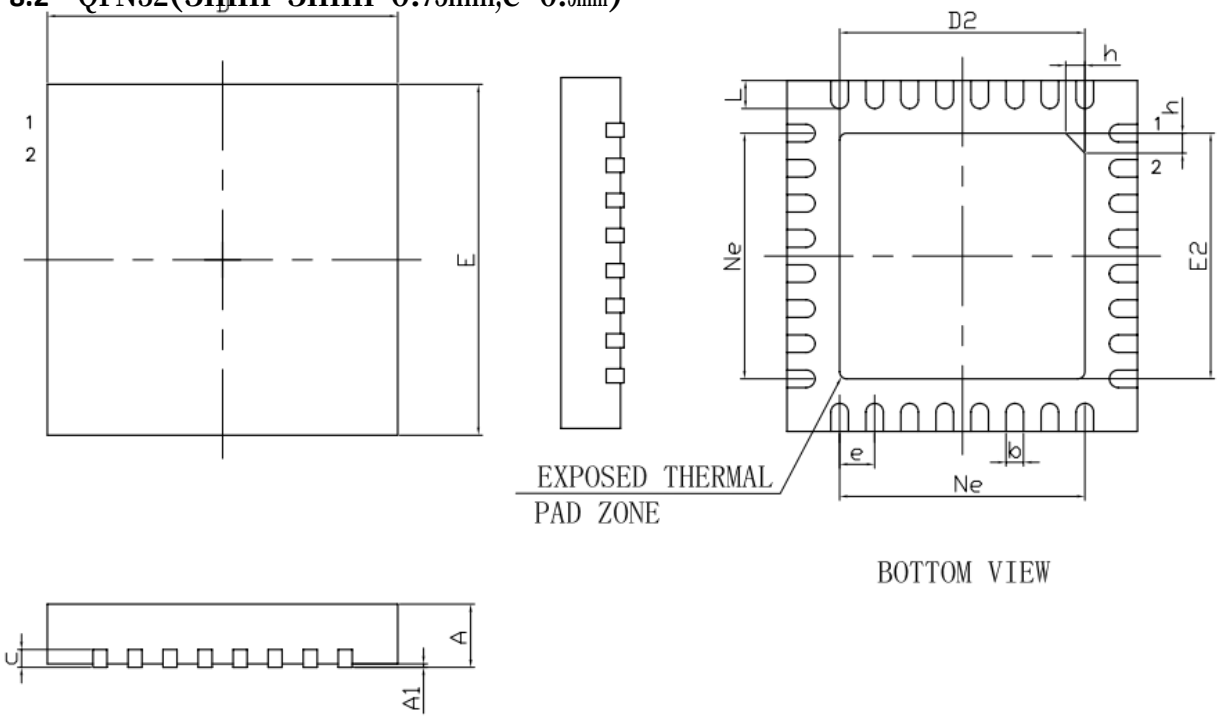

Figure 8-2

Table 8-2

SYMBOLS	MIN	NOR	MAX
	(mm)		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1		0.16REF	
c	0.15	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e		0.50BSC	
Ne		3.50BSC	
Nd		3.50BSC	
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.25	0.30	0.35
h	0.30	0.35	0.40

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9 Product naming rules

9.1 Product Model Description

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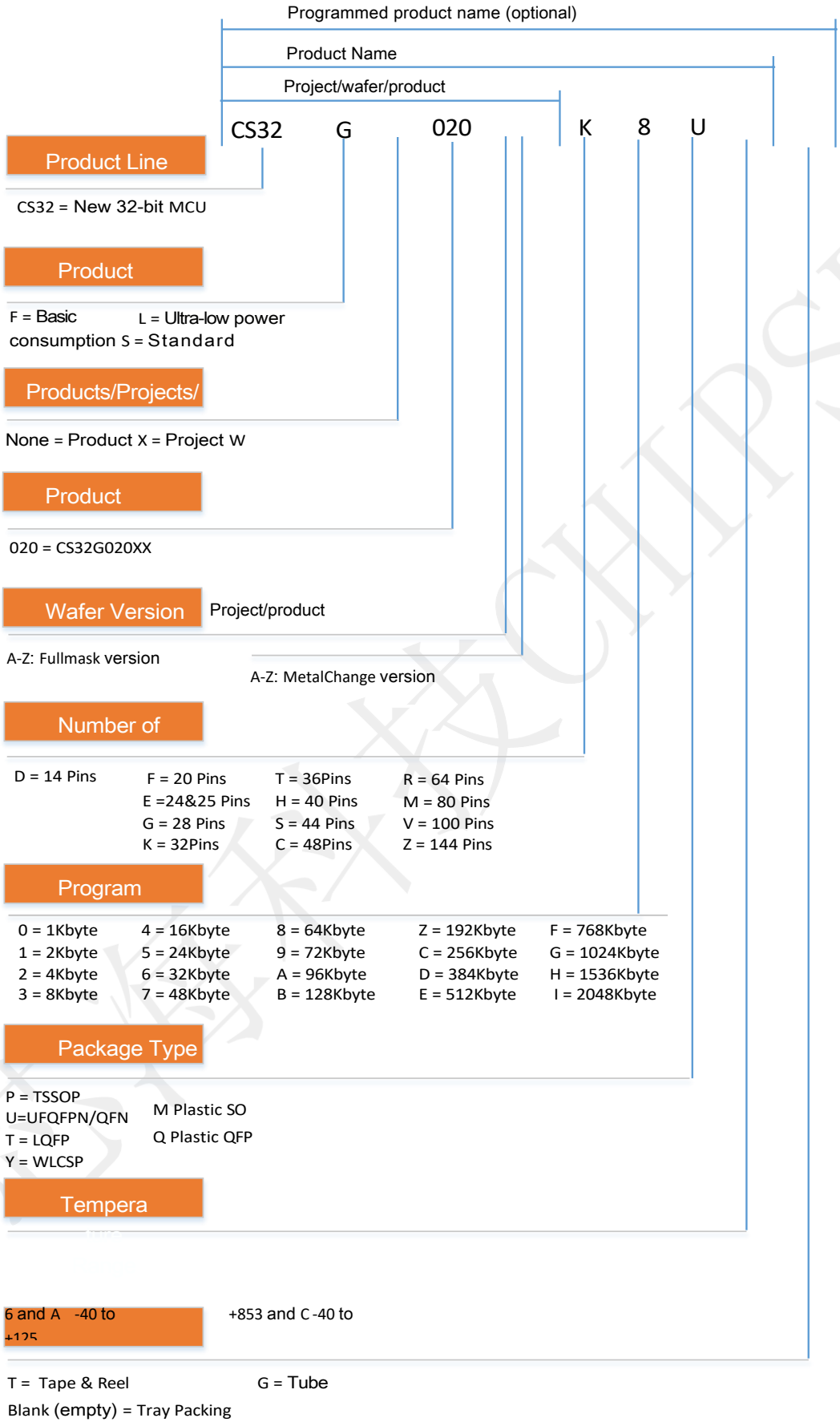

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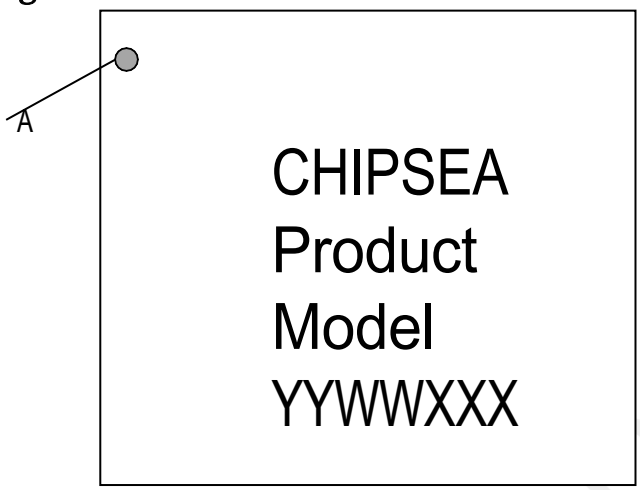
9.2 Product printing instructions



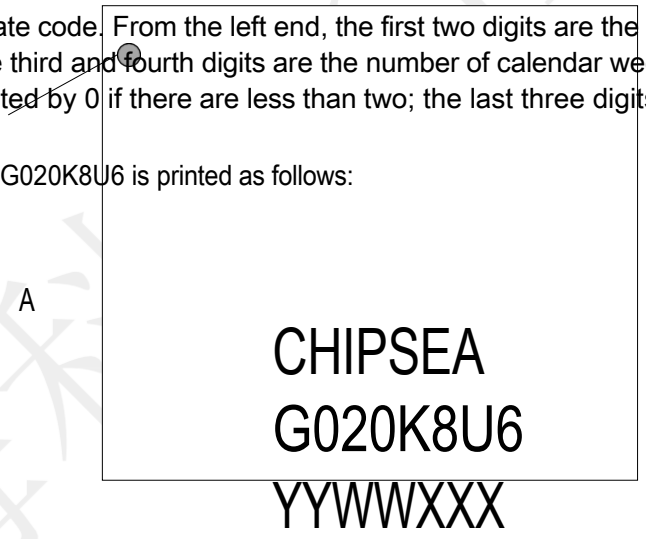
The front side of the chip is generally printed with 3 lines:

The first line is the company name, CHIPSEA.

The second line is the product model number. For some small size packages, the product model number will be reduced.

The third line is the date code. From the left end, the first two digits are the last two digits of the calendar year number; the third and fourth digits are the number of calendar weeks in the year, and the left end is complemented by 0 if there are less than two; the last three digits are the product random number.

For example, the CS32G020K8U6 is printed as follows:



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10 Ordering Information

Table 10-1

Product Model	Package	Environmental RoHS	Operating temperature	Packaging
CS32G020K8U6	QFN32	Yes	-40 ºC ~85 ºC	Pallet mounted
CS32G020E8U6	QFN24	Yes	-40 ºC ~85 ºC	Pallet mounted

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