Projeto Multiplicador

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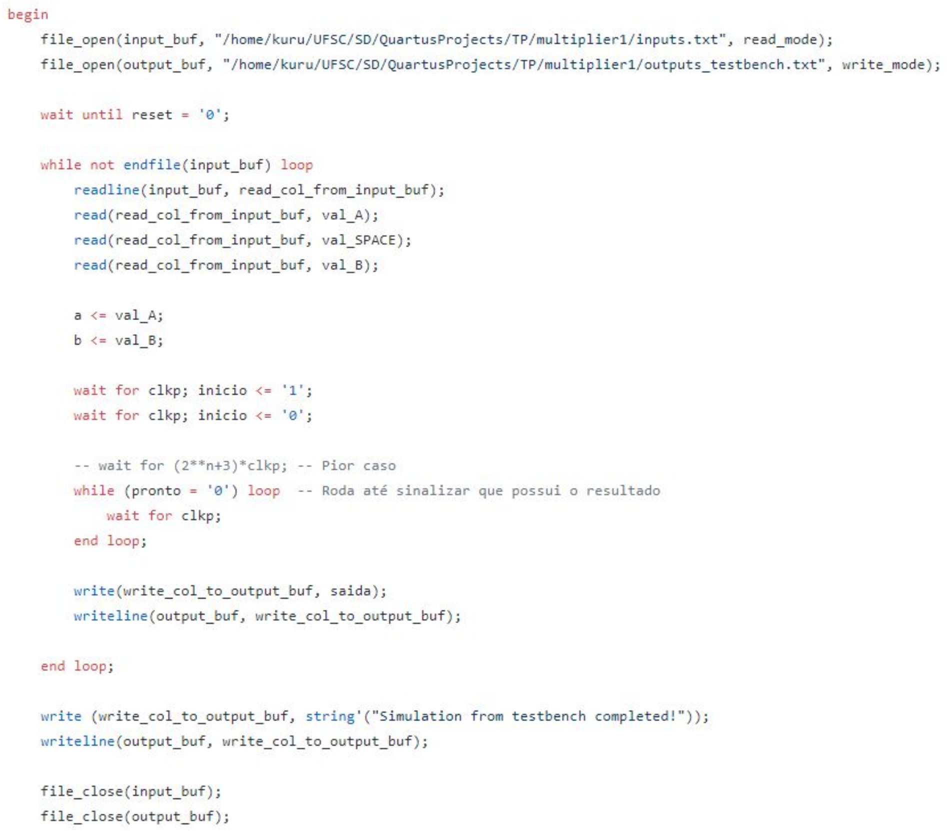
Projeto 1: Multiplicador por Somas Consecutivas

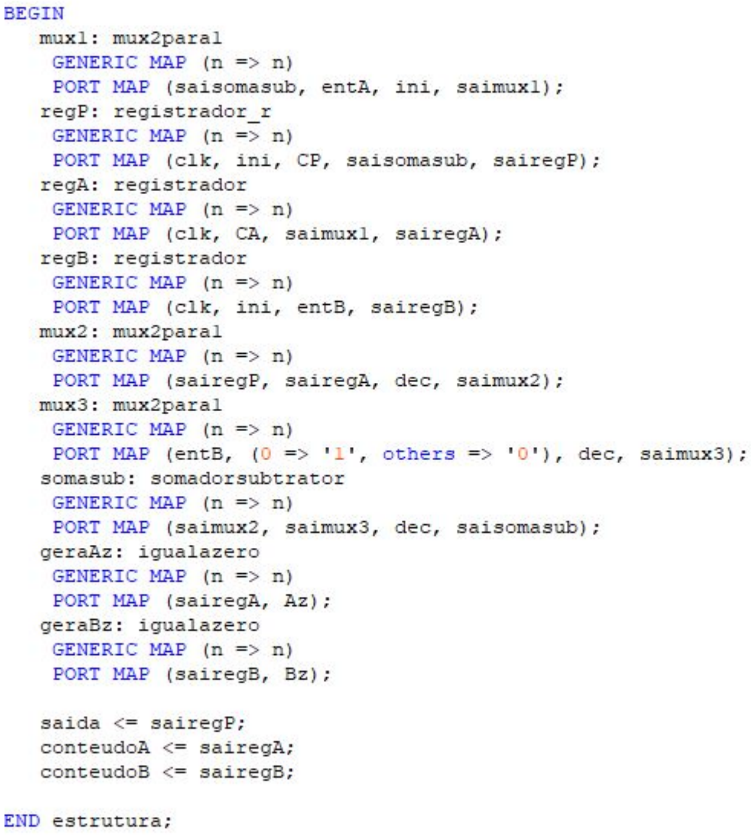


```
begin
    file_open(input_buf, "/home/kuru/UFSC/SD/QuartusProjects/TP/multiplier1/inputs.txt", read_mode);
    file_open(output_buf, "/home/kuru/UFSC/SD/QuartusProjects/TP/multiplier1/outputs_testbench.txt", write_mode);

    wait until reset = '0';

    while not endfile(input_buf) loop
        readline(input_buf, read_col_from_input_buf);
        read(read_col_from_input_buf, val_A);
        read(read_col_from_input_buf, val_SPACE);
        read(read_col_from_input_buf, val_B);

        a <= val_A;
        b <= val_B;

        wait for clkp; inicio <= '1';
        wait for clkp; inicio <= '0';

        -- wait for (2**n+3)*clkp; -- Pior caso
        while (pronto = '0') loop  -- Roda até sinalizar que possui o resultado
            wait for clkp;
        end loop;

        write(write_col_to_output_buf, saida);
        writeline(output_buf, write_col_to_output_buf);

    end loop;

    write (write_col_to_output_buf, string'("Simulation from testbench completed!"));
    writeline(output_buf, write_col_to_output_buf);

    file_close(input_buf);
    file_close(output_buf);
```

VHDs: Persistência de dados, para realização do testbench.

multiplier_tb.vhd

Projeto 1: Multiplicador por Somas Consecutivas

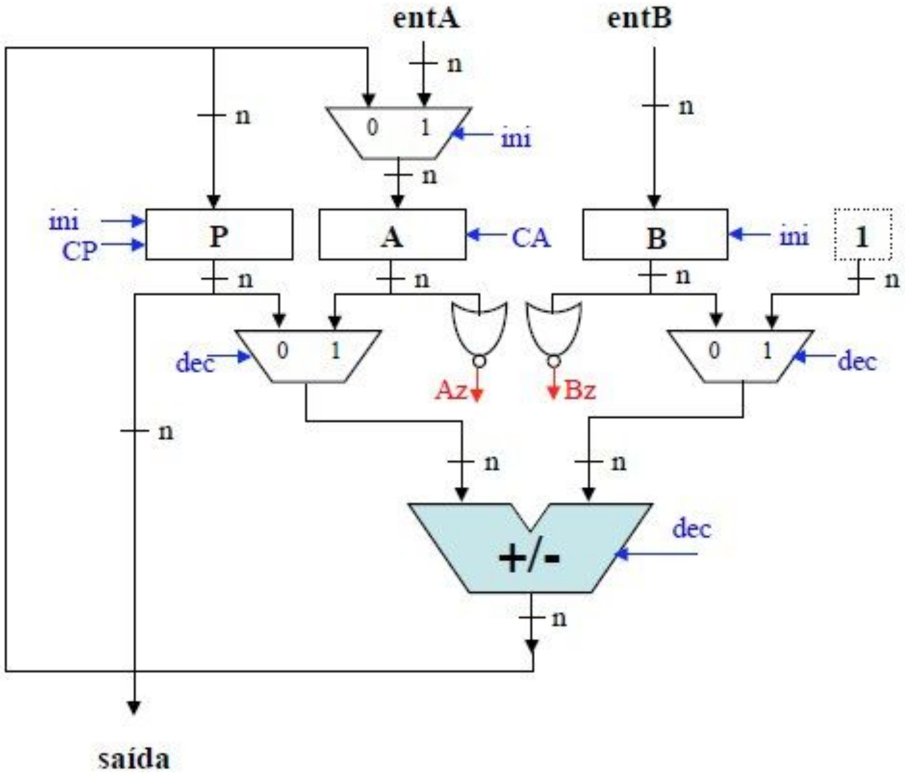


```
BEGIN
   mux1: mux2paral
    GENERIC MAP (n => n)
    PORT MAP (saisomasub, entA, ini, saimux1);
   regP: registrador_r
    GENERIC MAP (n => n)
    PORT MAP (clk, ini, CP, saisomasub, sairegP);
   regA: registrador
    GENERIC MAP (n => n)
    PORT MAP (clk, CA, saimux1, sairegA);
   regB: registrador
    GENERIC MAP (n => n)
    PORT MAP (clk, ini, entB, sairegB);
   mux2: mux2paral
    GENERIC MAP (n => n)
    PORT MAP (sairegP, sairegA, dec, saimux2);
   mux3: mux2paral
    GENERIC MAP (n => n)
    PORT MAP (entB, (0 => '1', others => '0'), dec, saimux3);
   somasub: somadorsubtrator
    GENERIC MAP (n => n)
    PORT MAP (saimux2, saimux3, dec, saisomasub);
   geraAz: igualazero
    GENERIC MAP (n => n)
    PORT MAP (sairegA, Az);
   geraBz: igualazero
    GENERIC MAP (n => n)
    PORT MAP (sairegB, Bz);

   saida <= sairegP;
   conteudoA <= sairegA;
   conteudoB <= sairegB;

END estrutura;
```

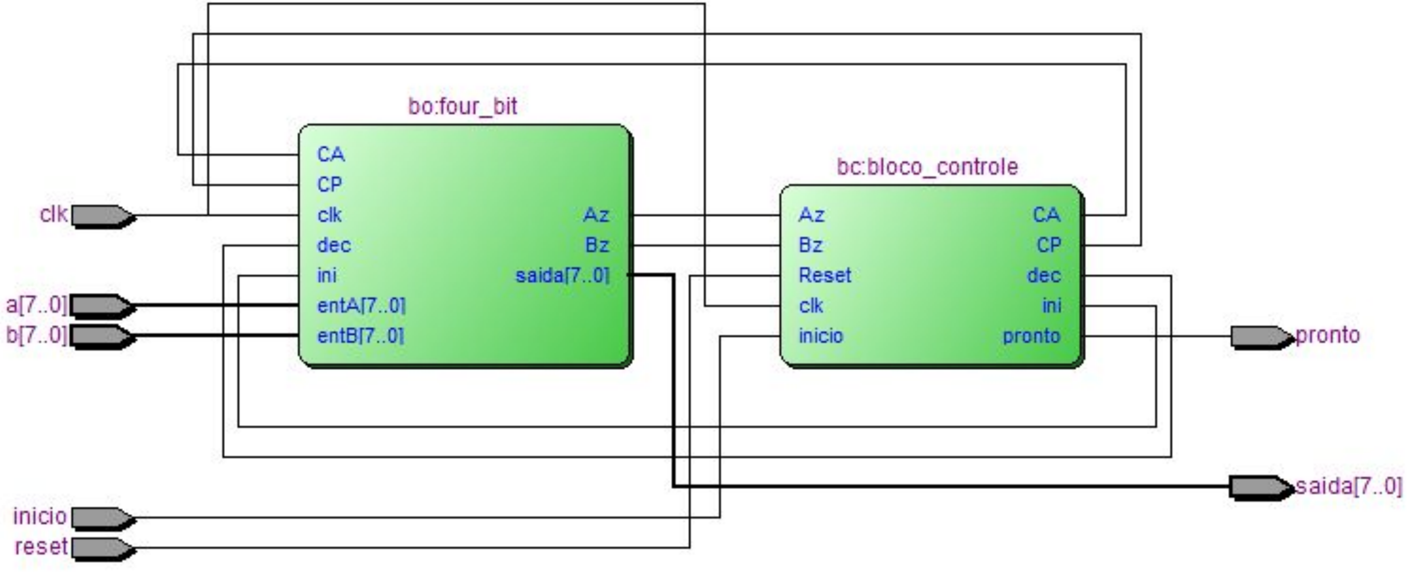
VHDs: BO(Bloco Operativo).

bo.vhd

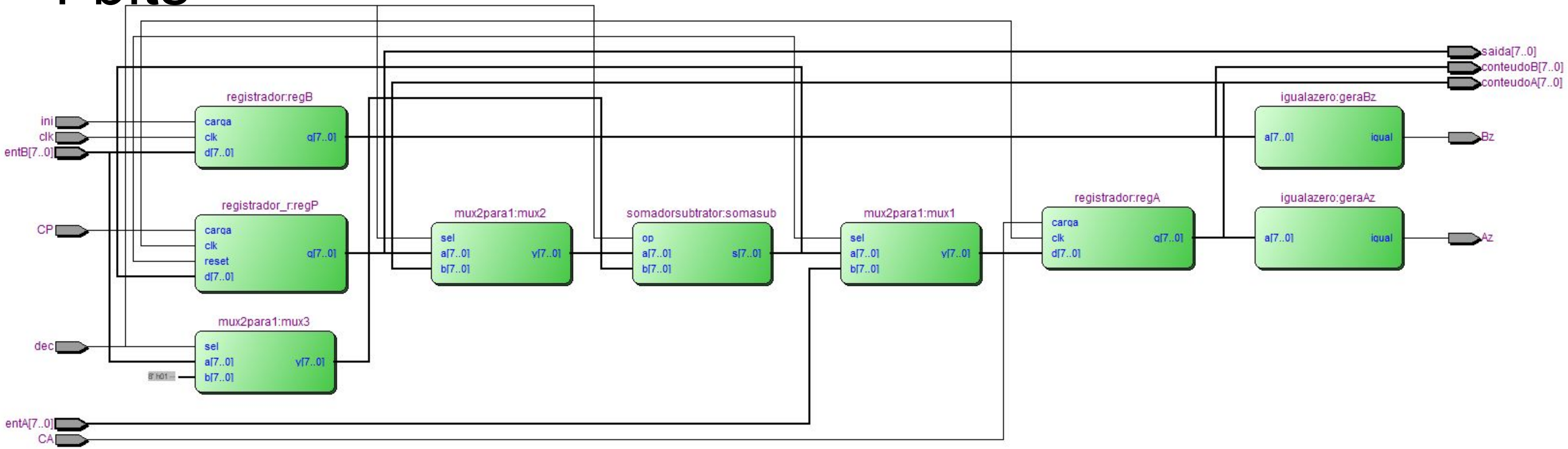
Projeto 1: Multiplicador por Somas Consecutivas



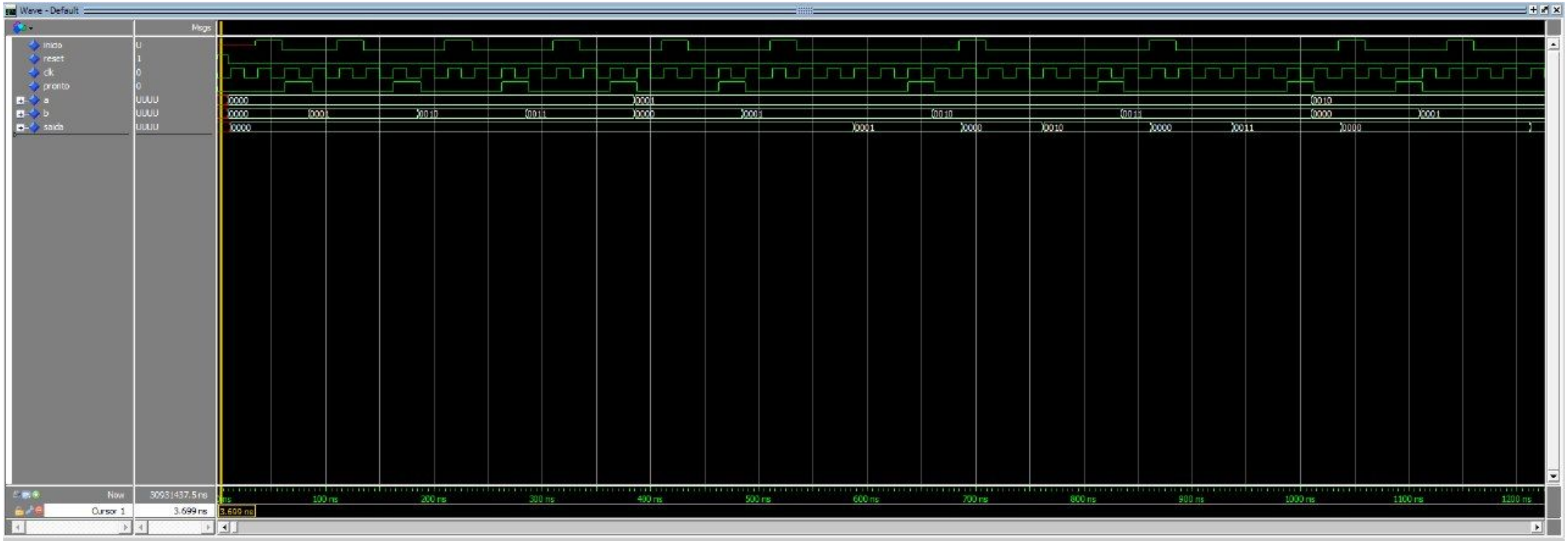
Projeto 1: Multiplicador por Somas Consecutivas 4 bits



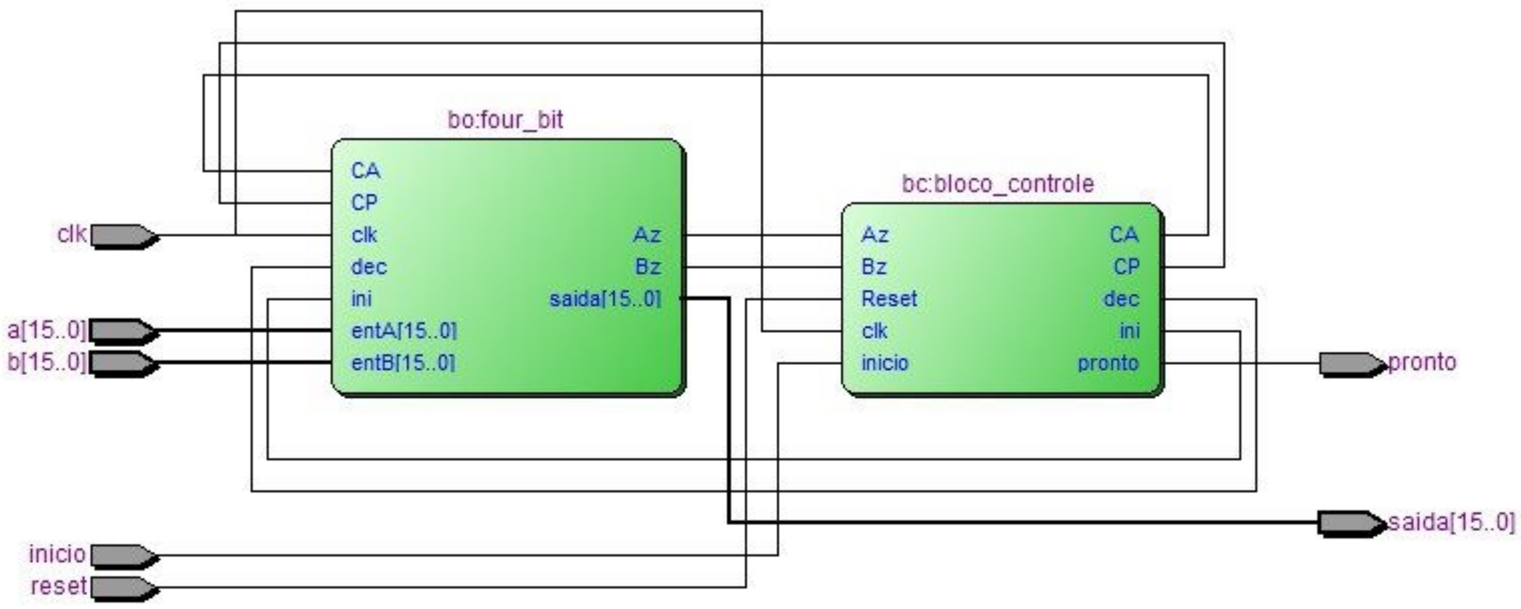
Projeto 1: Multiplicador por Somas Consecutivas 4 bits



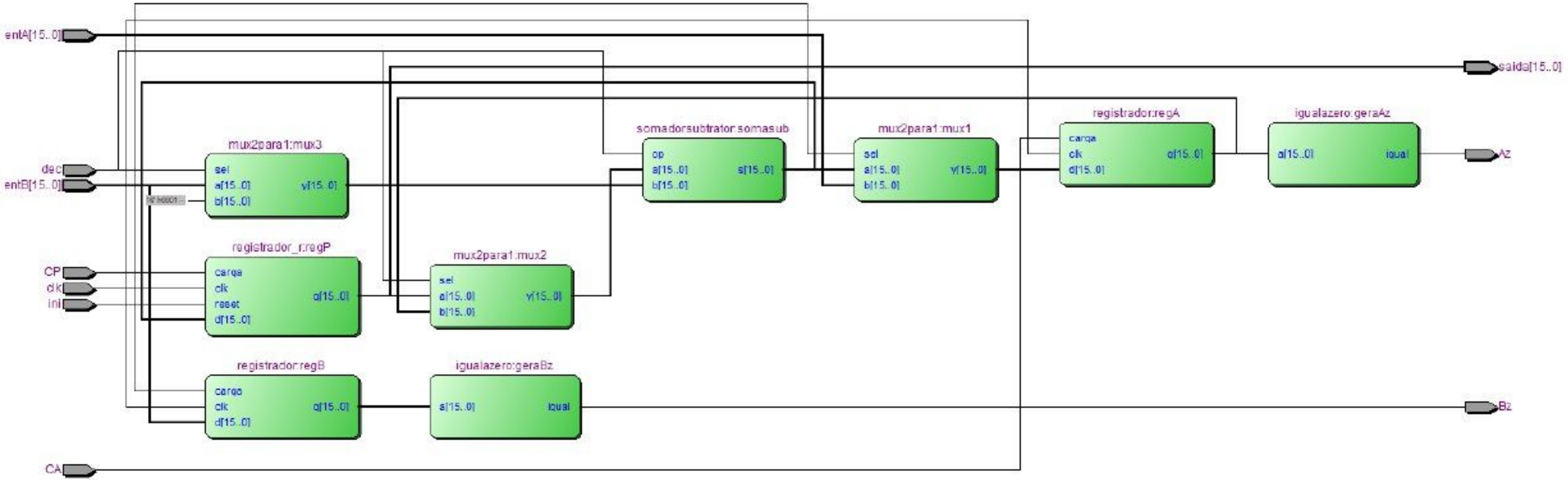
Projeto 1: Multiplicador por Somas Consecutivas 4 bits



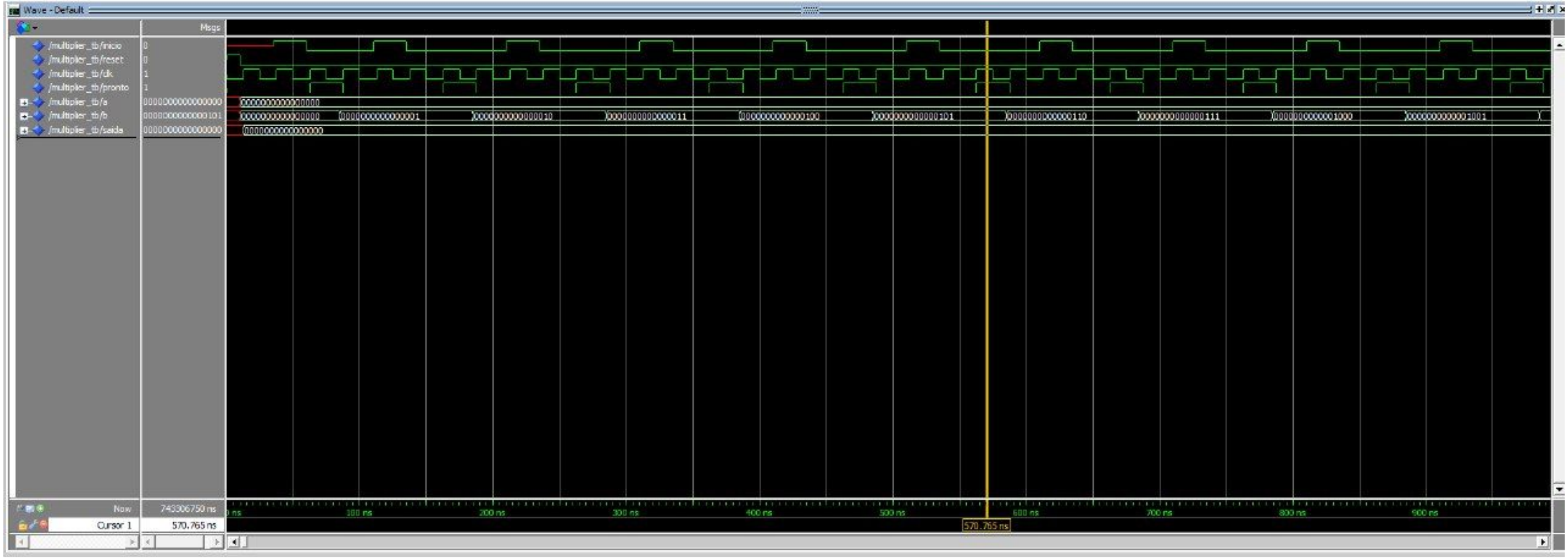
Projeto 1: Multiplicador por Somas Consecutivas 8 bits



Projeto 1: Multiplicador por Somas Consecutivas 8 bits



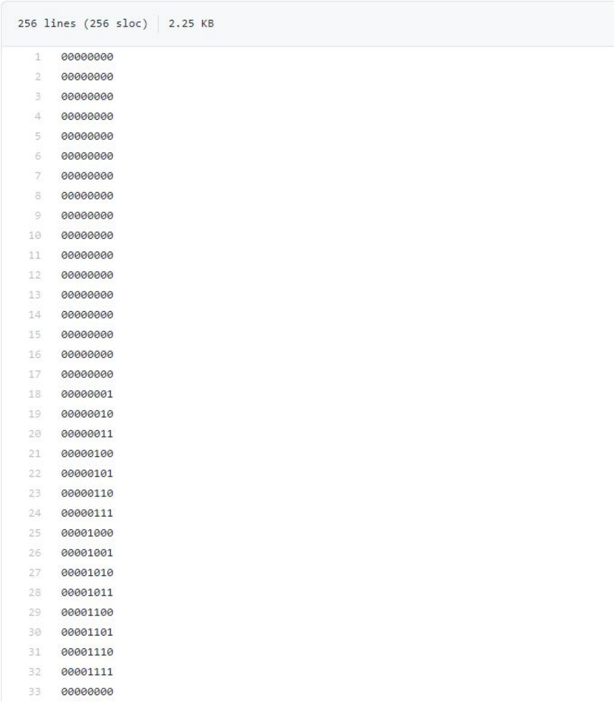
Projeto 1: Multiplicador por Somas Consecutivas 8 bits



```
Wave - Default
                          Msgs
/multiplier_tb/inicio     0
/multiplier_tb/reset      0
/multiplier_tb/clk        1
/multiplier_tb/pronto     1
/multiplier_tb/a          0000000000000000
/multiplier_tb/b          0000000000000101
/multiplier_tb/saida      0000000000000000

Now                       743306750 ns
Cursor 1                  570.765 ns
```

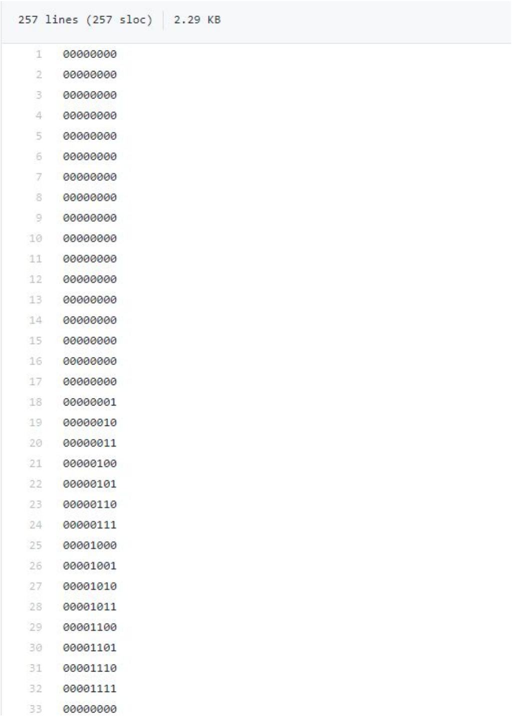
Projeto 1: Multiplicador por Somas Consecutivas

Resultados de Validação:



256 lines (256 sloc) | 2.25 KB

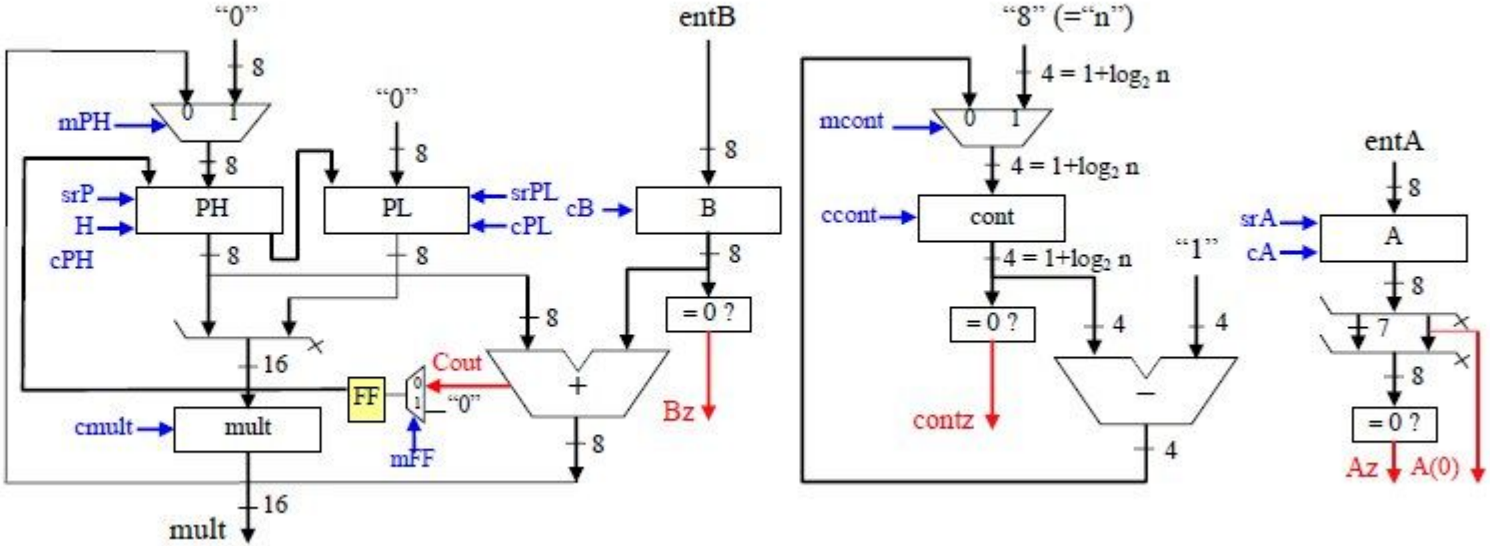
```
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000001
00000010
00000011
00000100
00000101
00000110
00000111
00001000
00001001
00001010
00001011
00001100
00001101
00001110
00001111
00000000
```



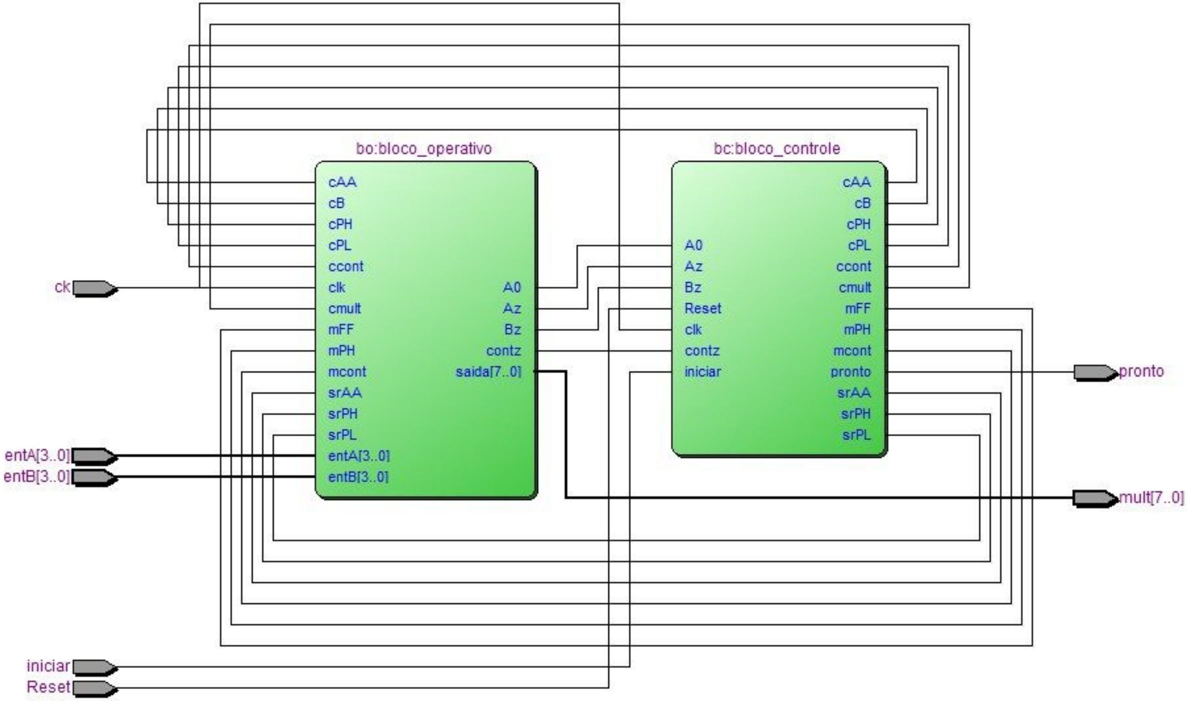
257 lines (257 sloc) | 2.29 KB

```
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000000
00000001
00000010
00000011
00000100
00000101
00000110
00000111
00001000
00001001
00001010
00001011
00001100
00001101
00001110
00001111
00000000
```

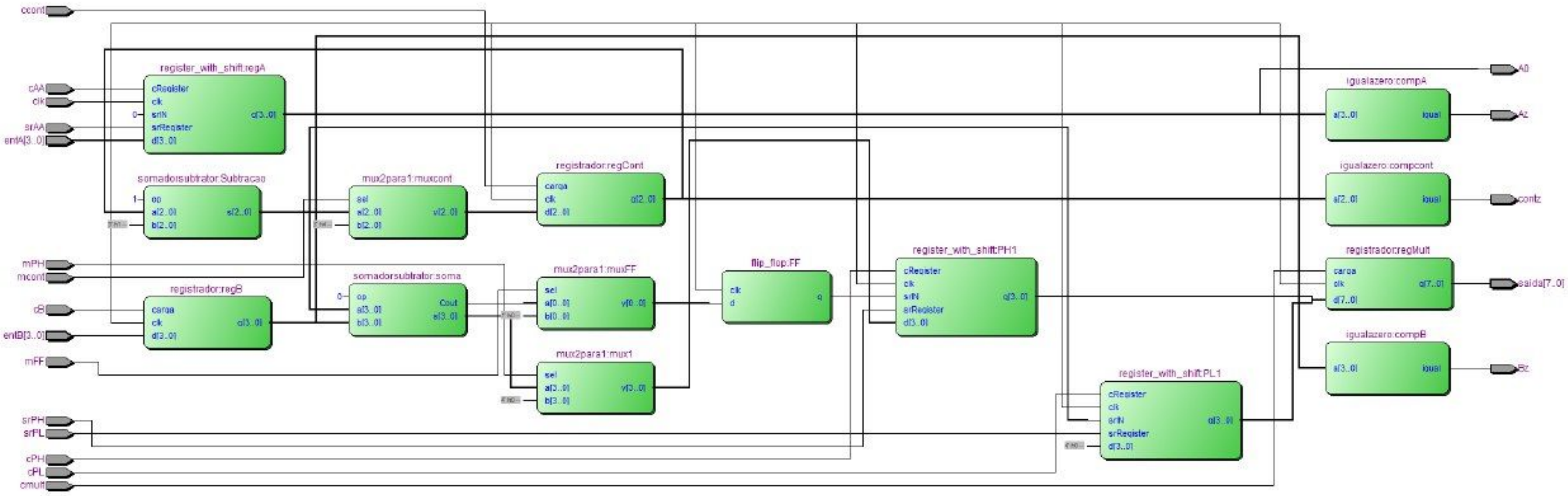
Projeto 2: Multiplicador Shifter



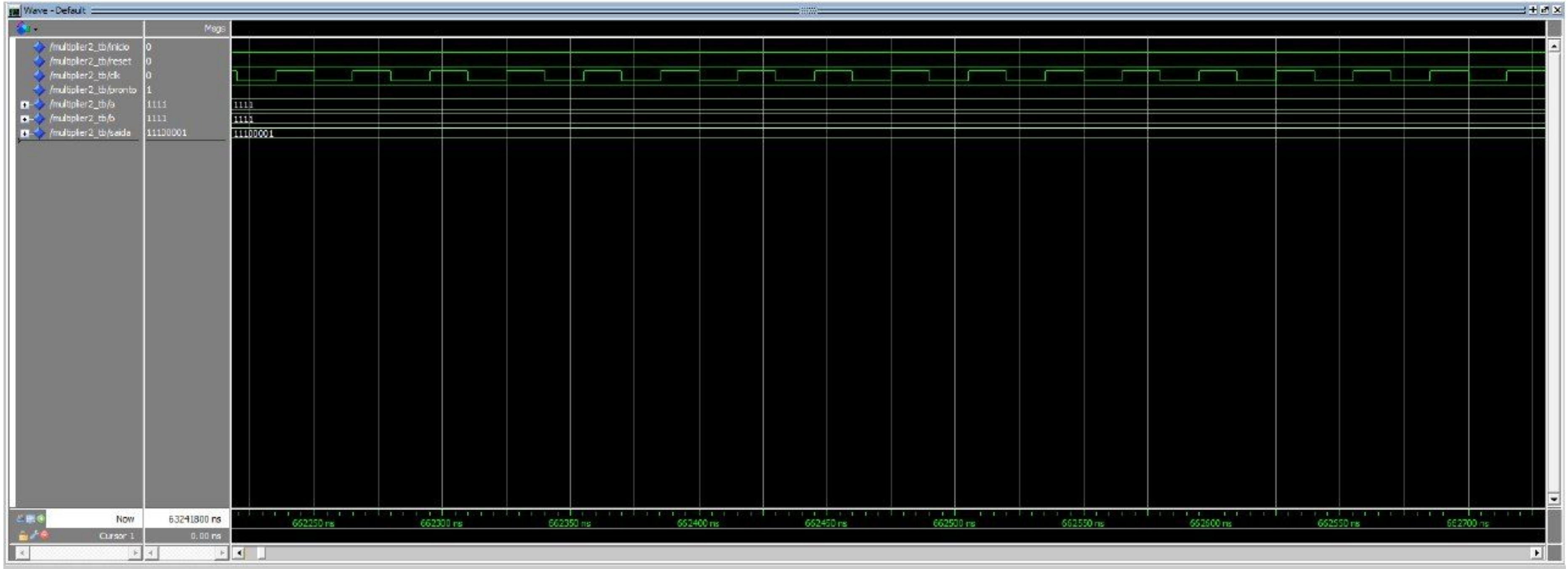
Projeto 2: Multiplicador Shifter (4 bits)



Projeto 2: Multiplicador Shifter (4 bits)



Projeto 2: Multiplicador Shifter (4 bits)

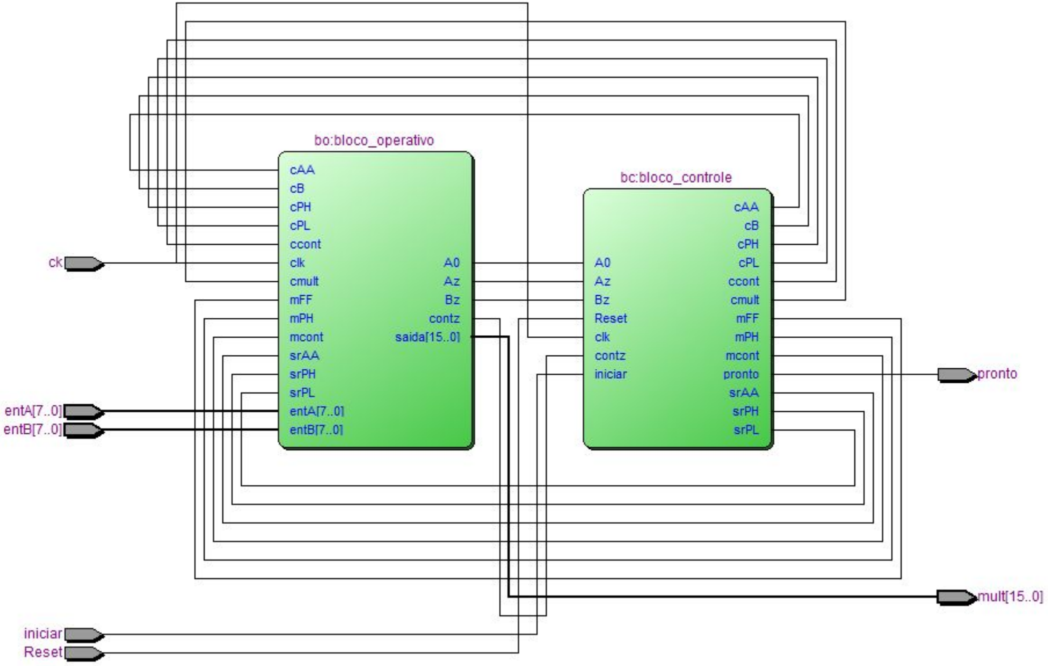


Wave - Default

	Msgs
/multiplier2_tb/inicio	0
/multiplier2_tb/reset	0
/multiplier2_tb/clk	0
/multiplier2_tb/pronto	1
/multiplier2_tb/a	1111
/multiplier2_tb/b	1111
/multiplier2_tb/saida	11100001
Now	63241800 ns
Cursor 1	0.00 ns

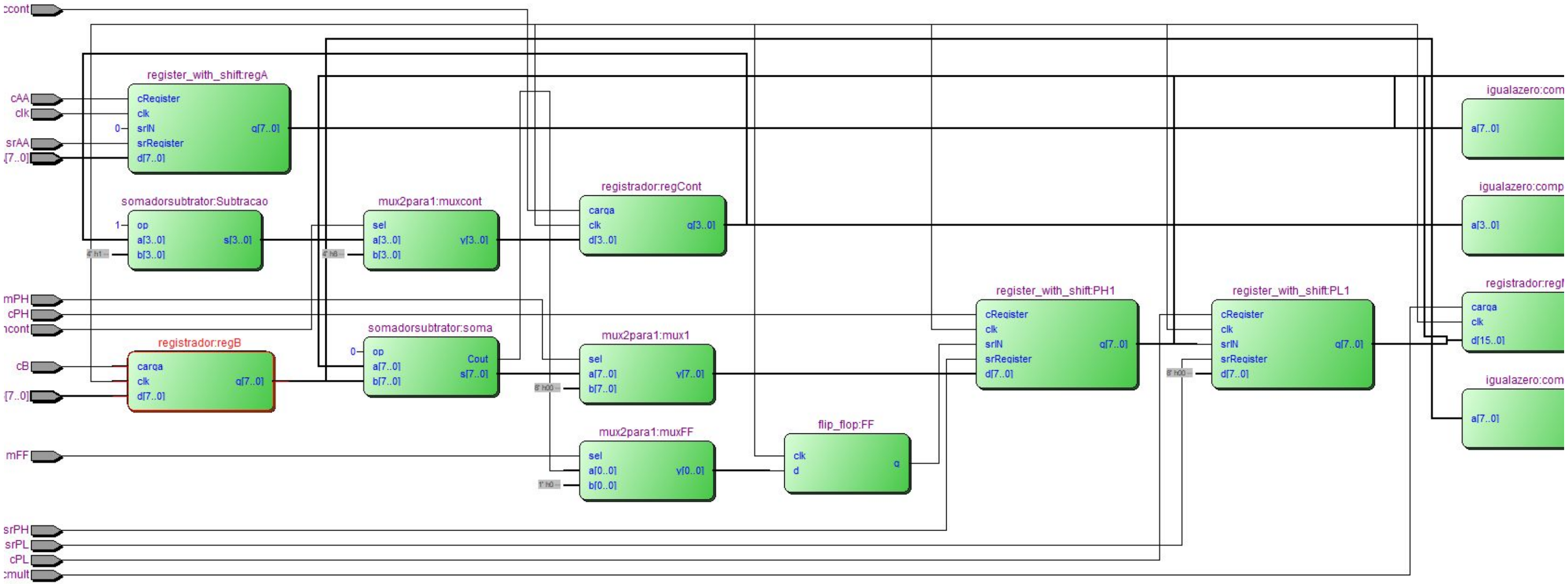
Projeto 2: Multiplicador Shifter (8 bits)

Netlists:

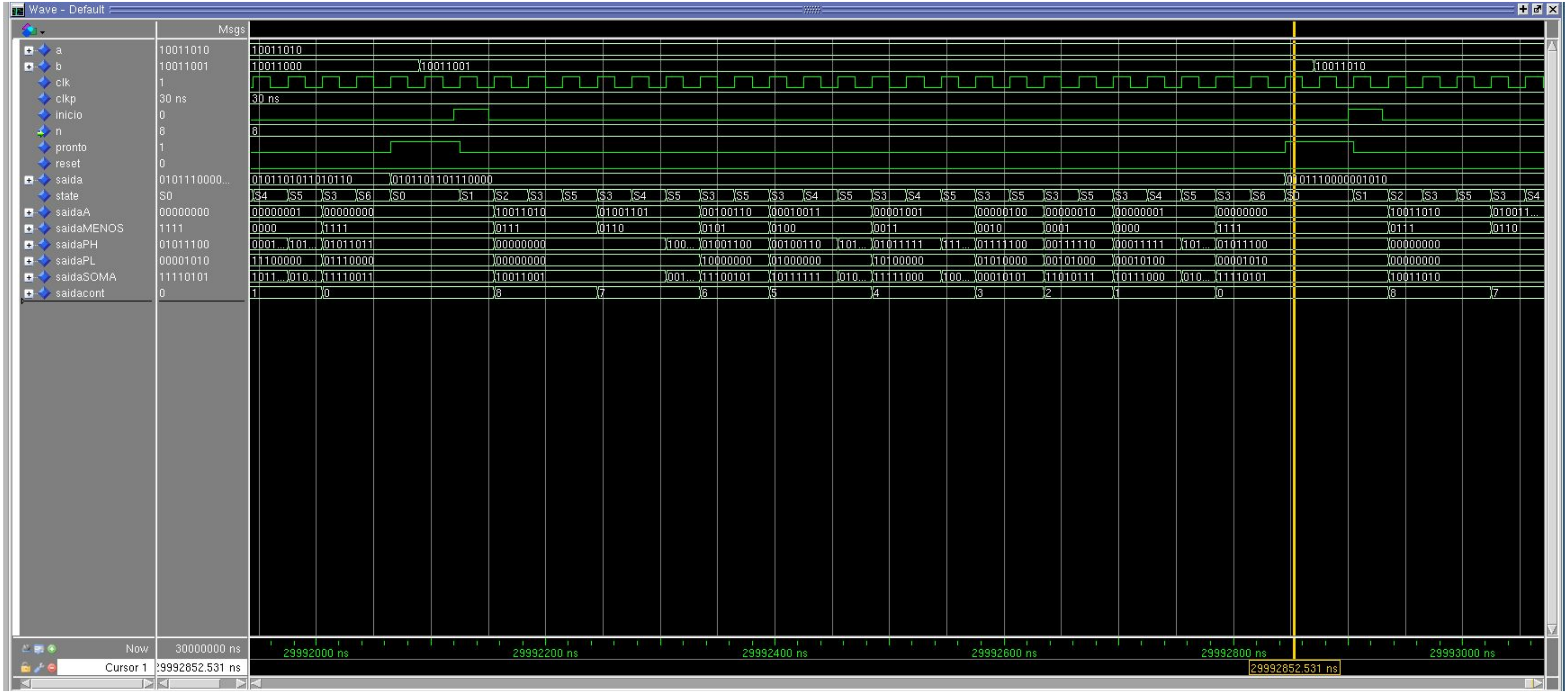


Projeto 2: Multiplicador Shifter (8 bits)

Netlists:



Projeto 2: Multiplicador Shifter (8 bits)



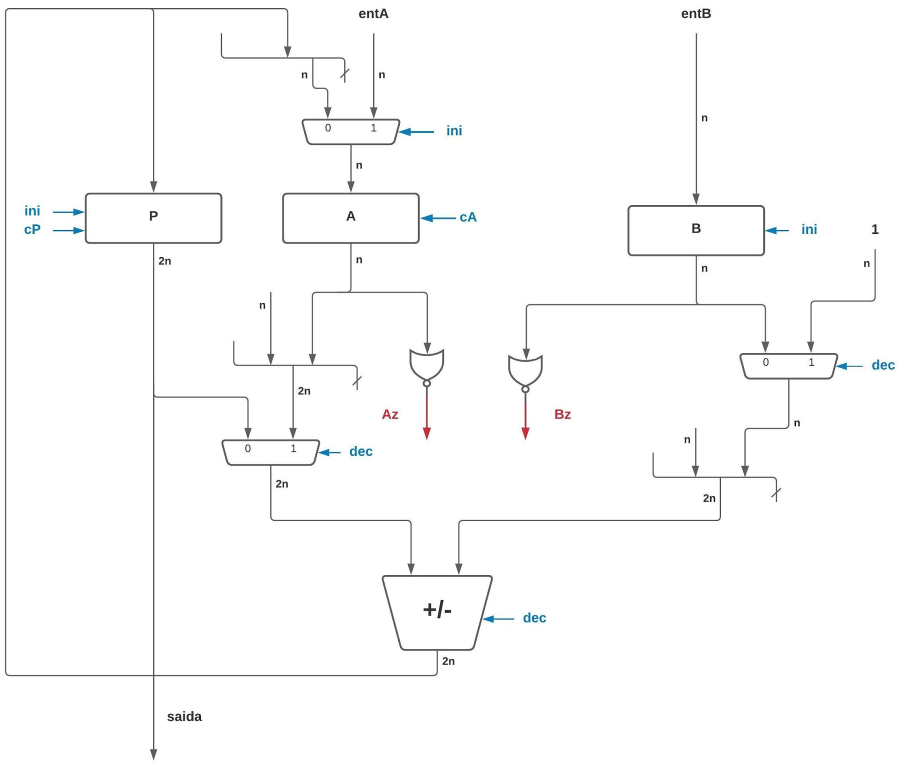
Wave - Default

	Msgs
a	10011010
b	10011001
clk	1
clkp	30 ns
inicio	0
n	8
pronto	1
reset	0
saida	0101110000...
state	S0
saidaA	00000000
saidaMENOS	1111
saidaPH	01011100
saidaPL	00001010
saidaSOMA	11110101
saidacont	0

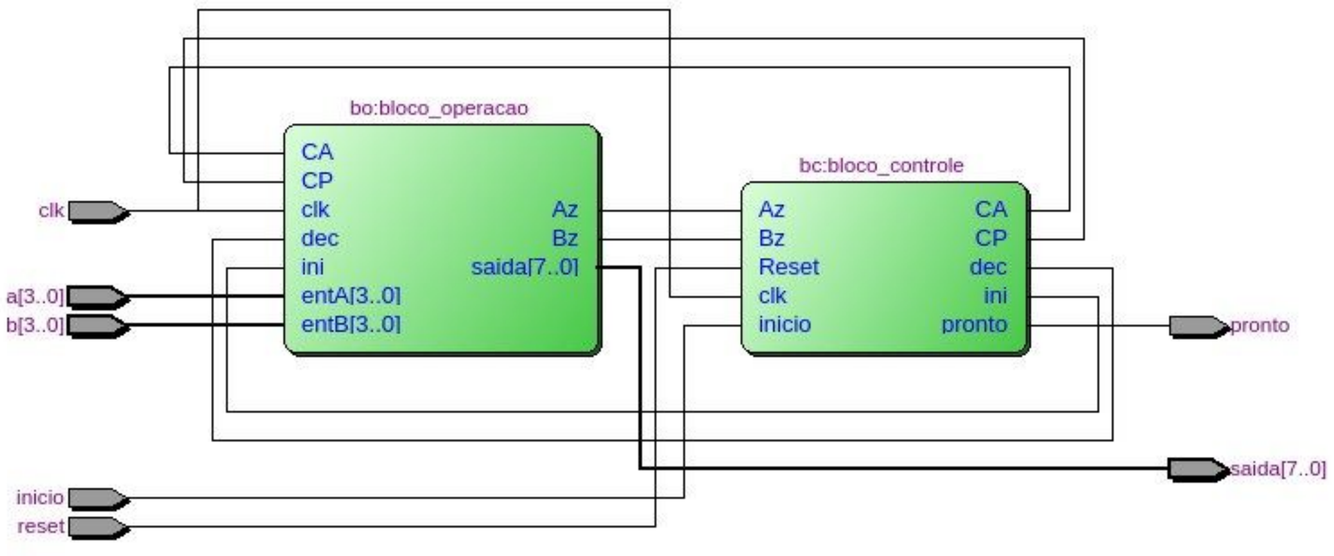
Now 30000000 ns

Cursor 1 29992852.531 ns

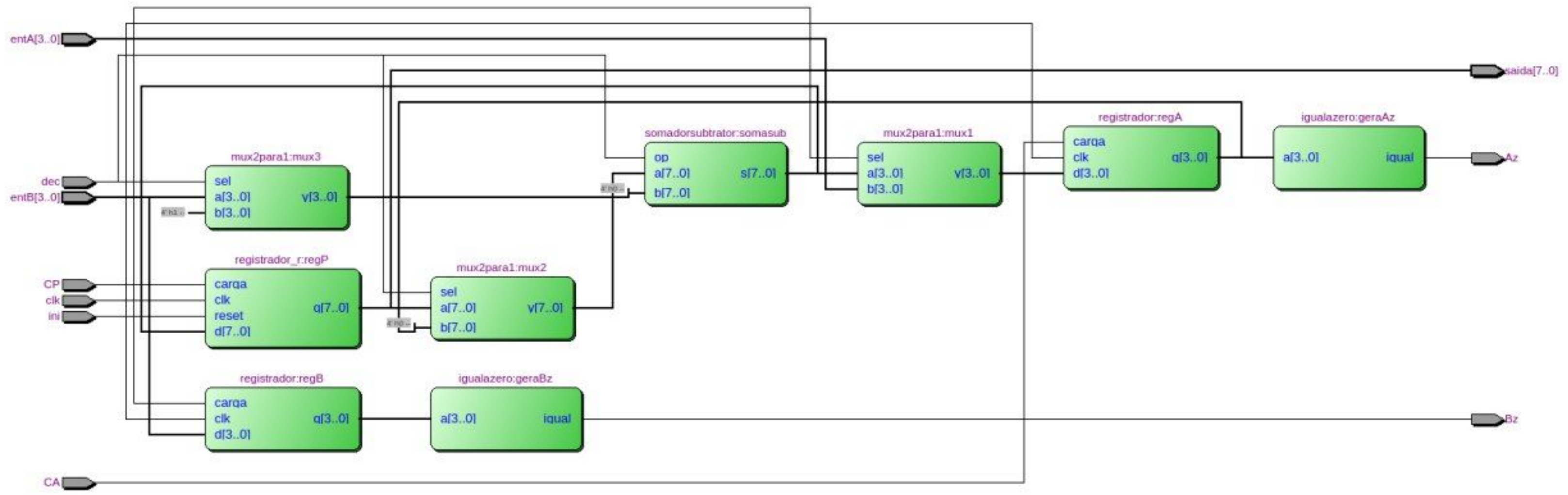
Projeto 3: Multiplicador por Somas Consecutivas Otimizado



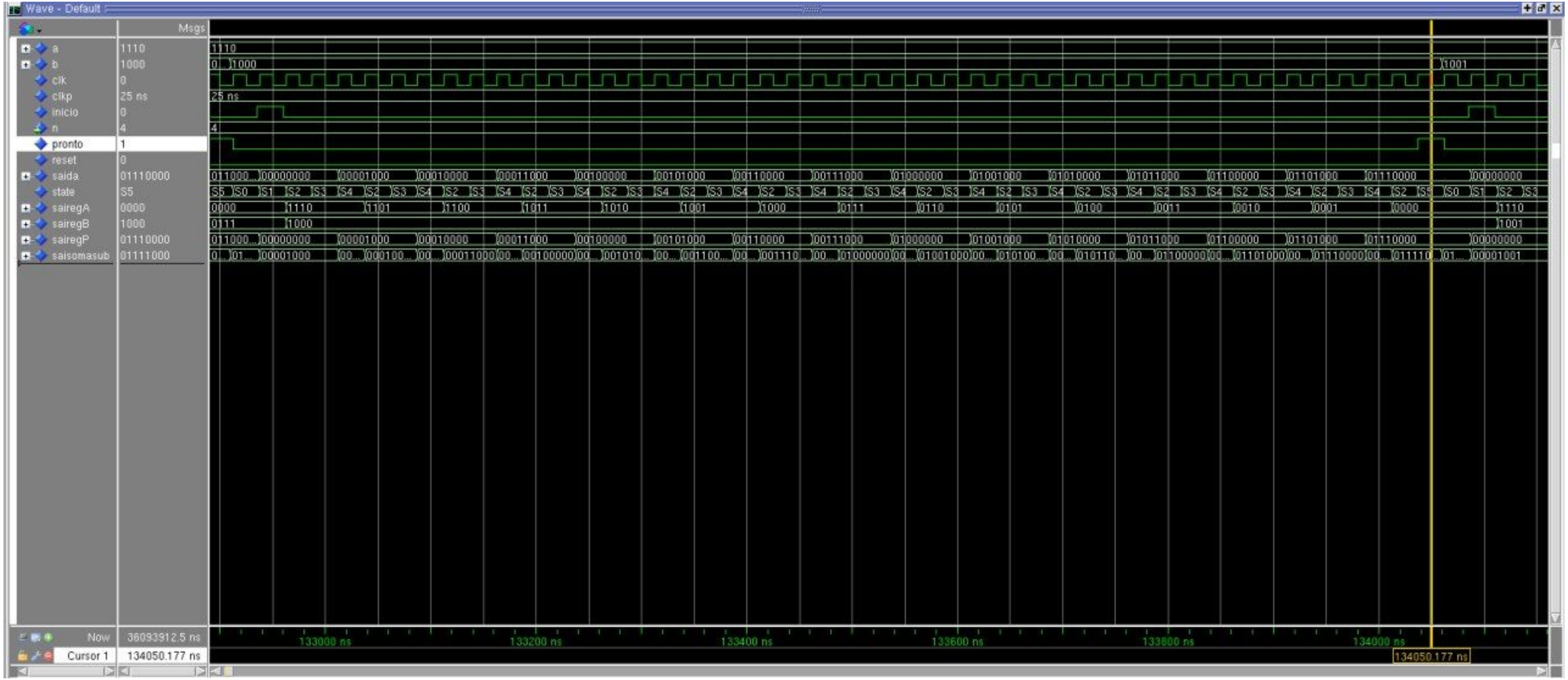
Projeto 3: Multiplicador por Somas Consecutivas Otimizado(4 bits)



Projeto 3: Multiplicador por Somas Consecutivas Otimizado(4 bits)



Projeto 3: Multiplicador por Somas Consecutivas Otimizado(4 bits)

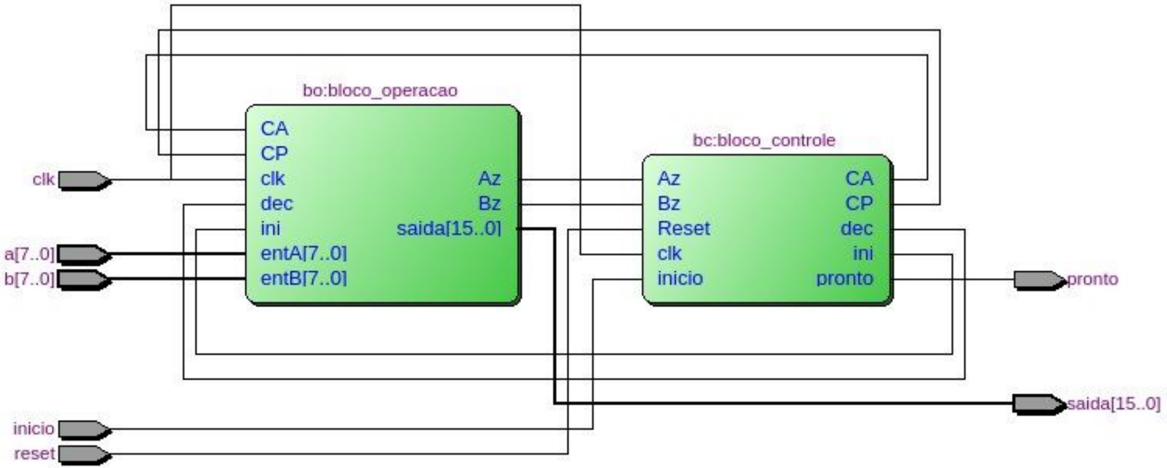


Wave - Default

	Msgs
a	1110
b	1000
clk	0
clkp	25 ns
inicio	0
n	4
pronto	1
reset	0
saida	01110000
state	S5
sairegA	0000
sairegB	1000
sairegP	01110000
saisomasub	01111000
Now	36093912.5 ns
Cursor 1	134050.177 ns

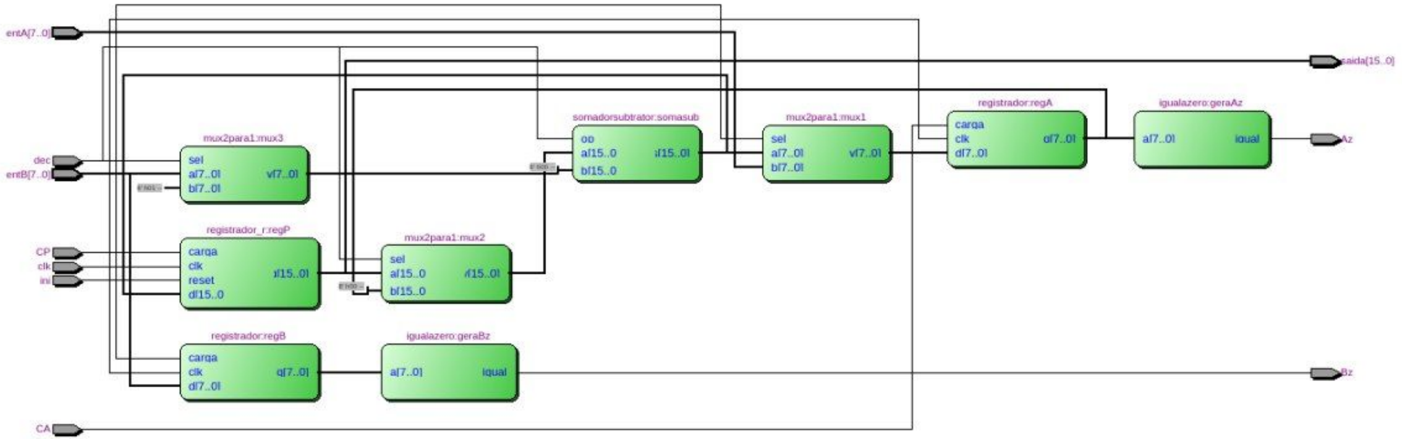
Projeto 3: Multiplicador por Somas Consecutivas Otimizado(8 bits)

Netlists:

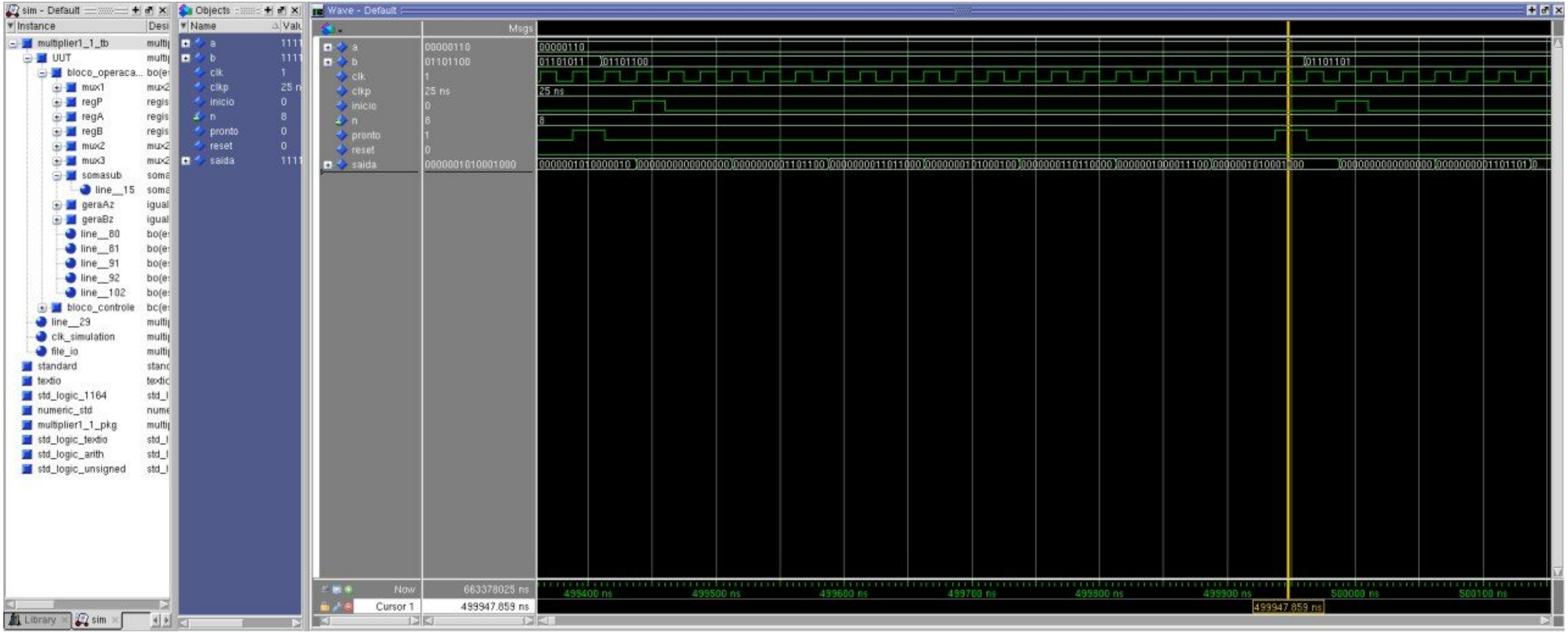


Projeto 3: Multiplicador por Somas Consecutivas Otimizado(8 bits)

Netlists:



Projeto 3: Multiplicador por Somas Consecutivas Otimizado(8 bits)



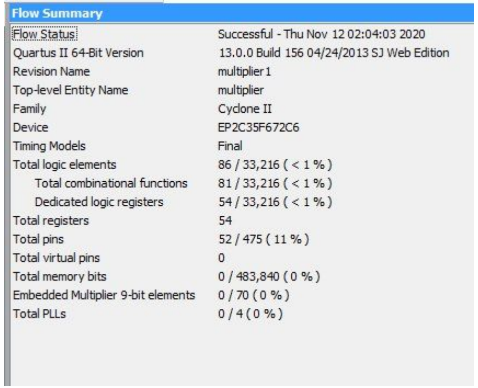
```
Instance               Desi
multiplier1_1_tb       multi
  UUT                  multi
    bloco_operaca...   bo(e:
      mux1             mux2
      regP             regis
      regA             regis
      regB             regis
      mux2             mux2
      mux3             mux2
      somasub          soma
        line__15       soma
      geraAz           igual
      geraBz           igual
      line__80         bo(e:
      line__81         bo(e:
      line__91         bo(e:
      line__92         bo(e:
      line__102        bo(e:
    bloco_controle     bc(e:
  line__29             multi
  clk_simulation       multi
  file_io              multi
standard               stand
textio                 textio
std_logic_1164         std_l
numeric_std            nume
multiplier1_1_pkg      multi
std_logic_textio       std_l
std_logic_arith        std_l
std_logic_unsigned     std_l
```

```
Name       Valu
a          1111
b          1111
clk        1
clkp       25 n
inicio     0
n          8
pronto     0
reset      0
saida      1111
```

```
a        00000110           00000110
b        01101100           01101011 )01101100                                    )01101101
clk      1
clkp     25 ns              25 ns
inicio   0
n        8                  8
pronto   1
reset    0
saida    0000001010001000   0000001010000010 )0000000000000000 )0000000001101100 )0000000011011000 )0000000101000100 )0000000110110000 )0000001000011100 )0000001010001000   )0000000000000000 )0000000001101101 )0...

Now       663378025 ns      499400 ns   499500 ns   499600 ns   499700 ns   499800 ns   499900 ns   500000 ns   500100 ns
Cursor 1  499947.859 ns                                                          499947.859 ns
```

Comparativos(8 bits):

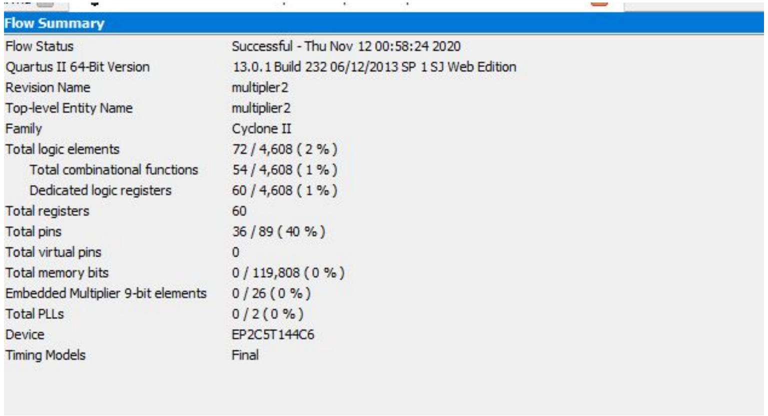
Numero 1:



Flow Summary

Flow Status	Successful - Thu Nov 12 02:04:03 2020
Quartus II 64-Bit Version	13.0.0 Build 156 04/24/2013 SJ Web Edition
Revision Name	multiplier1
Top-level Entity Name	multiplier
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	86 / 33,216 (< 1 %)
Total combinational functions	81 / 33,216 (< 1 %)
Dedicated logic registers	54 / 33,216 (< 1 %)
Total registers	54
Total pins	52 / 475 (11 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

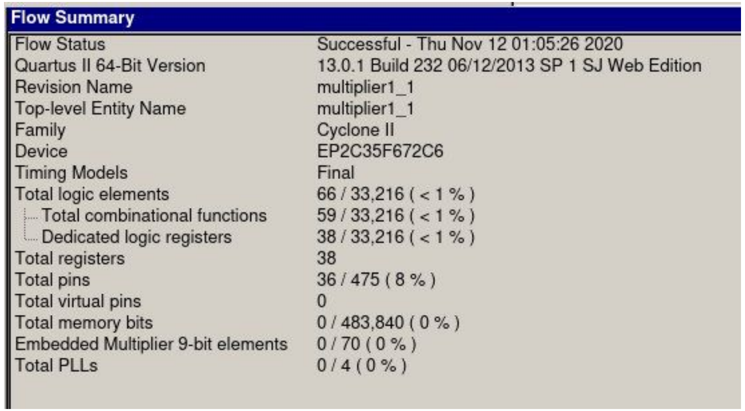
Numero 2:



Flow Summary

Flow Status	Successful - Thu Nov 12 00:58:24 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multipler2
Top-level Entity Name	multipler2
Family	Cyclone II
Total logic elements	72 / 4,608 (2 %)
Total combinational functions	54 / 4,608 (1 %)
Dedicated logic registers	60 / 4,608 (1 %)
Total registers	60
Total pins	36 / 89 (40 %)
Total virtual pins	0
Total memory bits	0 / 119,808 (0 %)
Embedded Multiplier 9-bit elements	0 / 26 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP2C5T144C6
Timing Models	Final

Numero 3:



Flow Summary

Flow Status	Successful - Thu Nov 12 01:05:26 2020
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	multiplier1_1
Top-level Entity Name	multiplier1_1
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	66 / 33,216 (< 1 %)
Total combinational functions	59 / 33,216 (< 1 %)
Dedicated logic registers	38 / 33,216 (< 1 %)
Total registers	38
Total pins	36 / 475 (8 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)