60 GHz DEMONSTRATOR

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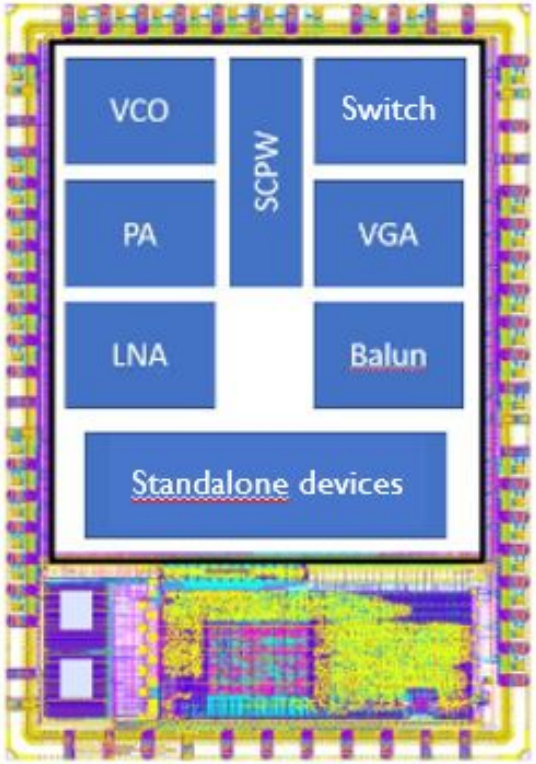
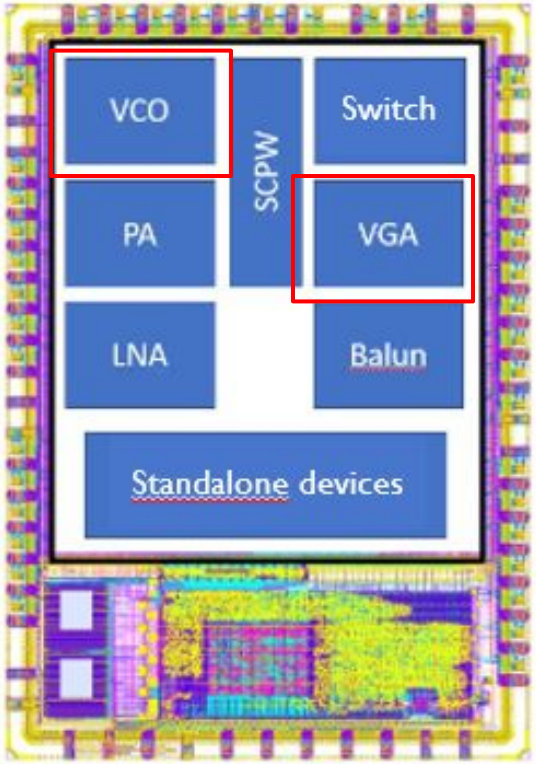
MOTIVATION

- We don't intend to design cutting-edge, state-of-the-art mmW circuits here, but instead we want to fulfill two goals:
  - Prove that it is possible to design mmW circuits in an open-source environment
  - Help the community by developing a (rough) OS RFIC design flow
- To this end, we propose submitting some of the necessary building blocks of any transceiver, turning the Caravel user area into a mini MPW:
  - Amplifiers: PA, LNA, VGA
  - Oscillator: VCO
  - RF switch
  - Balun and slow-wave line for impedance matching and low-loss interconnections
  - Standalone, diceable test circuits for RF MOSFET and Cascode



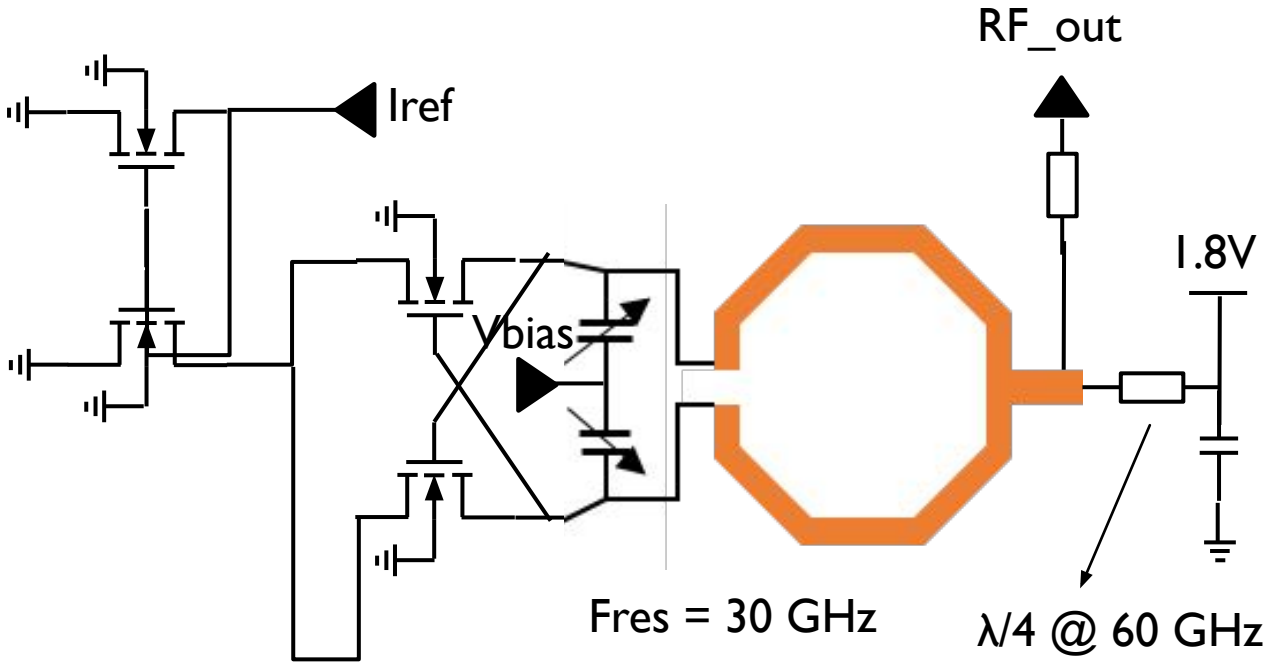
MOTIVATION

- A VCO is one of the most important building blocks for a RF transmission system, and is a good testbench for the quality of passive devices and of the active devices (MOSFETs)
- A VGA is very useful in a RF front-end to avoid saturation of the stages behind the LNA and to suppress sidelobes in beam-steering antenna arrays



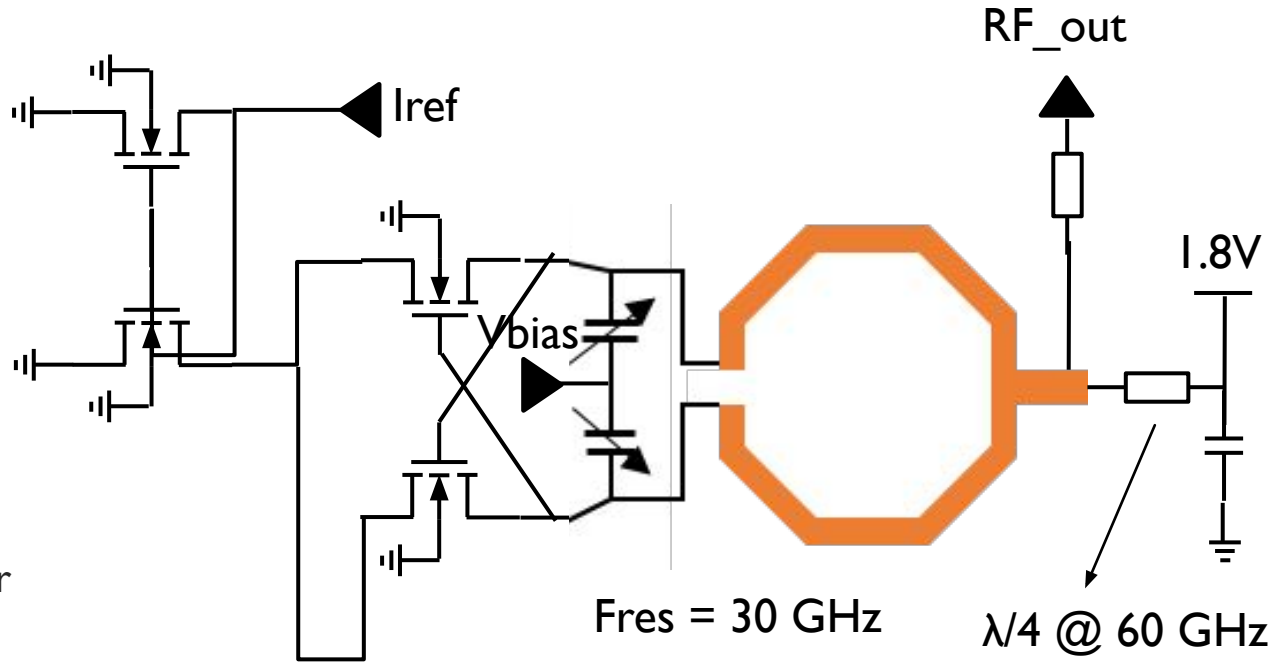
Voltage-Controlled Oscillator - VCO

- Cross-coupled pair-based VCO, lumped LC tank
  - Single-turn planar inductor, differential varactor bank to control the oscillation frequency
- CCP biased by a basic current mirror
  - Class A operation
- Push-push topology
  - 2nd harmonic is taken from the inductor center tap
  - Output will be matched to the 50-ohm RF pad
  - Tank resonates at 30 GHz



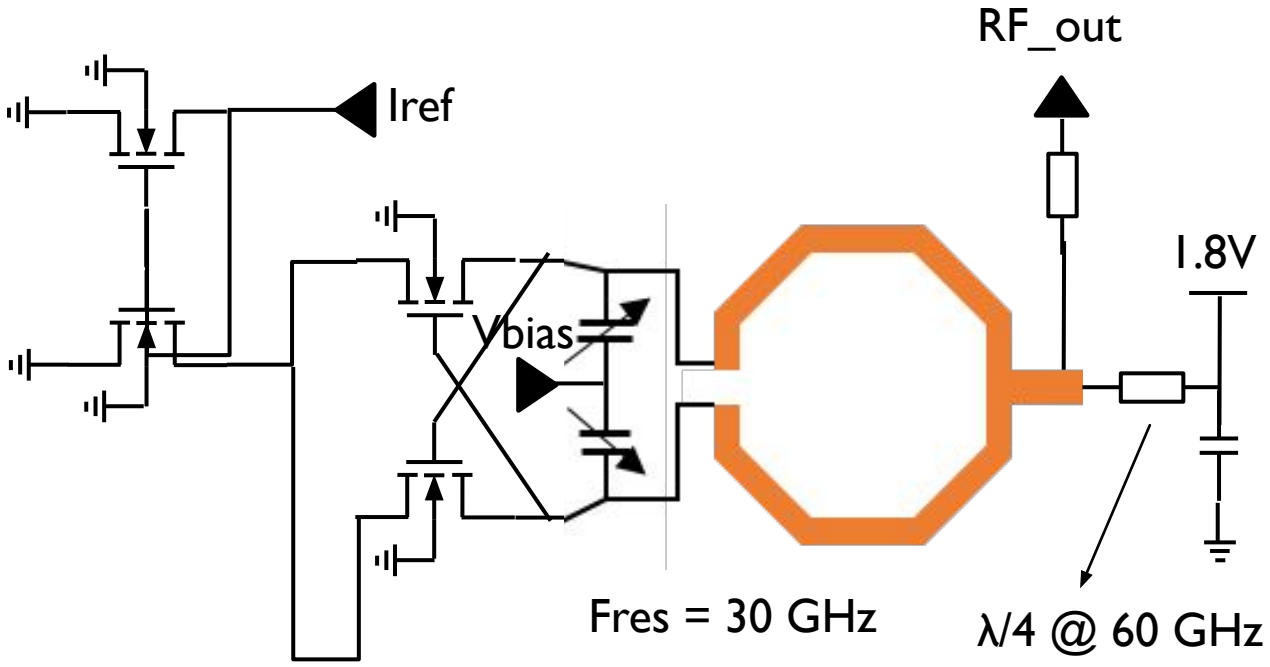
VCO

- CCP VCO is a proven oscillator design that sees widespread use in monolithic applications
- However, the performance is limited by the Q-factor of the varactor bank
- Design at a lower current density (0.15 mA/μm)
  - Produces larger fets with larger parasitic capacitance, but is safer as the biasing can be extended to augment loss compensation if the oscillations don't start
- Design uses RF MOSFET cells (aF08W0p84L0p15)
  - Modular nature of the devices makes the design flow easier since the high-frequency effects are already included in the spice model



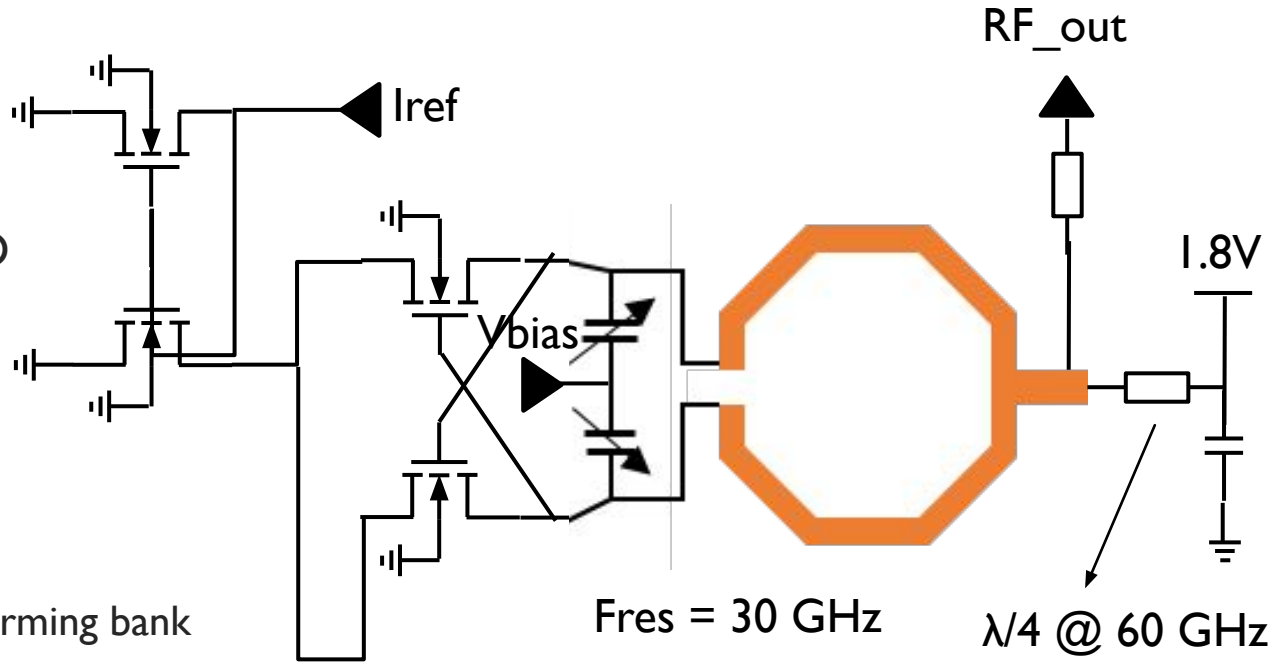
VCO

- Current mirror is a simple design, using two matched MOSFETs
  - Has lower output impedance than a cascode mirror
  - But offers more headroom
  - The available headroom for the current mirror is small, because most of the Vdd voltage has to fall on the CCP to maximize RF power output
- L = 150nm
  - Try to get a high AC output impedance
  - Larger L -> smaller ft and larger required Vov



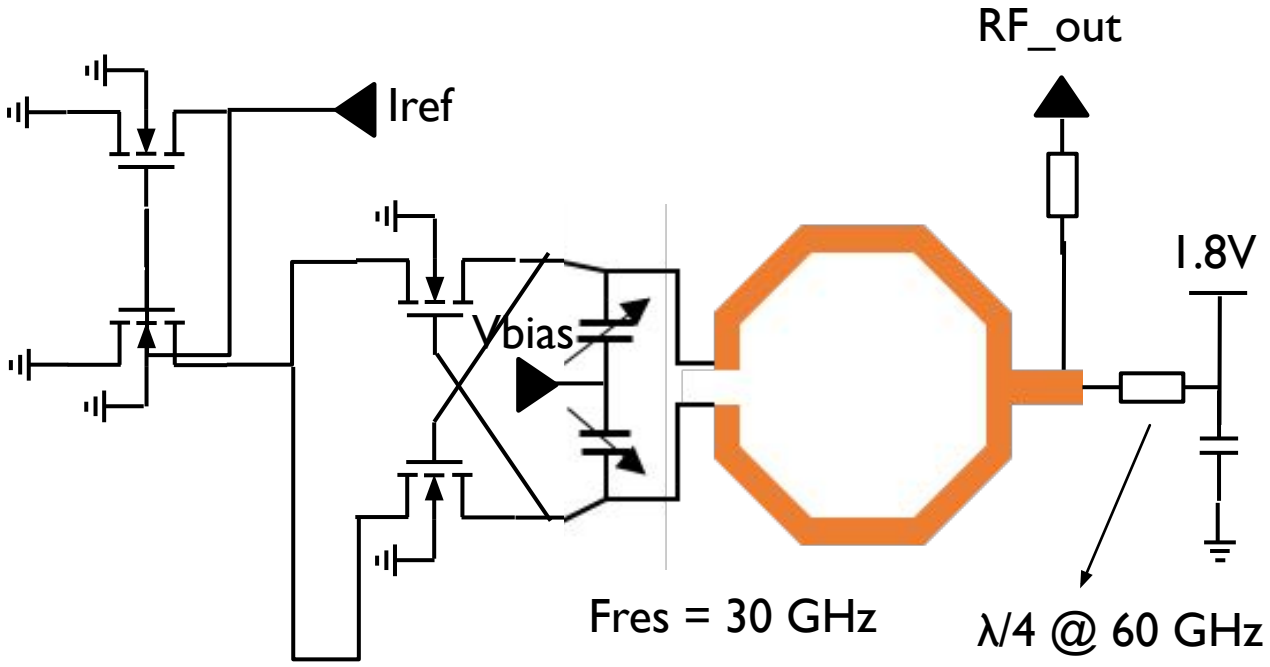
VCO

- Varactor bank, differential configuration
  - Varactor gate tied to the 1.8V supply
  - Biasing done through the source/drain contacts via a high-resistivity poly resistor
- Low Q-factor is the main design constraint for the VCO
  - And the main driving factor for the push-push topology
- Goal: find a W,L set that offers a minimum Q above 4 and a capacitance tune about 1
  - Ctr = (Cmax-Cmin)/Cnominal
  - And use multiple cells in parallel to arrive at a better-performing bank than a single, large varactor



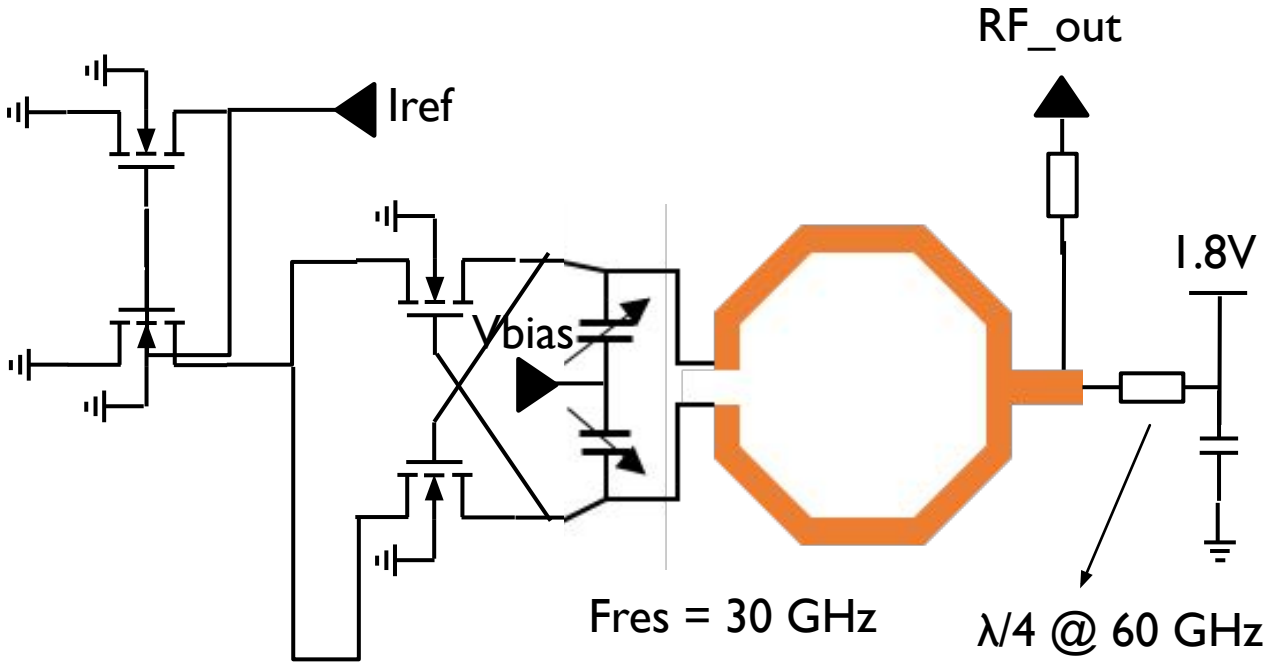
VCO

- Inductor
- Designed in ASITIC, verified in commercial tools
  - Equivalent PI model used in ngspice simulation



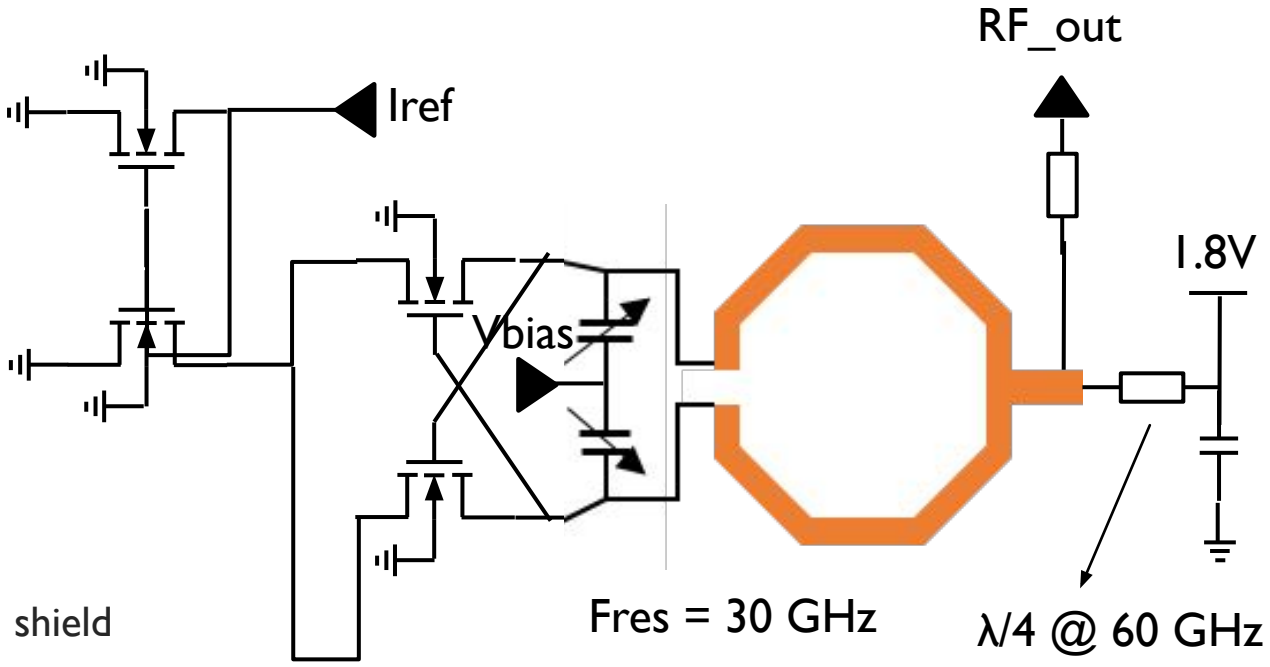
VCO

- Output matching
- SCPW designed using commercial tools
  - High Q-factor minimizes power loss
  - Equivalent RLRC model used in ngspice simulation

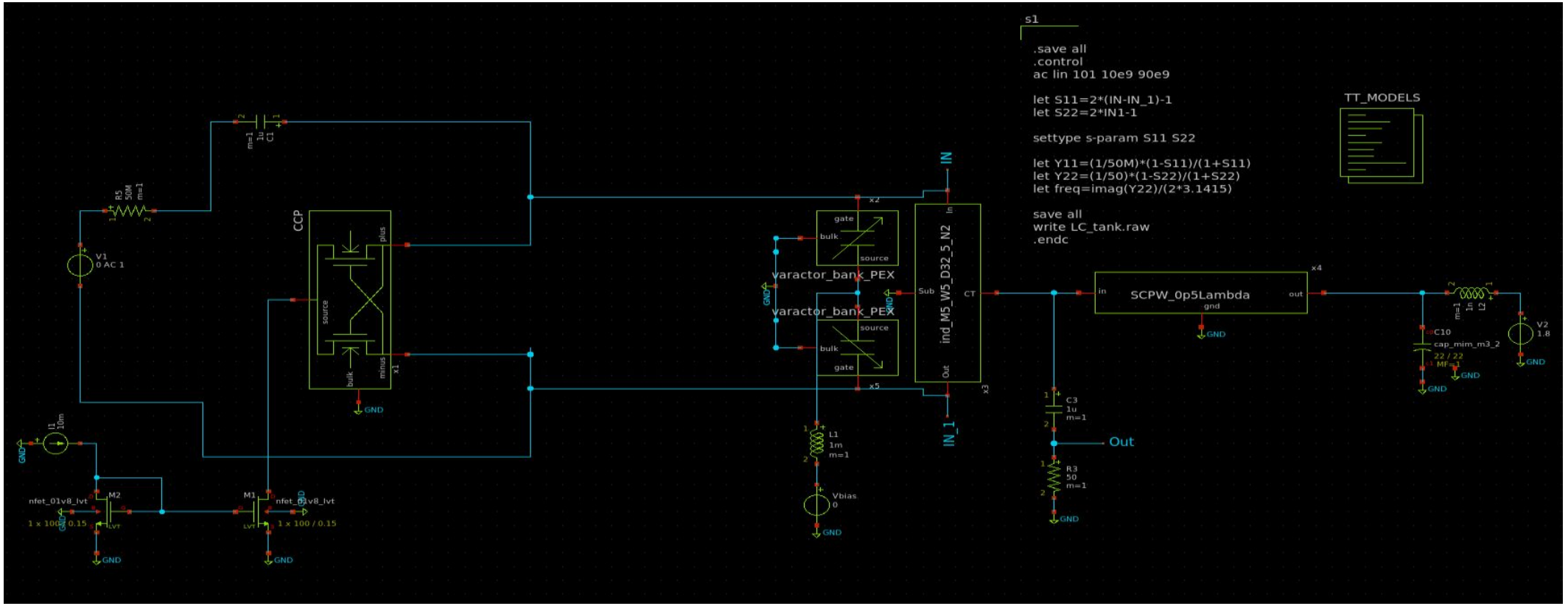


VCO - RESULTS

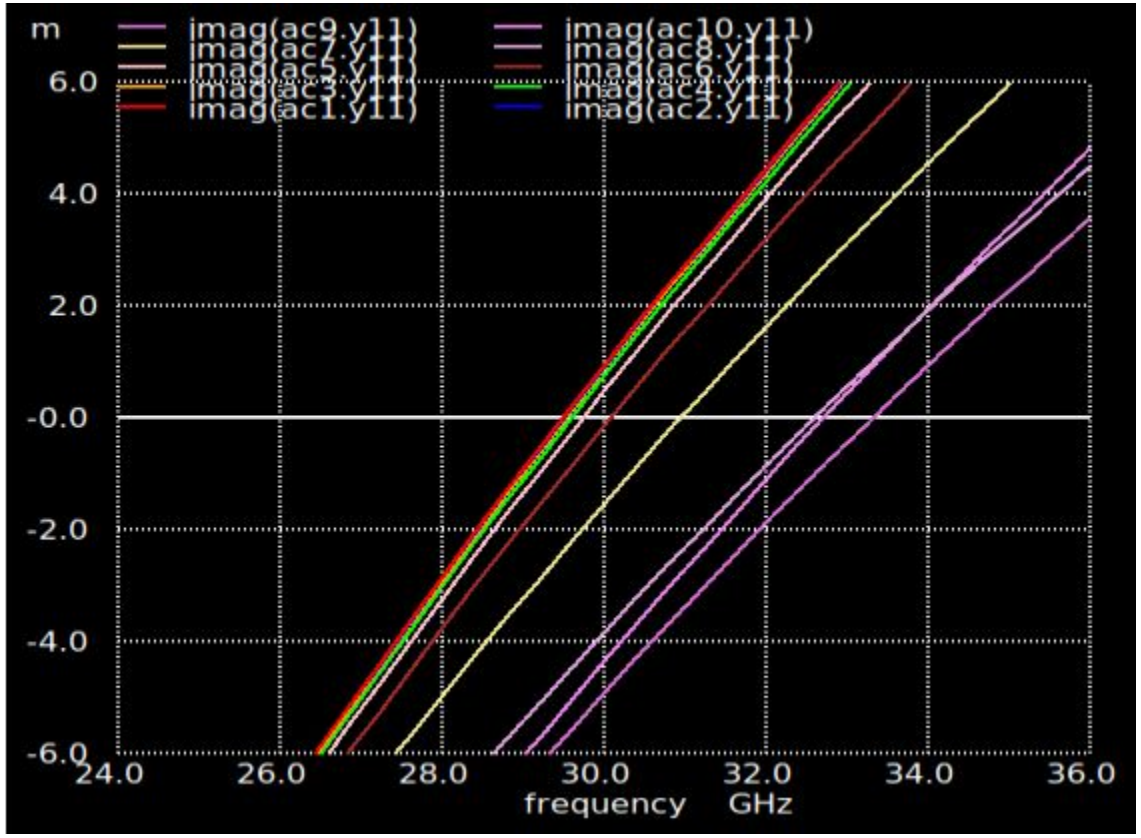
- CCP: 4 RF fets in parallel biased at 0.15 mA/µm
  - Total W of 26.88 µm, current consumption of 8 mA for the two fets
  - Maximum bias current of 0.35 mA/µm (18.9 mA)
- Current mirror: W = 100 µm, L = 150 nm
- Varactor bank: 35 units of W = 1.5 µm, L = 180 nm
  - Two banks required for differential operation
- Inductor: W = 10 µm, D = 130 µm
  - Custom LI+P+ guard ring included in the design, no ground shield



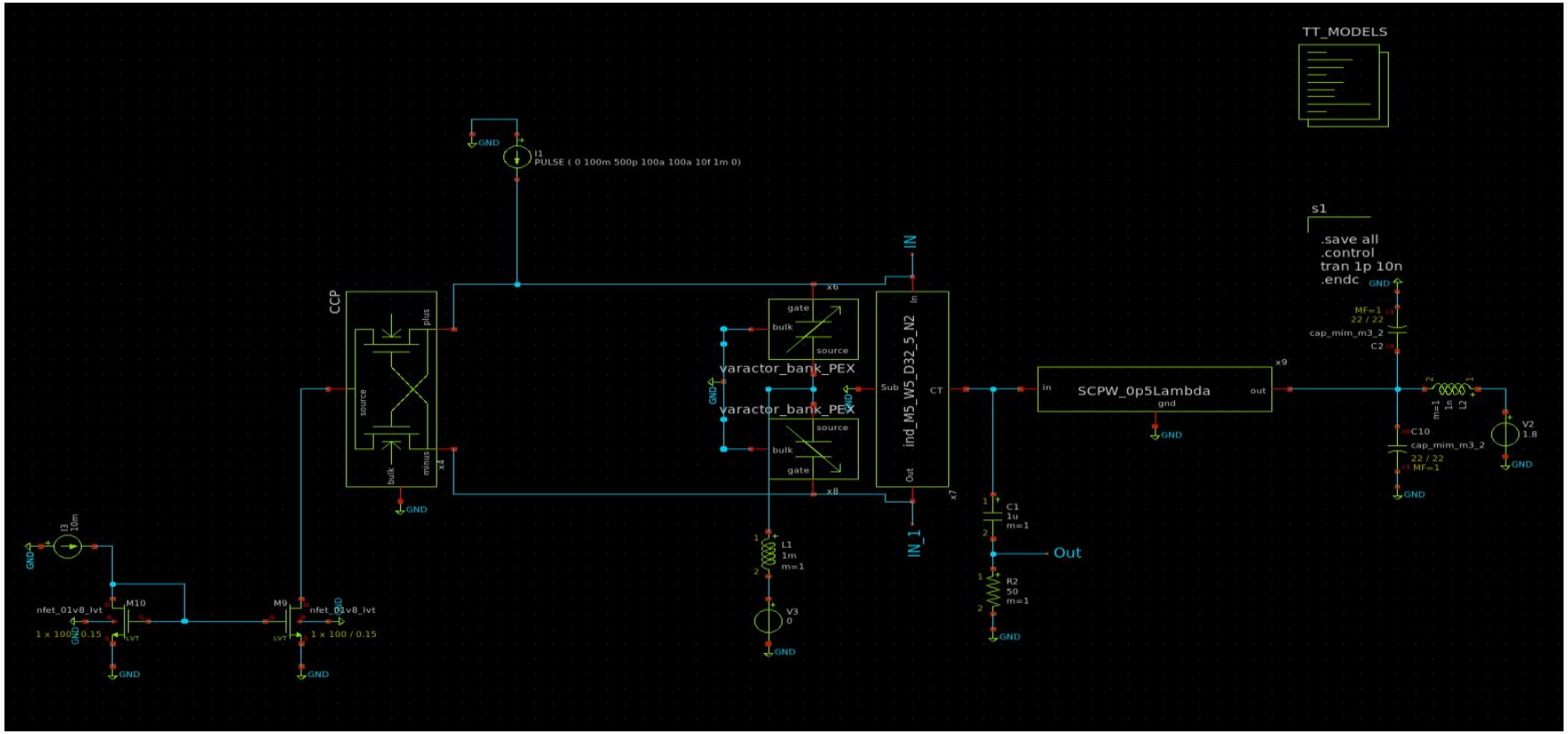
VCO - RESULTS


s1
.save all
.control
ac lin 101 10e9 90e9
let S11=2*(IN-IN_1)-1
let S22=2*IN1-1
settype s-param S11 S22
let Y11=(1/50M)*(1-S11)/(1+S11)
let Y22=(1/50)*(1-S22)/(1+S22)
let freq=imag(Y22)/(2*3.1415)
save all
write LC_tank.raw
.endc
TT_MODELS
IN
IN_1
Out
CCP
varactor_bank_PEX
varactor_bank_PEX
ind_M5_W5_D32_5_N2
SCPW_0p5Lambda
cap_mim_m3_2
nfet_01v8_lvt
nfet_01v8_lvt
V1
0 AC 1
V2
1.8
Vbias
0
GND

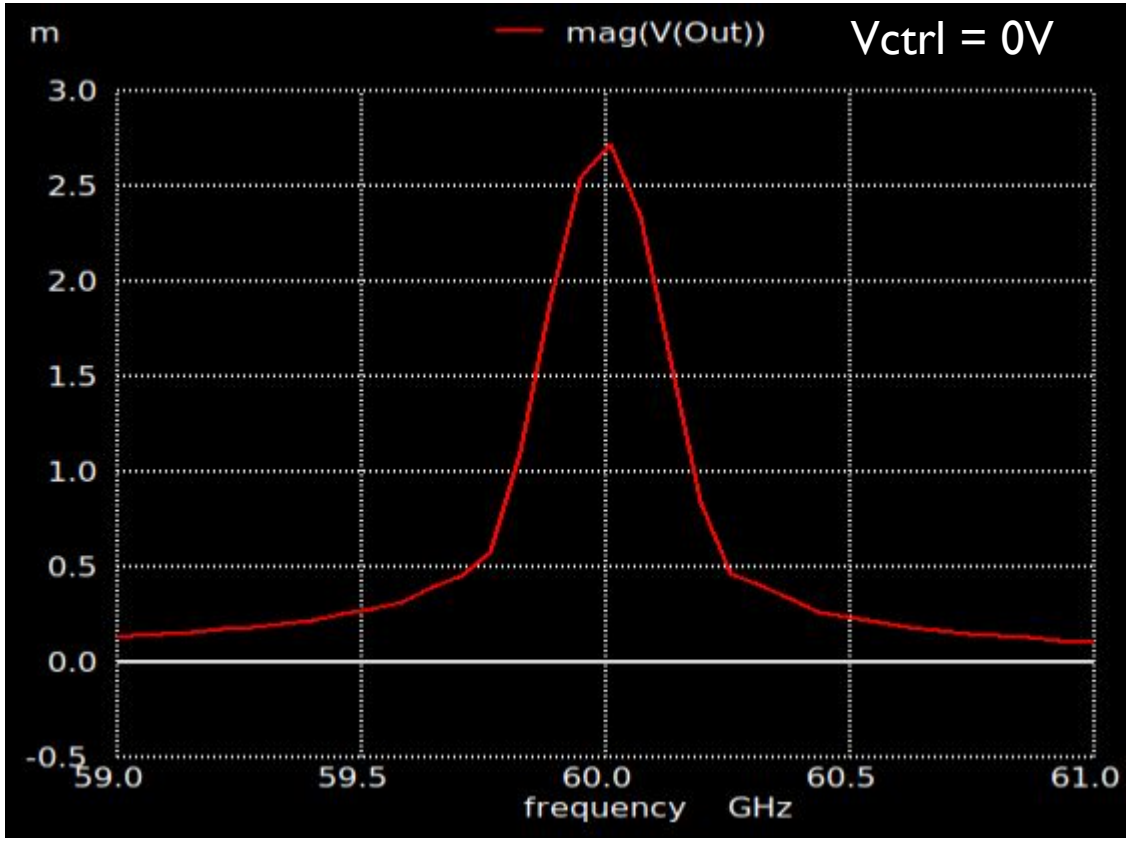
VCO - RESULTS

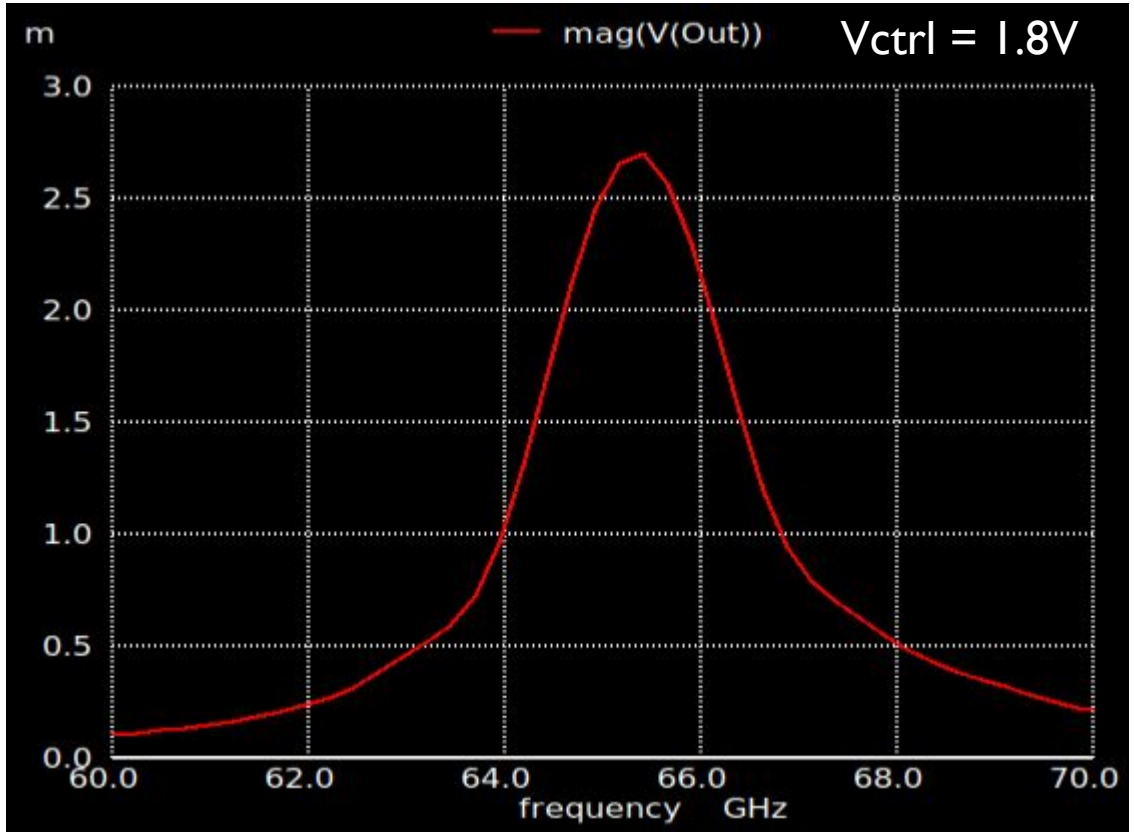

m
imag(ac9.y11)
imag(ac7.y11)
imag(ac5.y11)
imag(ac3.y11)
imag(ac1.y11)
imag(ac10.y11)
imag(ac8.y11)
imag(ac6.y11)
imag(ac4.y11)
imag(ac2.y11)
6.0
4.0
2.0
-0.0
-2.0
-4.0
-6.0
24.0
26.0
28.0
30.0
32.0
34.0
36.0
frequency GHz

VCO - RESULTS

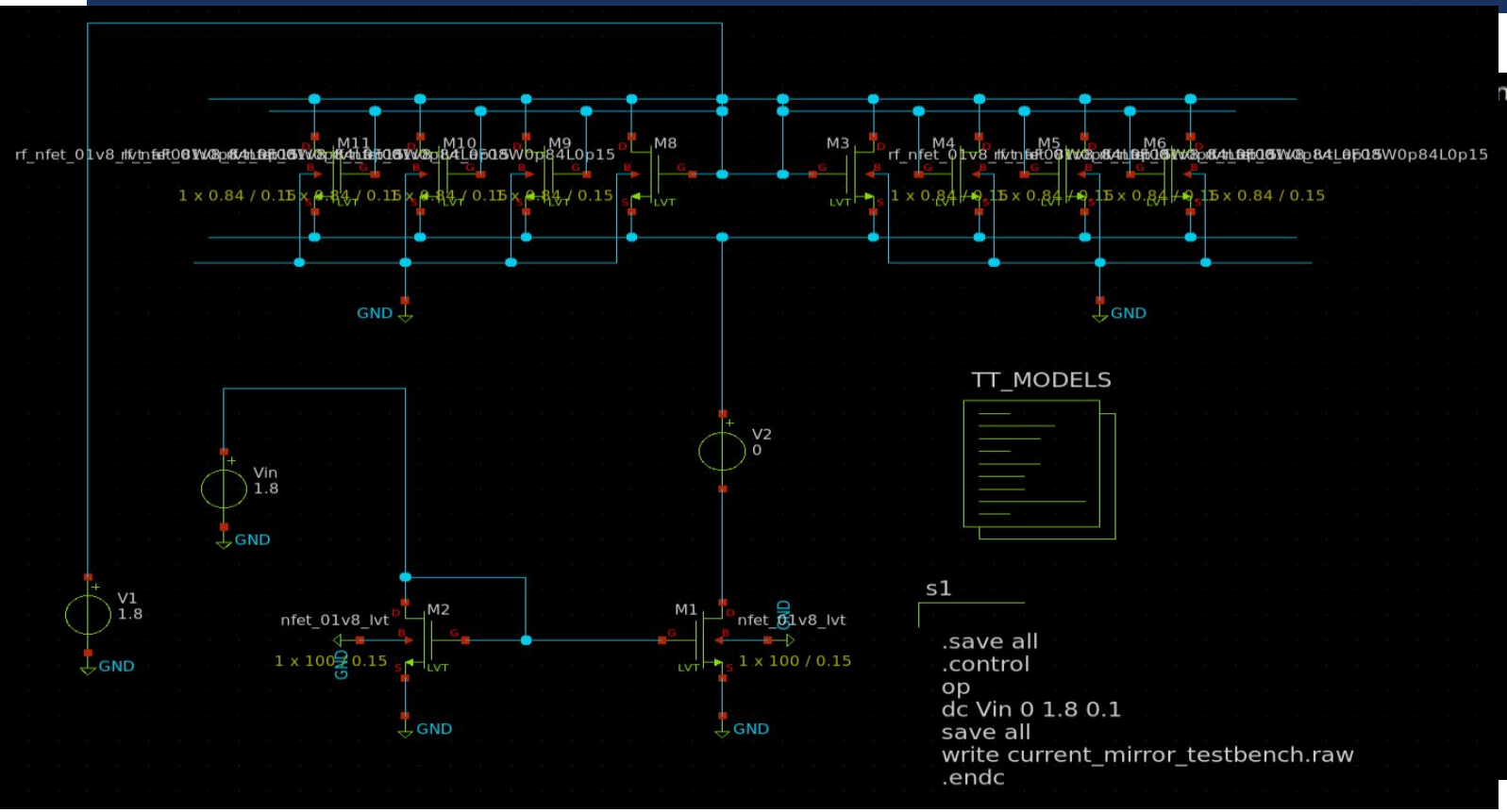

TT_MODELS
I3
PULSE (0 100m 500p 100a 100a 10f 1m 0)
GND
IN
CCP
plus
minus
source
bulk
x4
x6
x8
gate
bulk
source
varactor_bank_PEX
varactor_bank_PEX
Sub
CT
ind_M5_W5_D32_5_N2
In
Out
x7
IN_1
s1
.save all
.control
tran 1p 10n
.endc
SCPW_0p5Lambda
in
out
gnd
x9
MF=1
22 / 22
cap_mim_m3_2
C2
C10
V2
1.8
C1
1u
m=1
L1
1m
m=1
V3
0
R2
50
m=1
Out
I3
10m
M10
M9
nfet_01v8_lvt
1 x 100 / 0.15
LVT

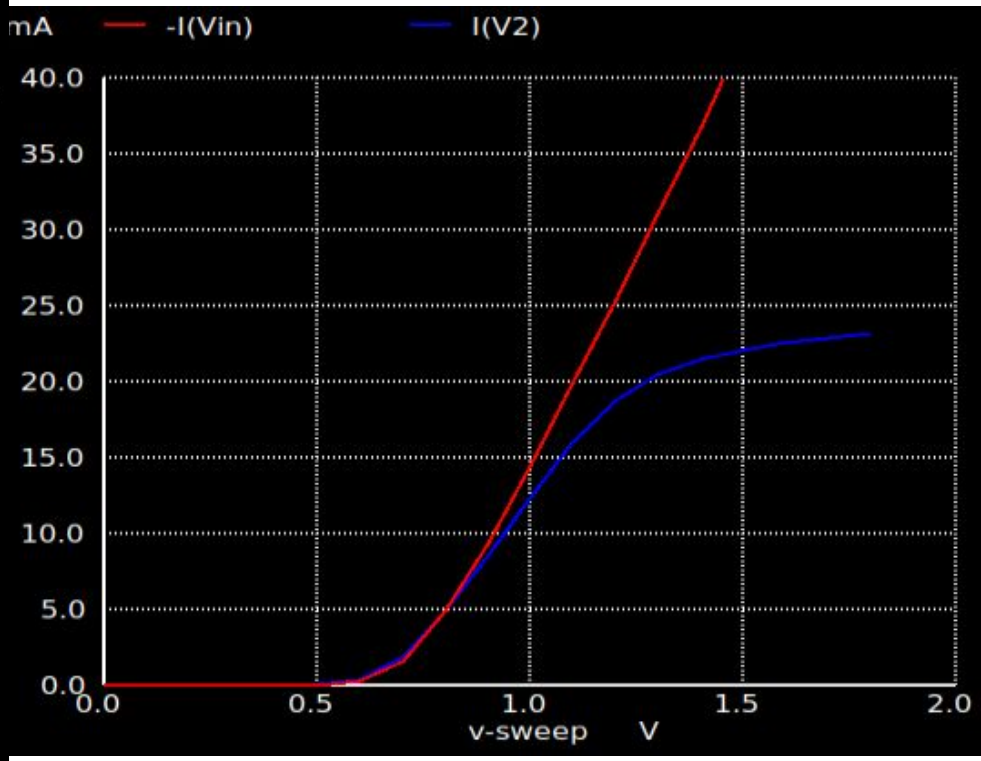
VCO - RESULTS


m
mag(V(Out))
Vctrl = 0V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
59.0
59.5
60.0
60.5
61.0
frequency GHz

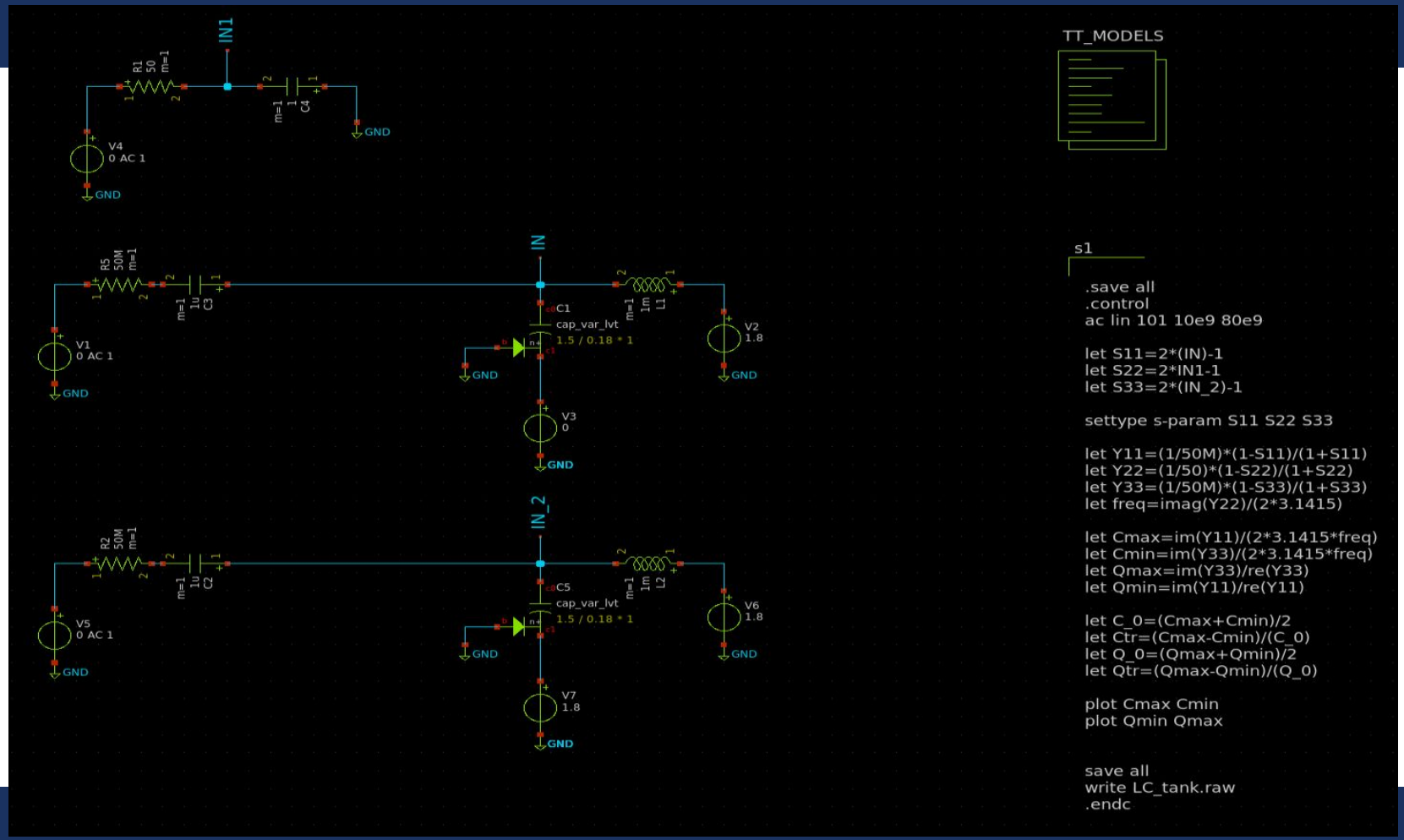

m
mag(V(Out))
Vctrl = 1.8V
3.0
2.5
2.0
1.5
1.0
0.5
0.0
60.0
62.0
64.0
66.0
68.0
70.0
frequency GHz

VCO - RESULTS

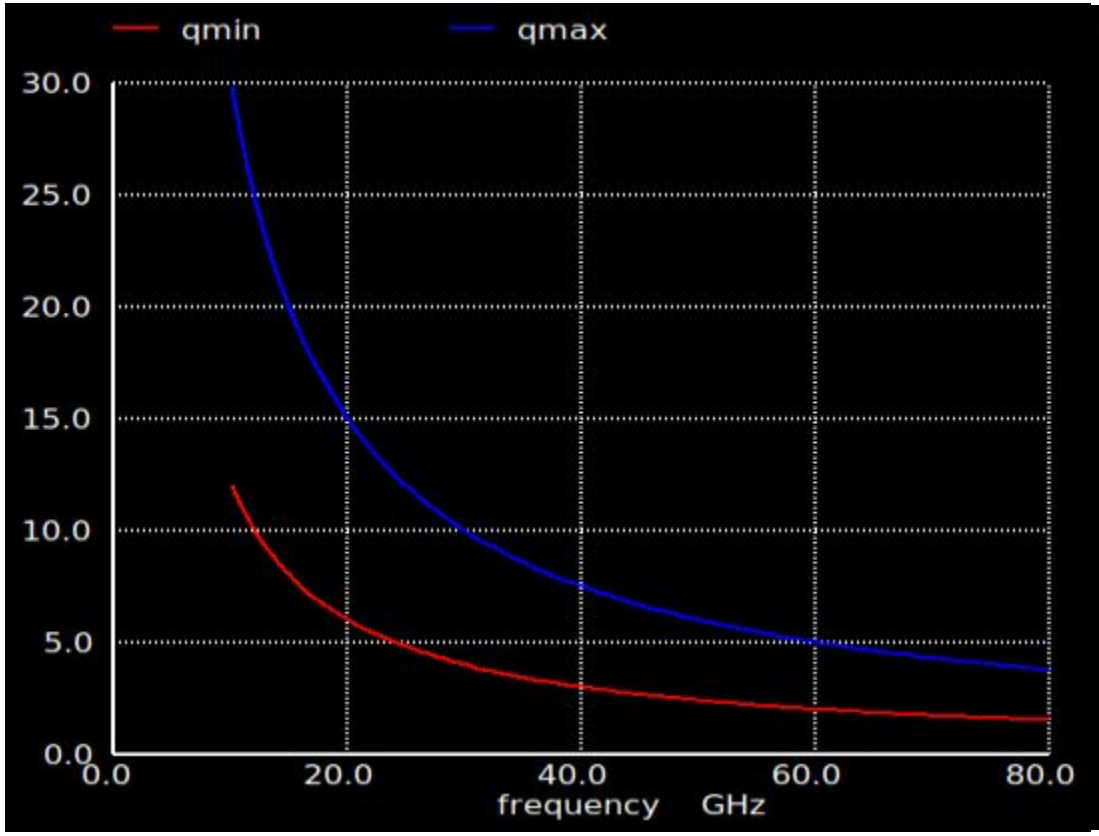

M11
M10
M9
M8
M3
M4
M5
M6
1 x 0.84 / 0.15
GND
TT_MODELS
V2
0
Vin
1.8
V1
1.8
M2
M1
nfet_01v8_lvt
1 x 100 / 0.15
s1
.save all
.control
op
dc Vin 0 1.8 0.1
save all
write current_mirror_testbench.raw
.endc

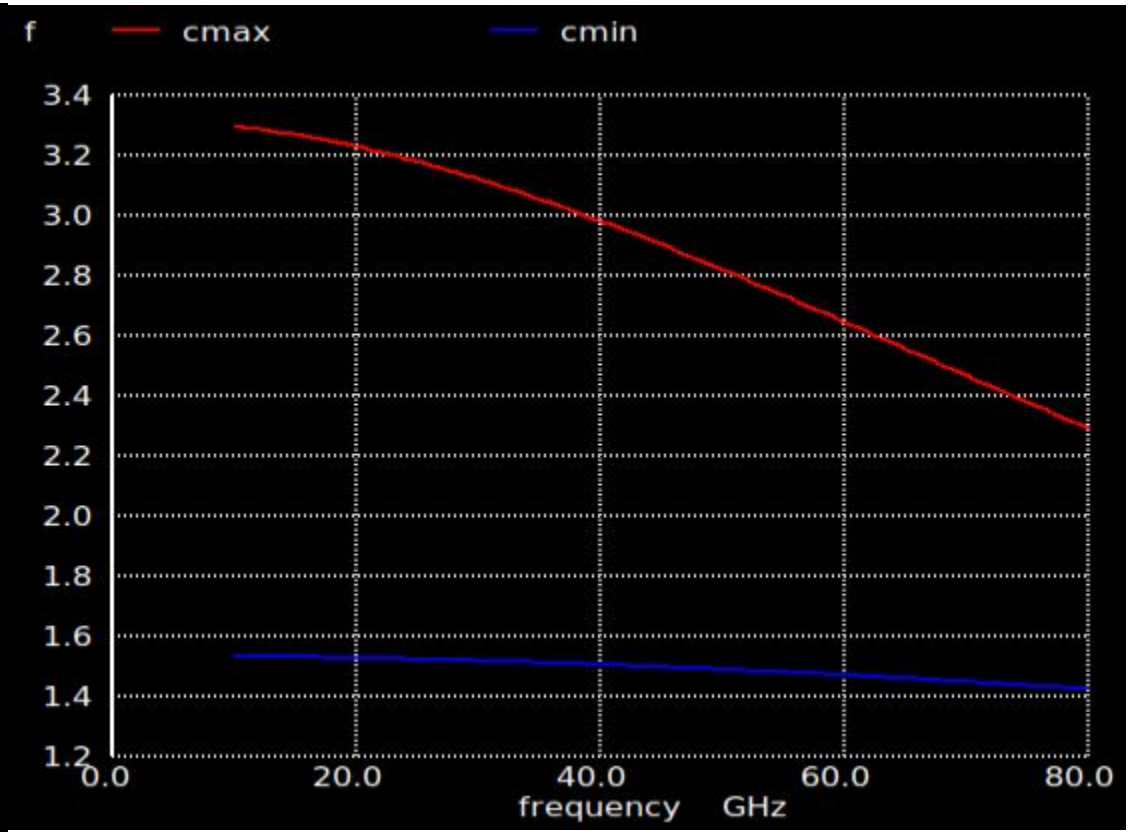

mA
-I(Vin)
I(V2)
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
0.0
0.5
1.0
1.5
2.0
v-sweep
V

VCO - RESULTS

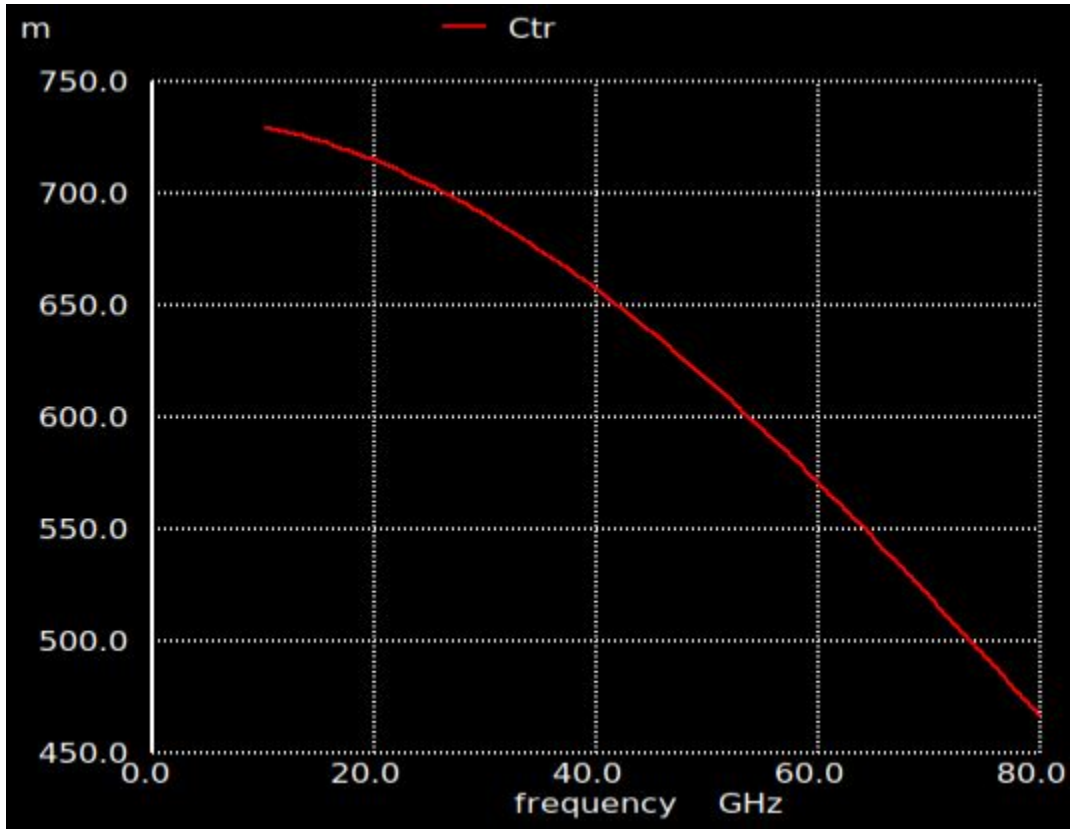

IN1
R1
50
m=1
C4
1
m=1
GND
V4
0 AC 1
GND
IN
R5
50M
m=1
C3
1u
m=1
V1
0 AC 1
GND
C1
cap_var_lvt
1.5 / 0.18 * 1
L1
1n
m=1
V2
1.8
GND
GND
V3
0
GND
IN_2
R2
50M
m=1
C2
1u
m=1
V5
0 AC 1
GND
C5
cap_var_lvt
1.5 / 0.18 * 1
L2
1n
m=1
V6
1.8
GND
GND
V7
1.8
GND
TT_MODELS
s1
.save all
.control
ac lin 101 10e9 80e9
let S11=2*(IN)-1
let S22=2*IN1-1
let S33=2*(IN_2)-1
settype s-param S11 S22 S33
let Y11=(1/50M)*(1-S11)/(1+S11)
let Y22=(1/50)*(1-S22)/(1+S22)
let Y33=(1/50M)*(1-S33)/(1+S33)
let freq=imag(Y22)/(2*3.1415)
let Cmax=im(Y11)/(2*3.1415*freq)
let Cmin=im(Y33)/(2*3.1415*freq)
let Qmax=im(Y33)/re(Y33)
let Qmin=im(Y11)/re(Y11)
let C_0=(Cmax+Cmin)/2
let Ctr=(Cmax-Cmin)/(C_0)
let Q_0=(Qmax+Qmin)/2
let Qtr=(Qmax-Qmin)/(Q_0)
plot Cmax Cmin
plot Qmin Qmax
save all
write LC_tank.raw
.endc

VCO - RESULTS

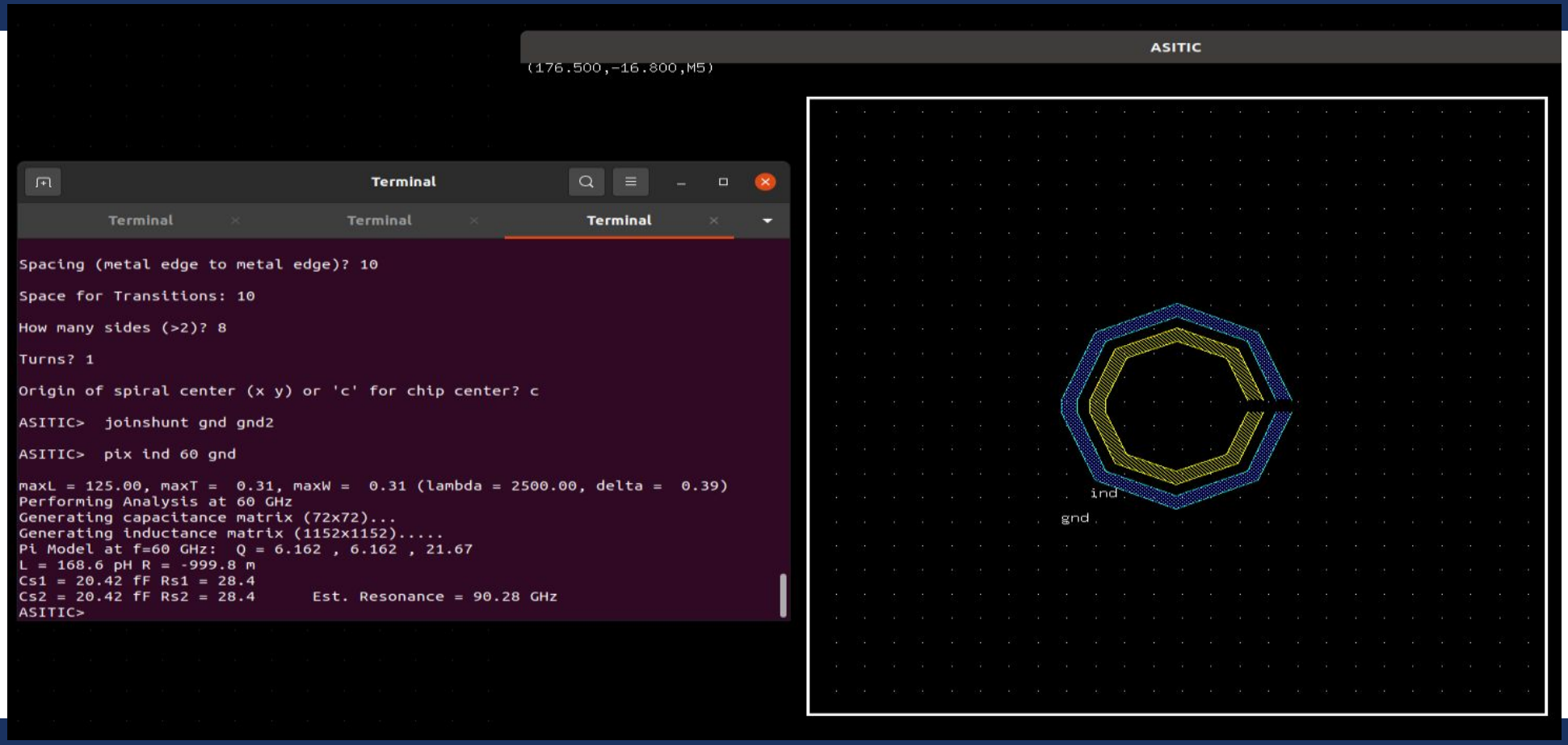

qmin
qmax
30.0
25.0
20.0
15.0
10.0
5.0
0.0
0.0
20.0
40.0
60.0
80.0
frequency GHz


f
cmax
cmin
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
0.0
20.0
40.0
60.0
80.0
frequency GHz

VCO - RESULTS

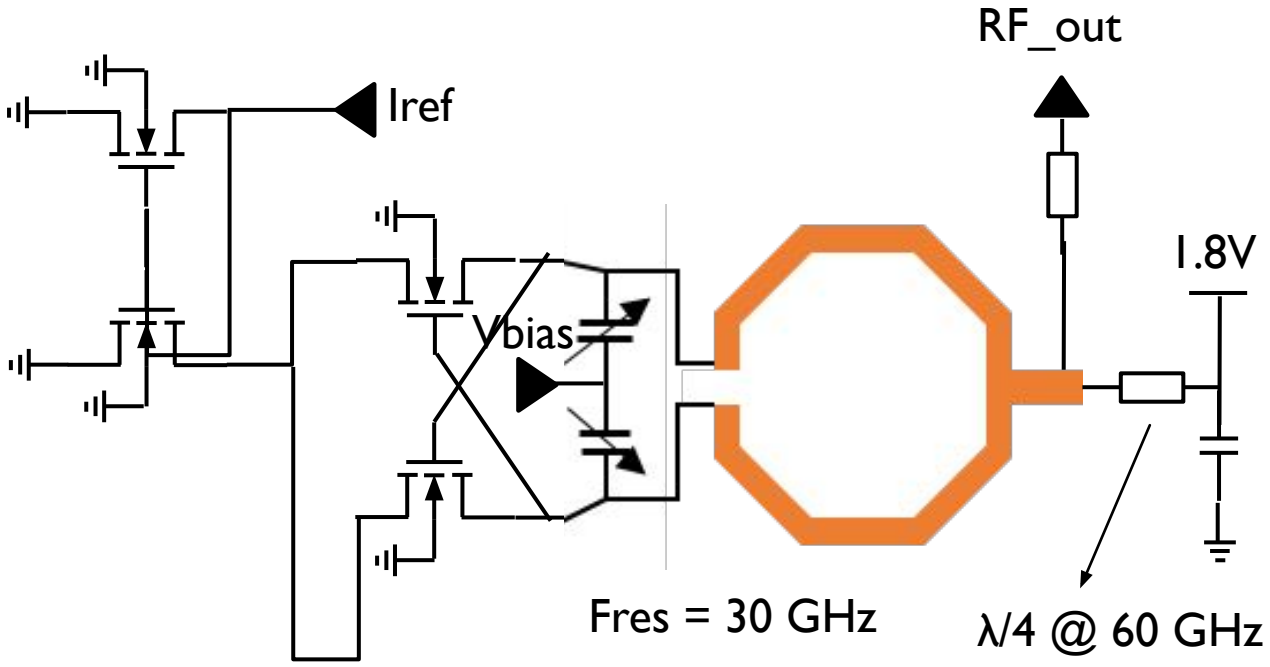

m
Ctr
750.0
700.0
650.0
600.0
550.0
500.0
450.0
0.0
20.0
40.0
60.0
80.0
frequency GHz

VCO - RESULTS


ASITIC
(176.500,-16.800,M5)
Terminal
Terminal
Terminal
Terminal
Spacing (metal edge to metal edge)? 10
Space for Transitions: 10
How many sides (>2)? 8
Turns? 1
Origin of spiral center (x y) or 'c' for chip center? c
ASITIC> joinshunt gnd gnd2
ASITIC> pix ind 60 gnd
maxL = 125.00, maxT = 0.31, maxW = 0.31 (lambda = 2500.00, delta = 0.39)
Performing Analysis at 60 GHz
Generating capacitance matrix (72x72)...
Generating inductance matrix (1152x1152).....
Pi Model at f=60 GHz: Q = 6.162 , 6.162 , 21.67
L = 168.6 pH R = -999.8 m
Cs1 = 20.42 fF Rs1 = 28.4
Cs2 = 20.42 fF Rs2 = 28.4 Est. Resonance = 90.28 GHz
ASITIC>
ind
gnd

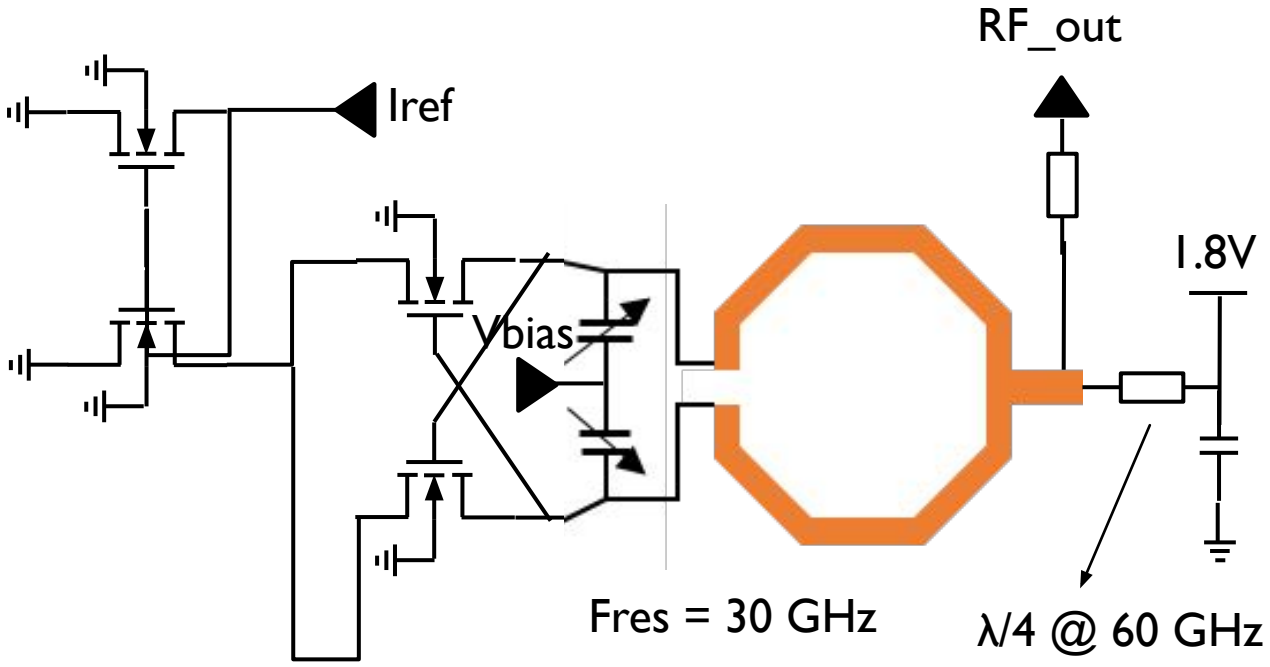
VCO – UNSIMULATED PARTS

- Output matching need to be done
- Plan: create a new testbench to measure the output reflection coefficient (S11 in a 1-port setup) and design a conjugate matching network



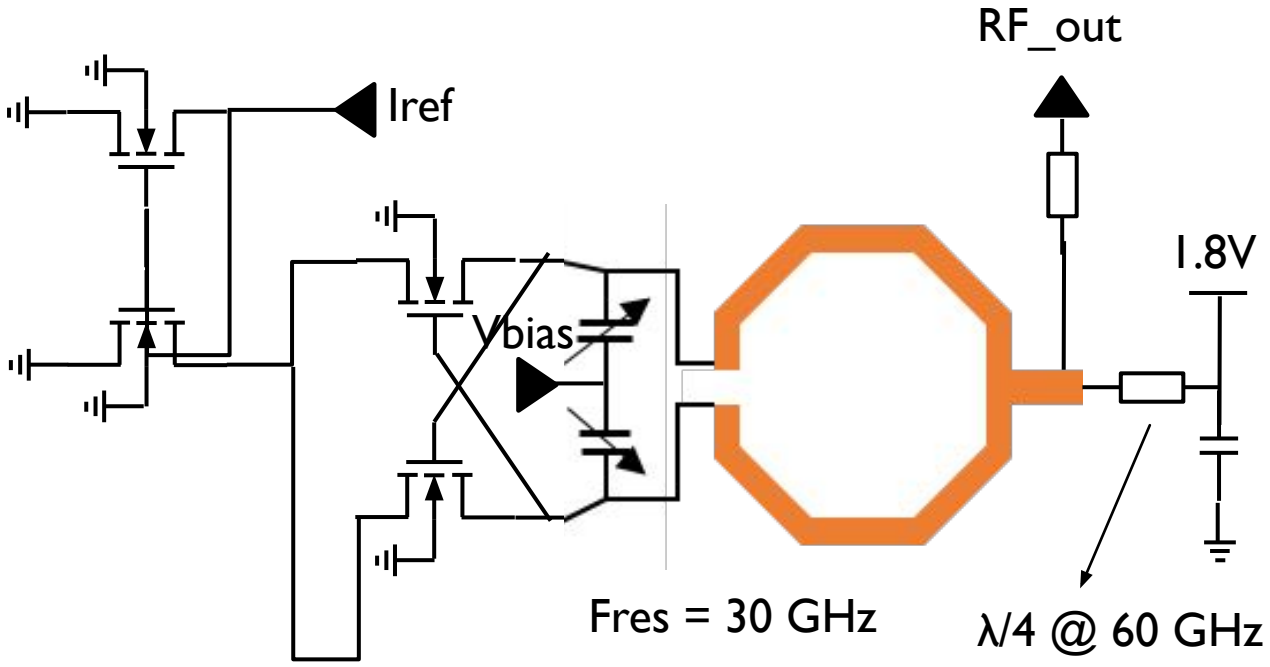
VCO – RESULTS VERSUS INITIAL GOALS

- Initial specs
  - 3 GHz tuning range at 60 GHz
  - Phase noise better than -100 dBc/Hz at 10 MHz offset from the carrier frequency
  - 18 mW of DC power consumption (VCO core only)
  - Maximum DC power consumption of 36 mW
  - Buffer with input capacitance smaller than 6 fF, output reflection loss smaller than 10 dB inside the V-band.



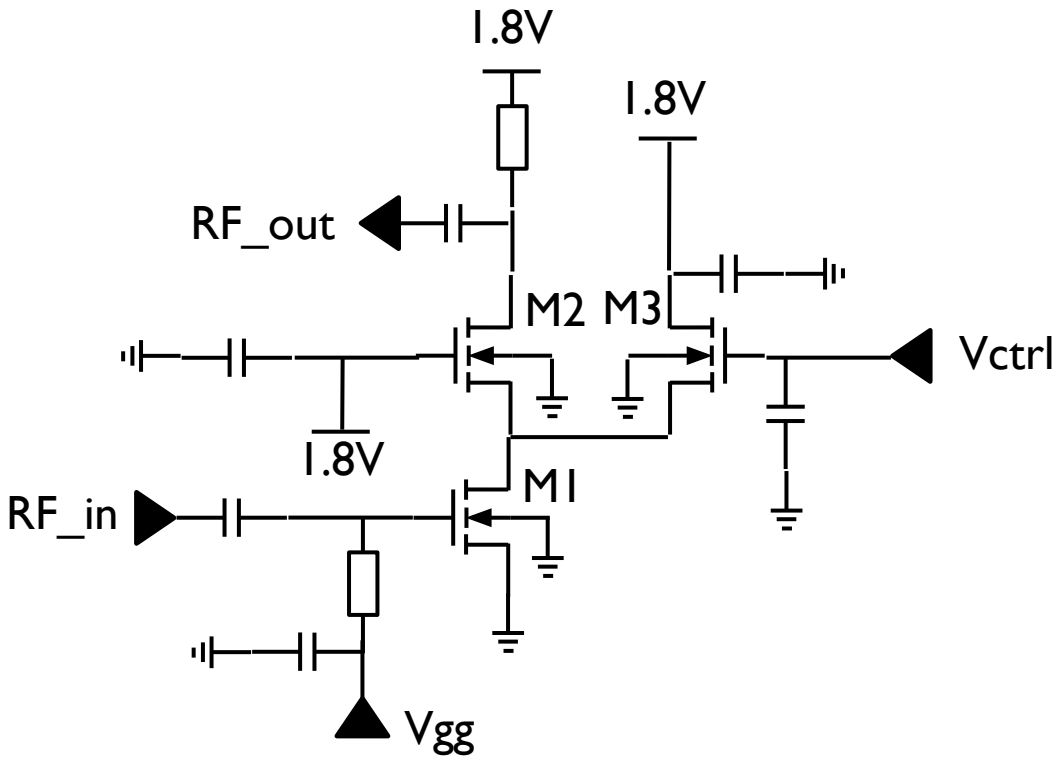
VCO – RESULTS VERSUS INITIAL GOALS

- Schematic level simulation specs
  - 5.7 GHz tuning range at 60 GHz
  - No phase-noise simulation capability
  - 14.4 mW of DC power consumption (VCO core only)
  - Maximum DC power consumption of 34 mW
  - No buffers needed



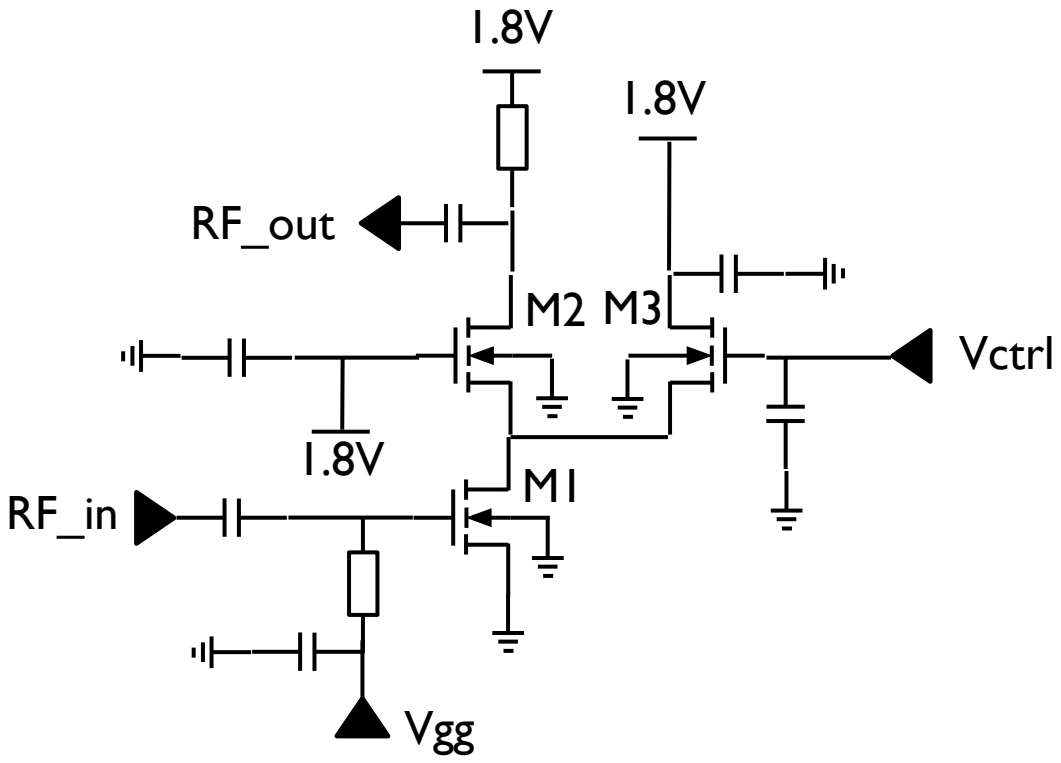
Variable Gain Amplifier - VGA

- Current-steering cascode topology
  - When Vctrl = 0, M3 is off and the gain is maximum
  - When Vctrl = 1.8V, M3 is on and shunts M2, gain is minimum
  - Since the drain current of M2 isn't disturbed, and because of the good IO isolation of the cascode topology, the output impedance isn't affected
- Vgg bias M1 and sets the maximum gain of the circuit
  - Vgg = 1V results in maximum ft
- Input and output impedance matching networks



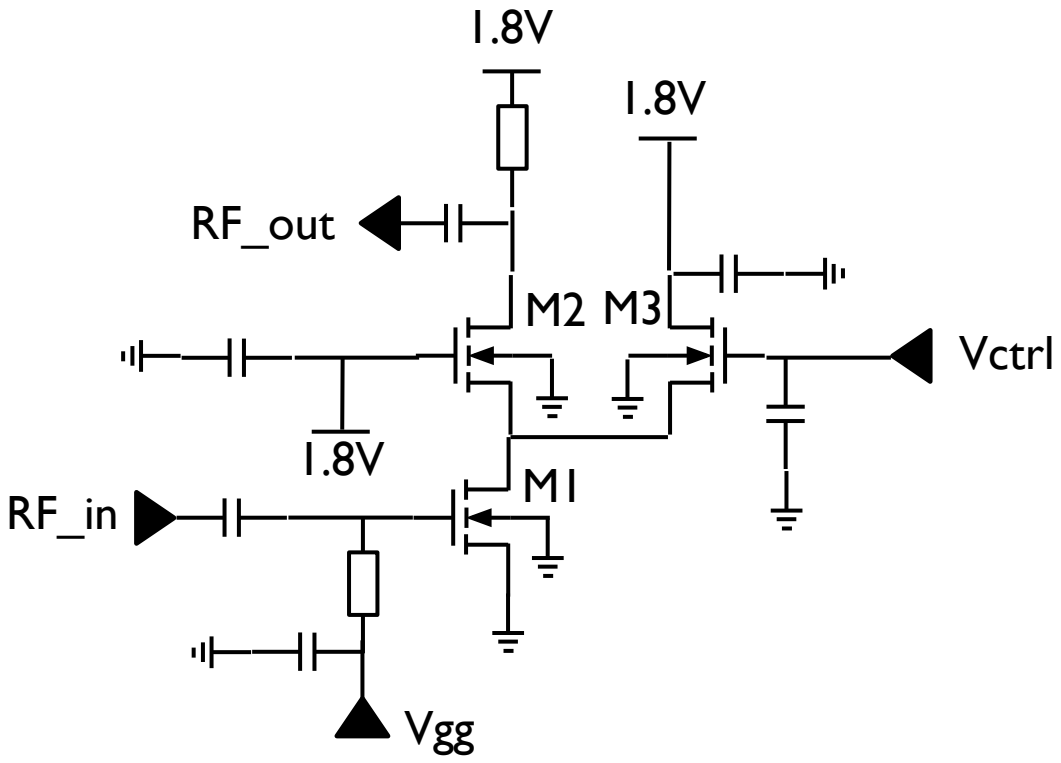
VGA

- Current-steering cascode is a simple, yet capable topology
  - Easier to implement than a Gilbert cell, as it doesn't need baluns and has fewer transistors
  - But is more prone to noise and to phase variation with Vctrl
- A simpler design maximizes the chances of success, as there are too many unknowns for the RF designers



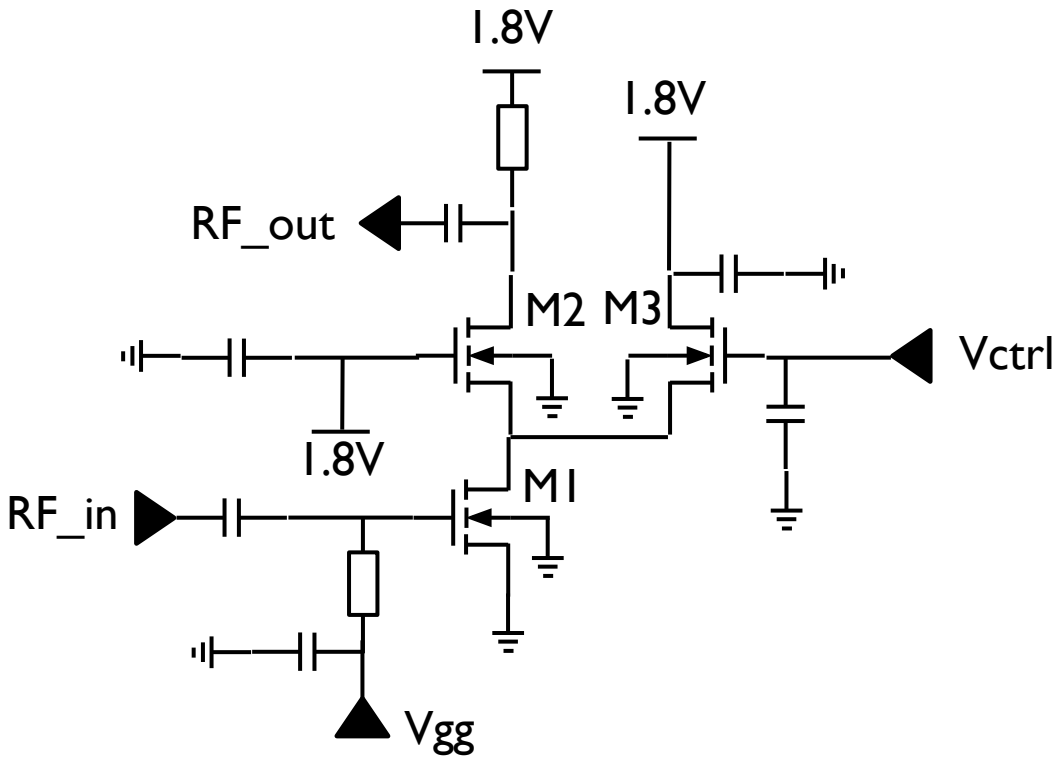
VGA

- Design procedure: find the ratio of W_{M1} and W_{M2} that maximizes the Maximum Available Gain (MSG)
  - Fixing $W_{M3} = W_{M2}$
- Design the output and input matching networks
  - MIM capacitors, TLine stubs to realize series drain load
  - S-CPW transmission line to minimize losses, and thus improve the amplifier gain
  - Single-frequency matching at 60 GHz
- RF_in and RF_out are the input and output of this amplifier, to be supplied by custom Ground-Signal-Ground pads



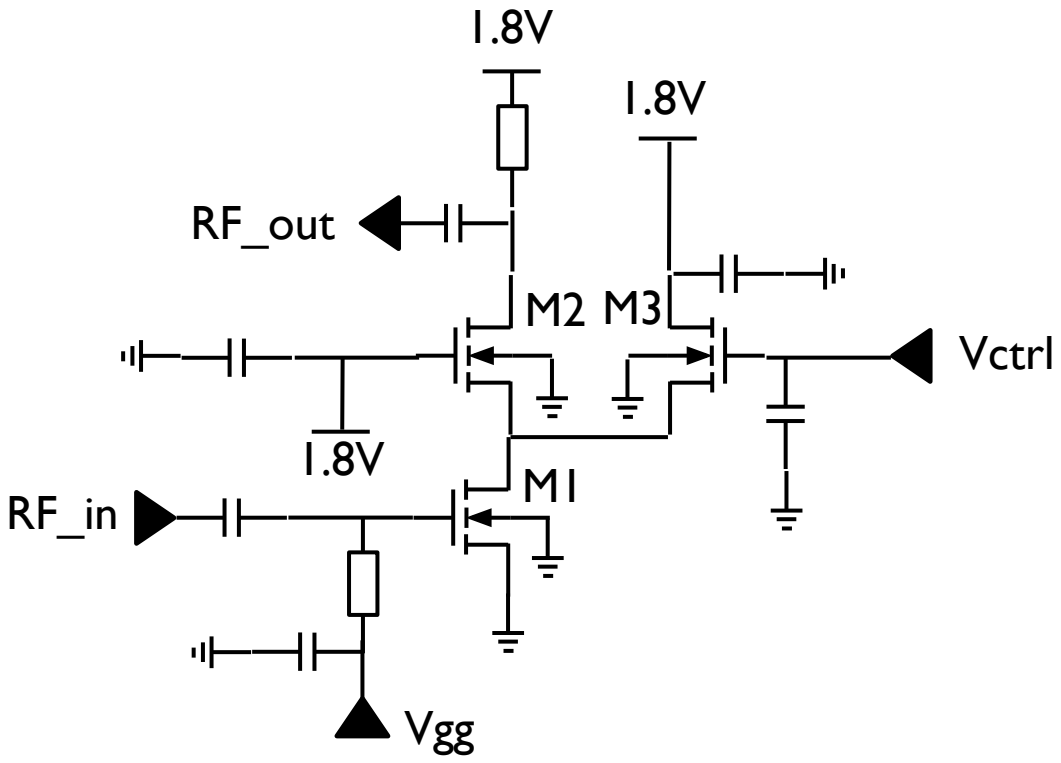
VGA

- MOSFET model: standard Pcell model with added series resistor to the gate to model non-quasi-stactic effects
- Instead of using the RF MOSFET cells…
  - Fixed cells make running parametric sweeps more difficult
  - The nqs resistor improves the accuracy in mmW frequencies



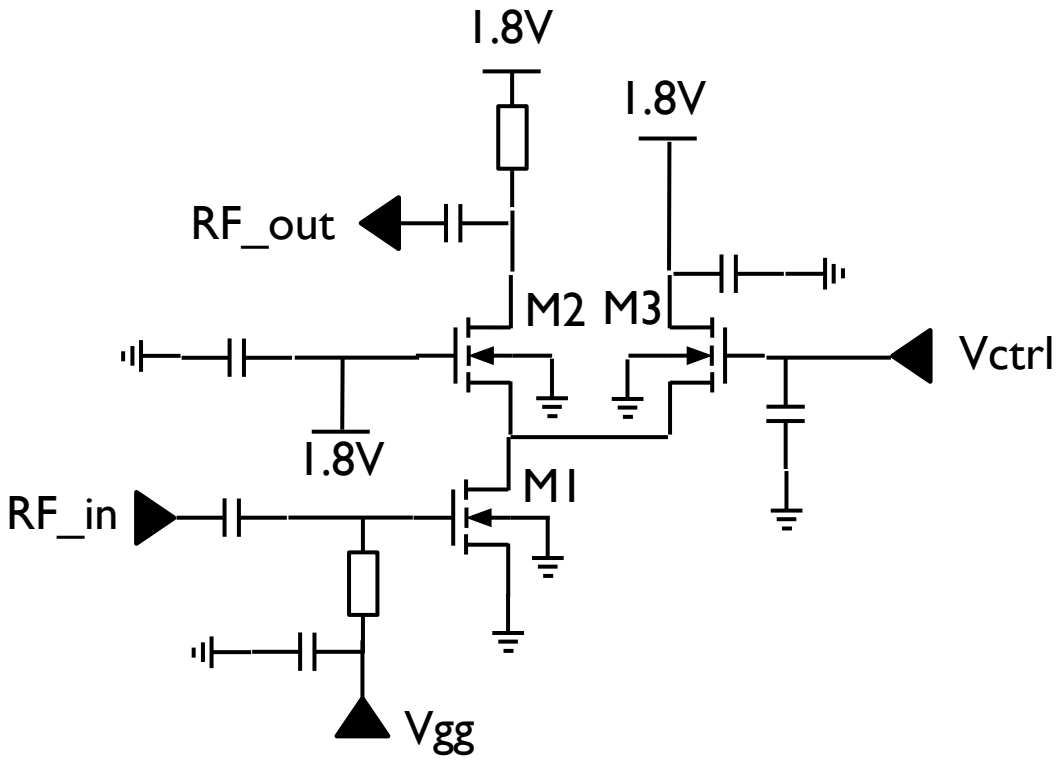
VGA

- Design steps for the amplifier core:
  - Xschem: built a testbench to run S-parameter simulations and export a s2p file
  - Design the input and output matching networks in commercial tools
  - Verification in xschem, generate the schematic netlist
  - Klayout: layout of the cascode transistor plus DC decoupling capacitors and DRC check (to be verified in Magic)
  - Netgen: LVS
  - Magic: parasitic extraction
  - Xschem: PLS

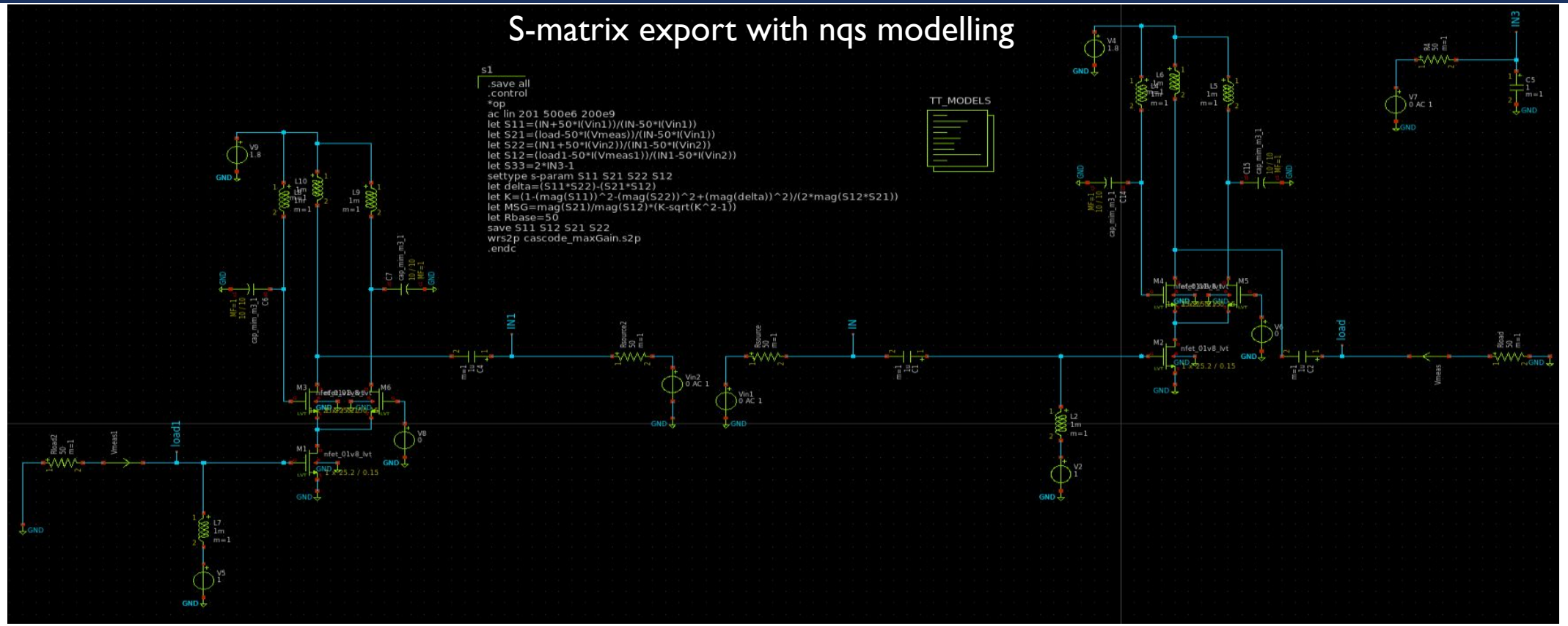


VGA - RESULTS

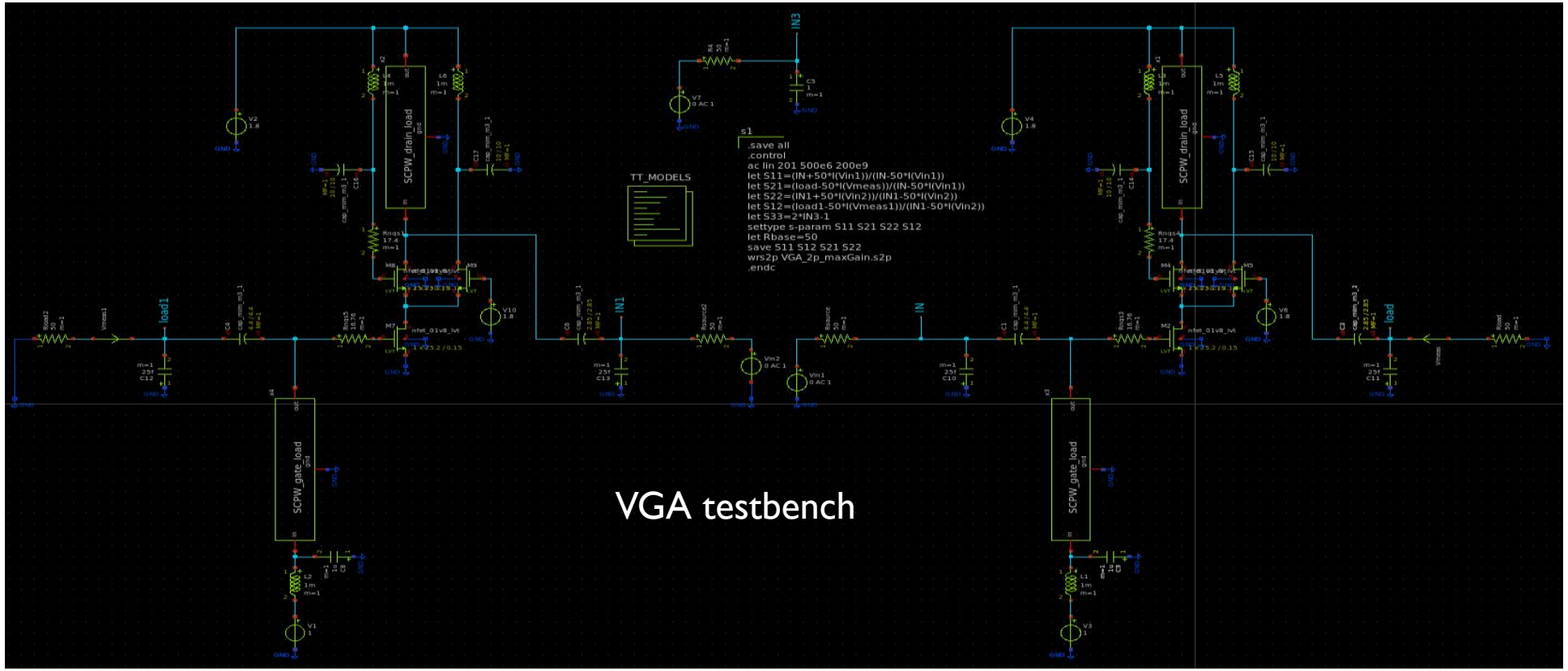
- Drain stub length = 280.45 µm, out capacitor 2.85 µm x 2.85 µm
- Gate stub length = 198.8 µm, in capacitor 4.4 µm x 4.4 µm
- $W_{M1} = W_{M2} = W_{M3}$ = 25.2 µm, L is fixed at 130 nm
- MOSFETs laid out as multifinger devices, Wfinger = 840 nm
  - Nf, thus, equals 30 for all devices
- DC current of 2.95 mA at maximum gain
  - 3 mA at minimum gain



VGA - RESULTS

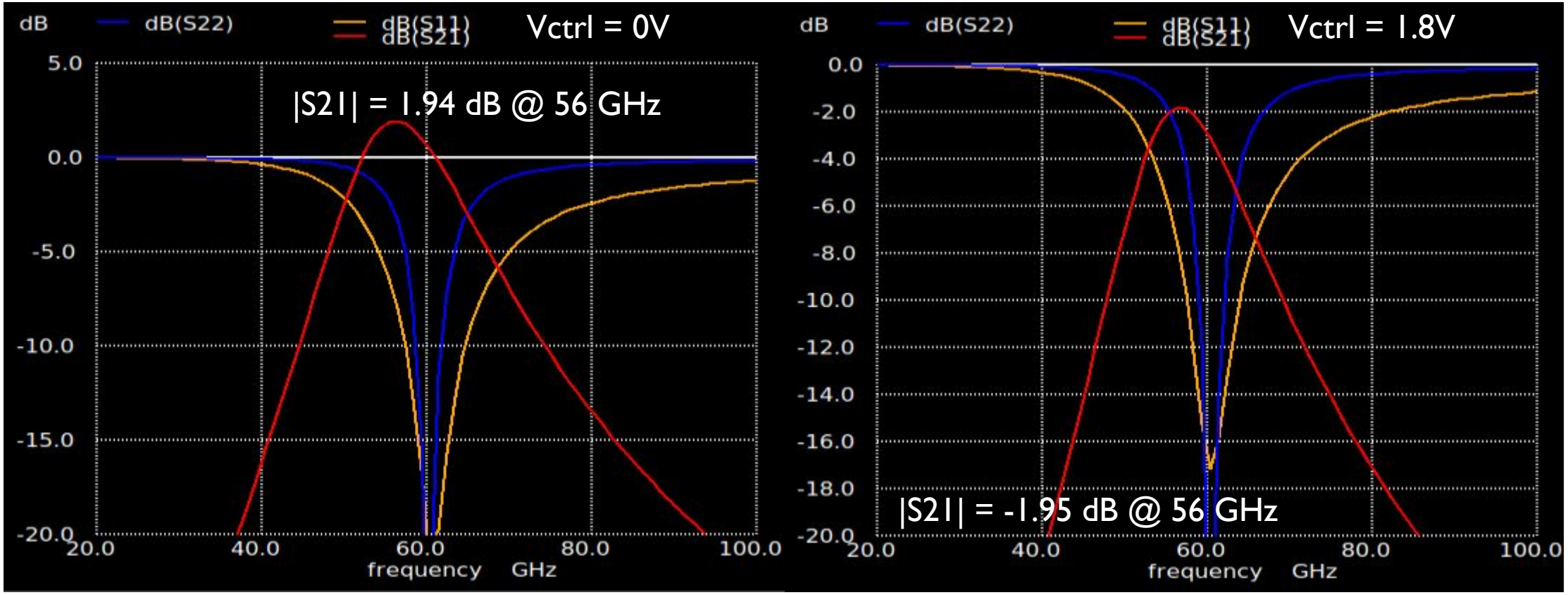

S-matrix export with nqs modelling
s1
.save all
.control
*op
ac lin 201 500e6 200e9
let S11=(IN+50*I(Vin1))/(IN-50*I(Vin1))
let S21=(load-50*I(Vmeas))/(IN-50*I(Vin1))
let S22=(IN1+50*I(Vin2))/(IN1-50*I(Vin2))
let S12=(load1-50*I(Vmeas1))/(IN1-50*I(Vin2))
let S33=2*IN3-1
settype s-param S11 S21 S22 S12
let delta=(S11*S22)-(S21*S12)
let K=(1-(mag(S11))^2-(mag(S22))^2+(mag(delta))^2)/(2*mag(S12*S21))
let MSG=mag(S21)/mag(S12)*(K-sqrt(K^2-1))
let Rbase=50
save S11 S12 S21 S22
wrs2p cascode_maxGain.s2p
.endc
TT_MODELS
IN1
IN
IN3
load
load1
Vmeas
Vmeas1
GND

VGA - RESULTS



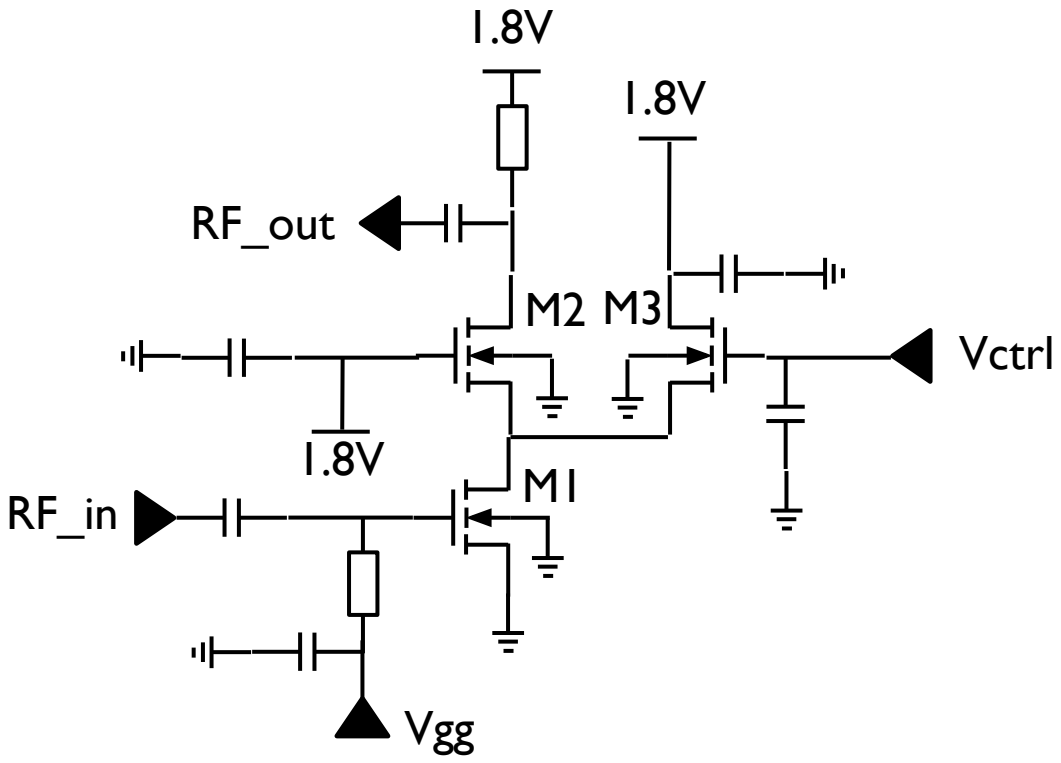
VGA testbench

VGA - RESULTS


dB
dB(S22)
dB(S11)
dB(S21)
Vctrl = 0V
|S21| = 1.94 dB @ 56 GHz
5.0
0.0
-5.0
-10.0
-15.0
-20.0
20.0
40.0
60.0
80.0
100.0
frequency GHz
dB
dB(S22)
dB(S11)
dB(S21)
Vctrl = 1.8V
0.0
-2.0
-4.0
-6.0
-8.0
-10.0
-12.0
-14.0
-16.0
-18.0
-20.0
|S21| = -1.95 dB @ 56 GHz
20.0
40.0
60.0
80.0
100.0
frequency GHz

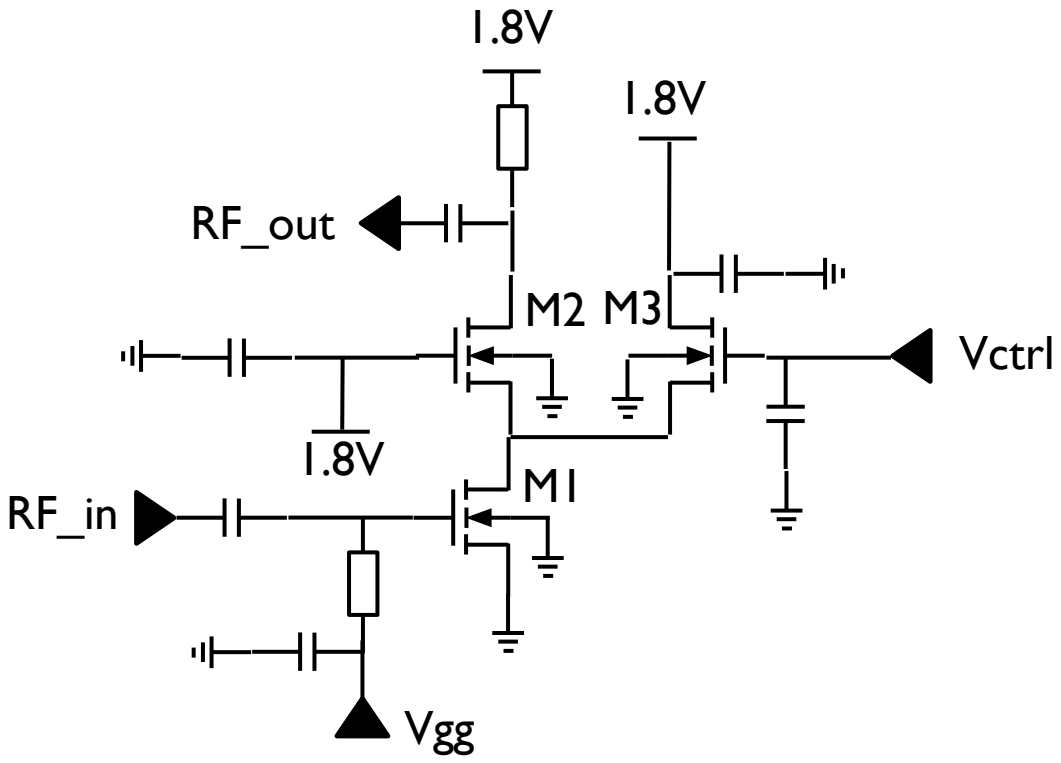
VGA - RESULTS

- 1.8 V and ground will be supplied externally via one of the Caravel analog IO pins
- Vgg and Vctrl will be supplied via Caravel GPIO used as analog pin
- Circuit will share 1.8V and Vgg pins with the LNA and PA, reducing the pin count to better accommodate all designs inside the user area
- RF pads plus accesses will be laid out inside the user area



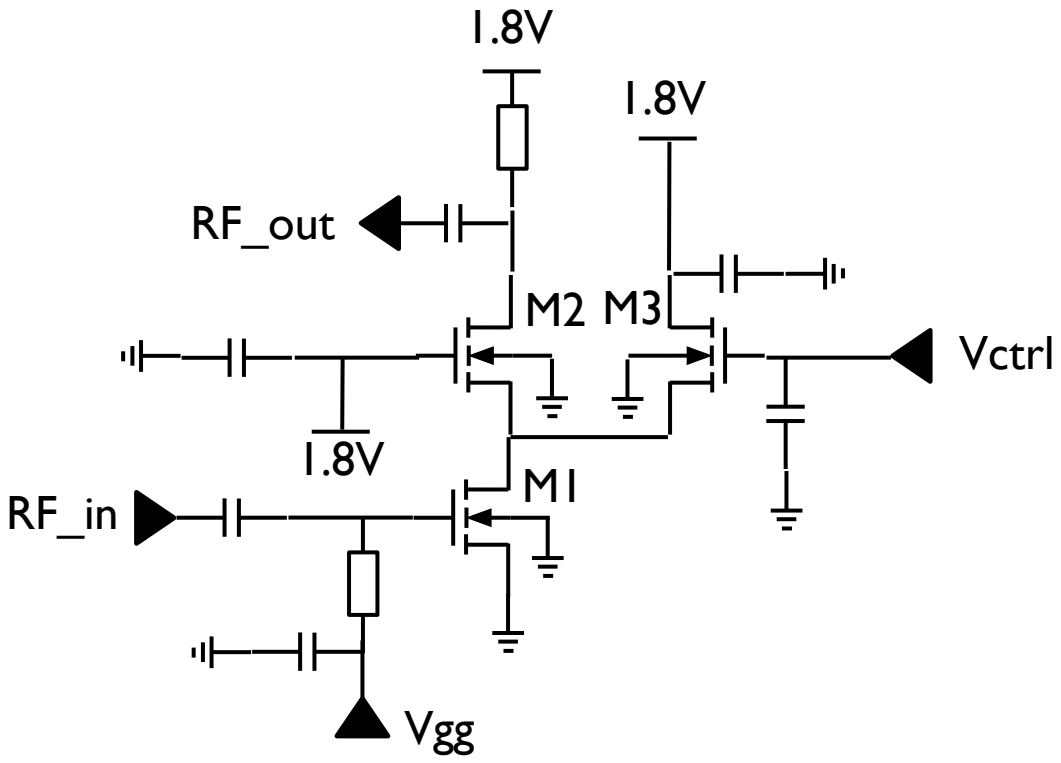
VGA – UNSIMULATED PORTIONS

- To-do: harmonic balance simulation to extract the non-linear behavior of this circuit
- AKA the 1 dB compression point and the 3th harmonic intercept points
- Plan: use ngspice script to run a nested .tran simulation, apply fft, measure the mag() of the fundamental and plot it against the input RF power



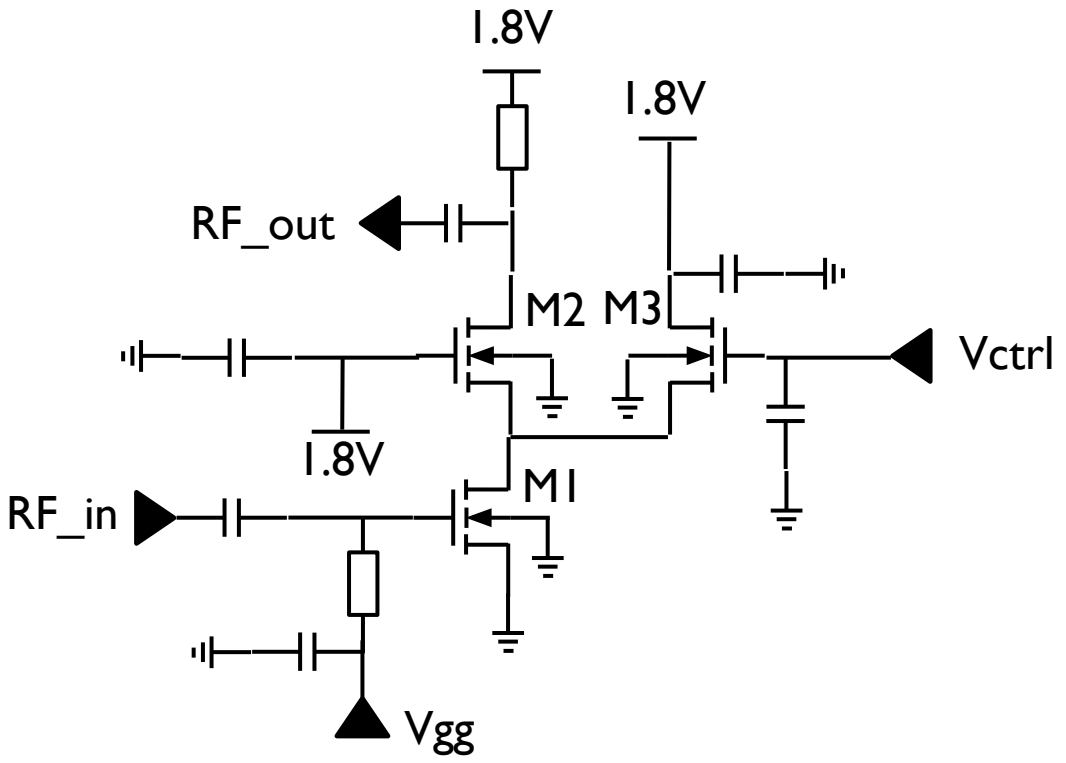
VGA – RESULTS VERSUS INITIAL GOALS

- Initial specs:
  - Maximum gain of 10 dB
  - Gain control range better than 20 dB (from -10 dB to +10 dB)
  - 10dB input and output bandwidth of 15% centered at 60 GHz
  - Typical DC power consumption of 20 mW per cell, maximum of 40 mW
  - Output 1dB compression point of -20 dBm.



VGA – RESULTS VERSUS INITIAL GOALS

- Schematic level simulation specs:
  - Maximum gain of 1.94 dB
  - Gain control range of 3.89 dB
  - 10dB input and output bandwidth of 5% centered at 60 GHz
  - Typical DC power consumption of 5.4 mW



Balanced to Unbalanced Transformer - BALUN

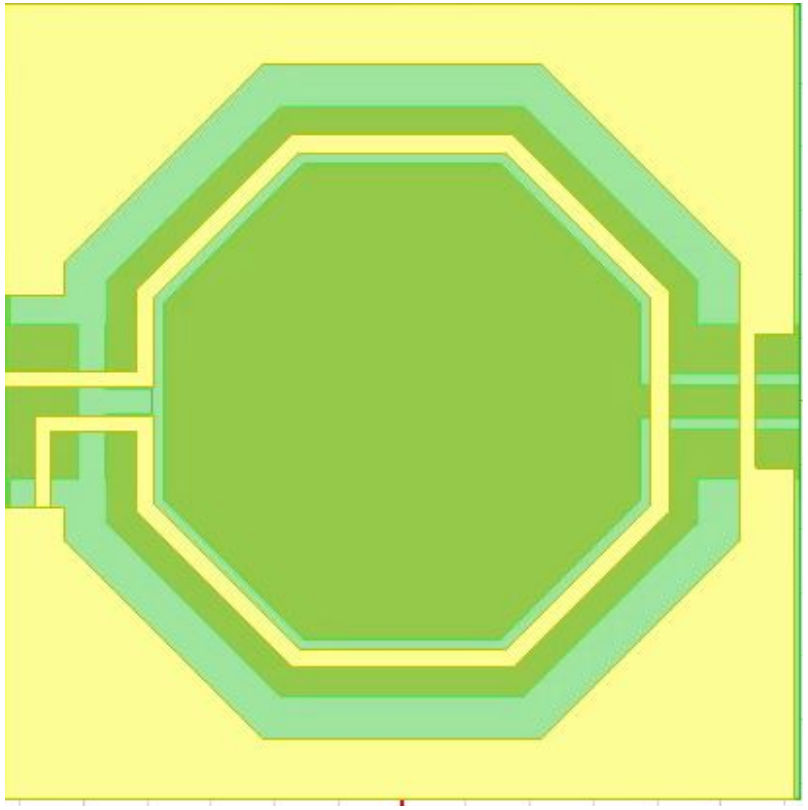
On-chip transformers are versatile components. They are commonly used as two- or three-port devices for impedance conversion, circuit isolation (DC decoupling, common mode rejection or RF chokes) or/and BALanced-to-UNbalanced (and vice versa) signal conversion. These characteristics make this element very common in building or connecting basic active blocks with the rest of the circuit of a millimeter-wave front-end.

In simulations, we can measure it as a two port device: one of them differential and the other single ended. That way, we can express the performance looking to the transmission (insertion loss) and reflected power (return loss).

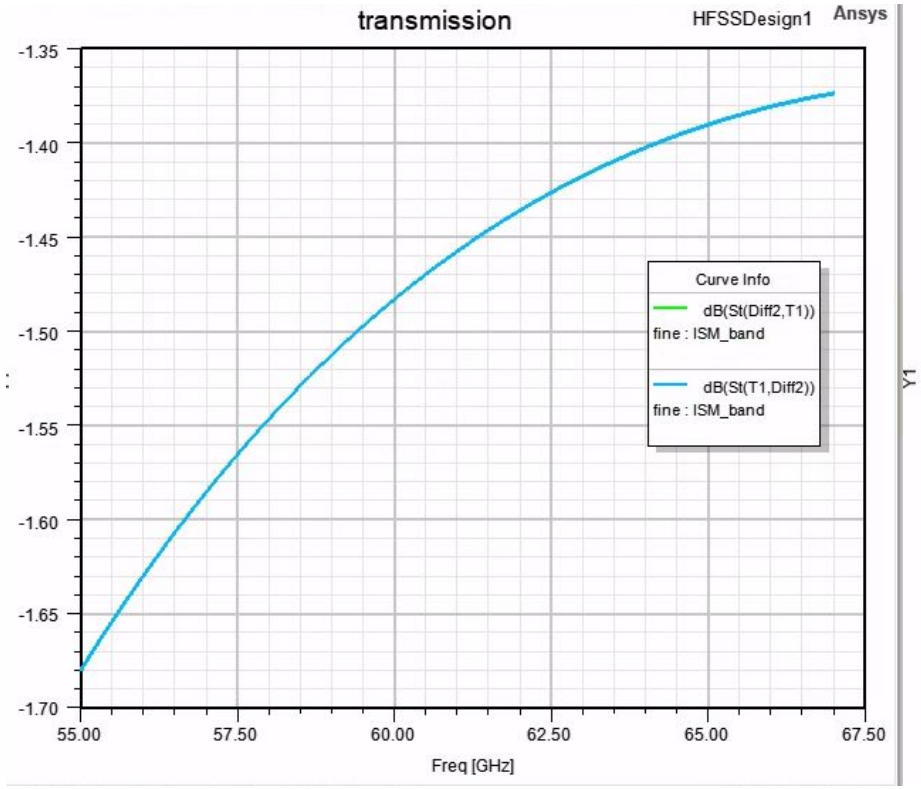
BALUN

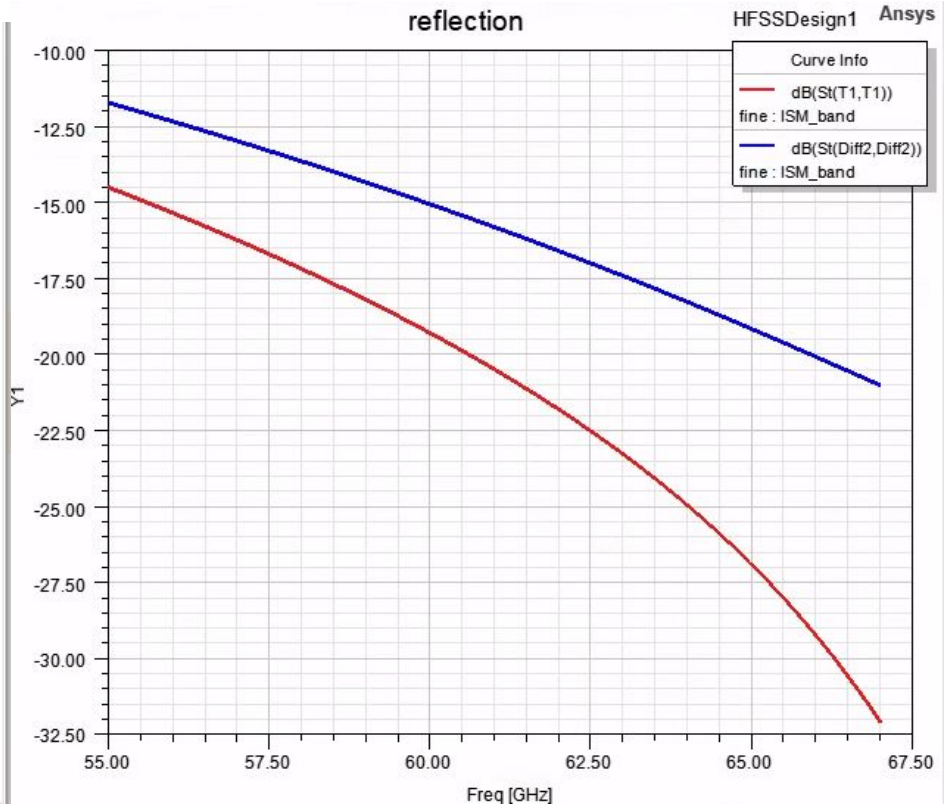
- Using a well-known octagonal winding shape, we created a coplanar waveguide structure;
- The primary is single-ended and is placed on metal 5; the secondary is differential and is in metal 4;
- The trace width is 4 um and the radius of the loop is aprox. 80um;

  Next step is to insert the RF pads into this layout.



BALUN - results





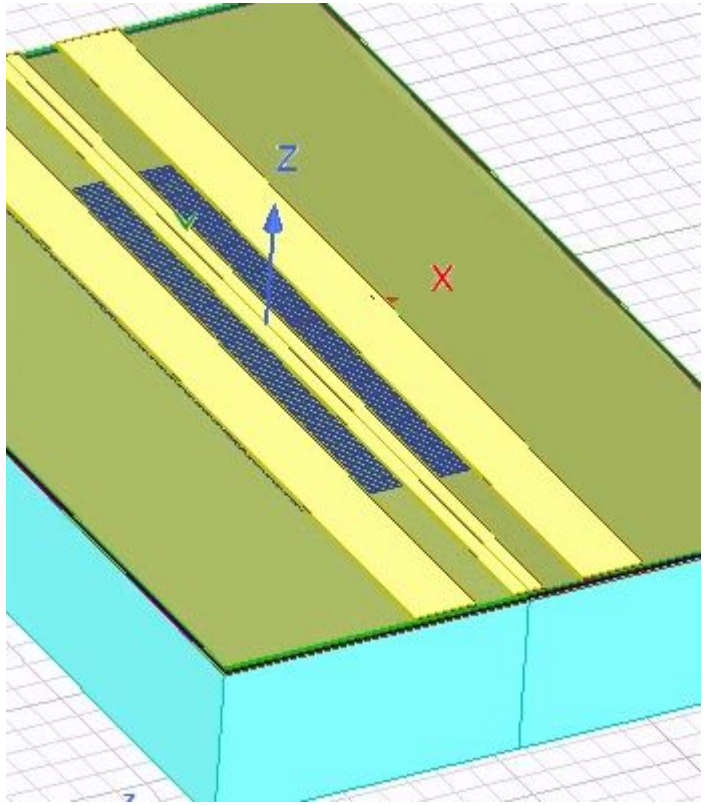
Slow-wave Transmission Line

A Coplanar Waveguide (CPW) transmission line was developed; by periodically adding transverse metal strips, placed over metal 2, it is possible to create a slow wave effect, in addition to preventing the electric field from penetrating the silicon.

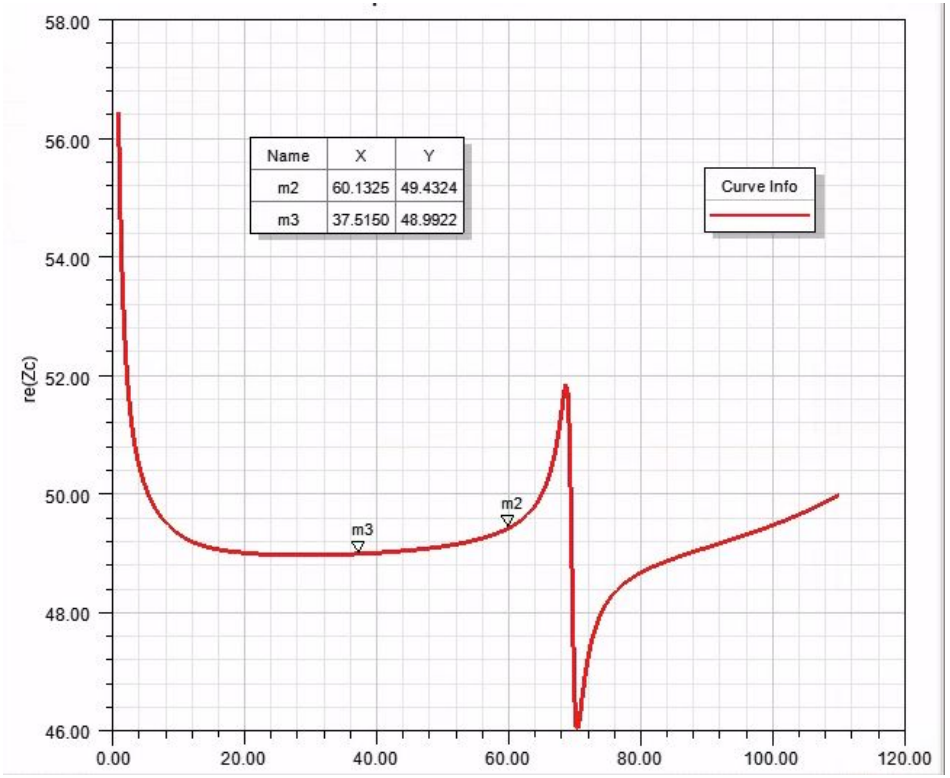
Our goal is to get a 50 Ohm transmission line with the highest quality factor (Q).

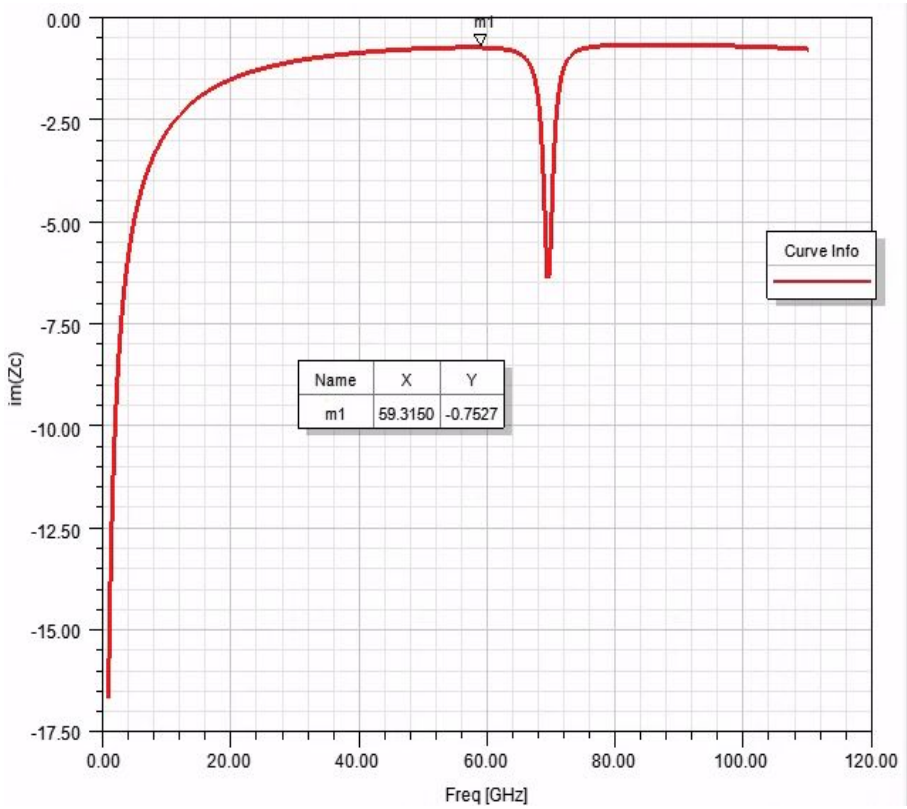
Dimensions:

Trace signal width: 24.4um
Trace ground width: 41.55um
Distance between above traces: 27.4um
Width of metallic strips: 0.45um
Metallic strips spacing: 3.1um



Slow-wave Transmission Line - results



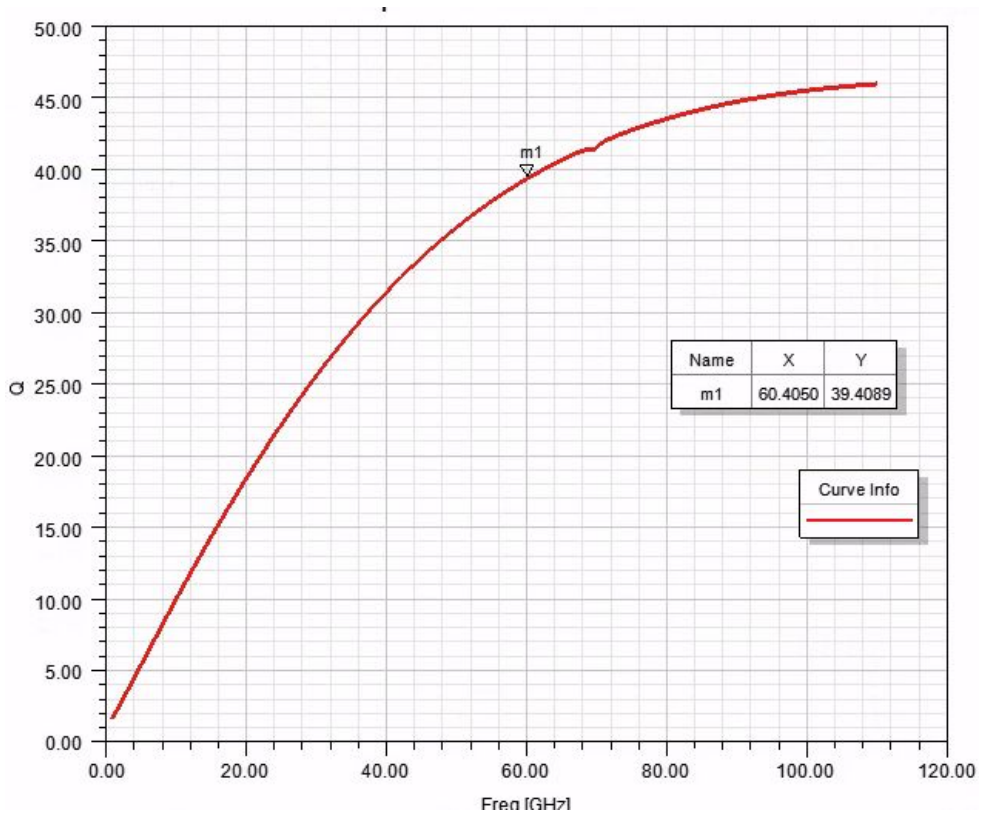


Slow-wave Transmission Line - results

The Quality Factor (Q) of a transmission line is a measure of how much energy the device stores in relation to how much it dissipates.

The figure on the side shows the Q of this line, which is calculated from the S parameters.

A	(((1+S11corr)*(1-S11corr)+S12cor*S12cor))/(2*S12cor)
B	50*(((1+S11corr)*(1+S11corr)-S12cor*S12cor))/(2*S12cor)
C	1/50*(((1-S11corr)*(1-S11corr)-S12cor*S12cor))/(2*S12cor)
Q	beta/(abs(2*re(gamma)))
S11corr	(S11+S22)/2
S12cor	(S12+S21)/2
Zc	sqrt(B/C)
beta	abs(teta/(silicon_l-dem*2))
er_eff	(3e8*beta/(2*pi*freq))^2
gamma	Acosh(A)/(silicon_l-2*dem)
teta	if(cang_rad(S12cor)>0,cang_rad(S12cor)-3.1415,cang_rad(S12cor))



Instead of the detector.. a switch

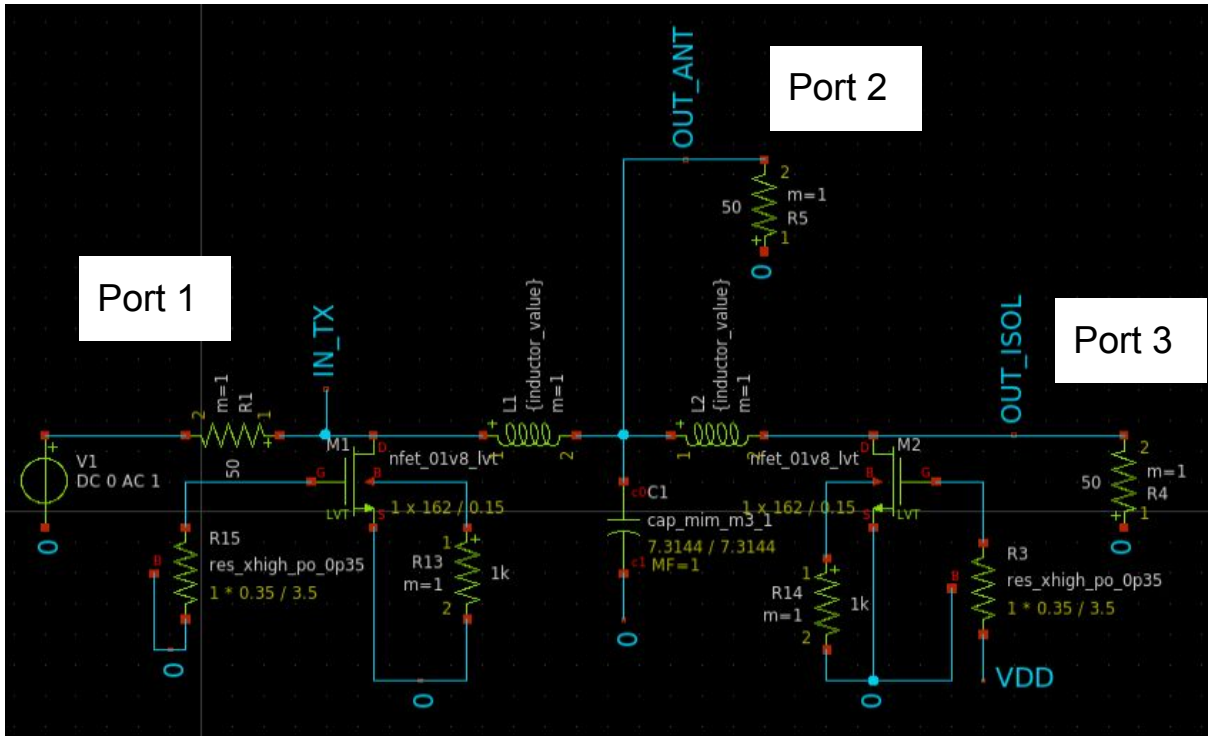
Our goal with the detector was to sample the forward signal. However, we didn't notice that sampling the signal without a directional coupler would measure the standing wave voltage (VSWR) at line point, and this changes as the load (or RF probe) changes. In general, directional couplers are implemented as distributed devices (transmission lines) using microwave techniques, which take up a considerable amount of space on the chip (proportional to the guided wavelength).

Therefore, we prefer not to implement this device. In this place, we will implement a Double Pole Single Throw (DPST) switch, which is very useful in adaptive circuits. Our device will be designed to be use in the front-end of a communication electronics device, allowing the same antenna to be shared between transmit and receive.

Switch - schematic

Notice that:

- signal leaving the circuit (IN_TX node) is divided between two paths: antenna (OUT_ANT) and isolation (OUT_ISOL) path.
- the directivity is measured as the S(2,1) parameter and must be maximized. The isolation, S(3,1), and should be minimized.



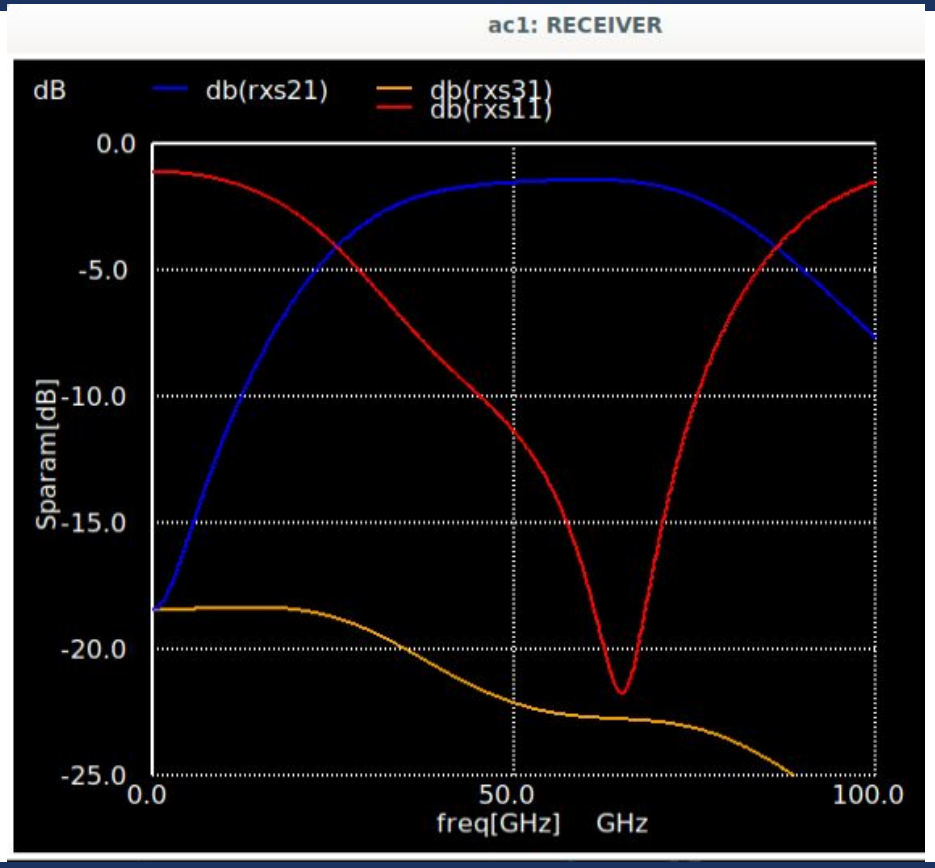
Switch - design flow

- The circuit was based on reference [A7];
- First, the off-capacitance and on-resistance per unit width of the transistor was estimated using the low-voltage 1.8V NMOS PDK MOSFET model; the formulas of the article give us a start point for the value of capacitance and inductances;
- Several Parameter Sweep Simulations were performed to obtain the final results for the components; this step would have been easy if we had been able to use ASCO optimization software;
- All simulations were analyzes of small AC signals, which were then transformed into parameter values. The next objective is to perform a power sweep to see the 1dB compression point of this switch.

Switch - results

For the reception path, the simulation shows:

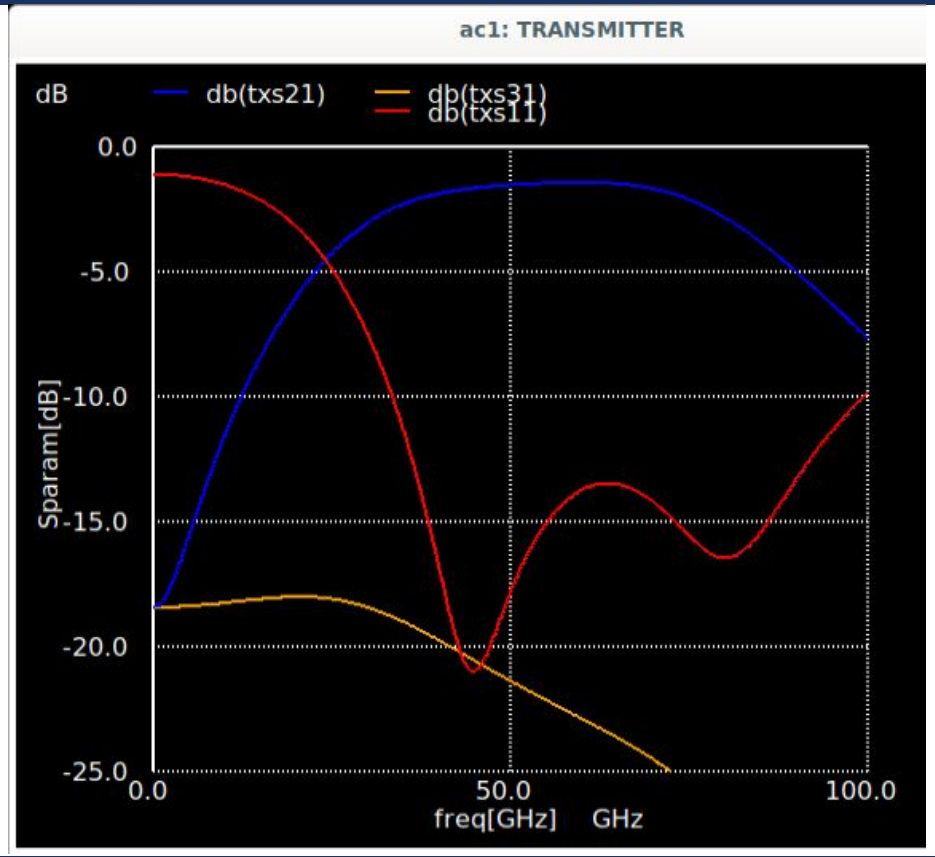
- return loss > 10dB for the range of 45 to 75 GHz;
- maximum insertion loss of 1.45 dB@~60GHz;
- minimum insertion loss for the 60 GHz ISM of 1.7 dB.



Switch - results

For the transmission path, the simulation shows:

- return loss > 10dB for the range of 38 to 99 GHz;
- maximum insertion loss of 1.43 dB@~60GHz;
- minimum insertion loss for the 60 GHz ISM of 2.1 dB.



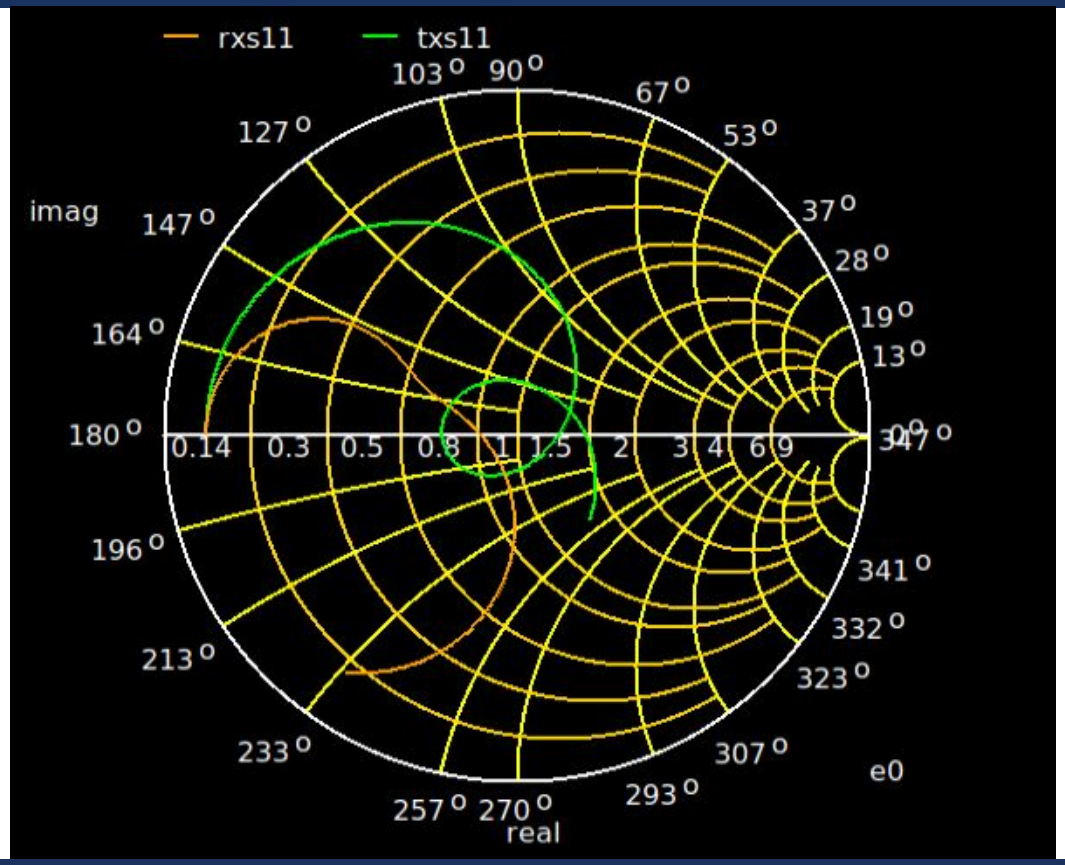
Switch - results

This figure shows the S(1,1) simulation from 50 MHz to 100 GHz and is put here to show the ngspice plotting capacity.

```
.param inductor_value=105p
*.param capacitor_value=107f
.save all
.control
op
ac lin 801 50e6 100e9
let txS11=2*IN_TX-1
let txS21=2*OUT_ANT
let txS31=2*OUT_ISOL

let rxS11=2*IN_ANT-1
let rxS21=2*OUT_RX
let rxS31=2*OUT1_ISOL

plot rxS11 txS11 smithgrid
.endc
```



Switch - state of the art

References	[S1]	[S2]	[S3]	[S4]	[S5]	[S6]	This work, for a while
Technology	90nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	55nm CMOS	55nm CMOS	130nm CMOS
Frequency [GHz]*	50-94	58-85	60-110	94-110	85-95	70-100	45-75
Max. Insertion [dB]	3.3	1.8	3-4	4.2	3.2 (TX) 3.6 (RX)	3.5	1.43
Max. Isolation [dB]	27	22	25	25	25 (TX) 20 (RX)	18	~25

* Measure as >10 dB return loss

Power Amplifier - PA

The PA consist of three single-ended, common-source stages biased in class A.

The first stage is biased at the peak fmax bias of 0.2mA/μm to maximize gain while its source degeneration inductance is set to LS = Z0/2πfT for 50-Ω matching. The second and third stages are biased at the optimum linearity current density of 0.28 mA/μm. The transistor width and bias current of the last stage are derived from load-line theory.

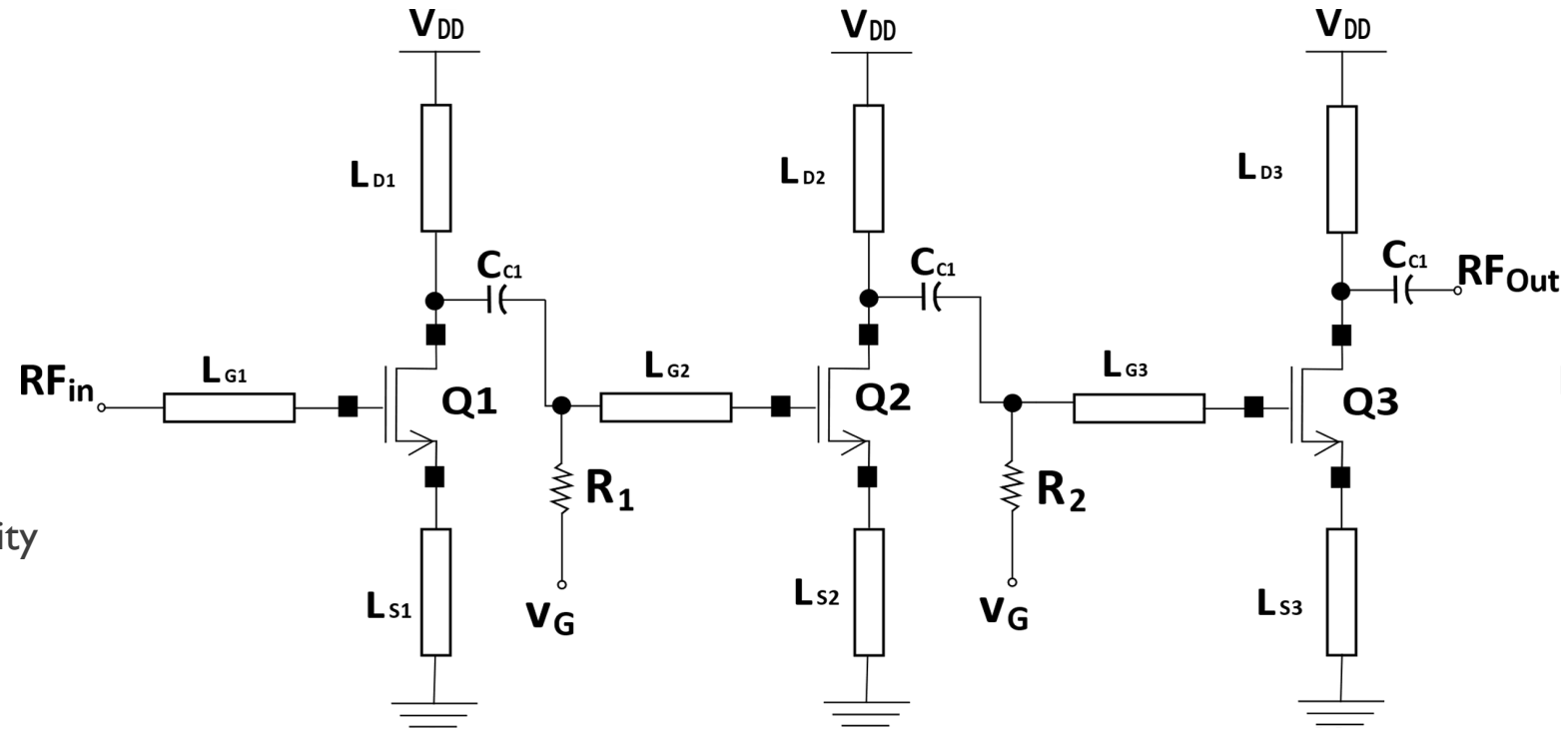
PA

Application: high data-rate wireless transmission

and mm-wave sensors

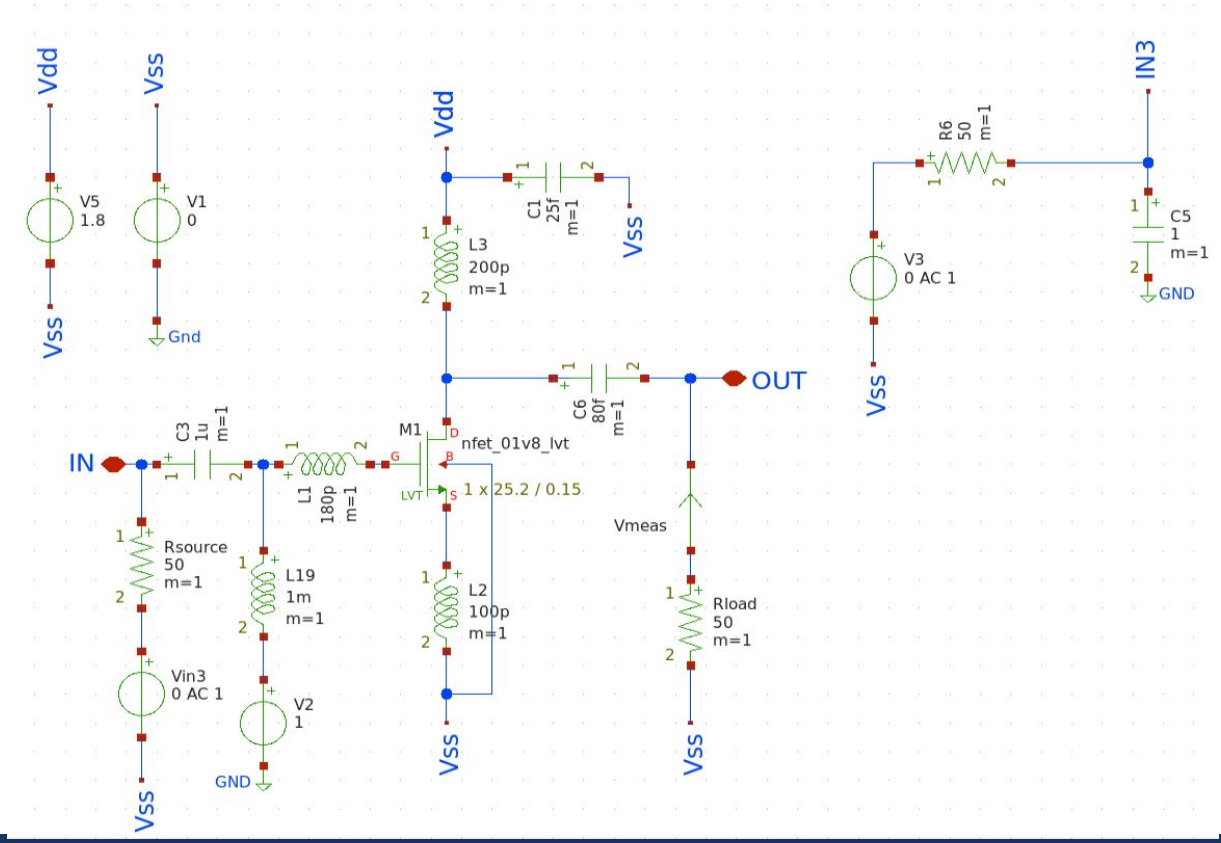
Main characteristics requirements:

- Class A, 3-stage CS topology
- Input /Output match 50Ω
- Branch currents scaled for optimal linearity



PA - results

- PA first stage test in 1.8V
- W =806µm, L = 4.8µm
- Input matched by LG and LS

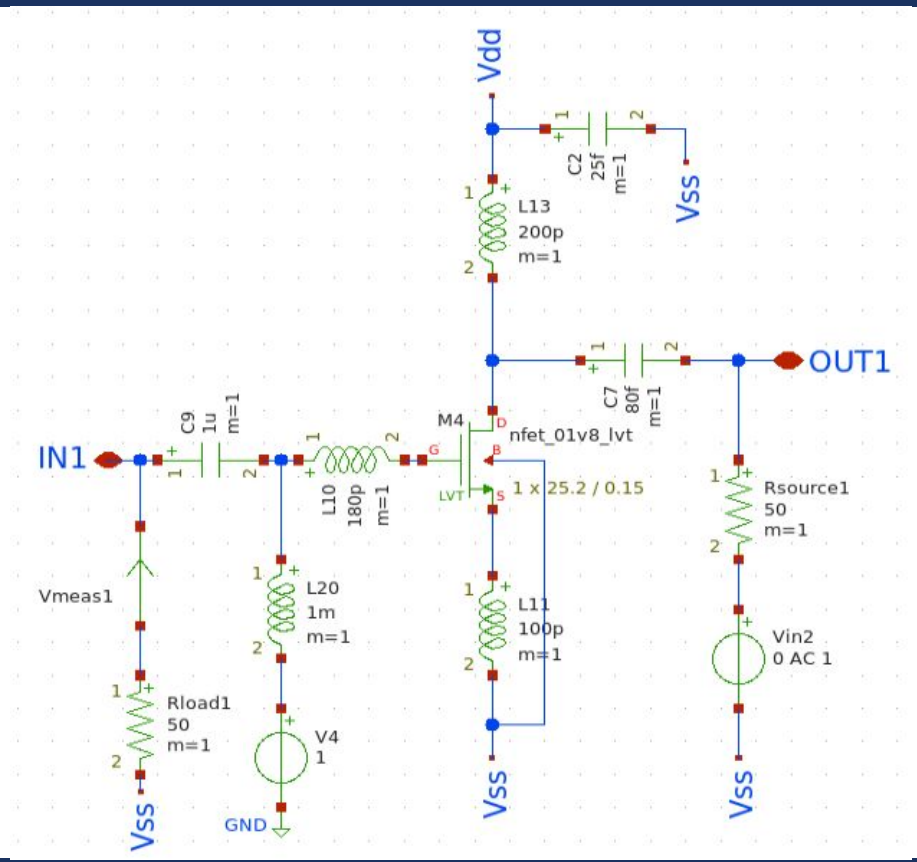


PA - results

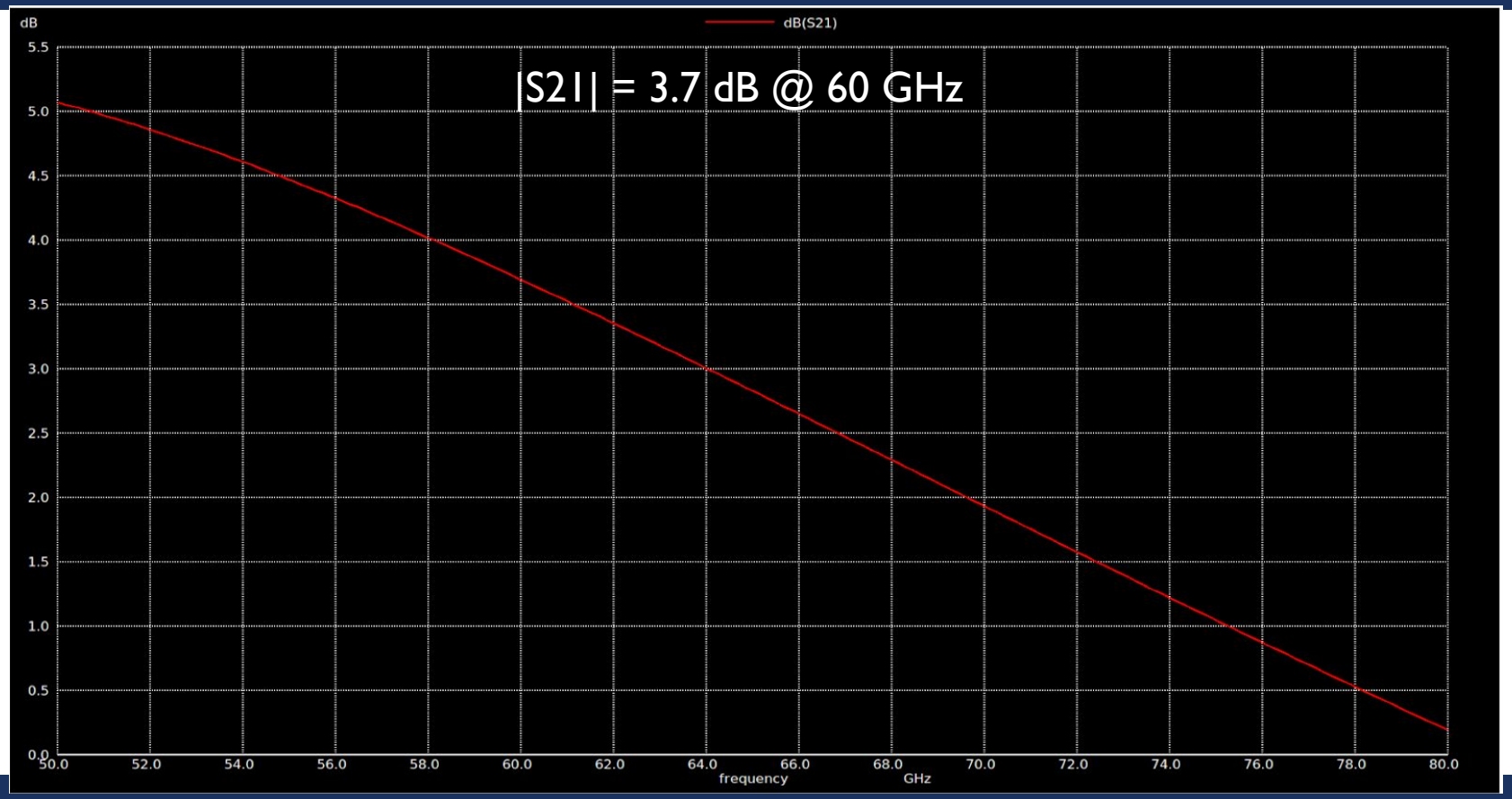
TT_MODELS

s1

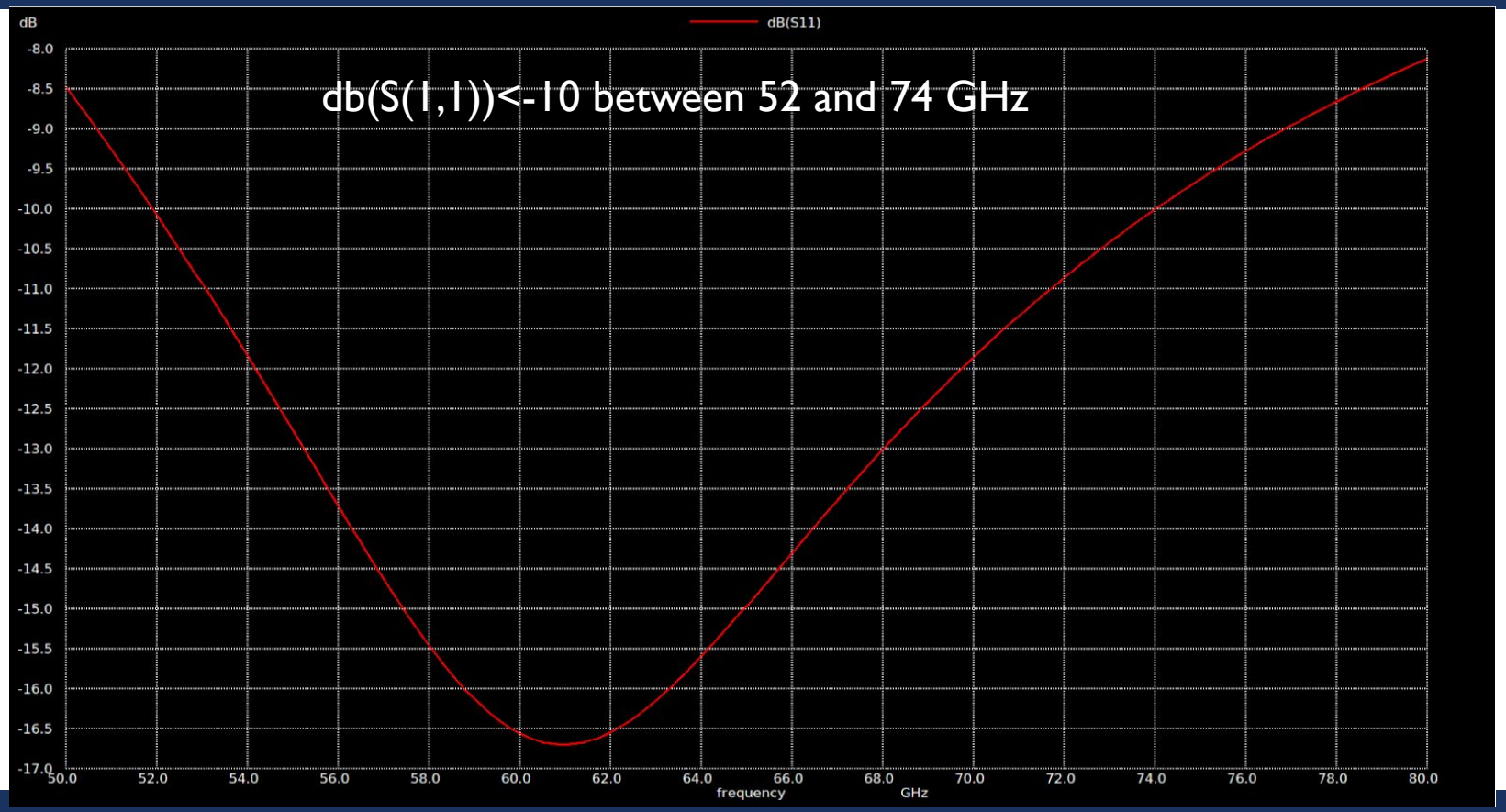
```
.save all
.control
op
ac lin 201 50e9 80e9
let S11=2*IN-1
let S21=2*OUT
let S22=2*OUT1-1
let S12=2*IN1
let S33=2*IN3-1
settype s-param S11 S21 S22 S12
let Rbase=50
let delta=(S11*S22)-(S21*S12)
let K=(1-(mag(S11))^2-(mag(S22))^2+(mag(delta))^2)/(2*mag(S12*S21))
let MSG=mag(S21)/mag(S12)*(K-sqrt(K^2-1))
let Y33=(1/50)*(1-S33)/(1+S33)
let freq=im(Y33)/(2*3.1415)
let Y11=((1-S11)*(50+S22*50)+S12*S21*50)/((50+S11*50)*(50+S22*50)-S12*S21*50*50)
let Y22=((1-S22)*(50+S11*50)+S12*S21*50)/((50+S11*50)*(50+S22*50)-S12*S21*50*50)
let Y21=(-2*50*S21)/((50+S11*50)*(50+S22*50)-S12*S21*50*50)
let Y12=(-2*50*S12)/((50+S11*50)*(50+S22*50)-S12*S21*50*50)
let Z11=Y11/((Y11*Y22)-(Y21*Y12))
let Z22=Y22/((Y11*Y22)-(Y21*Y12))
save S11 S12 S21 S22
wrs2p transPA1_2p.s2p
.endc
```



PA - results


dB
dB(S21)
|S21| = 3.7 dB @ 60 GHz
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
50.0
52.0
54.0
56.0
58.0
60.0
62.0
64.0
66.0
68.0
70.0
72.0
74.0
76.0
78.0
80.0
frequency
GHz

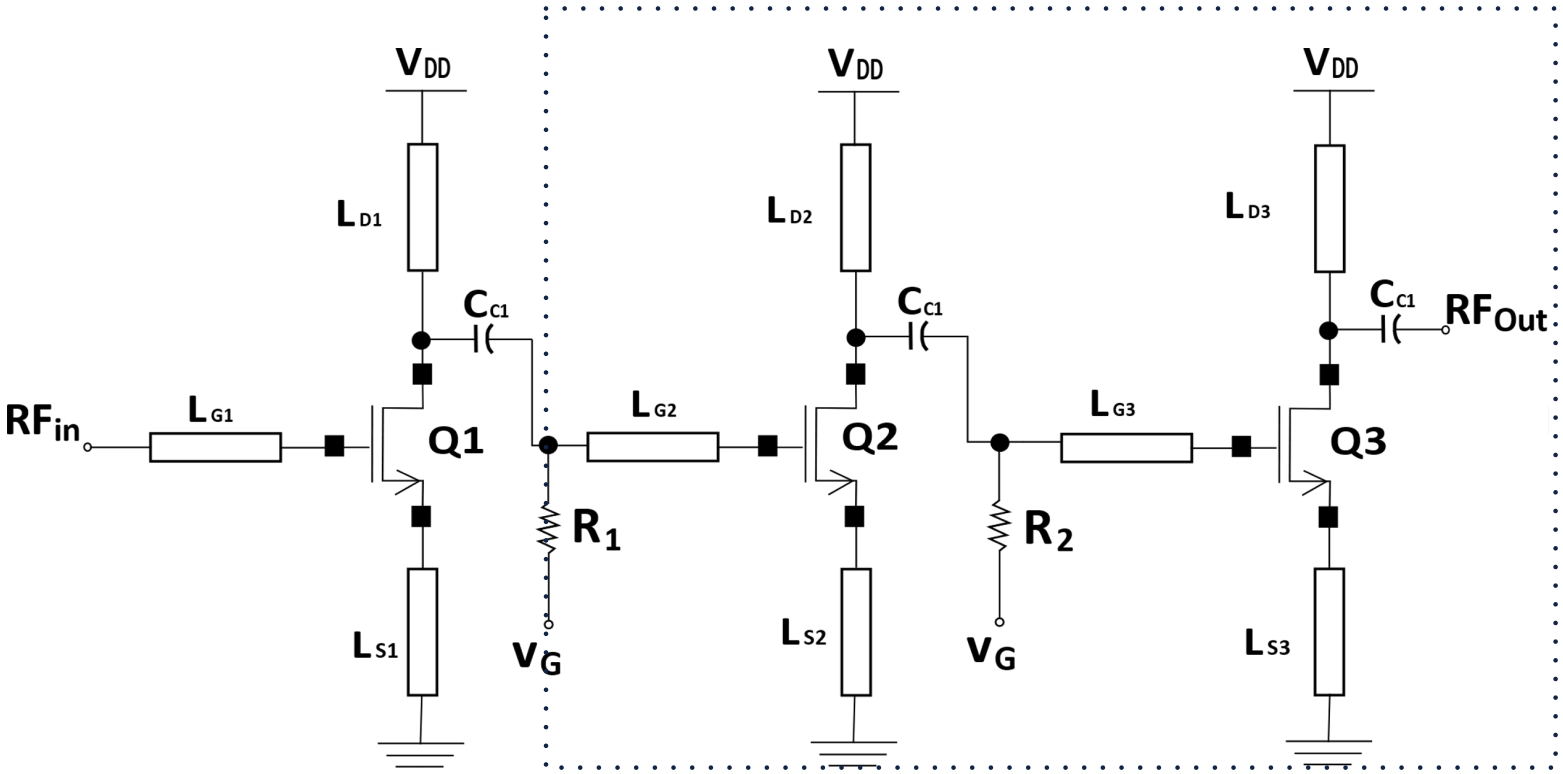
PA - results



db(S(1,1))<-10 between 52 and 74 GHz

PA – next steps

Output matching need to be stage to stage
Plan: create a new testbench to first stage matched the output
for second stage to matched, and after all schematic design a conjugate matching network



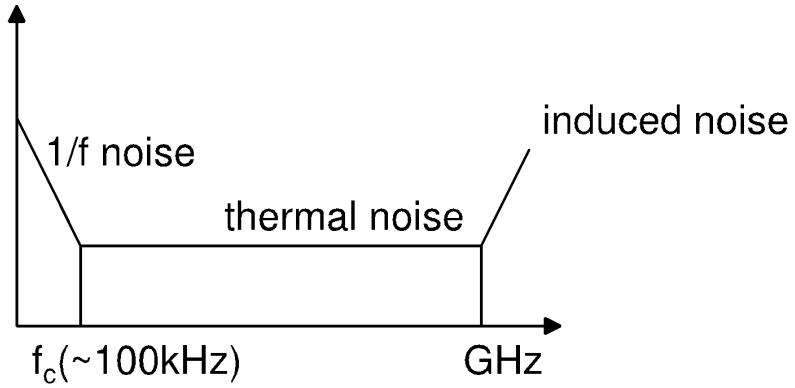
Low Noise Amplifier - LNA

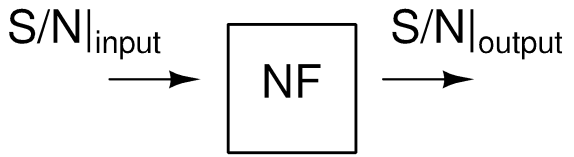
The presented RF/Analog block - LNA for the specific frequency of 60GHz is a viable option for new uses in bands such as Automotive and telecommunications applications. Although it is a challenging project, especially considering elements not present in commonly used bands, a standardized and widely known procedure is followed, the use of simulation tools and the available PDK opens new ways and forms for tests and prototypes of this type, at its In turn, it shows inconveniences that allow to document and consider for future new versions.

LNA - noise considerations

Transistor sources:

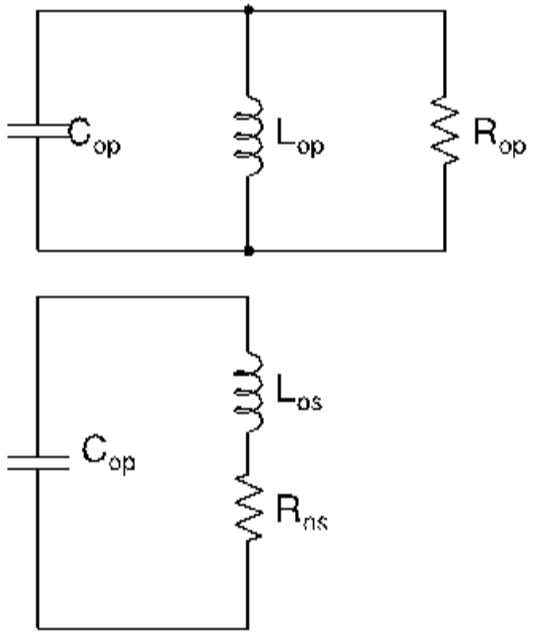
- Drain noise (thermal and flicker (1/f))
- Gate noise (routing parasitic, induced)
- Multiple fingers are recommended





LNA - LC TANK

- To increase the Q factor: ↑ R_{op} ; add series inductor with L_{op}



$$\boxed{R_{op} = R_{os}(1 + Q^2)}$$

$$\omega_o = 2\pi f_o$$

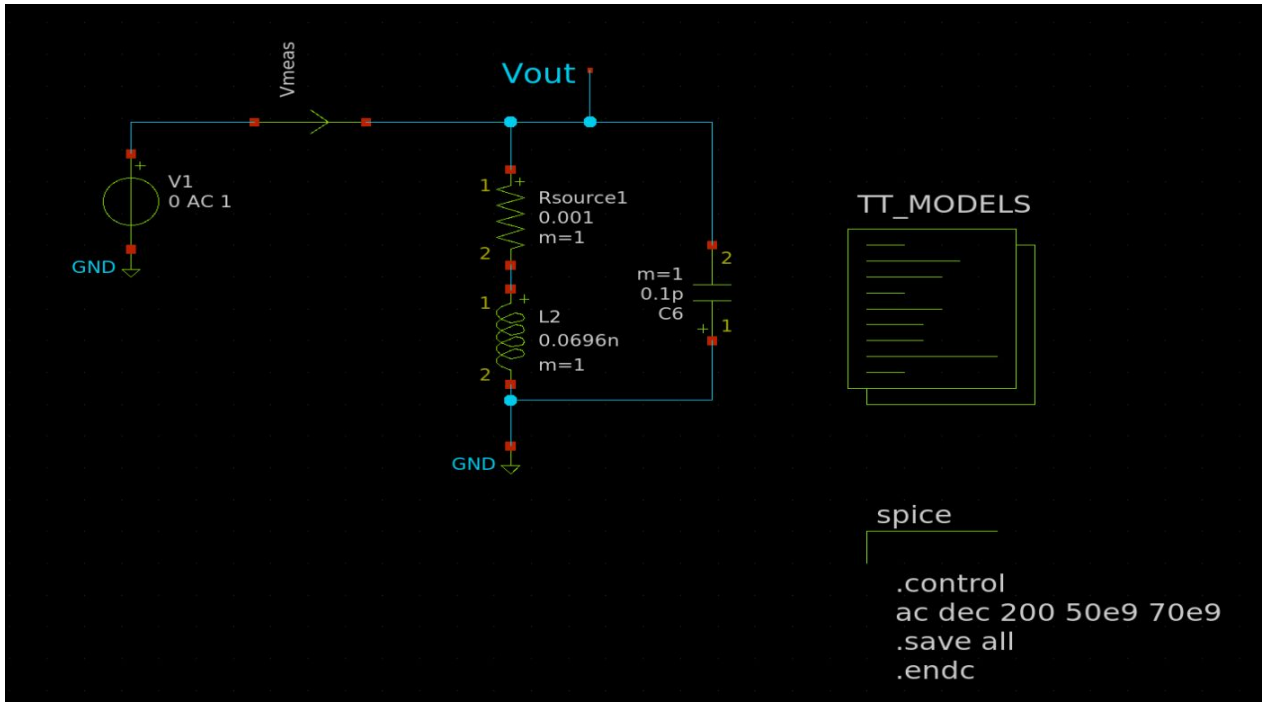
$$R_{os} = \frac{\omega_o L_{os}}{Q_{out}} \qquad C_{op} = \frac{1}{\omega_o^2 \cdot L_{op}}$$

$$\boxed{L_{op} = L_{os}(1 + 1/Q_{out}^2)}$$

$$\boxed{C_{os} = C_{op}(1 + 1/Q_{out}^2)}$$

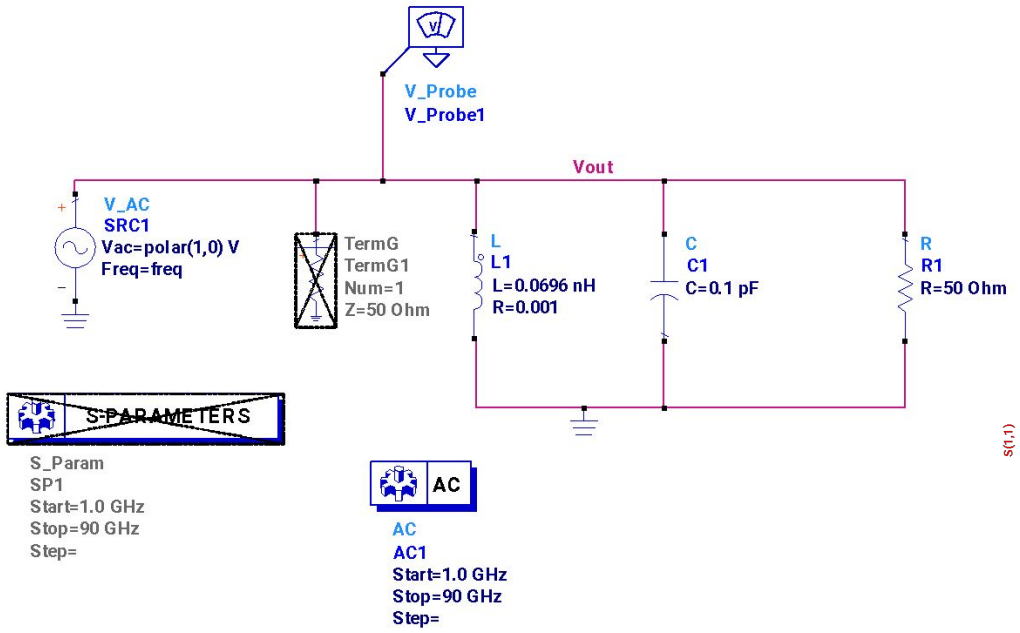
LNA - LC TANK

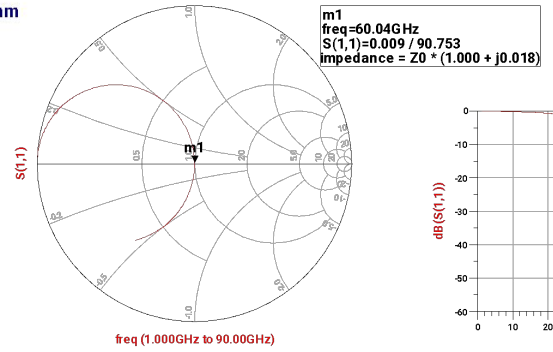
- To increase the Q factor: ↑ R_{op} ; add series inductor with L_{op}

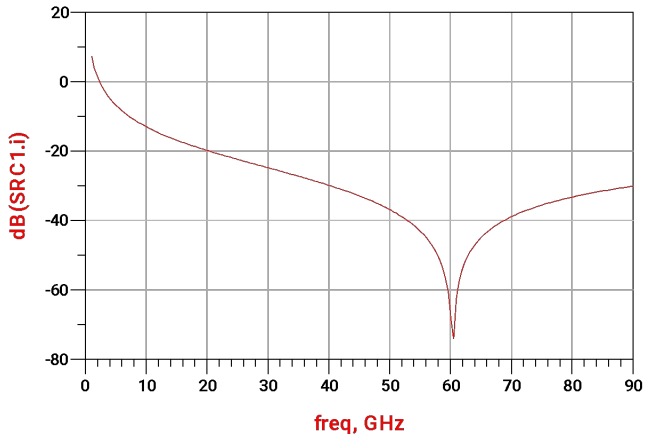


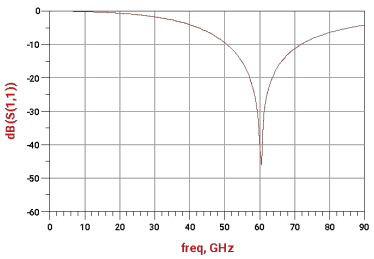
LNA - LC TANK

- To increase the Q factor: ↑ R_{op} ; add series inductor with L_{op}



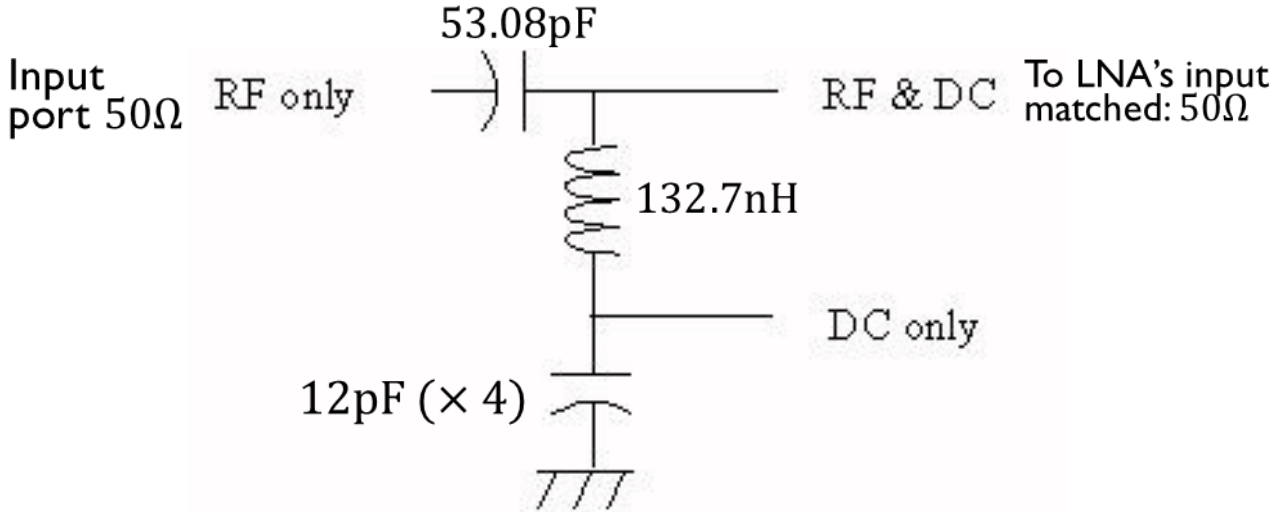




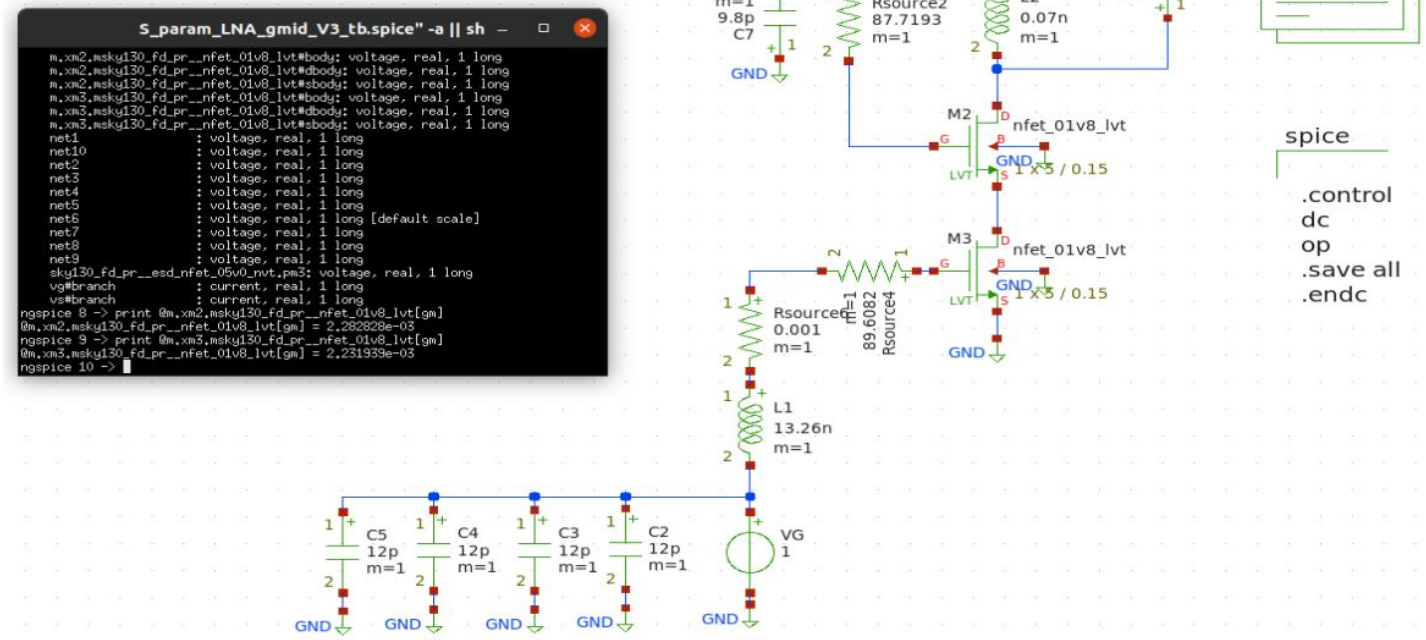


LNA - INPUT BIASING - T BIAS

- T bias, ratio :1000 @60GHz



LNA - DC OP CONDITIONS: NON QUASI STATIC ANALYSIS



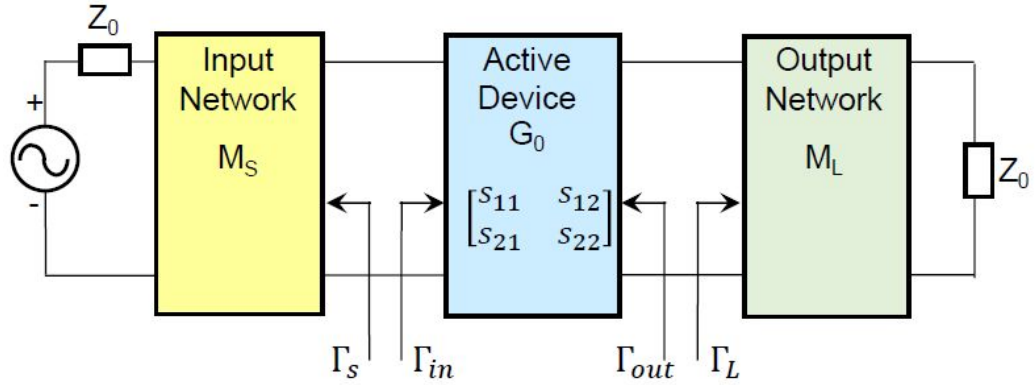
$$R_{source2} = \frac{1}{5 \times gm_{M2}}$$

$$R_{source4} = \frac{1}{5 \times gm_{M3}}$$

LNA - MATCHING

$$G_{max}(\Gamma_S, \Gamma_L, S) = \frac{P_{av,out}}{P_{del,in}} = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}), K \geq 1$$

K=Rollet stability factor



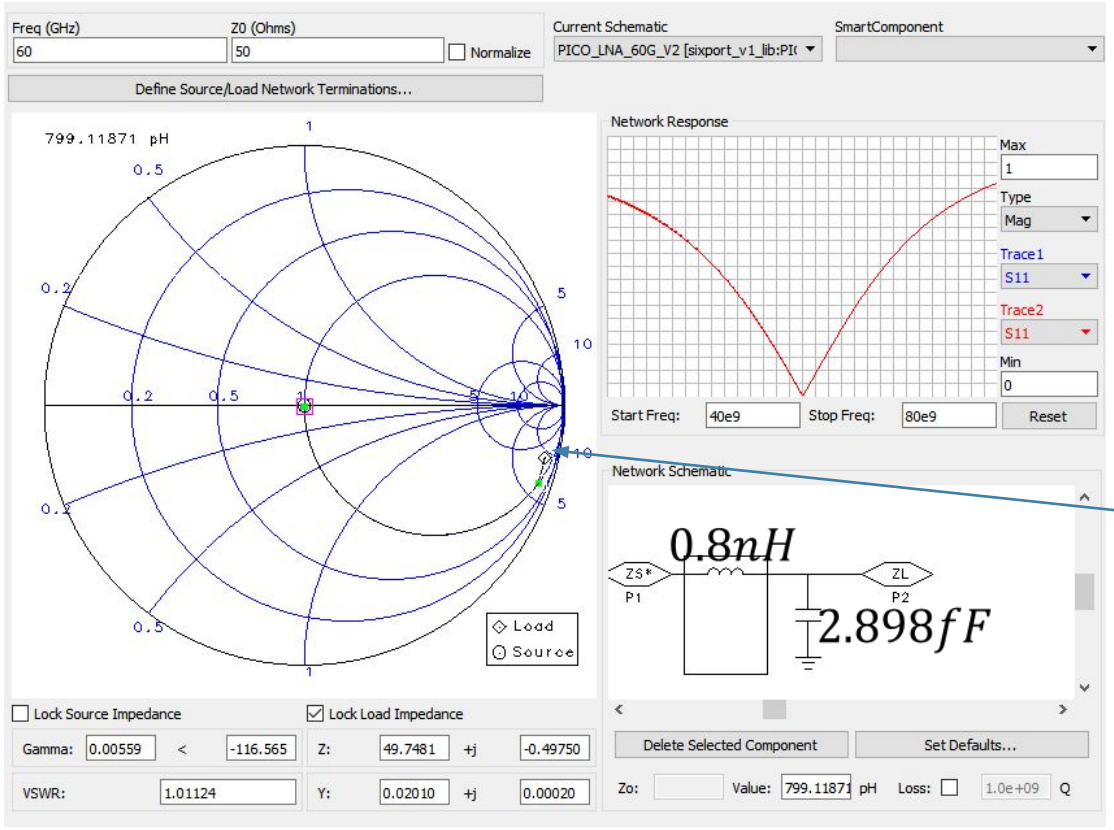
$\Gamma_{in} = \Gamma_S^*$ $\Gamma_{out} = \Gamma_L^*$

$Z_{in} = 110.57 - j440.981[\Omega]$
$Z_{out} = 13.622 - j25.788[\Omega]$

Simultaneous conjugate matching

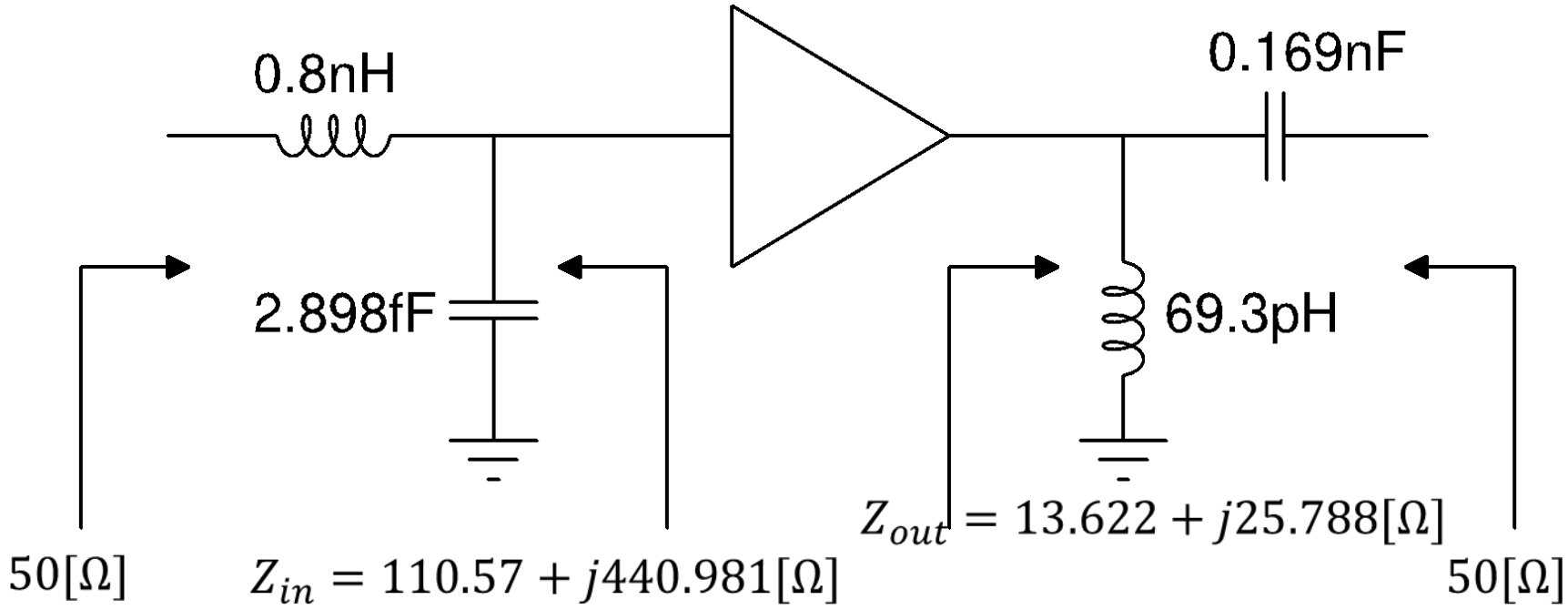
$\Gamma_S = 0.948\angle 12.2°$
$\Gamma_L = 0.65\angle 122.6°$

LNA - MATCHING

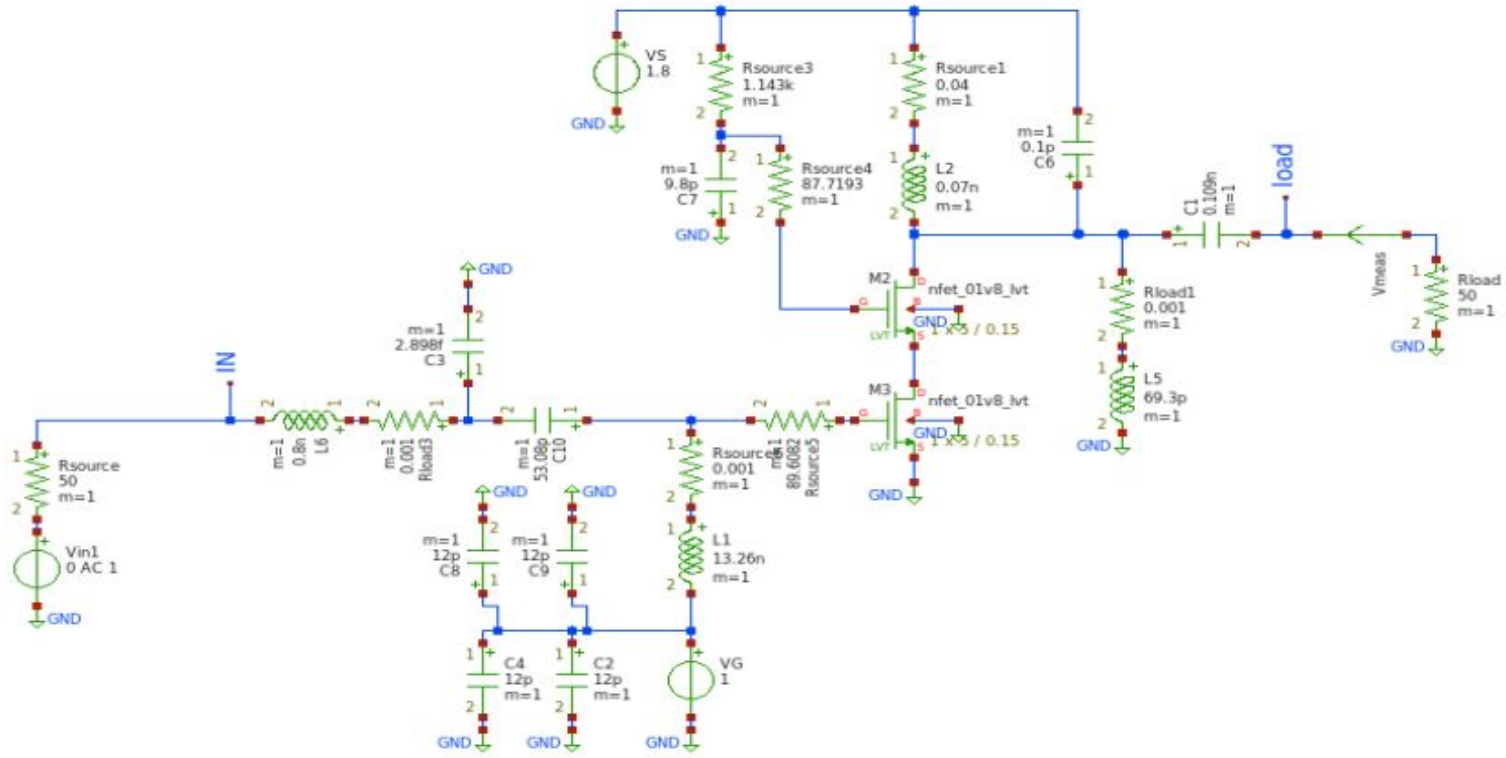


$$Z_{in} = 110.57 - j440.981[\Omega]$$

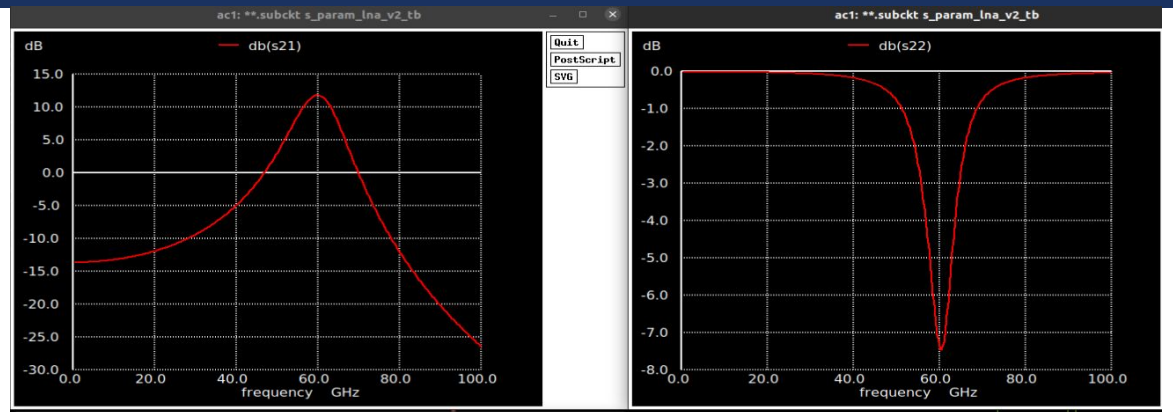
LNA - MATCHING

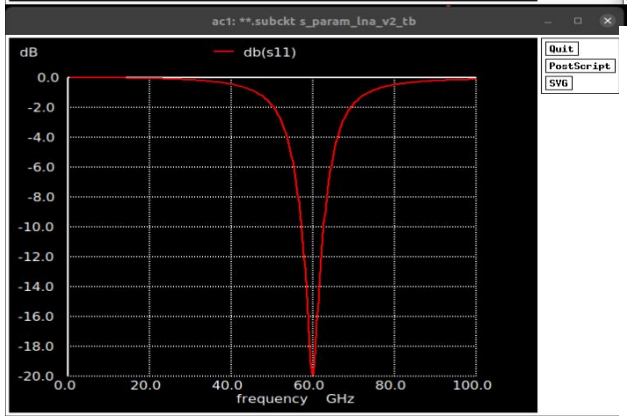


LNA - MATCHING



LNA - results



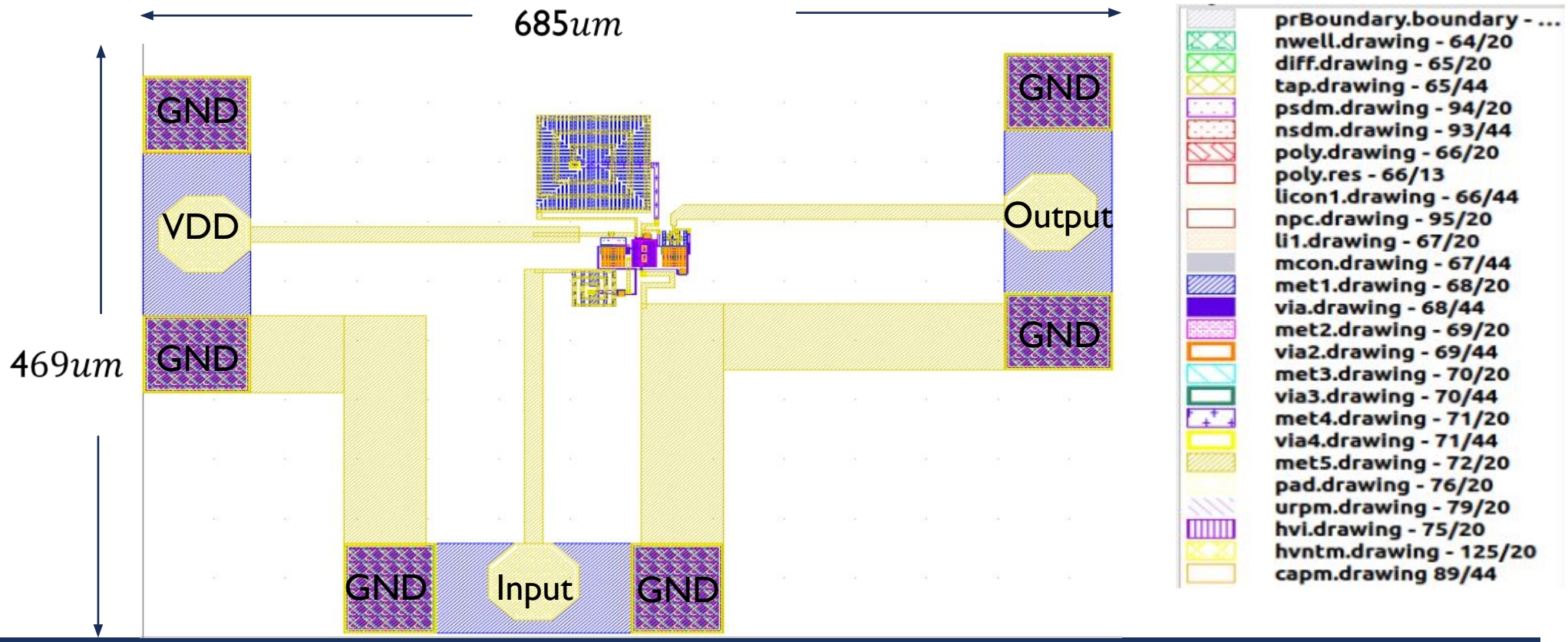


S(11) @60GHz	-19.75 dB
S(22) @60GHz	-7.48 dB
S(21) @60GHz	12 dB

LNA - next steps

- Procedure for noise analysis in Xschem.
- Add gm/Id analysis for amplifier gain improvement.
- Replace ideal models by micro stripline sub-blocks.
- Post layout simulations.
- Inter-blocks integration in layout.
- Post layout stability circles analysis.

LNA - early layout



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[S5] L. Chen et al., "A 90-GHz asymmetrical single-pole double-throw switch with >19.5-dBm 1-dB compression point in transmission mode using 55-nm bulk CMOS technology", IEEE Trans. Circuits Syst. I Reg. Papers, vol. 68, no. 11, pp. 4616-4626, Nov. 2021.
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[S7] J. He, Y. -Z. Xiong and Y. P. Zhang, "Analysis and Design of 60-GHz SPDT Switch in 130-nm CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 10, pp. 3113-3119, Oct. 2012, doi: 10.1109/TMTT.2012.2211380.

OUR DESIGNS AND CARAVEL

- Estimated total area of all our circuits (plus test devices): 4 mm^2
  - The 5 circuits presented here will be laid out to make most use of the area and to accommodate the contributions of teams USA1 and Austria
  - The test devices, which are very compact, will be placed in the empty spaces
- Number of pins after sharing:
  - 5 caravel analog pins
  - 3 GPIOs used as analog
- For the "internal" pin share, there are two options:
  - 1) Group the 5 circuits in two larger blocks (LNA+PA+VGA and Switch+VCO) to only use the 8 pins available
  - 2) Lay out each circuit and add an extra ground pad inside the layout of each circuit
- Pin routing will be done as follows:
  - For low impedance inputs and outputs: routing will be done in M5 to minimize IR drop
  - For high impedance inputs: routing will be done in M3, using M4 as interconnection layer

OUR DESIGNS AND CARAVEL

- Layout strategy for devices
  - MOSFET: multi-finger layout to improve performance in mmW
  - MIM capacitor: accesses done in the topmost metal of the device (M4 or M5), ground plane cut beneath the capacitor to reduce parasitic shunt capacitance to ground or substrate. A guard ring will be studied.
    - MOM capacitors, if needed, will be laid out in a completely custom way, also with guard ring and shield
  - SCPW, planar inductors: custom layout based on their design and simulation results, avoiding routing signals in LI because of its high sheet resistance. Inductors will receive custom LI+P+ guard rings to reduce substrate currents
  - MOS varactor: varactor bank will be laid out using multiple devices in parallel, gate as fixed bias, source/drain as bias input, substrate guard ring on each varactor to minimize cross-talk
  - Poly resistors: input and output in M1, guard ring grounded to reduce substrate currents

PLAN FOR NEXT WEEKS

- Chipathon deadlines
  - October 31st - circuits (almost) ready for tape-out
  - November 14th - tape-out deadline

- Our deadlines
  - October 7th - Active cells and passives laid out, DRC + LVS clean and PEX
  - October 14th - Final design ready, DRC + LVS clean locally
  - October 21st - Top cell DRC+LVS clean, mock caravel placement ready
  - October 28th - Buffer week to solve bugs and other (or any) unforeseen problems
  - November 4th - Coordinate with USA1 and Austria the final circuit placement plus pin routing
  - November 11th - Placement+routing ready, final pre-check ready
  - November 14th - The big day

LAYOUT STRATEGIES

- Active blocks: M5 inputs and outputs, M1 ground plane, Minimize ground inductance and propagation losses. MOSFETs have ft ~ 70 GHz, which pose real design issues. Thus, minimizing parasitics is paramount. This means that we're willing to sacrifice matching to reduce parasitics.

- Passive blocks: M5 signal, M1 ground (for microstrip-like structures and inductors), M1 or M2 for floating shield (SCPW). Since the metals are thin (1.2 um for M5, 845 nm for M4-3, 360 nm for M2-1) and not copper (which has about half of aluminum's resistivity), reducing propagation losses in the form of ohmic losses is paramount. Thus, M5 will be used as signal, and whenever possible, a M5+M4 combination will be studied.