NVIDIA Jetson AGX Xavier Developer Kit Carrier Board

Specification

SP-09778-001_v2.1 | June 2020

Document History

SP-09778-001_v2.1

Version	Date	Description of Change
1.0	August 9, 2018	Initial Release
1.7	July 24, 2019	**General** • Updated to use Jetson AGX Xavier throughout doc **Introduction** • Updated USB connections in main block diagram • Updated board placement figures **USB** Updated figure: • Added details of HDMI_DP connections • Added DP_AUX connections • Removed UPHY lanes not involved in USB-C connections **HDMI** Updated figure: • Added load switch & enable pin • Changed module pin names to be specific to HDMI_DP2 **UFS / Micro SD** • Updated figure: • Removed AC caps from UFS TX lines. • Removed PU on SD_POWER_SW_ON (GPIO21) line • Added PU on SD Detect line. **eSATA / USB Combo Connector** • Updated intro to indicate eSATA is GEN3, but PCIe side of bridge is GEN2. • Updated figure to add connection from NC_3 to VDD_1V_SATA_PHY supply **M.2 Key E** Updated figure: • Added OD buffer on WLAN disable (pin 56) line (& pull-up) • Removed PU on PEX_WAKE_N • Moved GPIO3_AP_WAKE_BT_M2 connection from pin 61 to pin 38. • Changed PU rail for GPIO30_M2_E_ALERT_R* to VDD_1V8. • Removed stuffing options for I2C interface & removed associated note. • Added level shifters on I2S3 & BT_WAKE_AP signals. Updated table: • Updated I2S3 IF to be level shifted • Updated pin 20 (BT_WAKE_AP) to add level shifter reference

Version	Date	Description of Change
		• Updated pin 32 & 36 (UART5_TX & RTS) to add buffer reference • Updated pin 58 & 60 (I2C GP2) to remove mention of stuffing option • Moved AP_WAKE_BT from pin 61 to 38 • Updated pin direction for pins 14, 53 **M.2 Key M** • Updated figure to add PU to pin 44 (ALERT*) **Camera Connector** • Updated pins 56, 57, 58 & 101 to be reserved for digital camera supplies **Audio Panel Header** • Updated pin direction for pins 1, 3, 5, & 9 **Expansion Header (40-pin)** • Updated module pin name for exp header pin 7 (MCLK05) • Updated pin direction for pin 18 **Automation Header** • Updated pin 7 to be CVB_STBY (STANDBY_ACK_N) • Updated pin direction for pins 2, 3, 4, & 7 **Miscellaneous** • Added I2C usage tables for module & carrier board. **Power** • Updated figure & supply allocation table to change 5V_AO regulator
2.0	January 14, 2020	• Updated memory to remove memory size • Added Pin 1 indicator to fan header in Figure 1-2 • Added Pin 1 indicators to camera connector, JTAG header, automation header, audio header, and voltage select jumper in Figure 1-3. • Added PCIe and SLVS to carrier board standard connectors • Removed connection figure from "Gigabit Ethernet Connector" section • Removed "Signal Name" column and added "Module Pin #" column in Table 2-4 • Added PCIe connector support for EndPoint and Root Port cards • Removed unused lower x8 section in Figure 2-1 • Included SLVS control signals connected to PCIe reset, wake, and clock request pins in Figure 2-1 • Show internal 3.3V pull-ups on the PCIe control in Figure 2-1 • Updated Table 2-6 with LSVS related information and PCIe receive lane descriptions • Updated notes to Table 2-6 • Removed text mentioning I2S and DMIC interfaces in Section 3.2 • Added 3x4 lane to CSI in Section 3.2 • Added note to Section 3.2

Version	Date	Description of Change
		• Removed C-PHY connection example from Figure 3-1 • Removed note related to SPI in Table 3-2 • Updated connector on the carrier board to Wieson G2100CE04C-008-H • Updated VBUS[2:1] power rail usage in Table 5-1 • Added Table 5-3 based on P2822 power tree
2.1	June 21, 2020	• Updated Figure 1-1 to combine level shifter blocks to the 4-pin expansion connector • Updated Figure 2-1 to include connected I2C lines from the module to connector pins, connected PRSNT1# to GND and updated name, and updated PRSNT2# and PERST# names • Updated pin description in Table 2-6 • Removed note regarding max length from Table 2-8 • Removed CSI and camera text from Table 2-12 • Added C-PHY camera CSI connections diagram (Figure 3-1) • Added Table 3-3 for C-PHY options • Updated Table 3-5 with rounded up largest carrier board delay across the interface for both I2S and SPI • Added Chapter 5 on mechanicals

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Chapter 1. Introduction

This specification contains recommendations and guidelines for engineers to follow to create modules for the expansion connectors on the NVIDIA® Jetson AGX Xavier™ carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

> **!** **CAUTION**: ALWAYS CONNECT THE JETSON AGX XAVIER AND ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE AC POWER JACK OR TYPE C CONNECTOR.
>
> The Jetson AGX Xavier Developer Kit carrier board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson AGX Xavier carrier board. NVIDIA will not replace units that have been damaged due to ESD discharge.

The Jetson AGX Xavier carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson AGX Xavier features and interfaces, enabling a highly flexible and extensible development platform. Go to https://developer.nvidia.com/embedded-computing or contact your NVIDIA representative for access to software updates and the developer SDK supporting the OS image and host development platform that you want to use. The developer SDK includes an OS image that you will load onto your Jetson AGX Xavier device, supporting documentation, and code samples to help you get started.

1.1 Jetson AGX Xavier Feature List

- Applications processor
  - Xavier
- Memory
  - 256-bit wide LPDDR4x DRAM
  - eMMC 5.1
- Network
  - RGMII I/F for 10/100/1000 BASE-T Ethernet
- Advanced power management
  - Dynamic voltage and frequency scaling
  - Multiple clock and power domains
  - Thermal transfer plate (TTP) and optional fan/heat sink

1.2 Carrier Board Feature List

- Connection to Jetson AGX Xavier
  - 699-pin (11x65) board-board connector
- Storage
  - MicroSD Card + UFS combo socket
  - USB / eSATA connector
- USB
  - 2 x USB type C connectors
- Wired Network
  - Gigabit Ethernet (RJ45 connector)
- PCI Express
  - Standard PCIe x16 connector (lower x8 used)
- Display
  - HDMI™ Type A connector
  - 2x VESA® DisplayPort™ (DP) routed to Type C connectors
- Camera Expansion Header
  - 120-pin (2x60) Board-Board
  - CSI: 6, x2 – 8, x4 (D-PHY or C-PHY)
  - Camera CLK, I2C and Control
- M.2 Key E Connector
  - PCIe x1 Lane, USB 2.0
  - I2S, UART, I2C, Control

- M.2 Key M Connector
  - PCIe x4 Lane, Control
- Expansion Header
  - 40-pin (2x20) header
  - I2C, SPI, UART, I2S, CAN, D-MIC
- UI and Indicators
  - Power, Reset and Force Recovery Buttons
  - LED: Main 5.0V Supply
- Debug
  - JTAG Connector (2x5-pin header)
- Miscellaneous
  - Fan Connector: 5V, PWM and Tach
- Power
  - DC Jack: 9V to 20V (19V Adapter included)
  - Main 5V Supply: NCP81239
  - Main 3.3V Supply: TPS53015
  - Main 1.8V Buck Supply: APW7307
  - USB VBUS Load Switches: RT9715 and APL3511
  - 12V Buck-Boost (PCIe): NCP81239
  - Load Switches/LDOs (SD/HDMI/Display/Camera)
- Developer Kit Operating Temperature Range
  - 0 ^{0}C to 35 ^{0}C

1.3 Jetson AGX Xavier Carrier Board Block Diagram

Figure 1-1 through Figure 1-3 show the block diagram and various placement views for Jetson AGX Xavier and the carrier board.

Figure 1-1. Jetson AGX Xavier Carrier Board Block Diagram

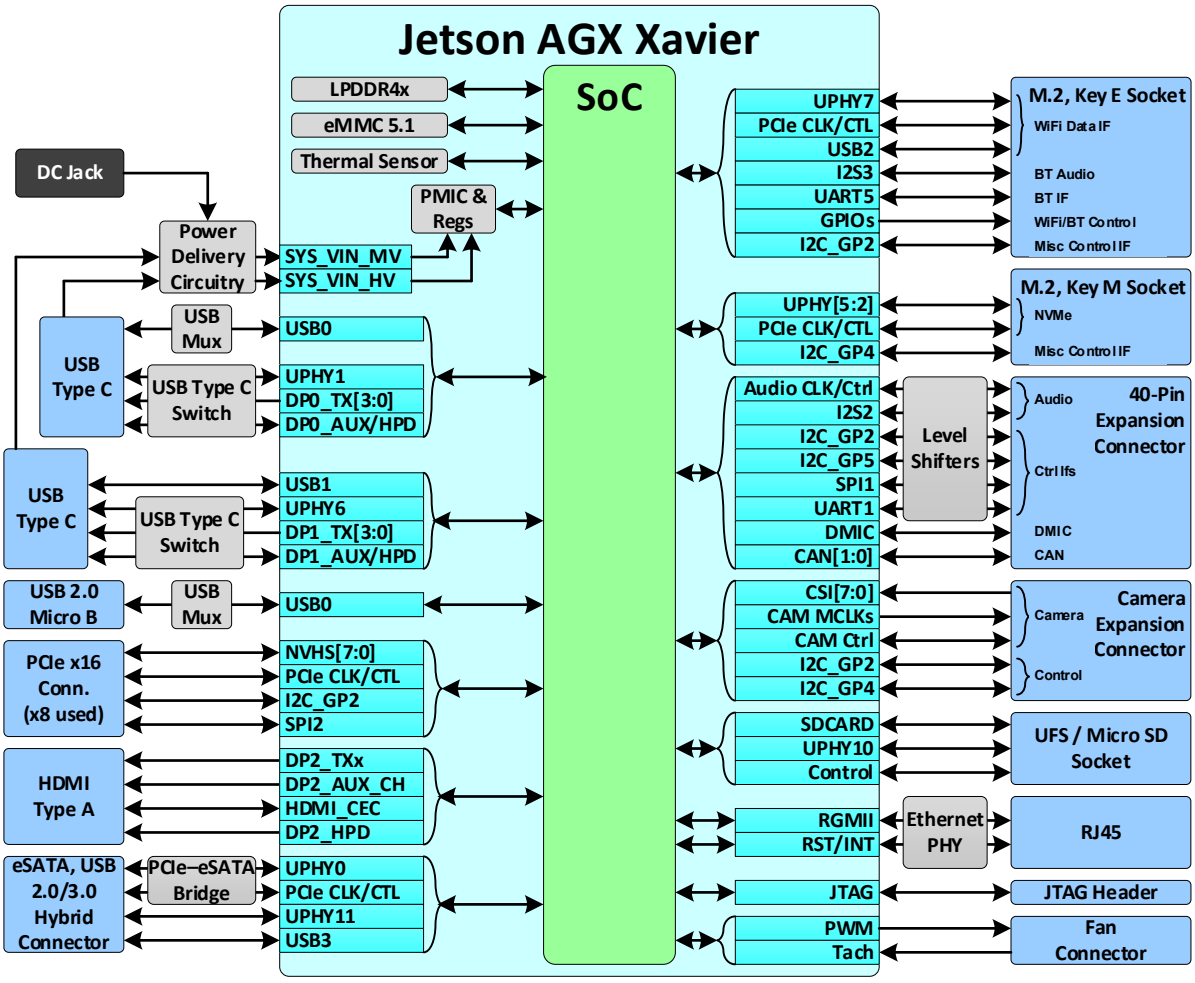
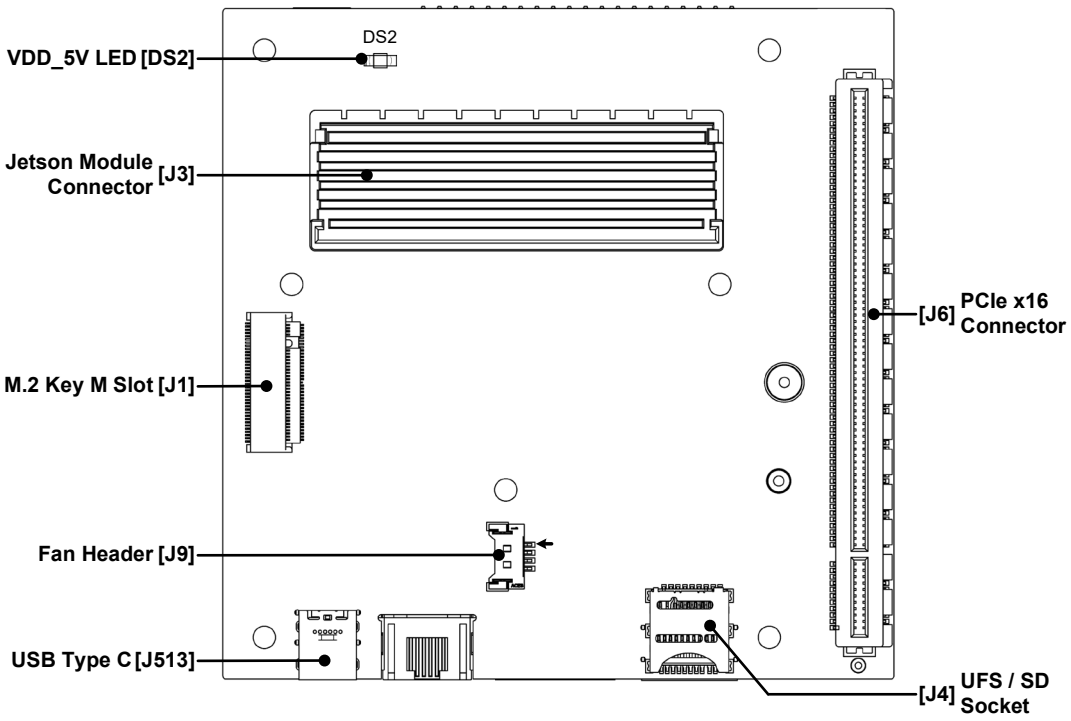
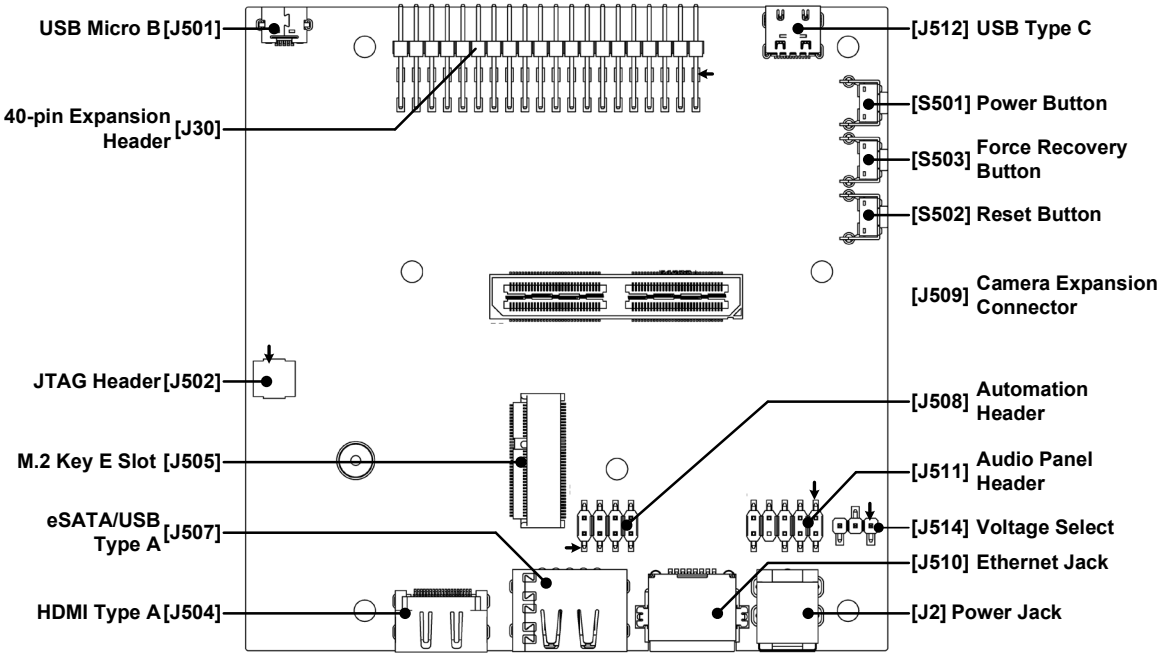


Figure 1-2. Jetson AGX Xavier Carrier Board Placement – Module Connector Side



J1 M.2 Key M Slot (75-pin)
J3 Jetson AGX Xavier Connector (65x11)
J4 MicroSD & UFS Socket
J6 PCIe x16 Connector
J9 Fan Header (4-pin, 1.25mm pitch)
J513 USB Type C Connector #2
DS2 VDD_5V LED

Figure 1-3. Jetson AGX Xavier Carrier Board Placement – Non-module Connector Side



J2	Power Jack	**J509**	Camera Connector (2x60, 0.5mm pitch)
J30	40-Pin Expansion Header (2x20, 2.54mm pitch)	**J510**	RJ45 Ethernet Jack
J501	Micro USB B Connector (for UART console)	**J511**	Audio Panel Header (2x5, 2.54mm pitch)
J502	JTAG Header (2x5, 1.27 pitch)	**J512**	USB Type C Connector #1
J504	HDMI Type A Connector	**J514**	Voltage select for Expansion Header Signal Level Shifters (1x3, 2.54mm pitch)
J505	M.2 Key E Connectivity Slot (75-pin)	**S501**	Power Button
J507	eSATA + USB 3.1 Type-A Connector	**S502**	Reset Button
J508	Automation Header (2x4, 2.54mm pitch)	**S503**	Force Recovery Button

Chapter 2. Jetson Carrier Board Standard Connectors

The Jetson AGX Xavier carrier board provides several standard expansion connectors to support additional functionality beyond what is integrated on the main platform board. This includes:

- USB 2.0 Micro B Connector
- USB 3.1: 2x Type C Connectors
- Gigabit Ethernet: RJ45 Connector
- HDMI: Type A Connector
- PCIe x16 Connector (PCIe or SLVS)
- UFS / Micro SD Card Socket
- eSATA: Standard SATA Connector, 22-pin including power
- M.2, Key E Slot
- M.2, Key M Slot
- Audio Panel Header
- JTAG

2.1 USB Ports

The carrier board supports two USB Type C Connectors (J512 and J513 shown in the figure below). These connectors support USB 3.1 and alternately DisplayPort. The USB connector J512 supports recovery mode. In addition, a USB 2.0 Micro B connector (J501) is supported. This connector provides access to a UART console and the carrier board Power/Reset/Force Recovery signals. Recovery mode is not supported on this connector.

Table 2-1. USB 2.0 Micro B Connector Pin Description – J501

Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	VBUS Supply	Power
2	USB0_N	F13	USB 2.0 #0 Data	Bidir
3	USB0_P	F12		
4	–	–	Unused	–
5	–	–	Ground	Ground

Table 2-2. USB 3.1 Type C Connector Pin Description – J512

Pin #	Module (Type C Re-driver / PD Ctrl) Pin Name	Module Pin #	Usage/Description	Type/ Direction	Pin #	Module (Type C Re-driver / PD Ctrl) Pin Name	Module Pin #	Usage/Description	Type/ Direction
A1	–	–	Ground	Ground	B1	–	–	Ground	Ground
A2	(TX1P)	–	USB 3.1 #0 Transmit 1 (or DP)	Output	B2	(USB0_TX2_DUT_P)	–	USB 3.1 #0 Transmit 2 (or DP)	Output
A3	(TX1N)				B3	(USB0_TX2_DUT_N)			
A4	–	–	USB VBUS Power	Power	B4	–	–	USB VBUS Power	Power
A5	(PD Ctrl – CC1_P1)	–	Type C #0 Config Channel 1	Bidir	B5	(PD Ctrl – CC2_P1)	–	Type C #0 Config Channel 2	Bidir
A6	USB0_P	F12	USB 2.0 #0 Data	Bidir	B6	USB0_P	F12	USB 2.0 #0 Data	Bidir
A7	USB0_N	F13			B7	USB0_N	F13		
A8	(SBU1)	–	Type C Sideband Use 1	Bidir	B8	(SBU2)	–	Type C Sideband Use 2	Bidir
A9	–	–	USB VBUS Power	Power	B9	–	–	USB VBUS Power	Power
A10	(RX2N)	–	USB 3.1 #0 Receive 2 (or DP)	Input	B10	(RX1N)	–	USB 3.1 #0 Receive 1 (or DP)	Input
A11	(RX2P)				B11	(RX1P)			
A12	–	–	Ground	Ground	B12	–	–	Ground	Ground
–	UPHY_RX1_N	C22	USB 3.0 #2	Input	–	UPHY_TX1_N	G22	USB 3.0 #2	Output
–	UPHY_RX1_P	C23			–	UPHY_TX1_P	G23		

Table 2-3. USB 3.1 Type C Connector Pin Description – J513

Pin #	Module (Type C Re-driver / PD Ctrl) Pin Name	Module Pin #	Usage/Description	Type/ Direction	Pin #	Module (Type C Re-driver / PD Ctrl) Pin Name	Module Pin #	Usage/Description	Type/ Direction
A1	–	–	Ground	Ground	B1	–	–	Ground	Ground
A2	(TX1P)	–	USB 3.1 #0 Transmit 1	Output	B2	(USB0_TX2_DUT_P)	–	USB 3.1 #0 Transmit 2	Output
A3	(TX1N)				B3	(USB0_TX2_DUT_N)			
A4	–	–	USB VBUS Power	Power	B4	–	–	USB VBUS Power	Power
A5	(PD Ctrl – CC1_P2)	–	Type C #0 Config Channel 1	Bidir	B5	(PD Ctrl – CC2_P2)	–	Type C #0 Config Channel 2	Bidir
A6	USB1_P	F12	USB 2.0 #0 Data	Bidir	B6	USB1_P	F12	USB 2.0 #0 Data	Bidir
A7	USB1_N	F13			B7	USB1_N	F13		
A8	(SBU1)	–	Type C Sideband Use 1	Bidir	B8	(SBU2)	–	Type C Sideband Use 2	Bidir
A9	–	–	USB VBUS Power	Power	B9	–	–	USB VBUS Power	Power
A10	(RX2N)	–	USB 3.1 #0 Receive 2	Input	B10	(RX1N)	–	USB 3.1 #0 Receive 1	Input
A11	(RX2P)				B11	(RX1P)			
A12	–	–	Ground	Ground	B12	–	–	Ground	Ground
–	UPHY_RX6_N	C22	USB 3.0 #0	Input	–	UPHY_TX6_N	G22	USB 3.0 #0	Output
–	UPHY_RX6_P	C23			–	UPHY_TX6_P	G23		

Notes:
1. The signal names in parenthesis come from the Type C Re-driver or PD Controller.
2. The USB[1:0]_TX/RX lines can alternately carry DP signaling. In that case, the SBU pins carry DP_AUX and CC1 pins carry HPD functionality.
3. In the Type/Dir column, Output is to USB Connectors. Input is from USB connectors. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

2.2 Gigabit Ethernet Connector

The carrier board implements an RJ45 connector (J510) along with the necessary magnetics device.

Table 2-4. Ethernet RJ45 Connector Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	Gigabit Ethernet MDI 0+ from Ethernet PHY	Bidir
2	–	–	Gigabit Ethernet MDI 0– from Ethernet PHY	Bidir
3	–	–	Gigabit Ethernet MDI 1+ from Ethernet PHY	Bidir
4	–	–	Gigabit Ethernet MDI 2+ from Ethernet PHY	Bidir
5	–	–	Gigabit Ethernet MDI 2– from Ethernet PHY	Bidir
6	–	–	Gigabit Ethernet MDI 1– from Ethernet PHY	Bidir
7	–	–	Gigabit Ethernet MDI 3+ from Ethernet PHY	Bidir
8	–	–	Gigabit Ethernet MDI 3– from Ethernet PHY	Bidir

Note: In the Type/Dir column, Output is to RJ45 connector. Input is from RJ45 connector. Bidir is for bidirectional signals.

2.3 HDMI Connector

A standard HDMI Type A connector (J504) is supported.

Table 2-5. HDMI Connector Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Direction
1	HDMI_DP2_TX0_P	D51	HDMI Transmit Data 2+	Output
2	–	–	Ground	Ground
3	HDMI_DP2_TX0_N	D52	HDMI Transmit Data 2–	Output
4	HDMI_DP2_TX1_P	B51	HDMI Transmit Data 1+	Output
5	–	–	Ground	Ground
6	HDMI_DP2_TX1_N	B52	HDMI Transmit Data 1–	Output
7	HDMI_DP2_TX2_P	A51	HDMI Transmit Data 0+	Output
8	–	–	Ground	Ground
9	HDMI_DP2_TX2_N	A50	HDMI Transmit Data 0–	Output
10	HDMI_DP2_TX3_P	C51	HDMI Transmit Clock+	Output
11		–	Ground	Ground
12	HDMI_DP2_TX3_N	C50	HDMI Transmit Clock–	Output
13	HDMI_CEC	J50	HDMI CEC	Bidir
14	–	–	Unused	Unused
15	DP2_AUX_CH_P	G53	HDMI DDC Clock	Bidir /OD
16	DP2_AUX_CH_N	G54	HDMI DDC Data	Bidir/OD
17	–	–	Ground	Ground
18	–	–	HDMI 5V Power	Power
19	DP2_HPD	K50	Hot Plug Detect	Input

Note: In the Type/Dir column, Output is to HDMI connector. Input is from HDMI connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

2.4 PCIe x16 Connector

The Jetson carrier board includes a standard PCIe x16 connector (J6). Only the first x8 portion of the connector is used to support up to 8 PCIe lanes. This connector can support PCIe Endpoint or Root Port cards or an SLVS camera adapter card.

Note: The following pairs of signals are tied together on the carrier board and the PCIe signal is pulled to 3.3V on the module: PEX_L5_RST_N and GPIO19, PEX_L5_CLKREQ_N and GPIO18, PEX_WAKE_N and SPI3_MOSI. If any of these SLVS control signals operate at 1.8V on the camera module, level shifters will be required.

Figure 2-1. PCIe x16 Connector Connections

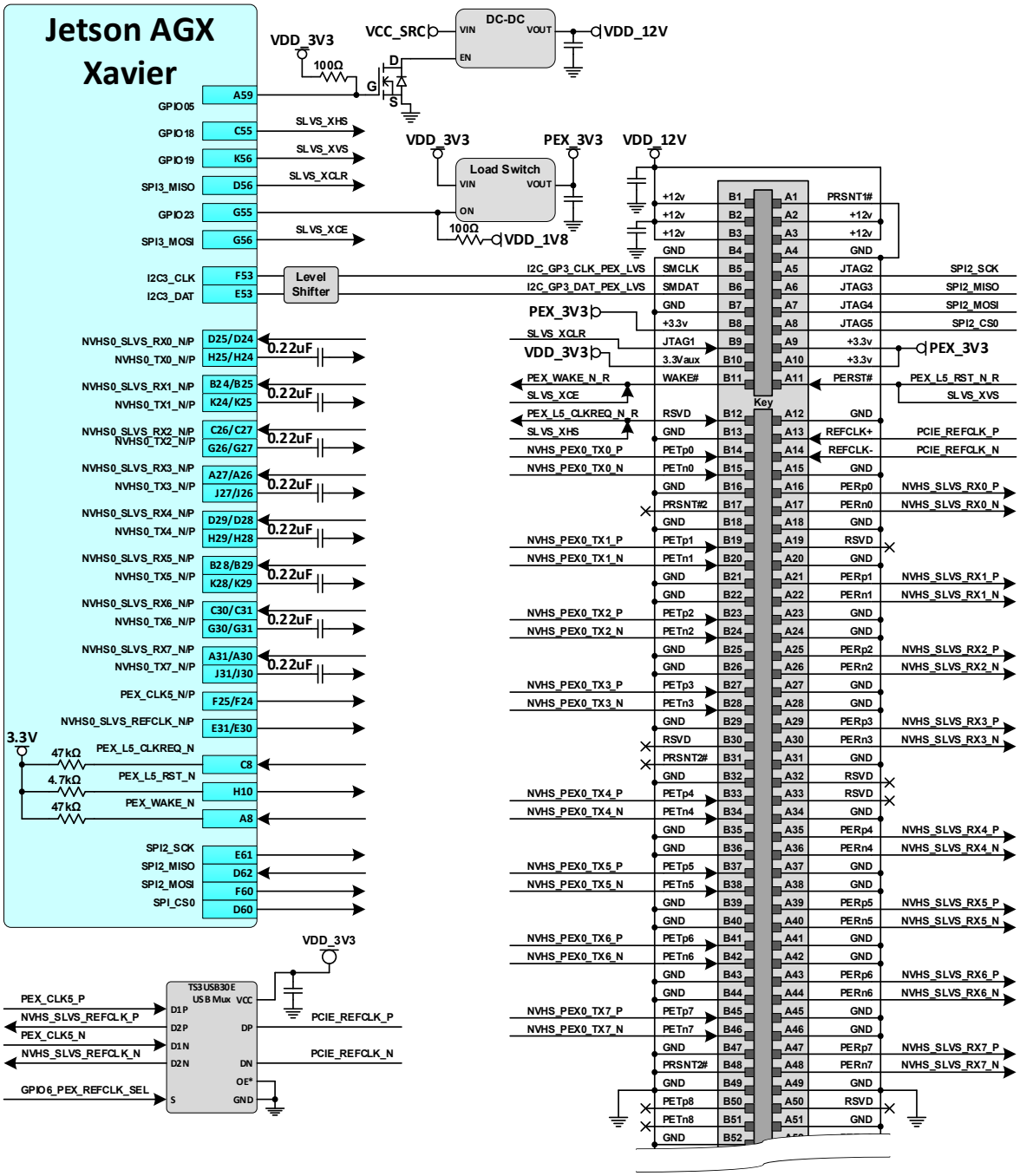


Table 2-6. PCIe 8-Lane Connector Pin Description

Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction	Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction
A1	–	–	Ground (PCIe PRSNT1#)	Ground	B1	–	–	12V Supply	Power
A2	–	–	12V Supply	Power	B2				
A3					B3				
A4	–	–	Ground	Ground	B4	–	–	Ground	Ground
A5	SPI2_SCK	E61	SPI 2 Clock	Output	B5	I2C_GP0_CLK		General I2C #0 Clock	Bidir/OD
A6	SPI2_MISO	D62	SPI 2 Master In/Slave Out	Input	B6	I2C_GP0_DAT		General I2C #0 Data	Bidir/OD
A7	SPI2_MOSI	F60	SPI 2 Master Out/Slave In	Output	B7	–	–	Ground	Ground
A8	SPI2_CS0	D60	SPI 2 Chip Select #0	Output	B8	–	–	3.3V supply (PEX_3V3)	Power
A9	–	–	3.3V supply (PEX_3V3)	Power	B9	SPI3_MISI	D56	SLVS XCLR	Output
A10					B10	–	–	3.3V Vaux supply (VDD_3V3)	Power
A11	PEX_L5_RST_N GPIO19 (See Note 1)	H10 K56	PCIe Lane 0 Reset SLVS_XVS	Output	B11	PEX_WAKE_N SPI3_MOSI	A8 G56	PCIe Wake (Shared) SLVS XCE	Input
A12	–	–	Ground	Ground	B12	PEX_L5_CLKREQ_N GPIO18 (See Note 3)	C8 C55	PCIe (#5) Clock Req. SLVS XHS	Bidir
A13	PEX_CLK5_P (Note 2) NVHS_SLVS_REFCLK_P	F24 E30	PCIe (#5) Ref Clock Output or SLVS Ref Clock Input	See Usage/Desc	B13	–	–	Ground	Ground
A14	PEX_CLK5_N (Note 2) NVHS_SLVS_REFCLK_N	F25 E31			B14	NVHS0_TX0_P	H24	PCIe (#5) Lane 0 Transmit	Output
A15	–	–	Ground	Ground	B15	NVHS0_TX0_N	H25		
A16	NVHS0_SLVS_RX0_P	D24	PCIe (#5) or SLVS Lane 0 Receive	Input	B16	–	–	Ground	Ground
A17	NVHS0_SLVS_RX0_N	D25			B17	–	–	Reserved	Reserved
A18	–	–	Ground	Ground	B18	–	–	Ground	Ground
A19	–	–	Reserved	Reserved	B19	NVHS0_TX1_P	K25	PCIe (#5) Lane 1 Transmit	Output
A20	–	–	Ground	Ground	B20	NVHS0_TX1_N	K24		
A21	NVHS0_SLVS_RX1_P	B25	PCIe (#5) or SLVS Lane 1 Receive	Input	B21	–	–	Ground	Ground
A22	NVHS0_SLVS_RX1_N	B24			B22				
A23	–	–	Ground	Ground	B23	NVHS0_TX2_P	G27	PCIe (#5) Lane 2 Transmit	Output
A24					B24	NVHS0_TX2_N	G26		
A25	NVHS0_SLVS_RX2_P	C27	PCIe (#5) or SLVS Lane 2 Receive	Input	B25	–	–	Ground	Ground
A26	NVHS0_SLVS_RX2_N	C26			B26				
A27	–	–	Ground	Ground	B27	NVHS0_TX3_P	J26	PCIe (#5) Lane 3 Transmit	Output
A28					B28	NVHS0_TX3_N	J27		
A29	NVHS0_SLVS_RX3_P	A26	PCIe (#5) or SLVS Lane 3 Receive	Input	B29	–	–	Ground	Ground
A30	NVHS0_SLVS_RX3_N	A27			B30	–	–	Reserved	Reserved
A31	–	–	Ground	Ground	B31				
A32	–	–	Reserved	Reserved	B32	–	–	Ground	Ground
A33					B33	NVHS0_TX4_P	H28	PCIe (#5) Lane 4 Transmit	Output
A34	–	–	Ground	Ground	B34	NVHS0_TX4_N	H29		
A35	NVHS0_SLVS_RX4_P	D28	PCIe (#5) or SLVS Lane 4 Receive	Input	B35	–	–	Ground	Ground
A36	NVHS0_SLVS_RX4_N	D29			B36				
A37	–	–	Ground	Ground	B37	NVHS0_TX5_P	K29	PCIe (#5) Lane 5 Transmit	Output
A38					B38	NVHS0_TX5_N	K28		
A39	NVHS0_SLVS_RX5_P	B29	PCIe (#5) or SLVS Lane 5 Receive	Input	B39	–	–	Ground	Ground
A40	NVHS0_SLVS_RX5_N	B28			B40				
A41	–	–	Ground	Ground	B41	NVHS0_TX6_P	G31	PCIe (#5) Lane 6 Transmit	Output
A42					B42	NVHS0_TX6_N	G30		
A43	NVHS0_SLVS_RX6_P	C31		Input	B43	–	–	Ground	Ground

Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction	Pin #	Module Pin Name	Module Pin #s	Usage/Description	Type/ Direction
A44	NVHS0_SLVS_RX6_N	C30	PCIe (#5) or SLVS Lane 6 Receive		B44				
A45	–	–	Ground	Ground	B45	NVHS0_TX7_P	J30	PCIe (#5) Lane 7 Transmit	Output
					B46	NVHS0_TX7_N	J31		
A47	NVHS0_SLVS_RX7_P	A30	PCIe (#5) or SLVS Lane 7 Receive	Input	B47	–	–	Ground	Ground
A48	NVHS0_SLVS_RX7_N	A31			B48			Ground (PRSTN2#)	
A49	–	–	Ground	Ground	B49			Ground	

Notes:

1. PEX_L5_RST_N and GPIO19, PEX_L5_CLKREQ_N and GPIO18, PEX_WAKE_N and SPI3_MOSI are tied together on the carrier board and the PCIe signals are pulled to 3.3V on the module. If these SLVS control signals operate at 1.8V on the camera module, level shifters will be required.
2. The selection for either PEX_CLK5_P/N or NVHS_SLVS_REFCLK_P/N is determined by a mux on the carrier board. The mux is controlled by the module GPIO6 pin (low = PEX_CLK5, high = SLVS_REFCLK.
3. Table shows only the PCIe x8 section of the connector as this is the only portion used. Other x16 signals are no-connects or GNDs.
4. In the Type/Dir column, Output is to the PCIe connector. Input is from the PCIe connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

Table 2-7. PCIe Card Maximum Trace Delays

Worst Case PCIe (GEN3) Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Trace Delay Allowed on PCIe Card (ps)	
	Stripline	Microstrip	Stripline	Microstrip
685	1600	1250	915	565

Table 2-8. SLVS Adapter Card Maximum Trace Delays

Max Trace Delay Allowed on SLVS (PCIe) Card (ps)
Stripline
310

2.5 UFS and Micro SD Card Socket

A combo UFS and Micro SD Card Socket (J4) is implemented. The SD card interface supports up to SDR104 mode (UHS-1). The UFS interface supports up to HS-GEAR 3.

Table 2-9. UFS and SD Card Combo Socket Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	Ground	Ground
2	UPHY_TX10_N	K12	UFS Transmit	Output
3	UPHY_TX10_P	K13		
4	–	–	Ground	Ground

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
5	UPHY_RX10_N	B13	UFS Receive	Input
6	UPHY_RX10_P	B12		
7	–	–	Ground	Ground
8	UFS0_REF_CLK	A6	UFS Reference Clock	Output
9	–	–	1.8V Power for UFS	Power
10	GPIO31	H60	UFS Card Detect	Input
11	–	–	Ground	Ground
12	–	–	3.3V Power for UFS & SD	Power
13	SDCARD_D1	F8	SD Card Data #1	Bidir
14	SDCARD_D0	E8	SD Card Data #0	Bidir
15	SDCARD_CLK	B6	SD Card Clock	Output
16	SDCARD_CMD	A5	SD Card Command	Bidir
17	SDCARD_D3	D6	SD Card Data #3	Bidir
18	SDCARD_D2	A4	SD Card Data #2	Bidir
19	GPIO02	L6	SD Card, Card Detect	Input
	GPIO21	B58	UFS & SD Card load switch enable	Output

Note: In the Type/Dir column, Output is to card socket. Input is from card socket. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

2.6 eSATA and USB 3.1 Type A Connector

The Jetson AGX Xavier carrier board has a hybrid connector supporting eSATA and USB 3.1 (J507). The eSATA interface is GEN3. The PCIe side of the PCIe-SATA bridge is GEN2. The USB 3.1 interface is GEN1.

Table 2-10. Hybrid USB 3.1 Gen1 and eSATA Connector Pin Description

c	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–		USB VBUS Power	Power	11	–		Ground	Ground
2	USB3_DN	G10	USB 2.0 #3	Bidir	12	UPHY_RX11_N	D13	USB 3.1 Receive	Input
3	USB3_DP	G11			13	UPHY_RX11_P	D12		
4	–	–	Ground	Ground	14	–		Ground	Ground
5					15	UPHY_TX11_N	H13	USB 3.1 Transmit	Output
6	–	–	SATA Transmit +	Output	16	UPHY_TX11_P	H12		
7			SATA Transmit –		17	–	–	Ground	Ground
8	–	–	Ground	Ground	18				
9	–	–	SATA Receive +	Input	19				
10			SATA Receive –		20				

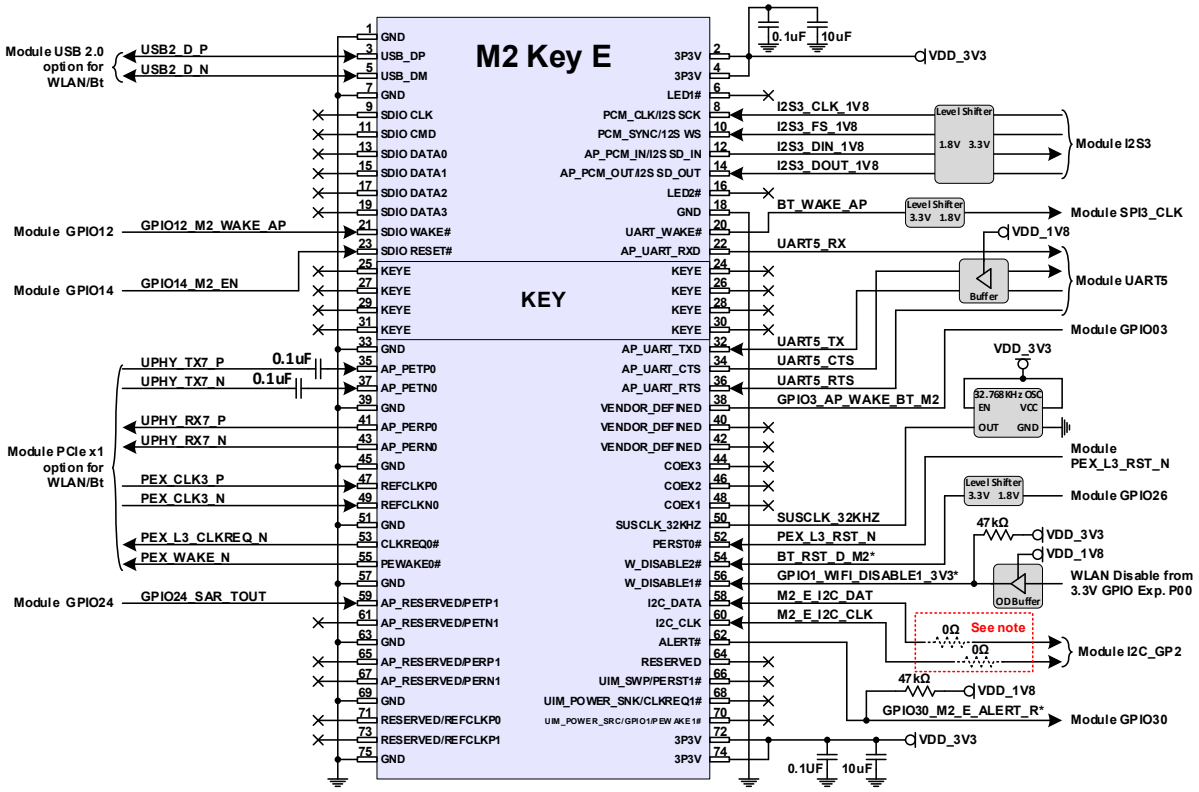
Note: In the Type/Dir column, Output is to connector. Input is from connector. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

2.7 M.2 Key E Expansion Slot

The Jetson carrier board includes a M.2, Key E Slot Mini-PCIe Expansion slot (J505). This includes interface options for WLAN/BT including PCIe (x1), USB 2.0, UART, I2S and I2C. The connections and power rails associated with the connector are shown in Figure 2-2.

Figure 2-2. M.2 Key E Connections



Note: Series 0Ω resistor pads are recommended on the I2C connections. Some non-compliant cards can cause issues if the M.2 I2C pins are connected to the module I2C interface. It is suggested these are left unstuffed unless the I2C interface on the M.2 socket is required.

Table 2-11. M.2 Key E Expansion Slot Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	Ground	Ground		–	–	–	–
3	USB2_P	A10	USB 2.0 Data	Bidir	2	–	–	Main 3.3V Supply	Power
5	USB2_N	A11			4				
7	–	–	Ground	Ground	6	–	–	Unused	Unused
9	–	–	Unused	Unused	8	I2S3_CLK	C59	I2S #3 (Level shifted to 1.8V)	Bidir
11					10	I2S3_FS	C60		Bidir
13					12	I2S3_SDIN	J59		Input

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
15					14	I2S3_SDOUT	K59		Output
17					16	–	–	Unused	Unused
19					18	–	–	Ground	Ground
21	GPIO12	E10	WLAN Wake AP	Input	20	GPIO13	G7	Bluetooth Wake AP (Level shifted to 3.3V)	Input
23	GPIO14	L15	WLAN Enable	Output	22	UART5_RX	H58	UART #5 Receive	Input
25	–	–	Unused	Unused	24	–	–	Unused	Unused
27					26				
29					28				
31					30				
33	–	–	Ground	Ground	32	UART5_TX	L5	UART #5 Transmit (Buffered)	Output
35	UPHY_TX7_P	H16	PCIe IF #3 Transmit	Output	34	UART5_CTS	H57	UART #5 Clear to Send	Input
37	UPHY_TX7_N	H17			36	UART5_RTS	K58	UART #5 Request to Send (Buffered)	Output
39	–	–	Ground	Ground	38	GPIO03	D54	AP Wake BT	Output
41	UPHY_RX7_P	D16	PCIe IF #3 Receive	Input	40	–	–	Unused	Unused
43	UPHY_RX7_N	D17			42				
45	–	–	Ground	Ground	44				
47	PEX_CLK3_P	F20	PCIe IF #3 Reference clock	Output	46				
49	PEX_CLK3_N	F21			48				
51	–	–	Ground	Ground	50	–	–	Suspend Clock (32KHz)	Output
53	PEX_L3_CLKREQ_N	J10	PCIe IF #3 Clock Request	Input	52	PEX_L3_RST_N	K9	PCIe IF #3 Reset	Output
55	PEX_WAKE_N	A8	PCIe Wake	Input	54	GPIO26	H51	WLAN Disable #2 (Level Shifted to 3.3V)	Output
57	–	–	Ground	Ground	56	GPIO01	J4	WLAN Disable #1 (Level Shifted to 3.3V)	Output
59	GPIO24	J51	RF Power Control or GPIO	Output	58	I2C2_DAT	K61	General I2C Interface #2 (See note)	Bidir/OD
61	–	–	Unused	Unused	60	I2C2_CLK	J61		
63	–	–	Ground	Ground	62	GPIO30	B55	M.2, Key E Connector Alert	Input
65	–	–	Unused	Unused	64	–	–	Unused	Unused
67					66				
69	–	–	Ground	Ground	68				
71	–	–	Unused	Unused	70				
73					72	–	–	Main 3.3V Supply	Power
75	–	–	Ground	Ground	74				

Note:

1. Series 0Ω resistor pads are recommended on the I2C connections. Some non-compliant cards can cause issues if the M.2 I2C pins are connected to the module I2C interface. It is suggested these are left unstuffed unless the I2C interface on the M.2 socket is required.
2. In the Type/Dir column, Output is to M.2 module. Input is from M.2 module. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

Table 2-12. M.2 Key E Card Maximum Trace Delays

Worst Case CSI Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Camera Module (ps)	
PCIe				
520	880		360	

Worst Case CSI Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Camera Module (ps)	
PCIe				
USB	Stripline	MicroStrip	Stripline	MicroStrip
375	1050	900	675	525
I2S				
600	3600		3000	

Note: For USB 2.0 max length allowed, the case with Common-Mode-Choke (CMC) is assumed. Longer length possible without CMC.

2.8 M.2 Key M Expansion Slot

The carrier board includes an M.2, Key M Slot NVMe Expansion slot (J1). This includes PCIe (x4) and I2C.

Table 2-13. M.2 Key M Expansion Slot Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	Ground	Ground	2	–	–	Main 3.3V Supply	Power
3					4				
5	UPHY_RX5_N	C18	PCIe IF #0 Lane 5 Receive	Input	6	–	–	Unused	Unused
7	UPHY_RX5_P	C19			8				
9	–	–	Ground	Ground	10				
11	UPHY_TX5_N	G18	PCIe IF #0 Lane 5 Transmit	Output	12	–	–	Main 3.3V Supply	Power
13	UPHY_TX5_P	G19			14				
15	–	–	Ground	Ground	16				
17	UPHY_RX4_N	A19	PCIe IF #0 Lane 4 Receive	Input	18	–	–	Unused	Unused
19	UPHY_RX4_P	A18			20				
21	–	–	Ground	Ground	22				
23	UPHY_TX4_N	J19	PCIe IF #0 Lane 4 Transmit	Output	24				
25	UPHY_TX4_P	J18			26				
27	–	–	Ground	Ground	28				
29	UPHY_RX3_N	D21	PCIe IF #0 Lane 3 Receive	Input	30				
31	UPHY_RX3_P	D20			32				
33	–	–	Ground	Ground	34				
35	UPHY_TX3_N	H21	PCIe IF #0 Lane 3 Transmit	Output	36				
37	UPHY_TX3_P	H20			38				
39	–	–	Ground	Ground	40	I2C4_CLK	D61	General I2C #4 (See note)	bidir
41	UPHY_RX2_N	B20	PCIe IF #0 Lane 2 Receive	Input	42	I2C4_DAT	E60		bidir
43	UPHY_RX2_P	B21			44	GPIO34	A55	M.2 Key M Alert	Output
45	–	–	Ground	Ground	46	–	–	Unused	Unused
47	UPHY_TX2_N	K20	PCIe IF #0 Lane 2 Transmit	Output	48				
49	UPHY_TX2_P	K21			50	PEX_L0_RST_N	D10	PCIe IF #0 Reset	Output
51	–	–	Ground	Ground	52	PEX_L0_CLKREQ_N	E11	PCIe IF #0 Clock Request	Input
53	PEX_CLK0_N	E14	PCIe IF #0 Reference Clock	Output	54	PEX_WAKE_N	A8	PCIe Wake (Level Shifted from 3.3V to 1.8V)	Input

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
55	PEX_CLK0_P	E15			56	–	–	Unused	Unused
57	–	–	Ground	Ground	58				
59	–	–	Unused	Unused	60				
61					62				
63					64				
65					66				
67					68	–	–	32KHz Suspend Clock	Output
69					70	–	–	Main 3.3V Supply	Power
71	–	–	Ground	Ground	72				
73					74				
75							–		

Notes:
1. Series 0Ω resistor pads are recommended on the I2C connections. Some non-compliant cards can cause issues if the M.2 I2C pins are connected to the module I2C interface. It is suggested these are left unstuffed unless the I2C interface on the M.2 socket is required.
2. In the Type/Dir column, Output is to M.2 module. Input is from M.2 module. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

Table 2-14. M.2 Key M Maximum Trace Delays – PCIe up to Gen3

Worst Case PCIe (GEN3) Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Trace Delay Allowed on M.2 Card (ps)	
	Stripline	Microstrip	Stripline	Microstrip
400	1600	1250	1200	850

2.9 Audio Panel Header

The Jetson carrier board includes a 10-pin (2x5, 2.54 mm pitch) audio panel header (J511). This can be used to connect to a standard PC audio panel to support connections to microphone, line-in, headphones, powered speakers, etc.

Figure 2-3. Audio Panel Header Connections

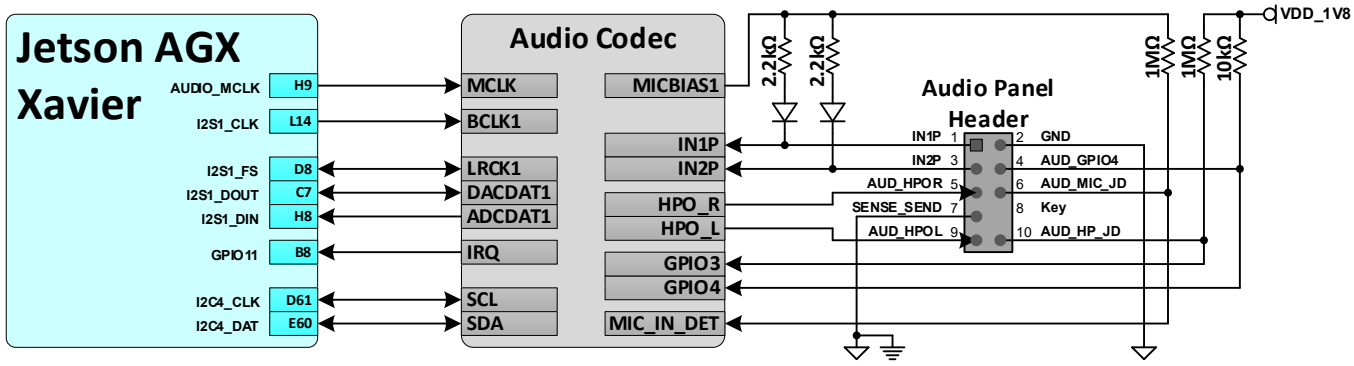


Table 2-15. Audio Panel Header Description

Pin #	Module (Codec) Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module (Codec) Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	(IN1P)	–	Microphone #1 input	Input	2	–	–	Ground	Ground
3	(IN2P)	–	Microphone #2 input	Input	4	(GPIO4)	–	Presense – detects if audio dongle is connected to header.	Input
5	(HPO_R)	–	Headphone output right channel	Output	6	(MIC_IN_DET)	–	Jack/Microphone detect pin	Input
7	NA	–	Pulled to analog GND	NA	8	Unused	–	Key	–
9	(HPO_L)	–	Headphone output left channel	Output	10	(GPIO3)	–	Headphone or jack detection	Input
–	AUDIO_MCLK	H9	Audio master clock	Output	–	I2S1_CLK	L14	I2S #1 clock	Output
–	GPIO11	B8	Audio interrupt	Input	–	I2S1_FS	D8	I2S #1 field select	Bidir
–	I2C4_CLK	D61	I2C #4 clock	Bidir	–	I2S1_DOUT	C7	I2S #1 data output	Output
–	I2C4_DAT	E60	I2C #4 data	Bidir	–	I2S1_DIN	H8	I2S #1 data input	Input

Note: In the Type/Dir column, Output is to audio panel header. Input is from audio panel header. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

2.10 JTAG Header

The Jetson carrier board has a 10-pin (2x5, 1.27 mm pitch) JTAG header (J502).

Table 2-16. JTAG Header Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
2	JTAG_TMS	E58	JTAG Test Mode Select	Input	1	–	–	Main 1.8V Supply	Power
4	JTAG_TCK	A60	JTAG Test Clock	Input	3	–	–	Ground	Ground
6	JTAG_TDO	D58	JTAG Test Data Out	Output	5				
8	JTAG_TDI	B60	JTAG Test Data In	Input	7				
10	SYS_RESET_N	L60	Main carrier board reset	Input	9	–	–	Detect presence of JTAG debugger connection. (FTDI GPIO Expander)	Input

Note: In the Type/Dir column, Output is to JTAG header. Input is from JTAG header. Bidir is for bidirectional signals.

Legend	Ground	Power	Reserved

Chapter 3. Carrier Board Custom Connectors

The Jetson carrier board supports several custom expansion headers:

- Jetson AGX Xavier Connector, 65x11
- Camera Expansion Header, 2x60, 0.5 mm pitch
- Expansion Header, 2x20, 2.54 mm pitch
- Audio Panel Header, 2x5, 2.54 mm pitch
- Fan Header, 4-pin, 1.25 mm pitch
- DC Power Jack

The Routing Guidelines for the interfaces supported on the expansion connectors can be found in the *Jetson AGX Xavier OEM Product Design Guide*. Those guidelines cover the PCB routing from the Jetson AGX Xavier to the peripheral device or actual device connector. When designing modules for one of the Jetson AGX Xavier expansion connectors, the routing on the carrier board must be accounted for. Tables are provided for the critical interfaces that provide the PCB delays on the carrier board. These delays are subtracted from the delays allowed in the *Jetson AGX Xavier OEM Product Design* Guide routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the *Jetson AGX Xavier OEM Product Design Guide* for other requirements (Impedance, trace spacing, skews between signals, etc.).

3.1 Module Connector

The carrier board interfaces to Jetson AGX Xavier using a 699-pin (65x11) connector (J3). The part number for the connector used on the carrier board can be found in the Jetson AGX Xavier Supported Component List (SCL) document. This interfaces with the module. See the *Jetson AGX Xavier Module Data Sheet* for the connector used on the module. The connector pinout can be found in the *Jetson AGX Xavier OEM Product Design Guide*.

3.2 Camera Expansion Header

The Jetson AGX Xavier carrier board includes a 120-pin (2x60, 0.5 mm pitch) camera expansion connector (J509). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A.

The mating connector is a Samtec QTH-060-01-H-D-A. The expansion connector includes interface options for multiple cameras. Refer to the *Jetson AGX Xavier Camera Module Hardware Design Guide* (DG-09364-001) for more information.

- CSI up to 3x4 lane or 6x2 lane
- CAM_I2C, Clock and Control GPIOs for the cameras
- I2C (2x in addition to CAM_I2C)

Note: Due to the CSI routing length on the carrier board and the additional connector between the module and the end device, D-PHY mode is supported only up to 1.5 Gbps.

Table 3-1. Camera Expansion Connector Pin Description

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	CSI0_D0_P	E42	CSI 0 Data 0	Input	2	CSI_1_D0_P	G41	CSI 1 Data 0	Input
3	CSI0_D0_N	E41			4	CSI_1_D0_N	G42		
5	–	–	Ground	Ground	6	–	–	Ground	Ground
7	CSI0_CLK_P	F43	CSI 0 Clock	Input	8	CSI_1_CLK_P	H43	CSI 1 Clock	Input
9	CSI0_CLK_N	F42			10	CSI_1_CLK_N	H42		
11	–	–	Ground	Ground	12	–	–	Ground	Ground
13	CSI0_D1_P	E39	CSI 0 Data 1	Input	14	CSI_1_D1_P	J41	CSI 1 Data 1	Input
15	CSI0_D1_N	E38			16	CSI_1_D1_N	J42		
17	–	–	Ground	Ground	18	–	–	Ground	Ground
19	CSI2_D0_P	A41	CSI 2 Data 0	Input	20	CSI_3_D0_P	E45	CSI 3 Data 0	Input
21	CSI2_D0_N	A42			22	CSI_3_D0_N	E44		
23	–	–	Ground	Ground	24	–	–	Ground	Ground
25	CSI2_CLK_P	B43	CSI 2 Clock	Input	26	CSI_3_CLK_P	F46	CSI 3 Clock	Input
27	CSI2_CLK_N	B42			28	CSI_3_CLK_N	F45		
29	–	–	Ground	Ground	30	–	–	Ground	Ground
31	CSI2_D1_P	C42	CSI 2 Data 1	Input	32	CSI_3_D1_P	G44	CSI 3 Data 1	Input
33	CSI2_D1_N	C41			34	CSI_3_D1_N	G45		
35	–	–	Ground	Ground	36	–	–	Ground	Ground
37	CSI4_D0_P	G48	CSI 4 Data 0	Input	38	CSI6_D0_P	K44	CSI 6 Data 0	Input
39	CSI4_D0_N	G47			40	CSI6_D0_N	K43		
41	–	–	Ground	Ground	42	–	–	Ground	Ground
43	CSI4_CLK_P	F48	CSI 4 Clock	Input	44	CSI6_CLK_P	J44	CSI 6 Clock	Input
45	CSI4_CLK_N	F47			46	CSI6_CLK_N	J45		
47	–	–	Ground	Ground	48	–	–	Ground	Ground
49	CSI4_D1_P	E47	CSI 4 Data 1	Input	50	CSI6_D1_P	H46	CSI 6 Data 1	Input
51	CSI4_D1_N	E48			52	CSI6_D1_N	H45		
53	–	–	Ground	Ground	54	–	–	Ground	Ground
55	–	–	Reserved for Low Voltage Digital Supply	Power	56	–	–	Reserved for Low Voltage Digital Supply	Power
57					58				
59	CSI5_D0_P	D42	CSI 5 Data 0	Input	60	CSI7_D0_P	A44	CSI 7 Data 0	Input
61	CSI5_D0_N	D43			62	CSI7_D0_N	A45		
63	–	–	Ground	Ground	64	–	–	Ground	Ground
65	CSI5_CLK_P	C44	CSI 5 Clock	Input	66	CSI7_CLK_P	B45	CSI 7 Clock	Input
67	CSI5_CLK_N	C45			68	CSI7_CLK_N	B46		

Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default	Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
69	–	–	Ground	Ground	70	–	–	Ground	Ground
71	CSI5_D1_P	D46	CSI 5 Data 1	Input	72	CSI7_D1_P	C47	CSI 7 Data 1	Input
73	CSI5_D1_N	D45			74	CSI7_D1_N	C48		
75	I2C3_CLK	F53	Camera I2C	Bidir	76	–	–	Unused	Unused
77	I2C3_DAT	E53			78				
79	–	–	Ground	Ground	80	–	–	Ground	Ground
81	–	–	2.8V Analog Camera supply (see note)	Power	82	–	–	2.8V Analog Camera supply (see note)	Power
83					84	–	–	Unused	Unused
85	–	–	Unused	Unused	86				
87	I2C2_CLK	J61	General Purpose I2C #2	Bidir/OD	88	MCLK03	H53	Camera #1 Master Clock	Output
89	I2C2_DAT	K61			90	GPIO15	F10	Camera #1 Powerdown	Output
91	MCLK02	J54	Camera #0 Master Clock	Output	92	GPIO16	F9	Camera #1 Reset	Output
93	UART4_CTS	L49	Camera #0 Powerdown	Output	94	MCLK04	H55	Camera #2 Master Clock	Output
95	UART4_TX	L4	Camera #0 Reset	Output	96	–	–	Unused	Unused
97	–	–	Unused	Unused	98				
99	–	–	Ground	Ground	100	–	–	Ground	Ground
101	–	–	Reserved for Digital Supply	Power	102	–	–	1.8V Camera supply.	Power
103			Unused	Unused	104	–	–	Unused	Unused
105	I2C4_CLK	D61	General I2C #4	Bidir/OD	106				
107	I2C4_DAT	K61			108	–	–	3.3V supply	Power
109	–	–	Unused	Unused	110				
111					112	–	–	Unused	Unused
113					114				
115	–	–	Ground	Ground	116	–	–	Ground	Ground
117	–	–	Unused	Unused	118	–	–	3.3V supply	Power
119	GPIO25	K49	System power enable	Output	120				

Note:

1. The 2.8V supply supports up to 600mA total from all three pins.
2. In the Type/Dir column, Output is to camera module. Input is from camera module. Bidir is for bidirectional signals.

Legend

Ground	Power	Reserved

Figure 3-1. Camera CSI Connections – C-PHY

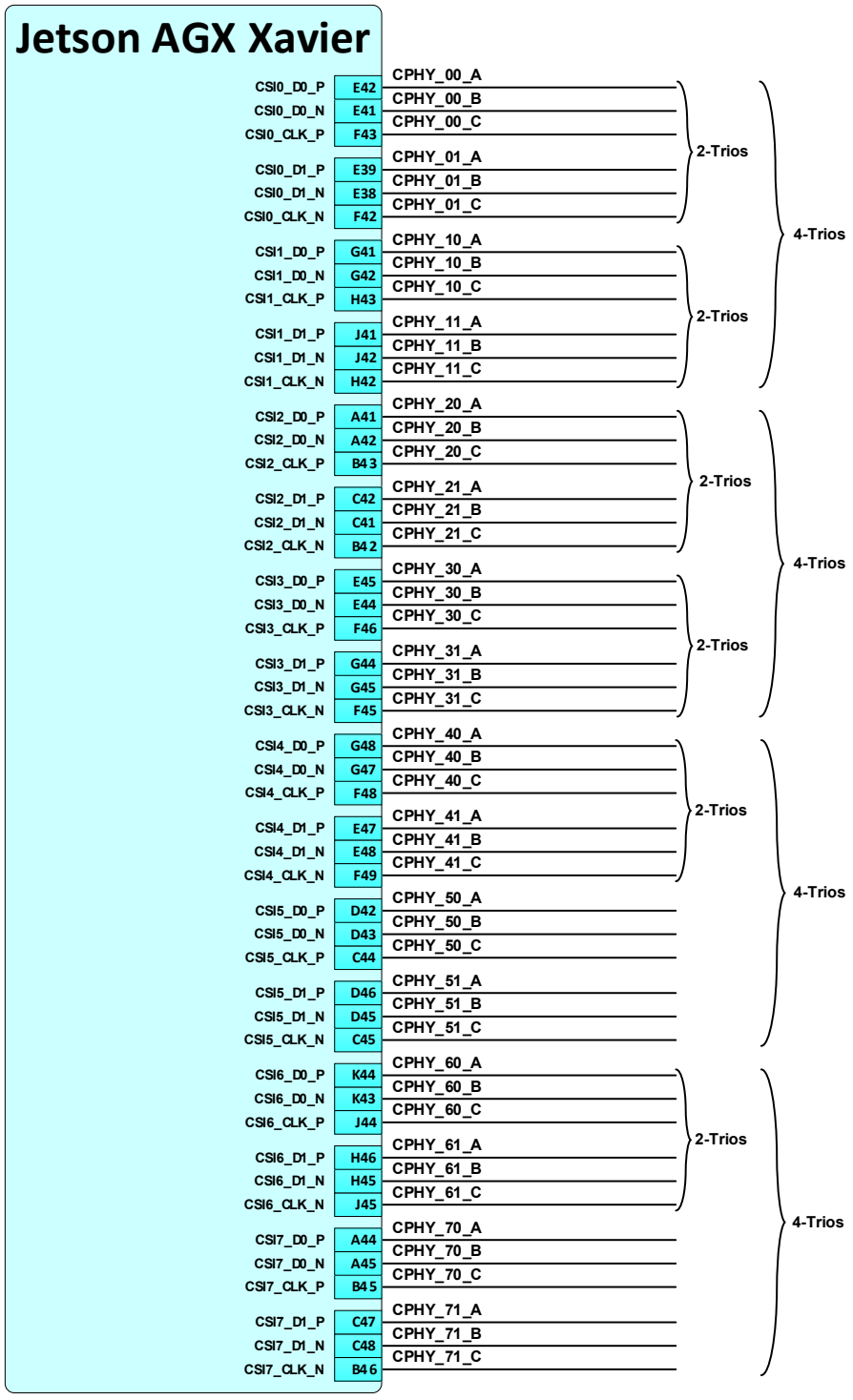
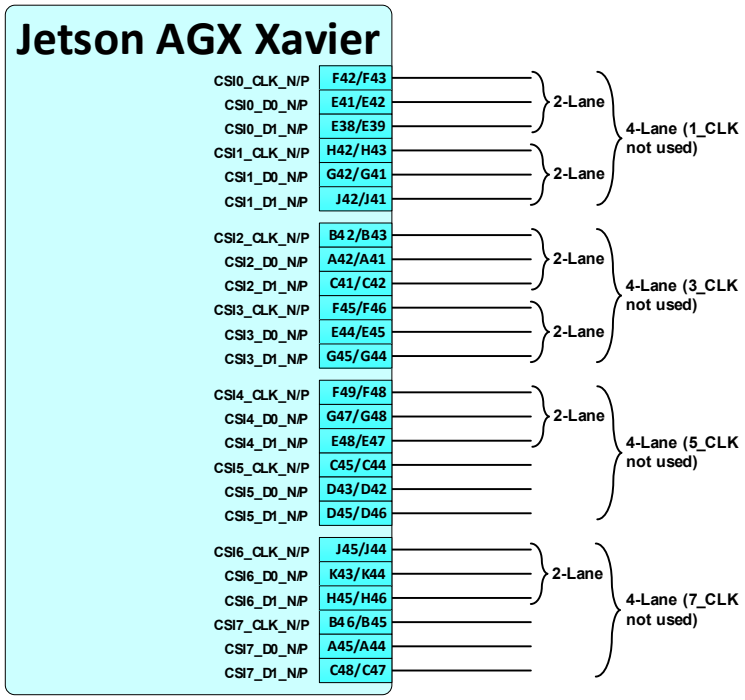


Figure 3-2. Camera CSI Connections – D-PHY



See the *Jetson AGX Xavier OEM Product Design Guide* for routing guidelines. Include the carrier board PCB trace delays in the following tables when calculating max trace length and for skew matching.

Table 3-2. Camera Module CSI PCB Trace Allowances – D-PHY

Worst Case CSI Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Camera Module (ps)	
	1Gbps	1.5Gbps	1Gbps	1.5Gbps
360	1100	800	740	440

Table 3-3. Camera Module CSI PCB Trace Allowances – C-PHY

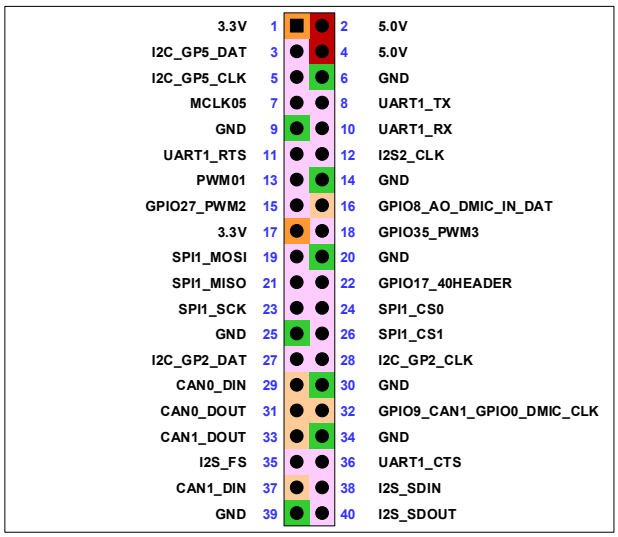
Worst Case CSI Carrier Board PCB Delay/Length (mm)	Max Trace Delay/Length Allowed (ps / mm)		Max Delay/Length for Camera Module (ps / mm)	
	1.7Gsps	1.3Gsps	1.7Gsps	1.3Gsps
50	SL – 700 / 100 MS – 600 / 100	SL – 1723 / 250 MS - 1477 / 250	SL – 350 / 50 MS – 300 / 50	SL – 1378 / 200 MS - 1182 / 200

Note: Max trace delays/lengths above assume CSI device is directly on the board that connects to the camera connector on the DevKit. If there is an additional connector between the camera connector and the end device, see the Jetson AGX Xavier OEM Product Design Guide for additional limitations on speed and/or delay/length.

3.3 40-Pin Expansion Header

The Jetson AGX Xavier carrier board includes a 40-pin (2x20, 2.54 mm pitch) expansion header (J30). The connector used on the carrier board is a Wieson G2100CE04C-008-H.

Figure 3-3. Expansion Header Top View



Note: Caution must be taken when using the CAN[1:0]_DIN, CAN[1:0]_DOUT pins (Exp. Conn. pins 37, 29, 33, and 31). These are pulled to 3.3V when system is powered on due to internal 3.3V pull-ups in the SoC enabled by default. If used, they should only be connected to 3.3V tolerant device pins. The voltage rail can be switched by software after boot to 1.8V, and the internal pull-ups can be disabled, but the initial power-on state of these pins is pulled to 3.3V.

The 40-pin expansion connector includes various audio and control interfaces including:

- I2S (See Note)
- Audio Clock and Control
- Digital Microphone IF
- I2C (x2) (See Note)
- SPI (See Note)
- UART (See Note)

Table 3-4. 40-Pin Expansion Header Pin Description

Pin #	Module Pin Name	Module Pin #	Tegra Pin Name	Usage/Description	Alternate Functionality	Type/ Direction	Pin Drive or Power Pin Max Current	Tegra GPIO Port #	Power-on Default	PU/PD on Module	Notes
1	–	–	–	Main 3.3V Supply	–	Power	1A	–	–	–	1
2	–	–	–	Main 5.0V Supply	–	Power	1A	–	–	–	1
3	I2C5_DAT	C53	DP_AUX_CH3_N	General I2C #5 Data	–	Bidir/OD	±1mA	–	Z	2.2KΩ PU	2
4		–		Main 5.0V Supply	–	Power	1A	–	–	–	1
5	I2C5_CLK	A53	DP_AUX_CH3_P	General I2C #5 Clock	–	Bidir/OD	±1mA	–	Z	2.2KΩ PU	2
6	–	–	–	Ground	–	Ground	–	–	–	–	–
7	MCLK05	L57	SOC_GPIO42	GPIO	Audio Master Clock	Bidir	±20uA	Q.06	PD	–	3
8	UART1_TX	K53	UART1_TX	GPIO	UART #1 Transmit	Output	±24mA	R.02	PD	–	4
9	–	–	–	Ground	–	Ground	–	–	–	–	–
10	UART1_RX	K54	UART1_RX	GPIO	UART #1 Receive	Input	–	R.03	Z	–	4
11	UART1_RTS	L51	UART1_RTS	GPIO	UART #1 Request to Send	Output	±24mA	R.04	PD	–	4
12	I2S2_CLK	G4	DAP2_SCLK	GPIO	Audio I2S #2 Clock	Bidir	±20uA	H.07	PD	–	3
13	GPIO32	J55	SOC_GPIO04	GPIO	PWM	Bidir	±20uA	R.00	PD	–	3
14	–	–	–	Ground	–	Ground	–	–	–	–	–
15	GPIO27	H52	SOC_GPIO54	GPIO	PWM	Bidir	±20uA	N.01	PD	–	3
16	GPIO08	B62	CAN1_STB	GPIO	Digital Mic Input Data	Input	±1mA	BB.00	PD	–	5
17	–	–	–	Main 3.3V Supply	–	Power	1A	–	–	–	1
18	GPIO35	L50	SOC_GPIO12	GPIO	PWM	Output	±20uA	H.00	Z	–	3, 7
19	SPI1_MOSI	D55	SPI1_MOSI	GPIO	SPI #1 Master Out/Slave In	Bidir	±20uA	±20uA	PU	–	3
20	–	–	–	Ground	–	Ground	–	–	–	–	–
21	SPI1_MISO	A56	SPI1_MISO	GPIO	SPI #1 Master In/Slave Out	Bidir	±20uA	Z.04	PU	–	3
22	GPIO17	A54	SOC_GPIO21	GPIO		Bidir	±20uA	Q.01	PD	–	3
23	SPI1_CLK	J57	SPI1_CLK	GPIO	SPI #1 Shift Clock	Bidir	±20uA	Z.03	PD	–	3
24	SPI1_CS0#	E55	SPI1_CS0	GPIO	SPI #1 Chip Select #0	Bidir	±20uA	Z.06	PU	–	3
25	–	–	–	Ground	–	Ground	–	–	–	–	–
26	SPI1_CS1#	B56	SPI1_CS1#	GPIO	SPI #1 Chip Select #1	Bidir	±20uA	Z.07	PU	–	3
27	I2C2_DAT	K61	GEN2_I2C_SDA	General I2C #2 Data	GPIO	Bidir/OD	±1mA	DD.00	Z	2.2KΩ PU	2
28	I2C2_CLK	J61	GEN2_I2C_SCL	General I2C #2 Clock	GPIO	Bidir/OD	±1mA	CC.07	Z	2.2KΩ PU	2
29	CAN0_DIN	F58	CAN0_DIN	GPIO	CAN #0 Data In	Input	±1mA	AA.03	PU	–	5
30	–	–	–	Ground	–	Ground	–	–	–	–	–
31	CAN0_DOUT	D59	CAN0_DOUT	GPIO	CAN #0 Data Out	Output	±1mA	AA.02	PU	–	5
32	GPIO09	C61	CAN1_EN	GPIO	Digital Mic Input Clock	Bidir	±1mA	BB.01	Z	–	5
33	CAN1_DOUT	H61	CAN1_DOUT	GPIO	CAN #1 Data Out	Output	±1mA	AA.00	PU	–	5

Pin #	Module Pin Name	Module Pin #	Tegra Pin Name	Usage/Description	Alternate Functionality	Type/ Direction	Pin Drive or Power Pin Max Current	Tegra GPIO Port #	Power-on Default	PU/PD on Module	Notes
34	–	–	–	Ground	–	Ground	–	–	–	–	–
35	I2S2_FS	E4	DAP2_FS	GPIO	AUDIO I2S #2 L/R Clock	Bidir	±20uA	I.02	PD	–	3
36	UART1_CTS	H54	UART1_CTS	GPIO	UART #1 Clear to Send	Input	–	R.05	PU	–	4
37	CAN1_DIN	B61	CAN1_DIN	GPIO	CAN #1 Data In	Input	±1mA	AA.01	PU	–	5
38	I2S2_DIN	F6	DAP2_DIN	GPIO	Audio I2S #2 Data in	Input	±20uA	I.01	PD	–	3, 7
39	–	–	–	Ground	–	Ground	–	–	–	–	–
40	I2S2_DOUT	F5	I2S_DOUT	GPIO	Audio I2S #2 Data Out	Output	±20uA	I.00	PD	–	3, 7

Notes:
1. This is current capability per power pin.
2. These pins connect to the SoC through a FXMA2102L8X level shifter. They are open-drain (either pulled up, or driven low by the SoC when configured as outputs). The voltage level at the header pins can be selected by J514 to be 1.8V (2-3) or 3.3V (1-2). The max drive that meets the data sheet VOL is 1mA.
3. These pins connect to TI TXB0108 level translators. The voltage level at the header pins is selectable (see Note #2). Due to the design of these devices, the output drivers are very weak so they can be overdriven by another connected device output for bidirectional support.
4. These pins connect to a SN74LVC4T245 buffer. The voltage level at the header pins is selectable (see Note #2).
5. These pins are directly connected to the SoC. The max drive that meets full data sheet VOL/VOH is 1mA.
6. For power-on default, PD = SoC Internal Pull-down, PU - SoC Internal pull-up, and Z – Tristate
7. In the Type/Dir column, Output is to expansion header. Input is from expansion header. Bidir is for bidirectional signals.
8. The direction indicated matches that indicated in the reference design schematics. These signals can be bidirectional.

Legend	Ground	5.0V Power Rail	3.3V Power Rail

3.3.1 40-Pin Expansion Header Interface Guidelines

See the *Jetson AGX Xavier OEM Product Design Guide* for routing guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length and for skew matching.

Table 3-5. 40-Pin Expansion Header Related Carrier PCB Trace Delays

Module Module Signal	Carrier Board PCB Delay max per pin (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)		Module Module Signal	Carrier Board PCB Delay max per pin (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)
I2S2	250	3600	3350		SPI1	200	1228	1028

Note: Max trace delay allowed for SPI assumes a single load case. If two loads are implemented, See the *Jetson AGX Xavier OEM Product Design Guide* for details.

3.4 Fan Control

The Jetson carrier board includes a 4-pin fan header (J9).

Figure 3-4. 4-Pin Fan Header – J9

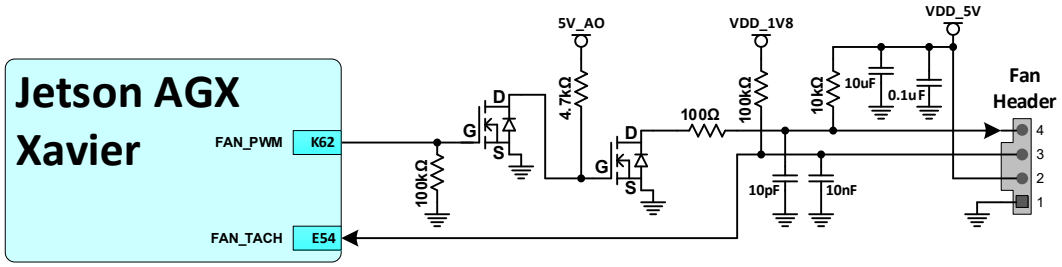


Table 3-6. Fan Connector Pin Description

Pin #	Module Pin Name	Module Pin #	Tegra Pin Name	Usage/Description	Type/Dir Default
1	–	–	–	Ground	Ground
2	–	–	–	Gated version of Main 5.0V Supply (Enabled by VDD_3V3_SLP)	Power
3	FAN_TACH	E54	SOC_GPIO22	Fan Tachometer signal	Input
4	FAN_PWM	K62	TOUCH_CLK	Fan Pulse Width Modulation signal	Output

Note: In the Type/Dir column, Output is to fan connector. Input is from fan connector. Bidir is for bidirectional signals.

Legend	Ground	Power

3.5 Automation Header

The Jetson carrier board includes an 8-pin header (J508) that makes accessible several critical system control signals.

Table 3-7. Automation Header Description

Pin #	Module Pin Name	Module Pin #	Tegra Pin Name	Usage/Description	Type/Dir Default
1	–	–	–	Ground	Ground
2	FORCE_RECOVERY_N	L10	SOC_GPIO00	Force Recovery Strap	Output
3	SYS_RESET_N	L60	SYS_RESET_N	System Reset – Connected to Reset Button on carrier board	Output
4	–	–	–	Power Button On – Connected to Power Button on carrier board	Output
5	–	–	–	Output from USB Type C PD Controller (See note)	Output
6	–	–	–	ACOK (USB Type C or DC Jack power OK). To button power-on controller.	Input
7	STANDBY_ACK_N	J60	SOC_PWR_REQ	Carrier board standby	Input
8	SYSTEM_OC_N	A61	BATT_OC	System Overcurrent indicator	Input

Notes: Auto-Power-On is enabled when Pin 5 and Pin 6 are tied together
In the Type/Dir column, Output is to header. Input is from header. Bidir is for bidirectional signals.

Legend	Ground	Power

3.6 DC Power Jack

The Jetson carrier board uses a DC power jack (J2) to bring in the power from the included DC power supply. The jack used on the Carrier board is a Singatron Enterprise 2DC-G213-B73F.

Table 3-8. DC Jack Pin Description

Pin #	Module Pin Name	Module Pin #	Tegra Pin Name	Usage/Description	Type/Dir Default
1	–	–	–	Option for Main DC input supplying SYS_VIN_HV (Typc C VBUS1 or VBUS2 are other options).	Power
2	–	–	–	Ground	Ground
3	–	–	–	Ground	Ground
4	–	–	–	Ground	Ground
5	–	–	–	Ground	Ground
6	–	–	–	Ground	Ground

Chapter 4. Miscellaneous

4.1 Buttons, Jumpers, and Indicators

Table 4-1 through Table 4-3 describe the buttons (switches), jumpers and indicators.

Table 4-1. Buttons

Button	Description	Usage
S501	Power button	Used to power system up if off, or power down if on. If held for >10 seconds, will shut down the system.
S502	Reset button	Used to force a full system reset.
S503	Recovery button	Used to enter Force Recovery Mode. Button is held down while either system is first powered on, or by pressing and releasing reset button while recovery button is pressed.

Table 4-2. Jumpers

Jumper	Description	Usage
J514	Voltage select header	Selects the level shifter voltage on the non-Jetson AGX Xavier side of the level shifters for the signals in the following list. When a jumper is on Pin 1 and Pin 2, 3.3V level is selected. When on Pin 2 and Pin 3, 1.8V level is selected. • Audio MCLK05, I2S2 • PWM[3:1] • SPI1 • UART1 • I2C_GP[5,2]

Table 4-3. LED Indicators

LED	Description	Usage
DS2	SOC Regulator Power LED (Green)	Indicates when the main 5.0V (VDD_5V) supply is enabled

4.2 I2C Interface Usage

The following tables show the I2C usage on the Jetson AGX Xavier module and developer kit carrier board.

Table 4-4. Jetson AGX Xavier I2C Interface Usage

Ctrl	Module Pin Names (Xavier Pins)	Usage on Module	I2C Address	Xavier Block	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM	7'h50	CONN	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	Current Monitors	7'h40 and 7'h41	AO	1KΩ to 1.8V (also current monitors via 1.8V-5V level shifters w/10k pull-ups to 5V)
I2C3	I2C3_CLK/DAT			CAM	1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P			EDP	1KΩ to 1.8V
I2C5	(PWR_I2C_SCL/SDA) On-module only	NA	NA	SYS	NA
I2C6	DP0_AUX_CH_N/P			EDP	None
I2C7	DP2_AUX_CH_N/P			EDP	None
I2C8	I2C4_CLK/DAT			AO	1KΩ to 1.8V
I2C9	I2C5_CLK/DAT			EDP	1KΩ to 1.8V

Table 4-5. Jetson AGX Xavier Developer Kit Carrier Board I2C Interface Usage

Ctrlr	Module Pin Names (Xavier Pins)	Usage on Carrier Board	I2C Address	Xavier Block	On-Module Pull-up/voltage
I2C1	I2C1_CLK/DAT	ID EEPROM	7h56	CONN	1KΩ to 1.8V
I2C2	I2C2_CLK/DAT	12V DC-DC USB PD Controller	7'h74 7'h08	AO	1KΩ to 1.8V (also Current Monitors via 1.8V-5V level shifters w/10k pull-ups to 5V)
I2C3	I2C3_CLK/DAT			CAM	1KΩ to 1.8V
I2C4	DP1_AUX_CH_N/P	Audio Codec	7'h1A	EDP	1KΩ to 1.8V
I2C6	DP0_AUX_CH_N/P			EDP	None
I2C7	DP2_AUX_CH_N/P			EDP	None
I2C8	I2C4_CLK/DAT			AO	1KΩ to 1.8V
I2C9	I2C5_CLK/DAT			EDP	1KΩ to 1.8V

Chapter 5. Mechanicals

Figure 5 1 and Figure 5 2 show the mechanical dimensions for the carrier board and the developer kit.

Notes: The following applies to Figure 5-1 and Figure 5-2

- Measurements are in Millimeters
- Tolerances unless otherwise specified are:

. X	± 0.25 mm
.XX	± 0.1 mm

Figure 5-1. Developer Kit Carrier Board Mechanical Dimensions

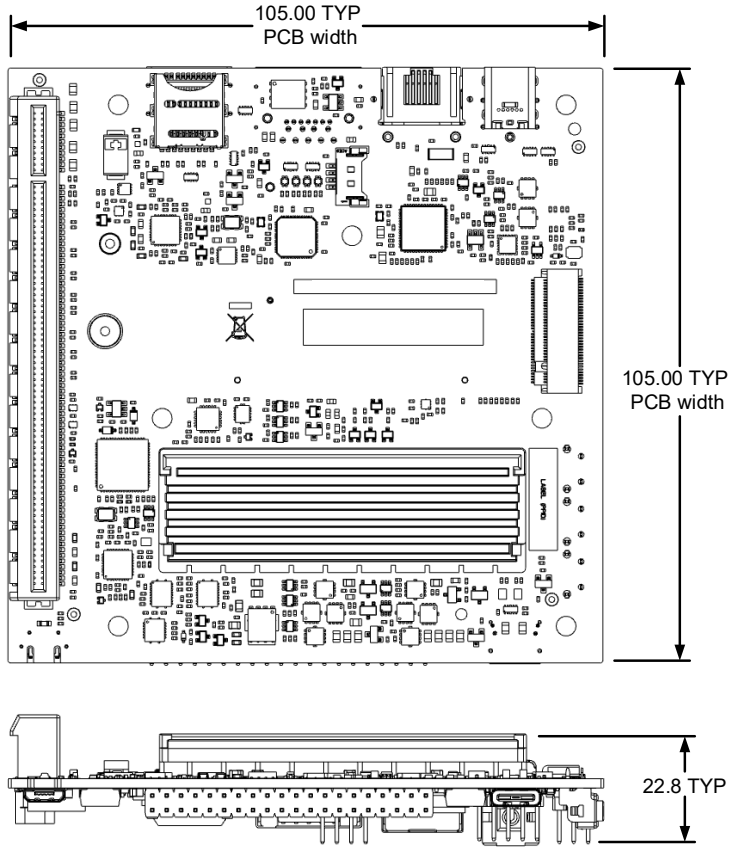
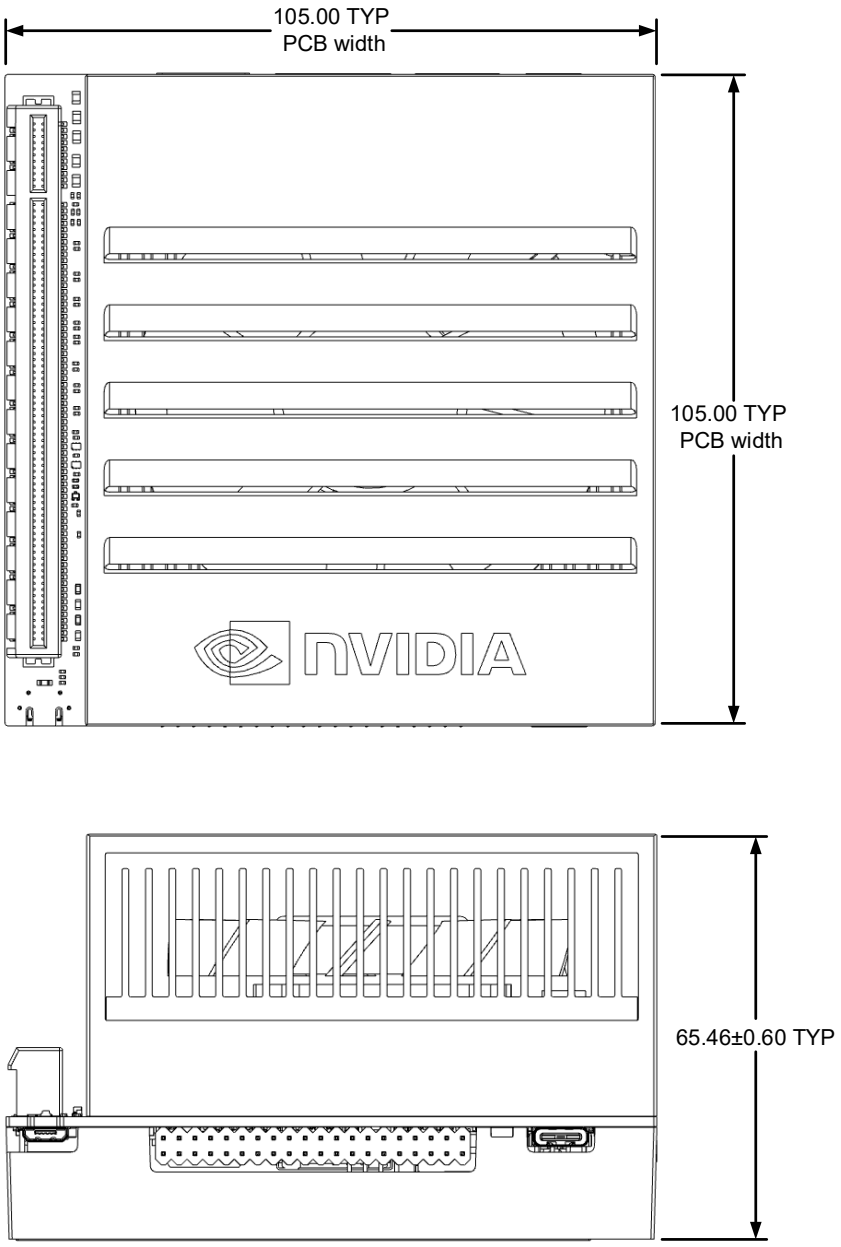


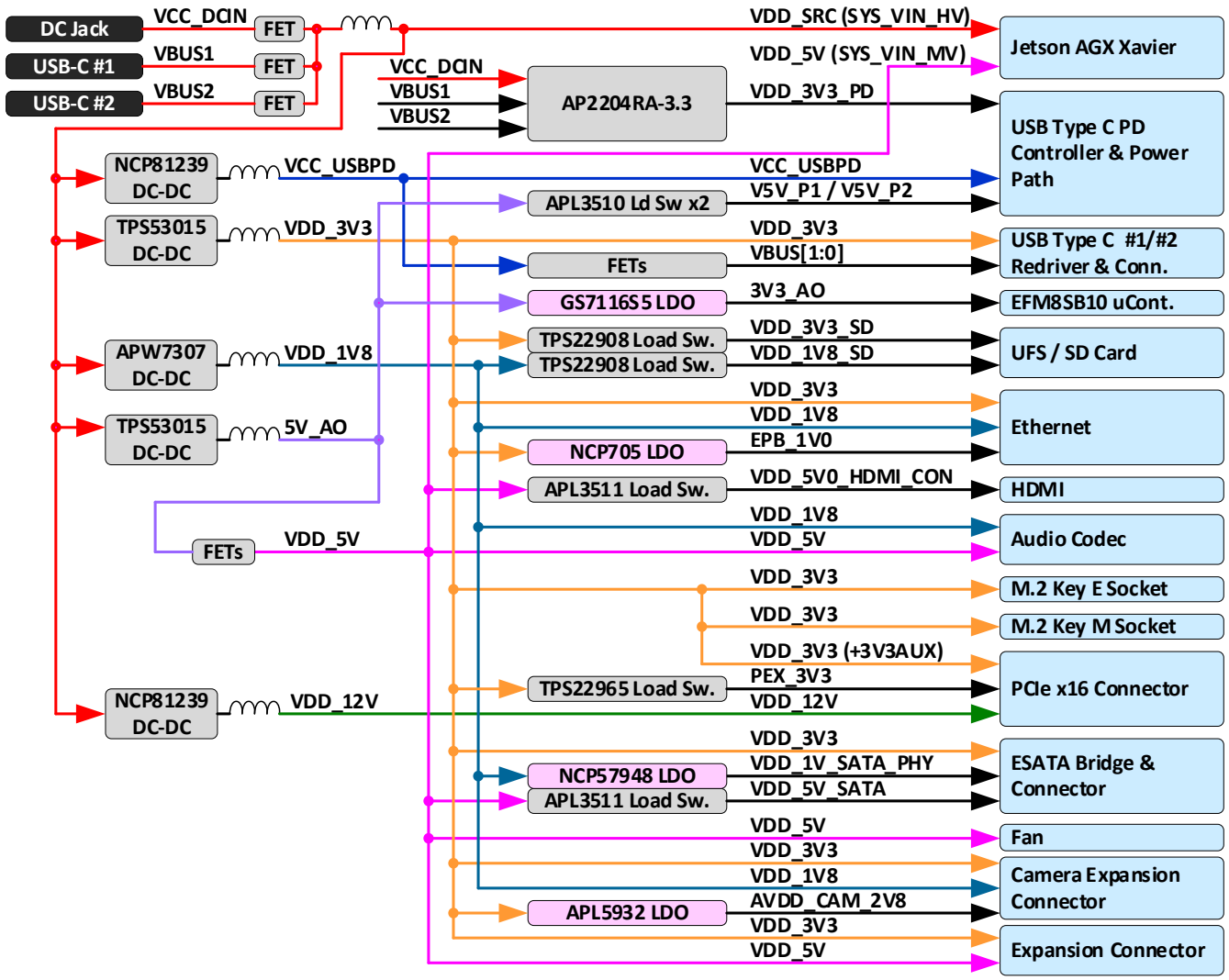
Figure 5-2. Developer Kit Mechanical Dimensions



Chapter 6. Interface Power

Figure 6-1 shows the interface connector power diagram.

Figure 6-1. Interface Connector Power Diagram



The following tables show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 6-1. Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable
VCC_SRC	Main power input from DC Adapter or USB type C VBUS[2:1]	9-20	FETs	DC Adapter or Type C USB	
VCC_USBPD		5-20	NCP81239 Regulator	VCC_SRC	
VDD_3V3_PD		3.3	AP2204RA-3.3 DC-DC	VCC_DCIN/VBUS[2:1]	VCC_DCIN, VBUS[2:1]
5V_AO	Always-on 5V supply	5.0	TPS53015 DC-DC	VCC_SRC	VDD_3V3_PD
VDD_5V	Main 5V supply	5.0	FETs	5V_AO	VIN_PWR_ON
VDD_3V3	Main 3.3V supply	3.3	TPS53015 DC-DC	VCC_SRC	CARRIER_PWR_ON
VDD_1V8	Main 1.8V supply	1.8	APW7307 DC-DC	VCC_SRC	CARRIER_PWR_ON
VDD_12V	12V rail for PCIe, Fan	12.0	NCP81239 DC-DC	VCC_SRC	Module GPIO05
VBUS[2:1]	VBUS pin from USB Type C connectors (alternative is DC Jack)	5-20	FETs	VCC_USBPD	PD Controller
PEX_3V3	PCIe x16 connector +3V3 rail supply	3.3	TPS22965 Load Switch	VDD_3V3	Module GPIO23
VDD_3V3_SD	SD Card & UFS VCC power rail	3.3	TPS22908 Load Switch	VDD_3V3	Module GPIO21
VDD_1V8_SD	UFS VCCQ2 power rail		TPS22908 Load Switch	VDD_1V8	Module GPIO21
EPB_1V0	Ethernet PHY DVDD power rail	1.0	NCP705 LDO	VDD_3V3	VDD_3V3
VDD_5V0_HDMI_CON	5V rail for HDMI connector	5.0	APL3511 Power Switch	VDD_5V0	Module GPIO20
VDD_1V_SATA_PHY	PCIe to eSATA bridge VDD power rail	1.0	NCP57948 LDO	VDD_1V8	VDD_1V8
VDD_5V_SATA	VBUS for USB portion of Hybrid eSATA connector.	5.0	APL3511 Load Switch	VDD_5V	Module GPIO22
DVDD_CAM_LV	Reserved for potential use as Camera Digital power rail	NA	NA	NA	NA
AVDD_CAM_2V8	Camera Analog power rail	2.8	APL5932 LDO	VDD_3V3	Module GPIO36

Table 6-2. Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (A)
VCC_SRC	Main power input from USB Type C connectors or DC Jack	9-20	5.0
VDD_5V	Main system 5V supply	5.0	9.5
VDD_3V3	Main system 3.3V supply	3.3	10.5
VDD_1V8	Main system 1.8V supply	1.8	2.8
VDD_12V	12V rail for PCIe connector & optionally for Fan	12	5.5
AVDD_CAM_2V8	Analog Camera rail	2.8	3.0

Notes:

1. The values shown in the "Max Current" column indicate the total power available on the expansion connectors minus the current used on the platform (not per connector pin).
2. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from VDD_12V, VDD_5V, VDD_3V3, or VDD_1V8 to generate the desired rail.

Table 6-3. Supply Current Capabilities Per Connector Per Supply

Power Rails	Connector	(V)	Max Allocated Current (A)
VDD_12V	Fan (optional)	12	0.45
	PCIe		3.0
VDD_5V	40-pin	5	1.0
	Fan (default)		0.15
VDD_3V3	PCIe 3.3V Aux	3.3	1.0
	Camera		1.44
	M.2 Key M		0.93
	M.2 Key E		0.8
PEX_3V3	PCIe 3.3V	3.3	3.0
AVDD_CAM_2V8	Camera	2.8	0.6
VDD_1V8	Camera	1.8	1.72

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