

CO102

Computer Hardware

Experiment

Lecture 06: VHDL – Sequential Statements 2

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Loop statement

- LOOP is used when a piece of code that must be copied several times.

```
[label:] FOR identifier IN range LOOP  
    statements;  
END LOOP [label];
```

Example of LOOP

```
FOR i IN 0 TO 2 LOOP  
    x(i) <= a AND w(i+2);  
    y(i) <= w(i);  
END LOOP;
```

is equivalent to:

```
x(0) <= a AND w(2);  
y(0) <= w(0);  
x(1) <= a AND w(3);  
y(1) <= w(1);  
x(2) <= a AND w(4);  
y(2) <= w(2);
```

Remark

- The range of LOOP must be a constant value.

For i IN 0 TO k LOOP

‘k’ must be a constant value, say 15.

LOOP example 2

```
library ieee;
use ieee.std_logic_1164.all;
entity loop2 is
port(
    din : in std_logic_vector(31 downto 0);
    dout : in std_logic_vector(31 downto 0));
end loop2;
architecture loop2_arch of loop2 is
begin
    process(din)
    begin
        for i in 0 to 31 loop
            dout(i) <= din(i);
        end loop;
    end process;
end loop2_arch;
```

Variable for PROCESS

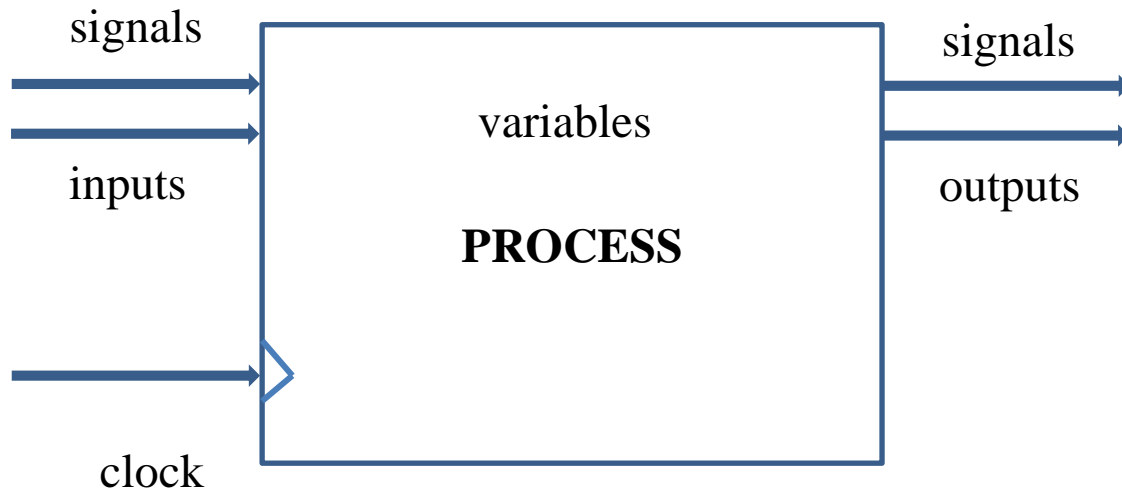
- Variable is only used inside PROCESS.

```
architecture test_arch of test is
-- signals are defined here.
signal a : std_logic;
begin
    process(din)
    -- variables are defined here.
    variable b : std_logic;
    begin
        statements;
    end process;
end test_arch;
```

Variable vs Signal

- Variables
 - Assignment symbol: `d1 := d0;`
 - Variables are updated immediately, the new value can be promptly used in the next line of code.
- Signals
 - Assignment symbol: `d1 <= d0;`
 - Signals will not be updated until the end of a PROCESS.

Variable vs Signal



Example

```
architecture test_arch of test is
  signal a : std_logic_vector(3 downto 0);
  signal result1 : std_logic_vector(3 downto 0);
  signal result2 : std_logic_vector(3 downto 0);
begin
  process(din)
    variable b : std_logic_vector(3 downto 0);
  begin
    a <= din + 1;
    b := din + 1;
    result1 <= a + 1;
    result2 <= b + 1;
  end process;
end test_arch;
```

Example

