Input or output	Signal name	R-format	lw	sw	beq	j	lui	slti
Inputs	op5	0	1	1	0	0	0	0
	op4	0	0	0	0	0	0	0
	op3	0	0	1	0	0	1	1
	op2	0	0	0	1	0	1	0
	op1	0	1	1	0	1	1	1
	op0	0	1	1	0	0	1	0
Outputs	RegDst	1	0	x	x	0	0	0
	ALUSrc	0	1	1	0	0	1	1
	MemtoReg	0	1	x	x	0	0	0
	RegWrite	1	1	0	0	0	1	1
	MemRead	0	1	0	0	0	x	x
	MemWrite	0	0	1	0	0	0	0
	Branch	0	0	0	1	0	0	0
	Jump	0	0	0	0	1	0	0
	ALUOp1	1	0	0	0	0	1	0
	ALUOp2	1	0	0	0	0	1	1
	ALUOp3	1	0	0	1	0	0	0