**Computer Hardware Experiments**

Lab\_06: 12-hour clock

**Name : Student\_ID:**

**Description**:

In this lab, you are going to implement a 12-hour clock with the following entity (myclock.vhd):

entity myclock is

port (

clk : in std\_logic;

reset : in std\_logic;

preset : in std\_logic;

hin : in std\_logic\_vector (3 downto 0);

min : in std\_logic\_vector (5 downto 0);

sin : in std\_logic\_vector (5 downto 0);

apin : in std\_logic;

hout : out std\_logic\_vector (3 downto 0);

mout : out std\_logic\_vector (5 downto 0);

sout : out std\_logic\_vector (5 downto 0);

apout : out std\_logic

);

end myclock;

This is a 12-hour digital clock, *hout* designates the hour, *mout* designates the minute, *sout* designates the second, and *pout* designates morning or afternoon. For example, if current time is 3:08:12 pm, then *hout* = 3, *mout* = 8, *sout* = 12, *apout* = 1. If current time is 9:08:12 am, then *hout* = 9, *mout* = 8, *sout* = 12, *apout* = 0.

The digital clock can increment by 1 second on every clock cycle, for example, the current time is 3:08:12, the time will be 3:08:13 in next clock cycle, and the time will be 3:09:00 after 47 clock cycles.

The meaning of other ports is as follows:

* **clk**: This is the clock signal. At the positive edge of every clock cycle, the digital clock can increment by 1 second.
* **reset:** This is an asynchronous reset. The output of the digital clock becomes 00:00:00 immediately when *reset* = ‘1’ no matter what the clock signal (**clk**) is.
* **hin**, **min**, **sin**, **apin**: These four signals are used to set the clock to a particular time.
* **preset**: This is an asynchronous signal, which is used to set the clock to a particular time. When *reset* = ‘0’ and *preset* = ‘1’, the digital clock will be set to a particular time immediately, i.e. *hout* = *hin*, *mout* = *min*, *sout* = *sin*, *apout* = *apin*. And the digital clock starts to count from this preset time when *preset* = ‘0’.

**Procedure**:

Step 1. Implement your clock.vhd.

Step 2. you need to write the experiment report.

The report should be composed of

1. The VHDL source code;
2. The simulation waveform.