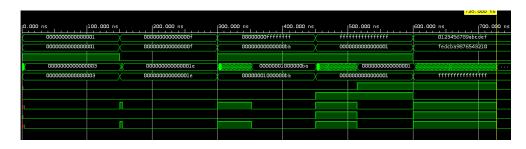
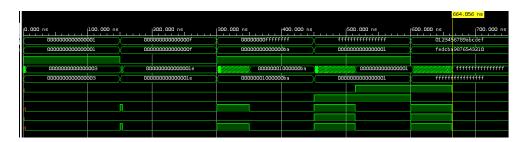
# Sample Waveforms:

With delay:

Ripple Carry Adder

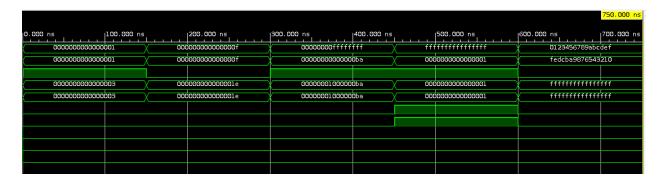


2x32 Carry Select Adder



Without delay:

Ripple Carry Adder

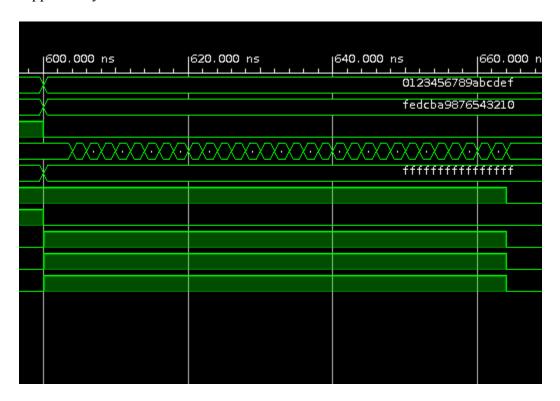


#### 2x32 Carry Select Adder

			583.483 ns				183 ns		
0.000 ns	00.000 ns	200.000 ns	300.000 ns	400.000 ns		500.000 ns	, 16	00.000 ns	700.000 ns
000000000000000000000000000000000000000	000	000000000000f	00000000fffff	fff	fff	ffffffffffff	$\equiv$ X	0123456789ab	def
000000000000000	000	00000000000000f	0000000000000	0ba	000	000000000000000001		fedcba9876543	3210
000000000000000	33 000	0000000000001e	0000000100000	0ba	000	00000000000001	$\equiv$ X	ffffffffffff	ffff
000000000000000000000000000000000000000	33 000	0000000000001e	0000000100000	Oba )	000	00000000000001	$\equiv$ $\times$	fffffffffff	ffff

Comparison of longest path delay:

## Ripple Carry Adder

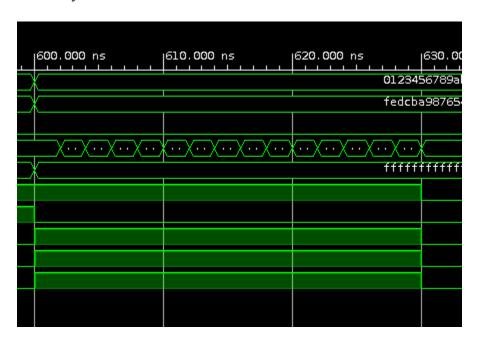


2x32 Carry Select Adder

#### Leonardo Mattos Martins U25267206 Lab 3 Write up

						728.0	000 ns				
600.000 ns	620.000 ns	640.000 ns	660.000 ns	680.000 ns	700.000 ns	720.000	ns				
0123456789abcde f											
fedcba9876543210											
XXXXXXXXXXX	(XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXX	(XXXXXXXXXXXXXX	(XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	XXXXXXXXXXXXX	$\infty$	ffffff.				
mmmmm											
				0123456789abcdef fedcba9876543210	0123456789abcdef fedcba9876543210	0123456789abcdef fedcba9876543210	600.000 ns   620.000 ns   640.000 ns   660.000 ns   660.000 ns   700.000 ns   720.000				

## 8x8 Carry Select Adder



# Questions to Answer:

What are the timings of your adders in gate delays?

RCA = 
$$2N$$
  
=  $2 * 64$   
=  $128$  gate delays

$$2x32 \text{ CSA}$$
 =  $2k + 2(j - 2)$   
=  $2*32 + 2(2 - 2)$   
= 64 gate delays

$$8x8 \text{ CSA}$$
 =  $2*8 + 2(8 - 2)$   
=  $28 \text{ gate delays}$ 

Are they what you expect? Why or why not?

The values above are reflected in the waveforms as the longest path delay. It is also shown how in most cases the bits do not propagate all the way through the adder and the time required is less than what was calculated.

Leonardo Mattos Martins U25267206 Lab 3 Write up

Explanation of timings: All testbenches use the same conditions to best evaluate their performance against each other. The test cases are: forcing an overall carry out, random large A&B input (w/ and w/o carry), random small A&B input (w/ and w/o carry), random combinations, and the largest amount of delay.