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Lab7 Write Up

Add “1 ahead” forwarding
For “1 ahead” forwarding, logic was implemented in the forwarding unit to check if the previous instruction (which is now in EX/MEM) featured one of the registers required for this operation, and if so, pass the EX/MEM version of the register as one of the inputs for the ALU.

Add “2 ahead” forwarding
For “2 ahead” forwarding, logic was implemented in the forwarding unit to check if the anti-previous instruction (which is now in MEM/WB) featured one of the registers required for this operation, and if so, pass the MEM/WB version of the register as one of the inputs for the ALU.

Add arbitration logic for deciding between 1 & 2 ahead
“1 ahead” and “2 ahead” logic are dealt with by mutual exclusivity, as for a single register either 1 or 2 ahead can occur, but not both.

Add logic for $0 write
An additional condition is added to the assignment of both ForwardA and ForwardB so they will be assigned to 0 if someone attempts to write to the $0 register, meaning no forwarding can occur and $0 cannot be written to.

Add logic for No Write
Checking the RegWrite flag at the EX/MEM and MEM/WB stages lets us check if an instruction such as LW or SW was executed meaning no forwarding is required.

Check register bypass works
This is accomplished experimentally via the testbench

Modified Hardware: A forwarding unit, and 2 MUXes responsible for all of the tasks described in the Lab 7 Description.

Diagram: