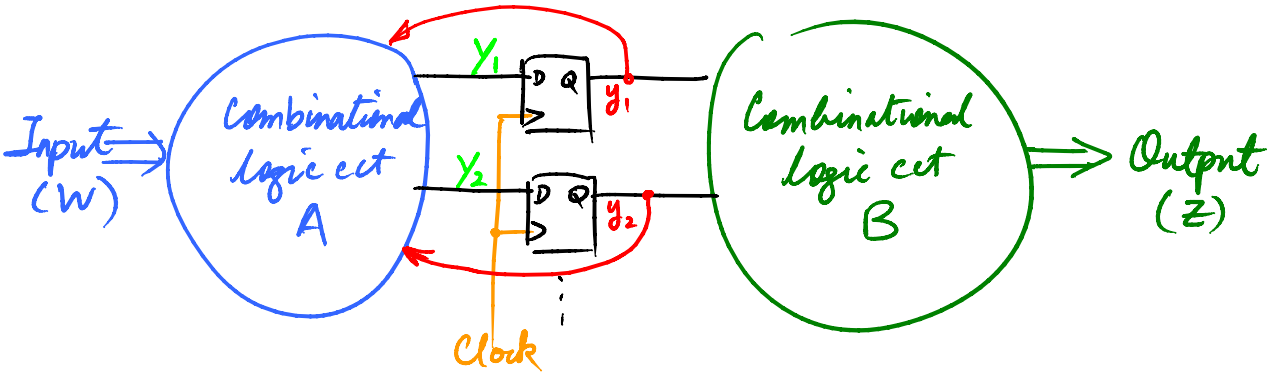
6.1-2 Finite State Machine (FSM) – moore model



A FSM is a sequential circuit that has inputs (W), finite states (y) and outputs (Z).

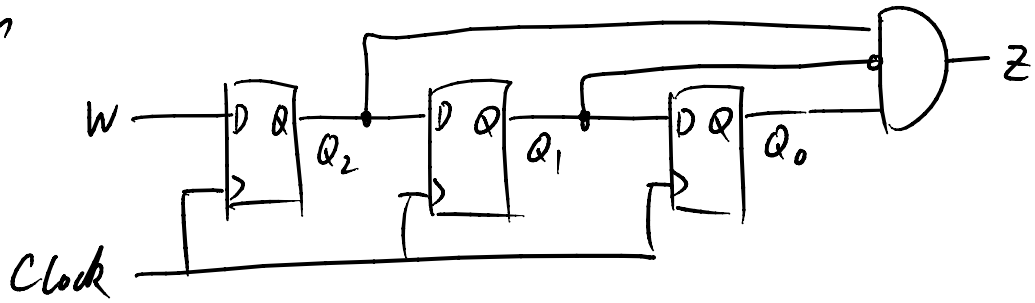
present states at any given clock cycle are represented by $y_1, y_2 \cdots$ (Q's of ffs)

next states are represented by $Y_1, Y_2 \cdots$ (D's of ffs)

Design example: design a FSM that controls a machine which receives a status signal (W) and produce an output ERROR signal (Z) when ever a pattern of "101" in three successive clock cycles has occured. i.e. Z should be set to "1" in the next clock cycle and then set back to "0" afterward.

Clock cycle:	1	2	3	4	5	6	7	8	9	...
W:	0	0	1	1	0	1	0	1	1	...
Z:	0	0	0	0	0	0	1	0	1	...

By inspection

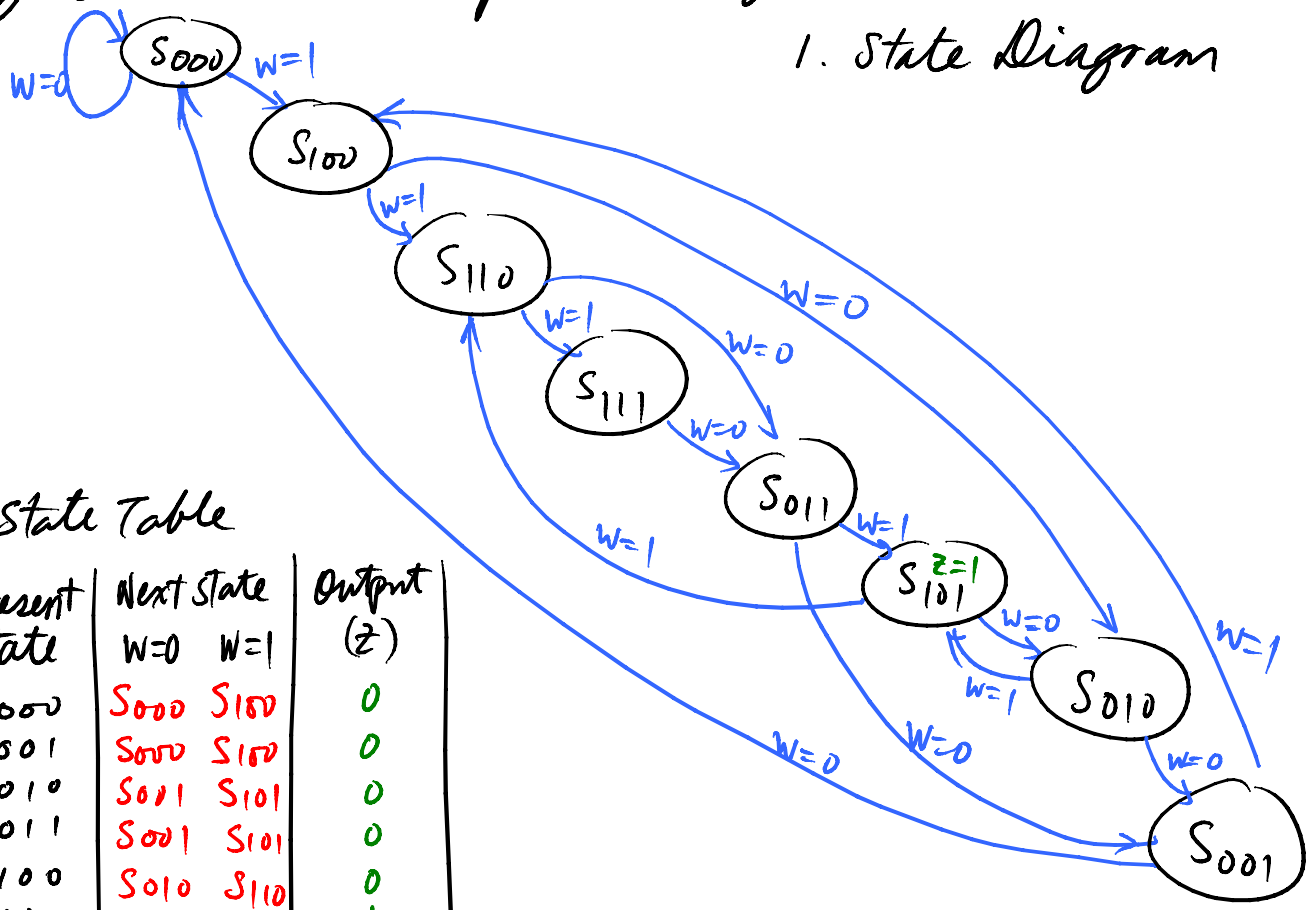


Design Procedure for FSM

1. Draw state diagram (from your understanding of the problem)
2. Draw State table (different form of the state diagram)
3. choose # of FFs to represent those states ($\geq \log_2$(# of states))
4. Draw state-assigned table (use FFs to encode states)
5. Derive the combinational logic blocks A & B.
6. Draw the FSM circuit.

→ go back to our "101" pattern recognition problem.

1. State Diagram



2. State Table

Present State	Next State W=0	Next State W=1	Output (z)
S000	S000	S100	0
S001	S000	S100	0
S010	S011	S101	0
S011	S001	S101	0
S100	S010	S110	0
S101	S010	S110	1
S110	S011	S111	0
S111	S011	S111	0

state names W — input

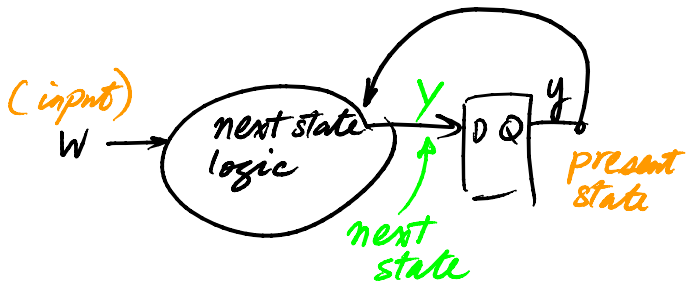
3. How many FFs are needed to represent 8 states? (3)

$y_2 y_1 y_0 = 000$ for S_{000}
$y_2 y_1 y_0 = 001$ for S_{001}
⋮

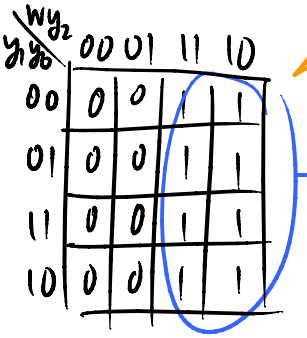
} state encoding or state assignment

4. State-assigned Table

Present state $y_2 y_1 y_0$	Next State W=0 $Y_2 Y_1 Y_0$	Next State W=1 $Y_2 Y_1 Y_0$	Output z
0 0 0	0 0 0	1 0 0	0
0 0 1	0 0 0	1 0 0	0
0 1 0	0 0 1	1 0 1	0
0 1 1	0 0 1	1 0 1	0
1 0 0	0 1 0	1 1 0	0
1 0 1	0 1 0	1 1 0	1
1 1 0	0 1 1	1 1 1	0
1 1 1	0 1 1	1 1 1	0



we want to find Y_2 as a function of W(input) and $y_2 y_1 y_0$ (present state)



K-map for Y_2

$Y_2 = W$

by inspection

$Y_1 = y_2$

$Y_0 = y_1$

5. find next-state logic and output logic expression.

output $z = y_2 \bar{y}_1 y_0$

6. Draw the FSM circuit