```
1   module part5(input [2:0]KEY, input [17:0]SW, output [17:0]LEDR, output [2:0]LEDG, output [6:
    0]HEX0);
2
3      wire [2:0]c;
4
5      part3 inst1(KEY, SW, LEDR, c);
6      part4 call(c, HEX0);
7
8      assign LEDG = c;
9
10  endmodule
11
```