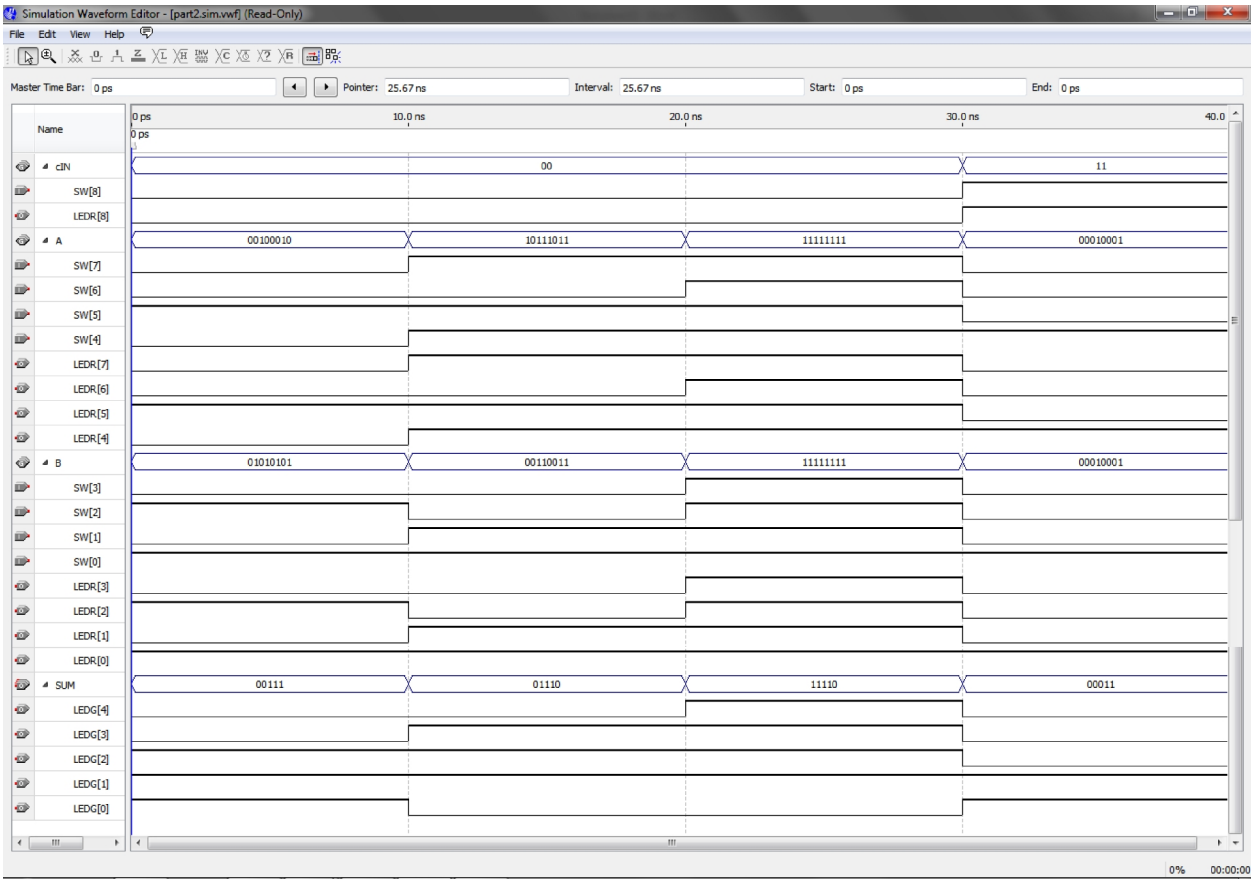
```
1   module part2(input [8:0]SW, output [8:0]LEDR, output [4:0]LEDG);
2
3      wire [3:0] A, B, S;
4      wire [2:0] C;
5      wire cIN, cOUT;
6
7      assign A = SW[7:4];
8      assign B = SW[3:0];
9      assign cIN = SW[8];
10
11     assign LEDR = SW;
12     assign LEDG[3:0] = S;
13     assign LEDG[4] = cOUT;
14
15     fullAdder FA1(A[0], B[0], cIN, S[0], C[0]);
16     fullAdder FA2(A[1], B[1], C[0], S[1], C[1]);
17     fullAdder FA3(A[2], B[2], C[1], S[2], C[2]);
18     fullAdder FA4(A[3], B[3], C[2], S[3], cOUT);
19
20    endmodule
21
22    module fullAdder(input a, b, cI, output s, cO);
23
24     wire d = a ^ b;
25     assign s = cI ^ d;
26     mux2to1 call(b, cI, d, cO);
27
28  endmodule
29
30  module mux2to1(input x, y, s, output m);
31
32     assign m = (~s & x) | (s & y);
33
34  endmodule
```


Simulation Waveform Editor - [part2.sim.vwf] (Read-Only)
File Edit View Help
Master Time Bar: 0 ps
Pointer: 25.67 ns
Interval: 25.67 ns
Start: 0 ps
End: 0 ps
Name
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0
cIN
00
11
SW[8]
LEDR[8]
A
00100010
10111011
11111111
00010001
SW[7]
SW[6]
SW[5]
SW[4]
LEDR[7]
LEDR[6]
LEDR[5]
LEDR[4]
B
01010101
00110011
11111111
00010001
SW[3]
SW[2]
SW[1]
SW[0]
LEDR[3]
LEDR[2]
LEDR[1]
LEDR[0]
SUM
00111
01110
11110
00011
LEDG[4]
LEDG[3]
LEDG[2]
LEDG[1]
LEDG[0]
0%
00:00:00