```
1   module part4(input [2:0]SW, output [6:0]HEX0);
2
3      wire [2:0]c = SW;
4      wire [6:0]temp;
5
6      assign temp[0] = ~c[2];
7      assign temp[1] = ~c[1] | (c[0] & ~c[2]);
8      assign temp[2] = (~c[1] & (c[0] | c[2])) | (~c[2] & c[1] & ~c[0]);
9      assign temp[3] = ~c[2] & c[1];
10     assign temp[4] = ~c[2] & (~c[1] | c[0]);
11     assign temp[5] = ~((c[1] | c[2]) & (c[1] | c[0]) & (c[2] | c[0]));
12     assign temp[6] = ~c[2] | ~(c[0] | c[1]);
13
14     assign HEX0 = ~temp;
15
16  endmodule
```