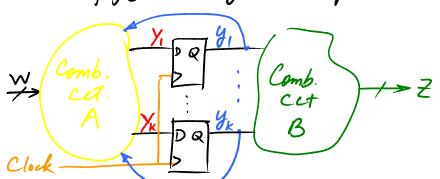
Finite State Machine (FSM)

Defin an FSM is a sequential circuit, that has imputes) W.

ff's called y and ontput(s) Z.



The FSM has a state at any given clock cycle which is represented by your year.

The next state Y.... X

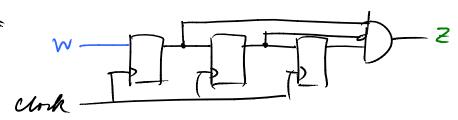
when a clock edge I occurs is dependent on values of inputs) w, as well as the present (current) state yi. yk.

Llesign enemple:

— We need to design a FSM that controls a machine which receives a status signal (W) and produces an ener signal (Z) when ever a pattern of 101 in three successive clock cycles has occured. That is Z should be set to "I" in the next clock cycle and then set back to "ofterward.

Clock cycle: 1 2 3 4 5 6 7 89 --W: 0 0 1 1 0 1 0 1 1 --Z: 0 0 0 0 0 0 1 0 1 ...

By inspection.

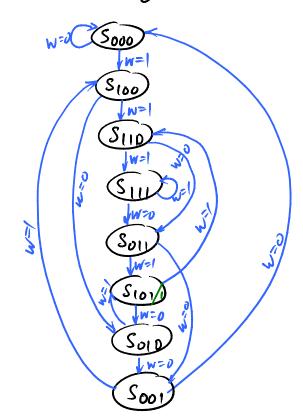


Design Procedure for FSM

- 1. Draw State Diagram (from your imagination)
- 2. Draw State Table
- 3. Choose the # of FF's (> log_(# of states)), also choose valuations of FF's to represent each state (state codes)
- 4. Draw State-assigned Table (using FF's codes)
- 5. Llerive Comb. Log A, and Comb. Log B.
- 6. Draw the FSM cet.

back to 101' pattern enample

1. State Diagram (based on the input information (W))



2. State Table

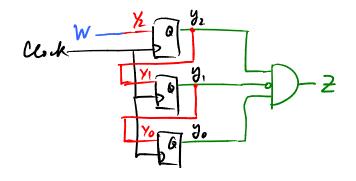
Present state	Next state	output 2
5000	Soon Sin	0
Soul	Som Sin	0
S010	S001 S101	0
S011	S001 S101	0
S100 S(01	Solo Silo	0
Sil	S010 S110	1
3111	Son 5111	0
- 4 4 4 1	Soll Sill	0

3. Charle # of TTS. => 3 929, yo = 000 for Soon 924, yo = 001 for Soul

4. Draw State-assigned table

Present S. 1 92 91 90		State	Output Z
 020100	Y2 Y1 Y0	Y2 Y1 Y0	
000	000	100	0
0 0 1	000	(5)	0
0 (0	001	101	O
011	0-01	(0 1	0
100	010	110	0
(0 1	010	110	1 1
1 (0	0(1	111	0
() (0(1	iii	0

6. Draw FSM cet



5. Derive Comb. cet A. and Comb. cet B

