University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Final Examination

ECE 241F - Digital Systems
December 17, 2012, 2:00 pm – 4:30 pm

Examiners: J. Anderson, K. Truong, B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS, USING THE BACK SIDE IF NECESSARY

1. No calculators or cell phones are allowed.
2. The number of marks available for each question is indicated in the square brackets [].
3. There are two extra blank pages at the end of the test for rough work.

AIDS ALLOWED: Textbook: **Fundamentals of Digital Logic with Verilog Design (**any edition, but no photocopies), and **ONE 8.5" x 11" sheet of paper** with notes of your choosing.

Last Name: _____

First Name: _____

Student Number: _____

Total Available Marks:

Question	1	2	3	4	5	6	7	8	9	10	Total
Marks Available	6	11	10	8	8	8	5	7	5	5	73
Marks Achieved											

[6] Q1.

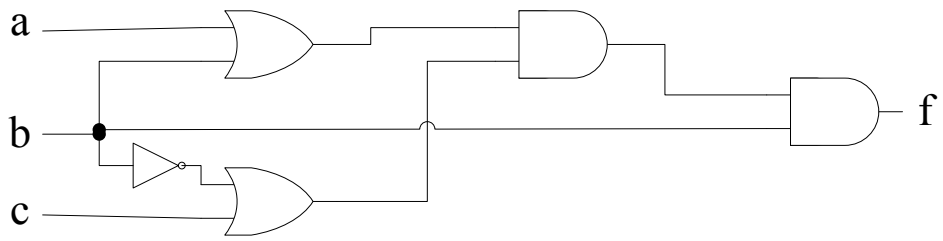
a) Fill in the blanks in the table below: [3]

8-bit 2's complement number	Signed decimal number
	19
11110101	

Specify the range of decimal numbers that can be represented as signed numbers (in 2's complement representation) using a word length of 8 bits.

_____ to _____

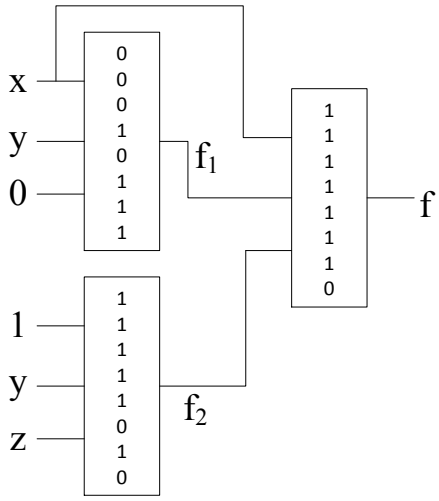
b) For the logic circuit shown below, reduce the circuit to achieve the minimum cost (cost = number of gates + number of inputs). Draw your reduced circuit using the basic logic gates (AND, OR and NOT). [3]



[11] Q2.

a) Implement the logic function, f (a, b, c) = ∑m (2, 4, 6, 7) using only 2-to-1 multiplexer(s) and use as few multiplexers as possible. Minterms are indexed from 0 to 7 (inclusive). As an example, minterm 1 corresponds to $\bar{a}\bar{b}c$. [5]

b) A logic function, f is implemented using three 3-LUTs as shown below. Determine the logic functions f_1, f_2 and f in the minimal sum-of-products (SOP) form in terms of the input variables x, y and z. All 3-LUTs are filled in according to the truth table shown in the box. [4]



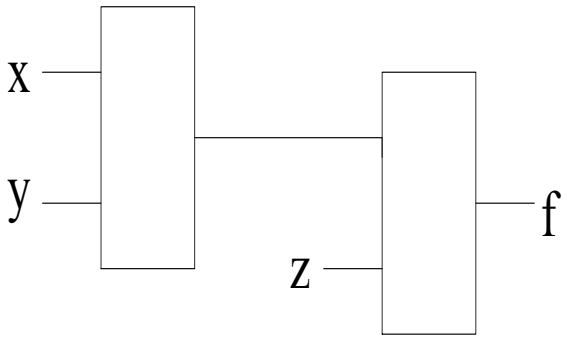
	a	b	c	f
a	0	0	0	
	0	0	1	
	0	1	0	
b	0	1	1	f
	1	0	0	
	1	0	1	
c	1	1	0	
	1	1	1	

$f_1 =$

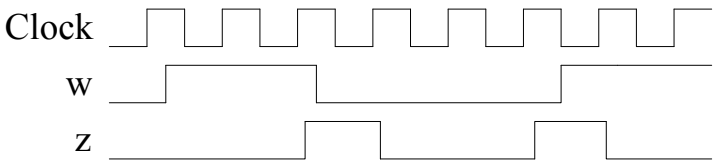
$f_2 =$

$f =$

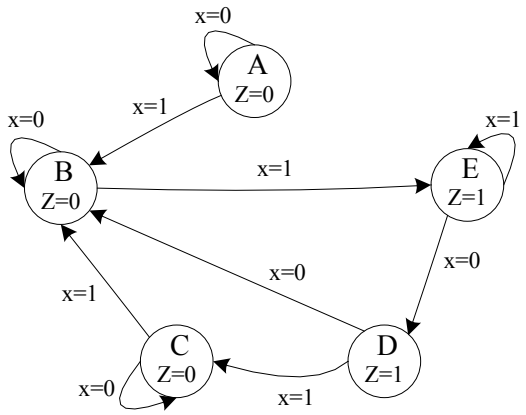
c) Implement the logic function, f from b) using two 2-LUTs given below by filling in the truth tables inside the 2-LUTs. [2]



[10] Q3. Consider a sequential digital system with an input ***w*** and a ***clock***, and the output ***z***. Starting from an initial reset state, this system examines the value of ***w*** in three successive clock cycles, and if an odd number of "0" bits are detected out of these three bits, then the system sets the output ***z*** to 1 (for one clock cycle) in the following clock cycle. Otherwise ***z*** will be 0. The system then resumes checking the next 3-bits of the data stream ***w***. A partial timing diagram is given below as an example. Draw a state diagram for this FSM. Use as few states as possible in your design.



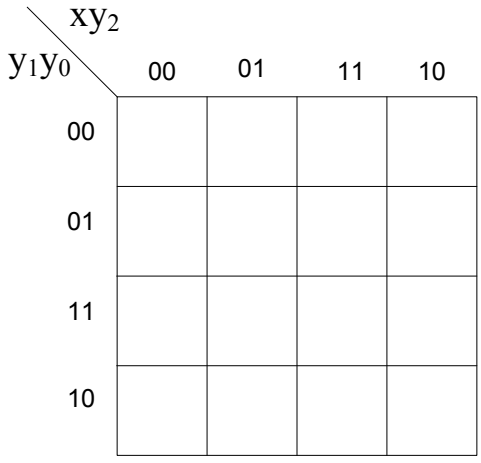
[8] Q4.
Consider the following finite state machine (FSM), with input *x* and output z.

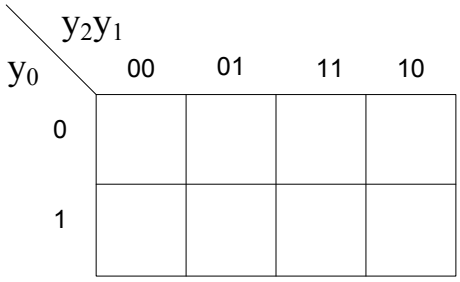


a) Fill in the state-assigned table that corresponds to this FSM. [2]

Current State		**Next State**		**Output, z**
		x = 0	**x = 1**	
Name	**$y_2\ y_1\ y_0$**	**$Y_2\ Y_1\ Y_0$**	**$Y_2\ Y_1\ Y_0$**	
A	**0 0 0**			
B	**0 0 1**			
C	**0 1 0**			
D	**0 1 1**			
E	**1 0 0**			

b) Use the two K-maps below to determine the optimized product-of-sums (POS) expressions for the output logic (z) and the next-state logic for state bit Y_1. [3]





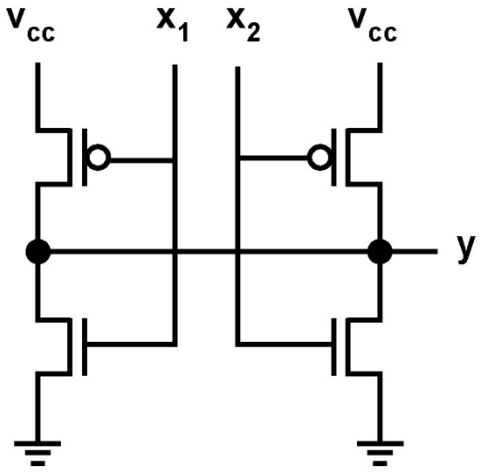
z =

Y_1 =

c) Give the circuit diagram for this FSM that shows all three state flip-flops, but just the next state logic for state bit Y_1 and the output logic (z). [3]

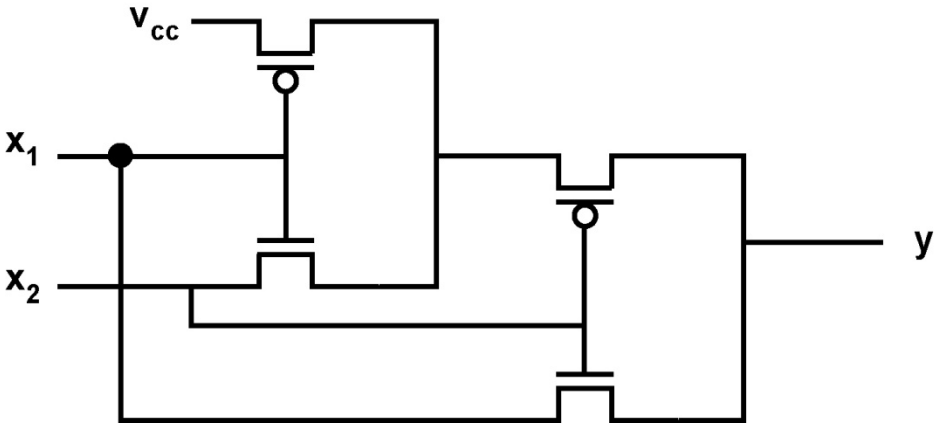
[8] Q5.

a) Does the below transistor-level circuit have any problems? If yes, explain the problem in no more than 1 sentence. Note: V_{cc} is the voltage level representing logic-1. [2]



ANSWER:

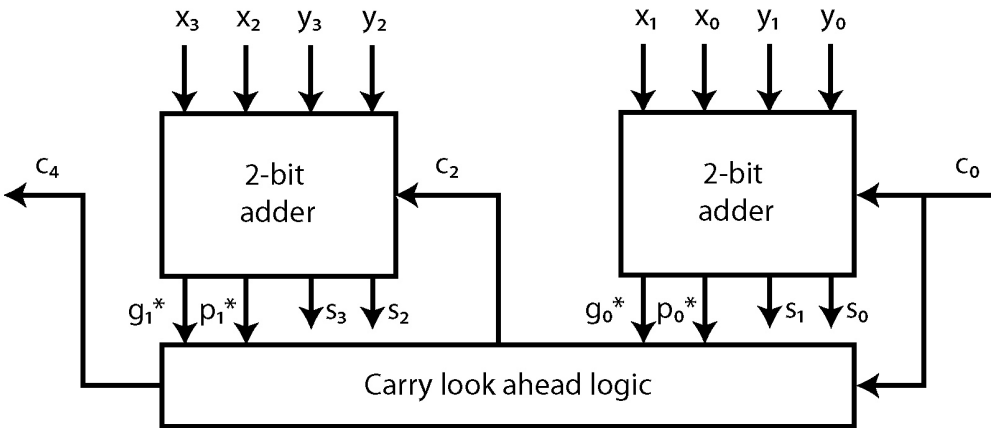
b) Consider the following transistor-level design of a 2-input logic gate. Derive the truth table of the output **y** in terms of the inputs $\mathbf{x_1}$ and $\mathbf{x_2}$. Place your answer in the truth table beside the circuit. Indicate (on the truth table) situations where the output is a "weak" 1/0 (if any). [3]



x_1	x_2	y	Weak (yes/no)?
0	0		
0	1		
1	0		
1	1		

c) Draw the CMOS transistor circuit for the function **f = ab + cd**. [3]

[8] Q6. Consider the following 4-bit adder, which uses a modified version of carry look ahead. It is implemented with 2-bit adders.



a) Derive the minimal SOP expression for g_1^*, g_0^*, p_1^* and p_0^* in terms of the input bits. [4]

b) Derive the minimal SOP expression for c4 and c2 in terms of g_1^*, g_0^*, p_1^*, p_0^* and c_0. [2]

c) Determine the critical path of this adder and the number of gate delays (or levels of gates) in the critical path. [2]

[5] Q7. Consider the following Verilog code.

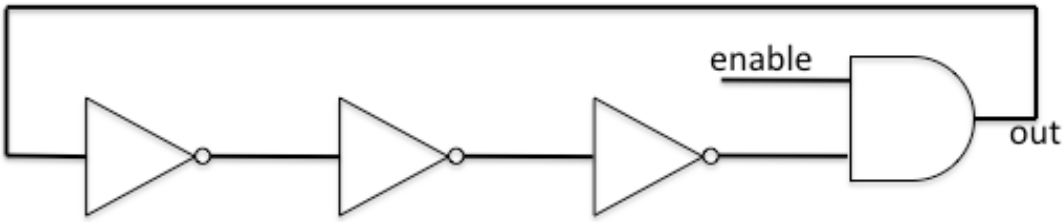
```
module example (clk, resetn, y);
        input clk, resetn;
        output y;
        reg [2:0] y, Y;
        parameter [2:0] A=3'b000, B=3'b001, C=3'b010, D=3'b011,
                        E=3'b100, F=3'b101, G=3'b110, H=3'b111;

        always @ (y)
        begin
                case (y)
                        A: Y<= B;
                        B: Y<= C;
                        C: Y<= D;
                        D: Y<= E;
                        E: Y<= F;
                        F: Y<= G;
                        G: Y<= H;
                        H: Y<= A;
                endcase
        end

        always @ (posedge clk or negedge resetn)
        begin
                if (resetn == 0) y <=A;
                else y <= Y;
        end
endmodule
```

a) Draw the state diagram implemented by the Verilog code. [3]

b) In no more than 1 sentence, what does the Verilog code implement? [2]

[7] Q8.

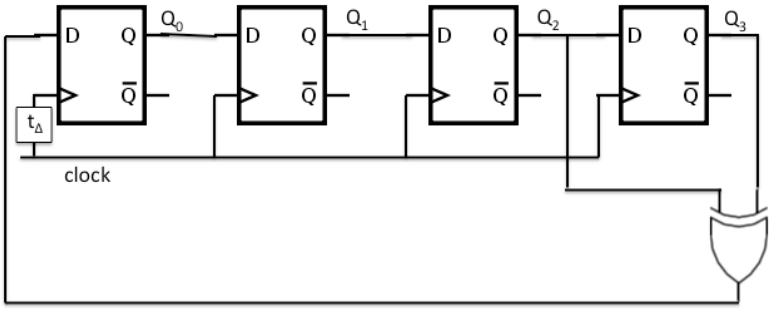
a) Consider the following circuit which is called a ring oscillator:



Assuming that the inverter delay is 0.5ns and the AND gate delay is 1.5ns, explain the behavior of the circuit when enable = 0, and when enable = 1. Explain your reasoning. [2]

Consider the 4-bit linear-feedback shift register (LFSR) below. The delays in the circuit are as follows:

	Min	Max
t_{hold}	0.5ns	
t_{su}	0.8ns	
t_{cq}	1.0ns	1.2ns
t_{xor}	1.0ns	1.2ns



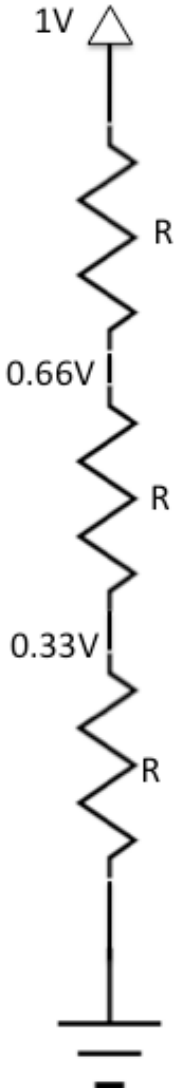
b) Observe that t_Δ is a delay that is added to the arrival time of the clock at the left-most flip-flop. Given that t_Δ is 0ns, what is the minimum clock period at which the circuit will operate? Show your work. [2]

c) With t_Δ as 0ns, are there any hold-time problems with the circuit? Show your work. [1]

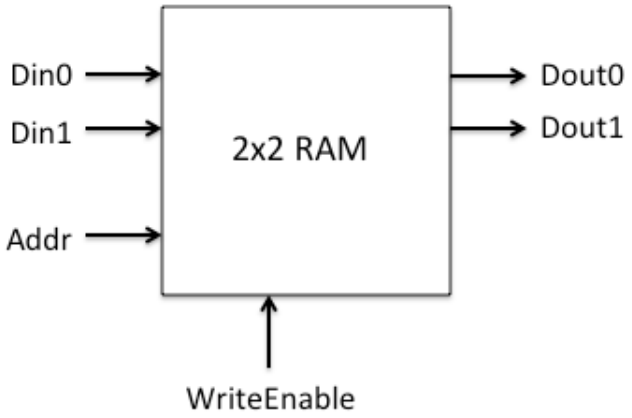
d) Determine a value for t_Δ that minimizes the clock period of the circuit, while ensuring that the circuit continues to operate correctly. State the value of t_Δ and also the new minimum clock period. Show your work. [2]

[5] Q9. Consider the voltage divider circuit below. Extend the circuit below to realize a 2-input, 1-output digital-to-analog converter (DAC). Your DAC's inputs should be labeled x and y; your DAC's output should be labeled z. The required functionality of the DAC is shown below. **Important:** you may only use inverters, AND gates and transmission gates to realize the DAC.

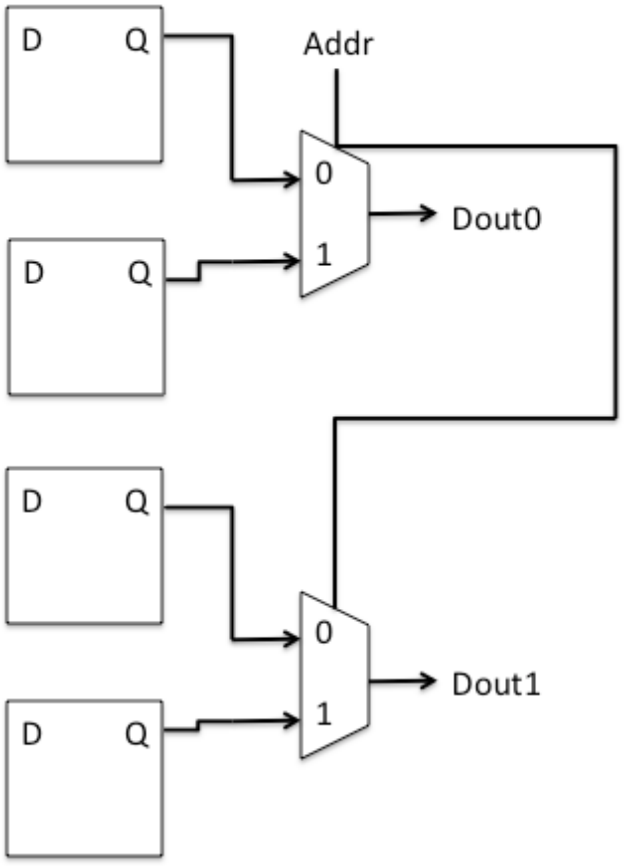
x	y	z
0	0	0V
0	1	0.33V
1	0	0.66V
1	1	1V



[5] Q10. Design a 2x2 RAM using D latches and logic gates. As shown in the figure below, the RAM should have separate input and output data ports. The RAM's write enable input (WriteEnable) input is active-high. A partial schematic (with the RAM's read functionality) is shown below. Complete the schematic by adding logic gates and wires to implement the RAM's write functionality.



COMPLETE THE SCHEMATIC:



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