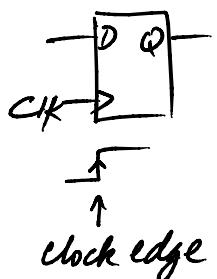


## 5.15 Propagation delay & timing analysis

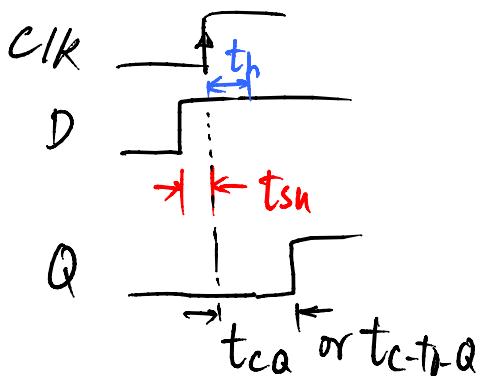


FF timing parameters:  $t_{su}$ ,  $t_h$  and  $t_{co}$

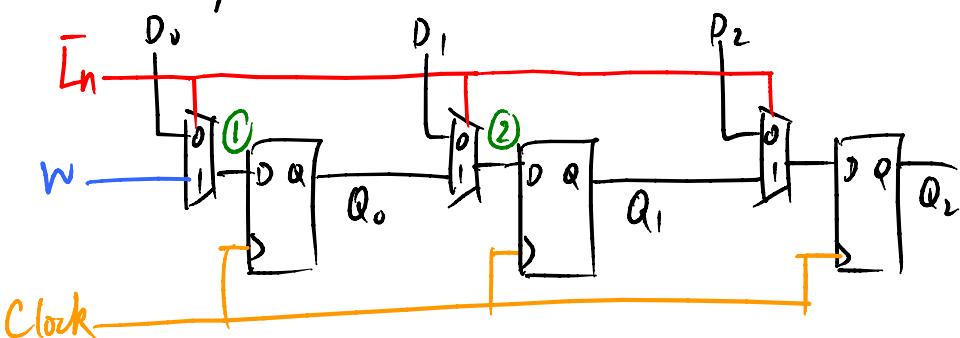
$t_{su}$  = set-up time - the window before the clock edge in which D should not be changed

$t_h$  : hold time - the window after the clock edge in which D should remain unchanged

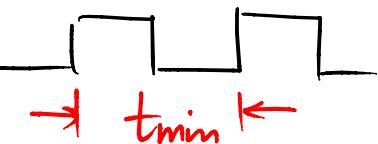
$t_{co}$  = clock-to-Q time - propagation delay for Q to copy D after the clock edge.



Consider a shift register circuit.



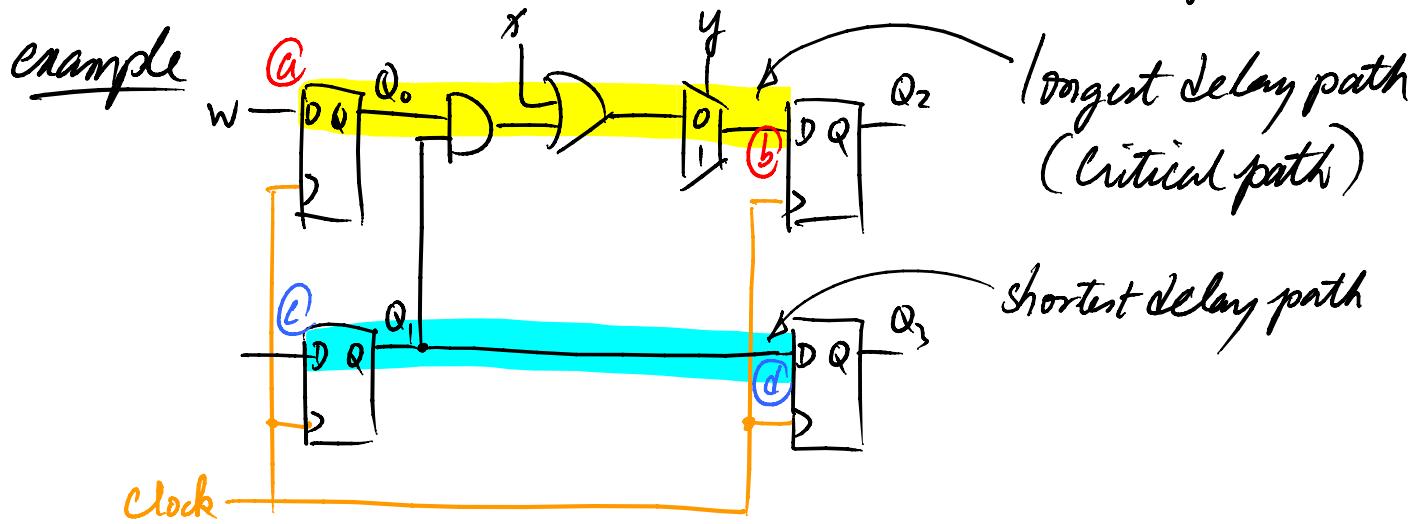
How fast can the Clock be?



How long will it take for a signal at ① to travel to ②?

$$t_{min} = t_{C \rightarrow Q} + t_{max} + t_{su}, \quad \text{the max. clock frequency is } f_{max} = \frac{1}{T_{min}}$$

e.g.  $t_{max} = 2\text{ns}$ ,  $t_{su} = 1\text{ns}$ ,  $t_{cq} = 1.5\text{ns}$ ,  $t_{min} = 4.5\text{ns}$ ,  $f_{max} = 200\text{MHz}$



$\textcircled{a} \rightarrow \textcircled{b}$

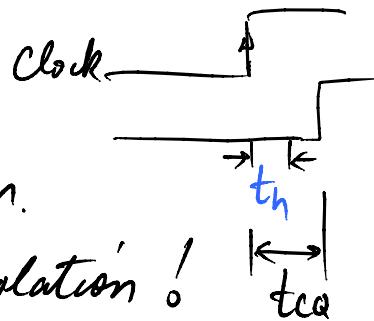
$$t_{min} = t_{cq} + t_{AND} + t_{OR} + t_{max} + t_{su} \Rightarrow f_{max} = \frac{1}{t_{min}}$$

Hold time issue

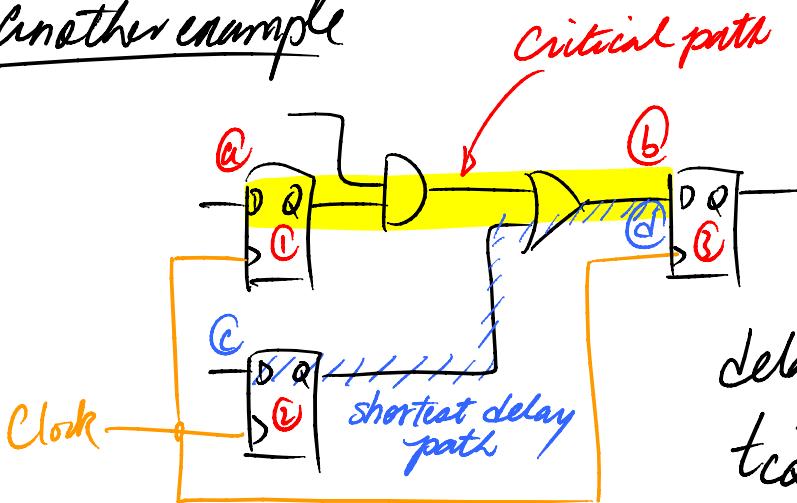
delays from  $\textcircled{c} \rightarrow \textcircled{d}$ :  $t_{cq}$

if  $t_{cq} > t_h$  there will be no problem.

if  $t_{cq} < t_h$  there is a hold time violation!



another example



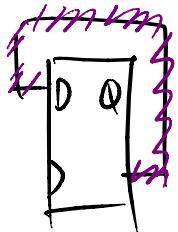
$$t_{min} = t_{cq} + t_{AND} + t_{OR} + t_{su} \quad (\text{max})$$

$$f_{max} = \frac{1}{t_{min}}$$

delay from  $\textcircled{c} \rightarrow \textcircled{d}$ :

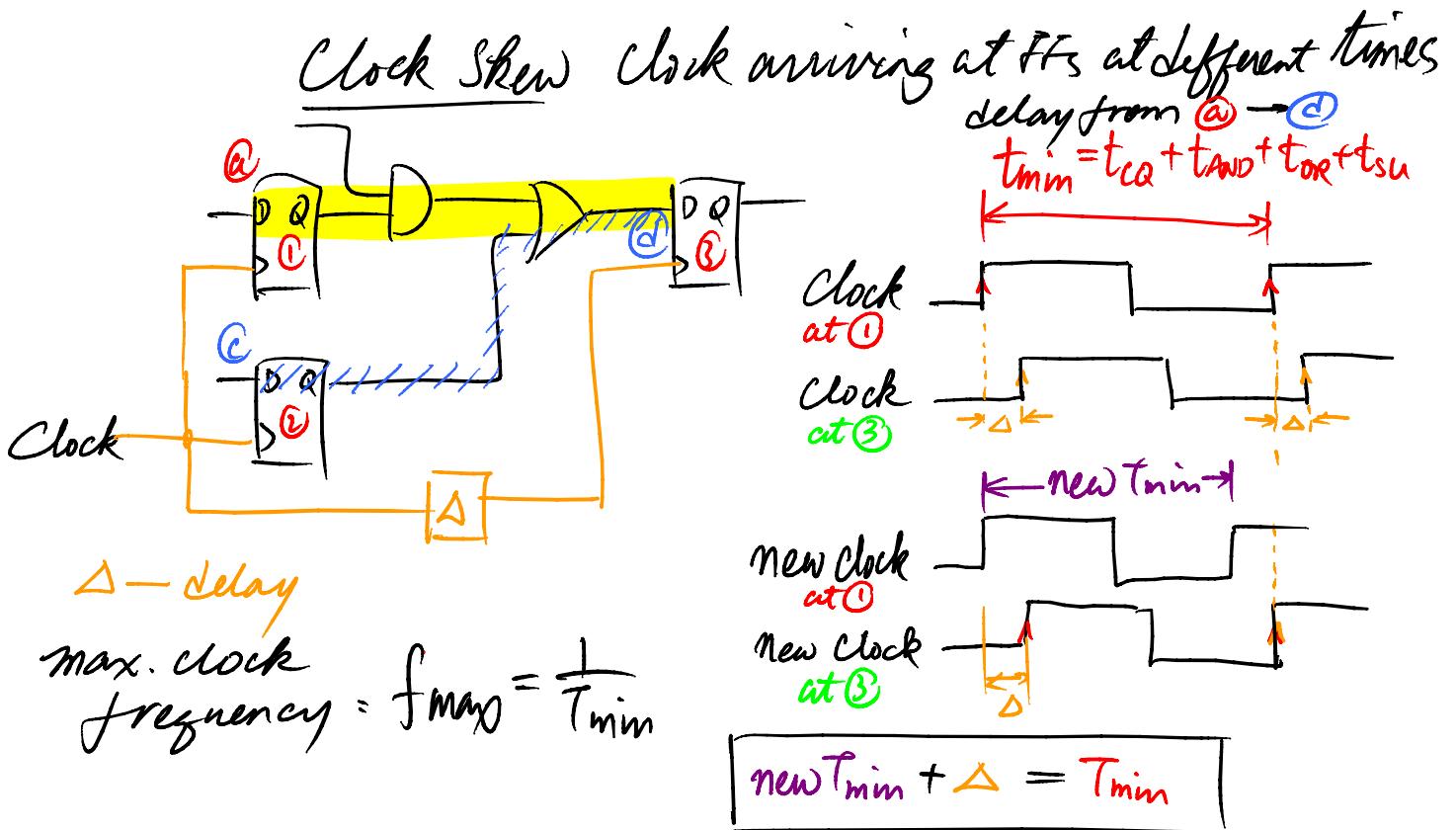
$t_{cq}(\text{min}) + t_{OR}(\text{min})$  if  $> t_h$

no hold time violation

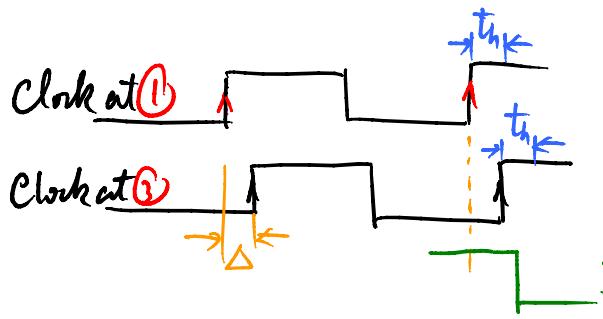


if  $t_{ca} > t_h$  then there is no hold time violation.  
usually it is the case.

If any violation of either  $t_{hn}$  or  $t_h$ , it means that the cct. may not work reliably!



One must check whether there is a hold time violation because of the clock skew ( $\Delta$ ).



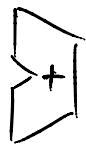
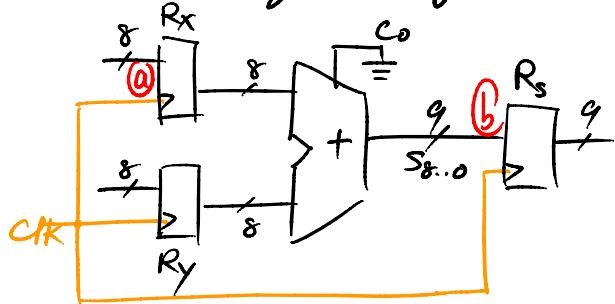
This could happen:

satisfied hold time requirement  
✓ with clock skew

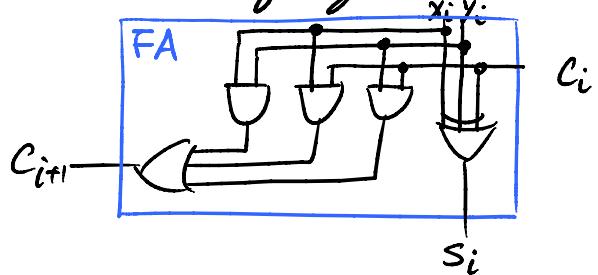
Data ← hold time violation with ( $\Delta$ ) delay

## Timing Analysis Examples

Consider the following circuit



is a 8-bit ripple carry adder  
consists of eight Full Adders



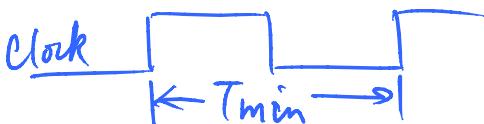
Gate	(max) delay(ns)	(min) delay(ns)
XOR	2	0.5
AND	2	0.5
OR	1	0.5
CtoQ	2	0.5
tsu	2	
t <sub>h</sub>	1.5	

$$C_8 \leftarrow l_0 - l_1 - l_2 - l_3 - l_4$$

a) What is the min. clock period for which this ckt. will function correctly?

$$C_8 \text{ bit} \rightarrow \text{longest delay}, T_{\min} = (t_{\text{AND}}(\text{max}) + t_{\text{XOR}}(\text{max})) \times 8 + t_{\text{CtoQ}}(\text{max}) + t_{\text{tsu}} = 28 \text{ ns}$$

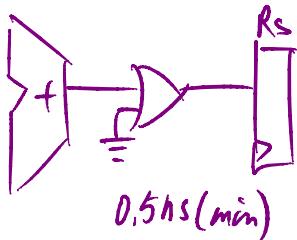
Registers (R<sub>x</sub>, R<sub>y</sub>)



b) Determine if the hold time for all of the FFs in R<sub>s</sub> are met. For those FFs which the hold time is violated, give a change to the ckt. (using only gates in the table above) that corrects the problem. Your correction should increase the minimum clock period in a) as little as possible.

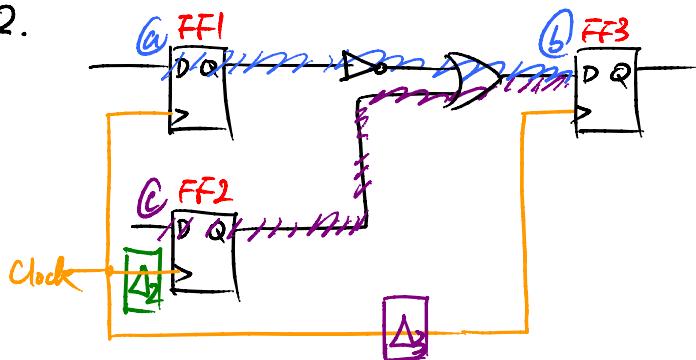
shortest delay path:  $t_{\text{CtoQ}}(\text{min}) + t_{\text{XOR}}(\text{min}) = 0.5 + 0.5 = 1 \text{ ns} < t_h(1.5 \text{ ns})$

Hence hold time violation (for S<sub>i</sub>)



add an OR gate for each bit.

2.

parameters

$$t_{su} = 3 \text{ ns}$$

$$t_h = 2 \text{ ns}$$

$$t_{INV} = 3 \text{ ns (max.) } 1 \text{ ns (min.)}$$

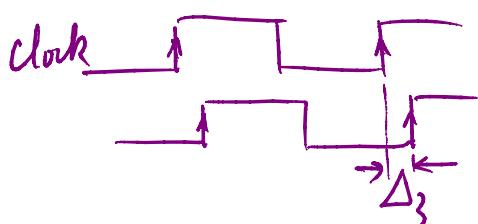
$$t_{DQ} = 5 \text{ ns (max.) } 3 \text{ ns (min.)}$$

$$t_{CQ} = 4 \text{ ns (max.) } 2 \text{ ns (min.)}$$

a) What is the minimum period of the clock?

Critical path:  $T_{min} = t_{CQ(\max)} + t_{NOT(\max)} + t_{DQ(\max)} + t_{su} = 15 \text{ ns}$   
 $\textcircled{a} \rightarrow \textcircled{b}$

b) If it were possible to delay the arrival of the clock to FF3, how much can it be delayed? What can the new minimum period be?



shortest delay path:  $(\textcircled{c} \rightarrow \textcircled{b})$

$$t_{CQ(\min)} + t_{DQ(\min)} = 5 \text{ ns}$$

given  $t_h = 2 \text{ ns}$ , there is  $5 - 2 = 3 \text{ ns}$  room to shorten the clock period.

$$\text{new } T_{min} = T_{min} - 3 \text{ ns} = 15 - 3 = 12 \text{ ns.}$$

c) If it were also possible to delay the clock arrival to FF2 in addition to the clock delay to FF3 (in b), how much can the delay be? What can the new minimum clock period be now?

$\Delta_2 = 1 \text{ ns}$  ( $t_{NOT(\min)} = 1 \text{ ns}$ ) signals from FF2 can be delayed by 1 ns before arriving at  $\textcircled{b}$

now, the shortest path delay is 6 ns instead of 5 ns (as in b)  
 there is 1 ns more room to shorten the clock period with.

$$\text{Hence the newest } T_{min} = 12 \text{ ns} - 1 \text{ ns} = 11 \text{ ns}$$

→ essentially there is  $6 \text{ ns} - t_h(2 \text{ ns}) = 4 \text{ ns}$  room to shorten the original clock period from 15 ns to 11 ns. (the new  $\Delta_3 = 4 \text{ ns}$ )