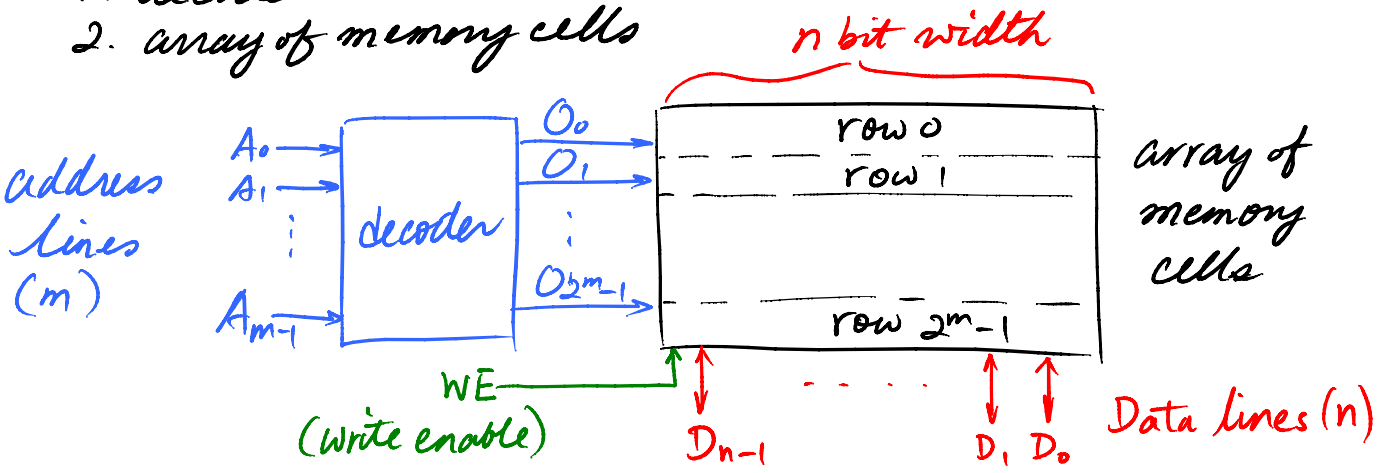
Electronic Memory

— All memory units consists of two parts:

1. decoder
2. array of memory cells



Decoder: a ckt. of inputs (m) and 2^m outputs. which uses one-hot encoding. ex for m=3

A_2 A_1 A_0	O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0 ← output
0 0 0	0 0 0 0 0 0 0 1
0 0 1	0 0 0 0 0 0 1 0
0 1 0	0 0 0 0 0 1 0 0
0 1 1	0 0 0 0 1 0 0 0
1 0 0	0 0 0 1 0 0 0 0
1 0 1	0 0 1 0 0 0 0 0
1 1 0	0 1 0 0 0 0 0 0
1 1 1	1 0 0 0 0 0 0 0

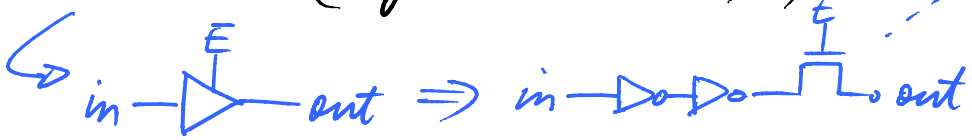
for a typical comp. processor, # of address lines = 32. the total rows addressable is $2^{32} = 4,294,967,296$ (4G)

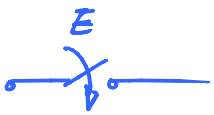
Memory cell array

— based on two basic concepts

① storage cells (feedback loop)

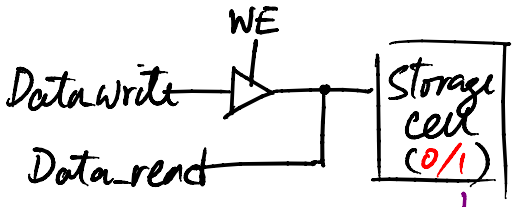
② tri-state (logic values: 0, 1, z)





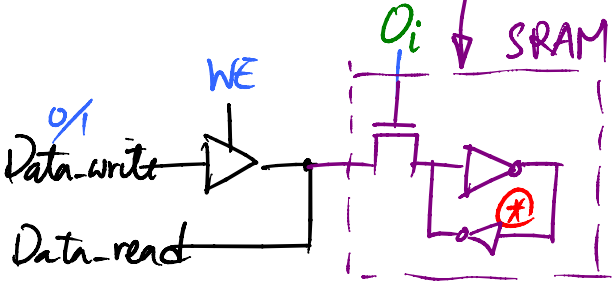
E	in	out
0	X	z (no connection)
1	0	0
1	1	1

tri-state in action



if WE = 1, allows us to store data on Data_write into the storage cell.

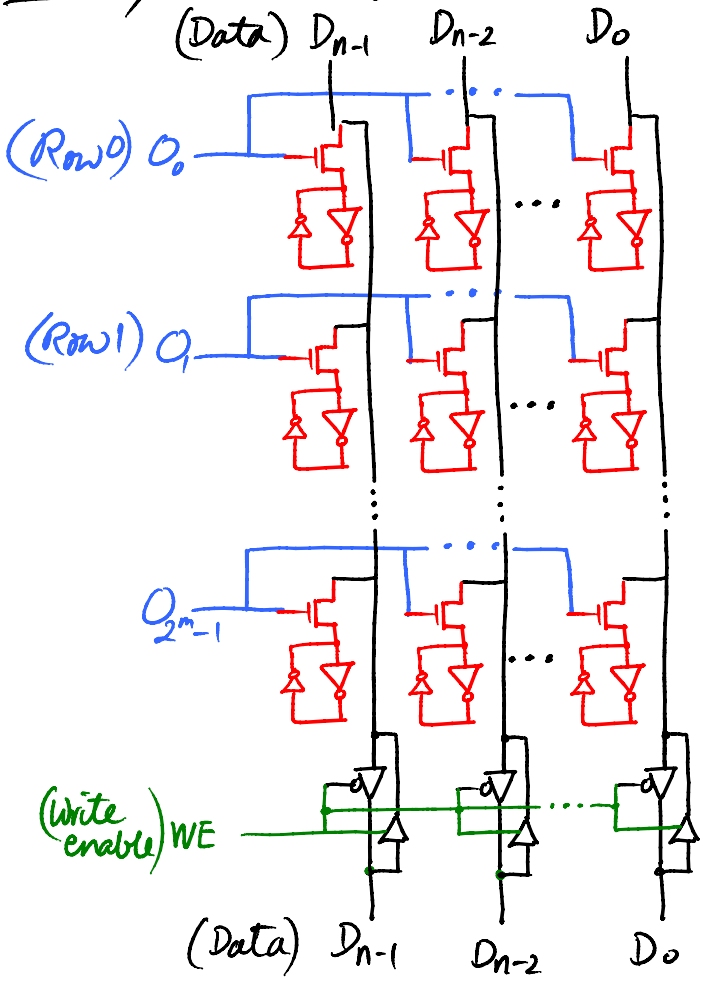
if WE = 0, allows us to read the data from the storage cell through Data_read.



O_i – output of the decoder

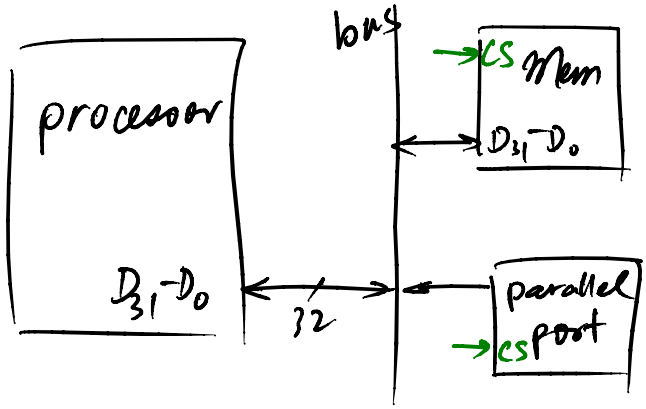
* this "weaker" inverter allows for data to be written into the storage cell (ie allows data to change 1→0 or 0→1)

Array of memory cells



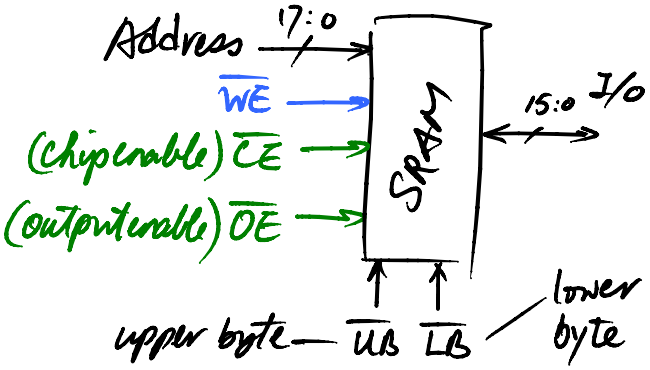
Q: Why would we need the tri-state buffers on the data outputs?

A: In an application, such as a computer, the memory chip is just one of several chips that have to share the data wires (bus)



CS – chip select

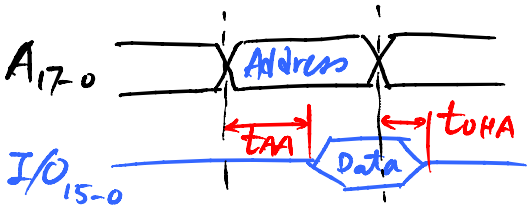
example: memory chip IS61LV25616
A2-10



– To use the chip, we need to obey the timing requirements

To read a row of data

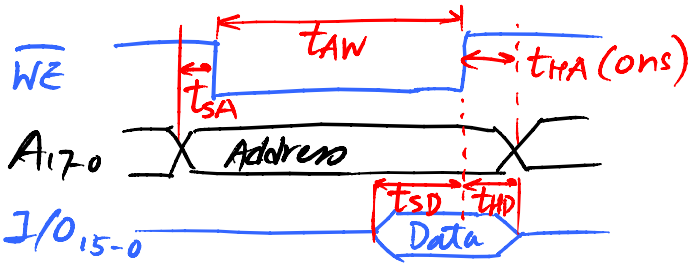
$\overline{CE} = \overline{OE} = 0$, $\overline{WE} = 1$



t_{AA} – address access time (10ns)

t_{OHA} – output hold address

To write a row of data ($\overline{CE} = 0$)



t_{SA} – setup address time (0ns)

t_{AW} – address width time (8ns)

t_{SD} – setup data time (6ns)

t_{HD} – hold data time (0ns)