University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

Midterm Examination

ECE 241F - Digital Systems
Wednesday October 10, 2012, 6:15 – 7:45 pm

Duration: 90 minutes
Examiners: J. Anderson, K. Truong, B. Wang

ANSWER ALL QUESTIONS ON THESE SHEETS,
USING THE BACK SIDE IF NECESSARY

1. No calculators or cell phones are allowed.
2. The number of marks available for each question is indicated in the square brackets [].
3. There are two extra blank pages at the end of the test for rough work.

AIDS ALLOWED: Textbook: **Fundamentals of Digital Logic with Verilog Design (**any edition, but no photocopies), and **a single sheet of 8.5" x 11" paper** with notes of your choosing. No photocopies of the textbook will be permitted.

Last Name: _____

First Name: _____

Student Number: _____

Please Indicate Which Lab Section You Are In

Monday Morning [ ]
Monday Afternoon [ ]
Tuesday Afternoon [ ]
Friday Morning [ ]

Total Available Marks:

Question	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Total
Marks Available	9	8	9	10	8	9	9	5	67
Marks Achieved									

[9] Q1. For this question, use algebraic manipulation to find the minimized SOP or POS expressions. Specify the rules of Boolean algebra used for simplification in each step. Higher marks will be given to solutions using fewer steps.

i) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal SOP form for this function. [2]

$$f = \bar{a}d + ad + b\bar{c}d + \bar{a}b\bar{c}\bar{d} + ab\bar{c}\bar{d}$$

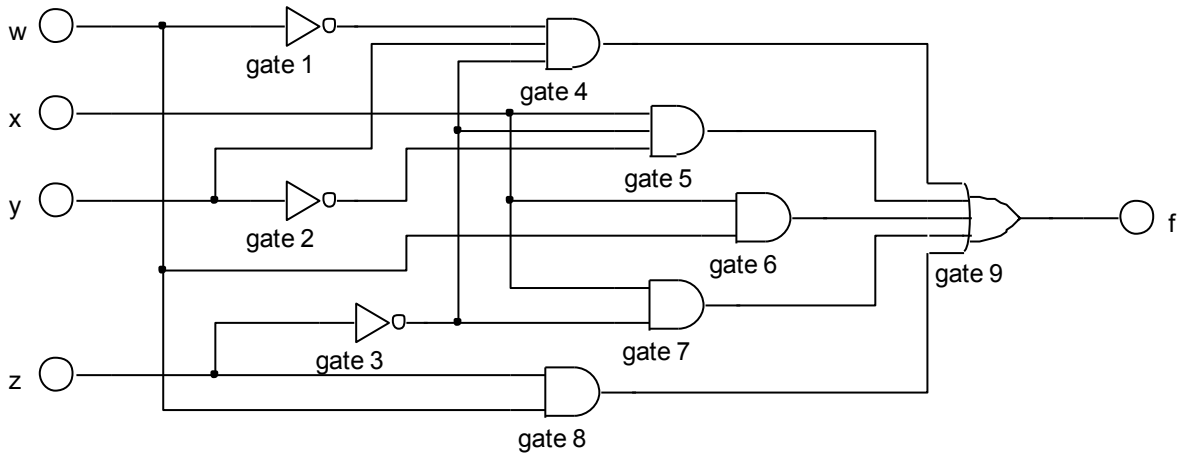
ii) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal SOP form for this function. [3]

$$f = (x + y)(x + z) + (x + w)(x + y)(x + y + z)$$

iii) Use Boolean algebra to minimize the following expression. Your final answer should be the minimal POS form for this function. [4]

$$f = a\bar{c} + d + \bar{a}c$$

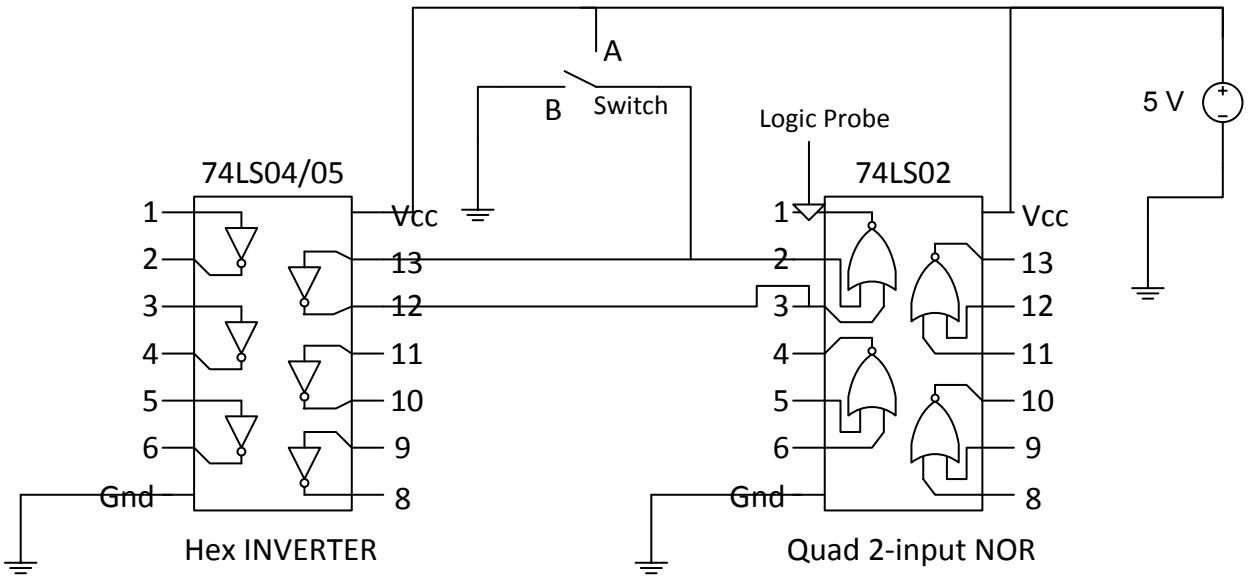
[8] Q2. Using the K-map below, determine which gate(s) can be removed from the following circuit to reduce the cost (total number of gates + total number of inputs) as much as possible. Show your work. *Note: you may not create any new gates, only remove the existing one(s), and you may not remove individual inputs to an AND gate unless the entire AND gate is to be removed.*



wx / yz	00	01	11	10
00				
01				
11				
10				

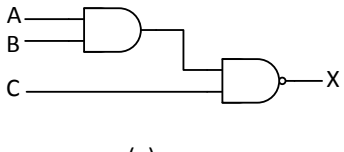
[9] Q3.

i) Diane built the logic circuit shown below, the logic probe is always OFF (0) whether the switch is in position A or B. Is the problem with the inverter or the NOR, or is there no problem? Explain your answer. [4]



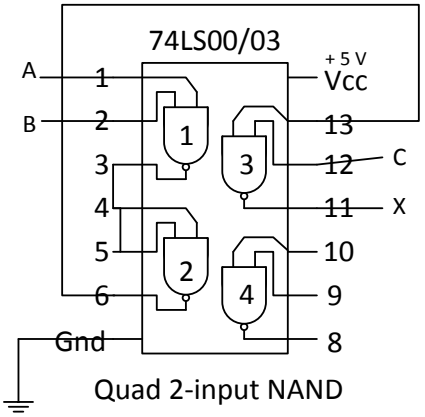
ii) Bobby constructed the same circuit as Diane on his protoboard, the logic probe's light comes ON (1) when the switch is in position B. Further testing with the probe shows that pins 2 and 3 of the NOR IC are both LOW (0). Is anything wrong? If so, where is the fault? [2]

iii) The logic circuit in (a) shown below is implemented by making connections to the 7400 IC chip as shown in (b). The circuit is not working properly. The problem could either be in the IC connections or in the IC itself. The data table in (c) is completed by using a logic probe at each pin. Identify the problem and explain why. [3]



(a)

Test conditions:
A=1, B=1, C=1,
X should equal 0



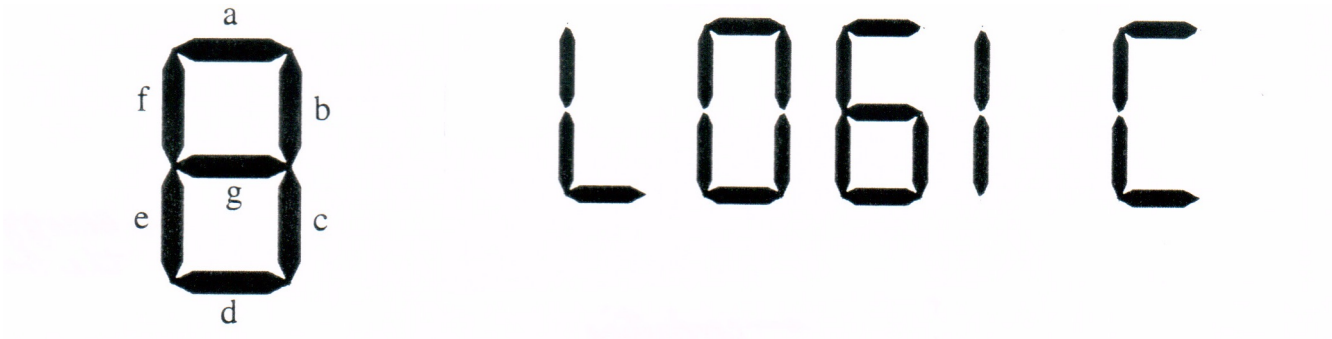
Quad 2-input NAND

(b)

Probe on pin:	Indicator light
1	On
2	On
3	Off
4	Off
5	Off
6	Off
7	Off
8	On
9	Dim
10	Dim
11	On
12	On
13	Off
14	On

(c)

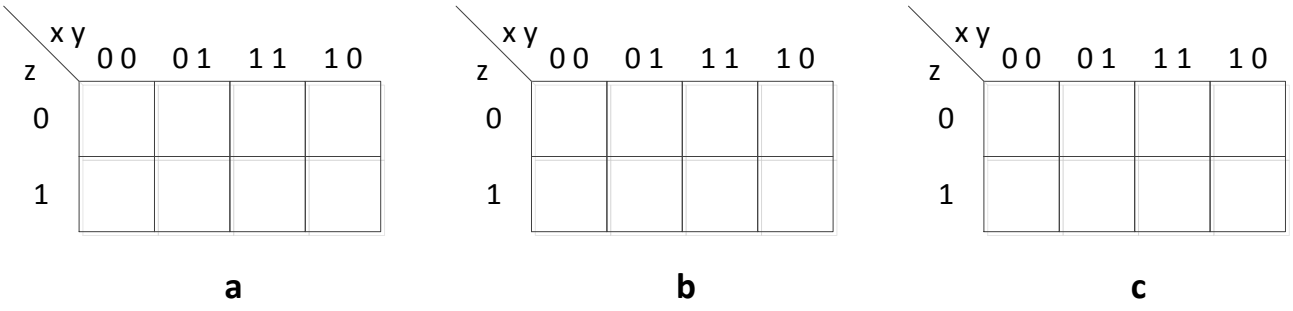
[10] Q4. A 7-segment display has 7 individual segments (a to g) which can be turned "on" or "off" individually to display alphabetic characters. You are asked to display the word LOGIC as follows:



i) Assuming that each letter from the word LOGIC is selected with a 3-bit (xyz) code, complete the truth table below for all segments (a to g). Assume that a segment turns "on" when a logic 1 is asserted. [3]

	x	y	z	a	b	c	d	e	f	g
L	0	0	0							
O	0	0	1							
G	0	1	0							
I	0	1	1							
C	1	0	0							
	1	0	1							
	1	1	0							
	1	1	1							

ii) Fill in the K-maps below for output segments **a**, **b** and **c** only. [1]



iii) Find the SOP expressions for **a**, **b** and **c** in order to achieve minimum total cost (consider sharing gates). [4]

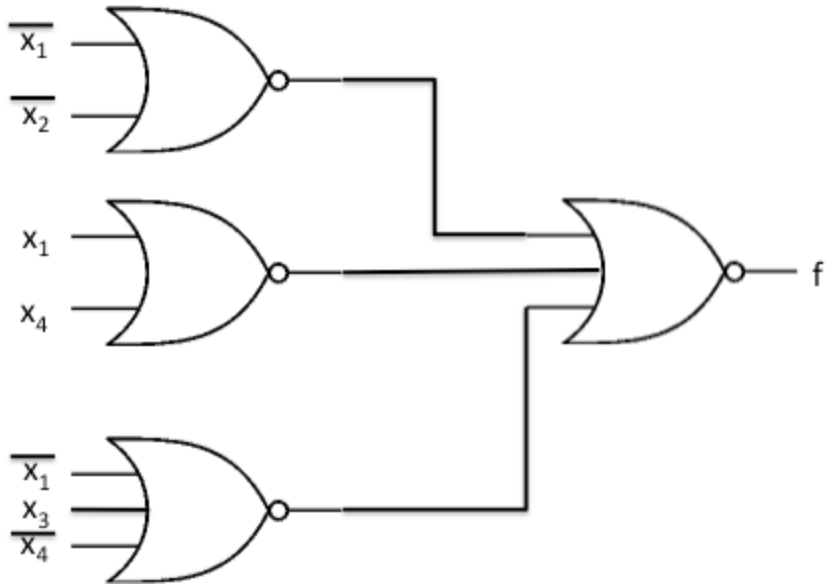
a =

b =

c =

iv) Draw a multi-output logic circuit implementation that produces the outputs **a**, **b** and **c** using only AND, OR, and NOT gates. Your circuit should implement the functions determined in step iii) [2]

[8] Q5. Consider the following logic circuit:

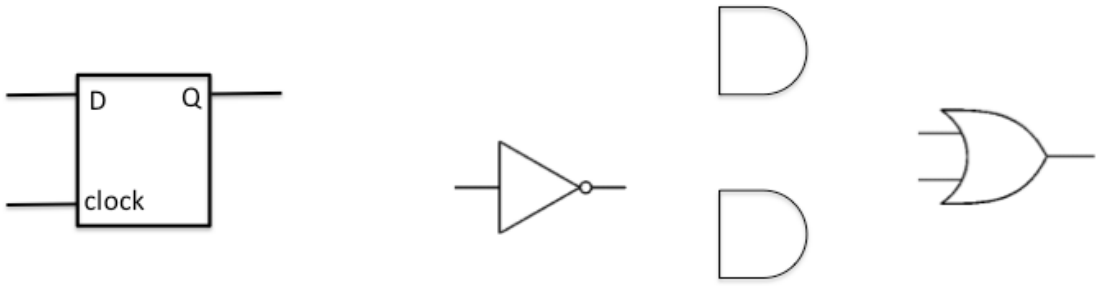


i) Write the logic function for *f* in product-of-sums (POS) form: [2]

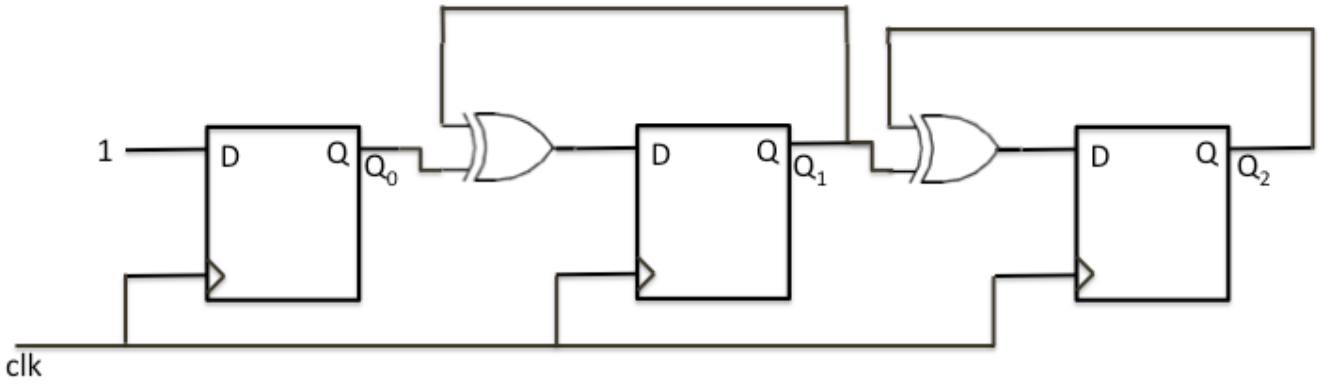
ii) Draw a logic function for *f* using a minimum number of NAND gates. You may only use NAND gates, and your NAND gates may have either 2 or 3 inputs. In your circuit, you may assume that the circuit input signals (x_1, x_2, x_3 and x_4) are freely available in both true and complemented form. [6]

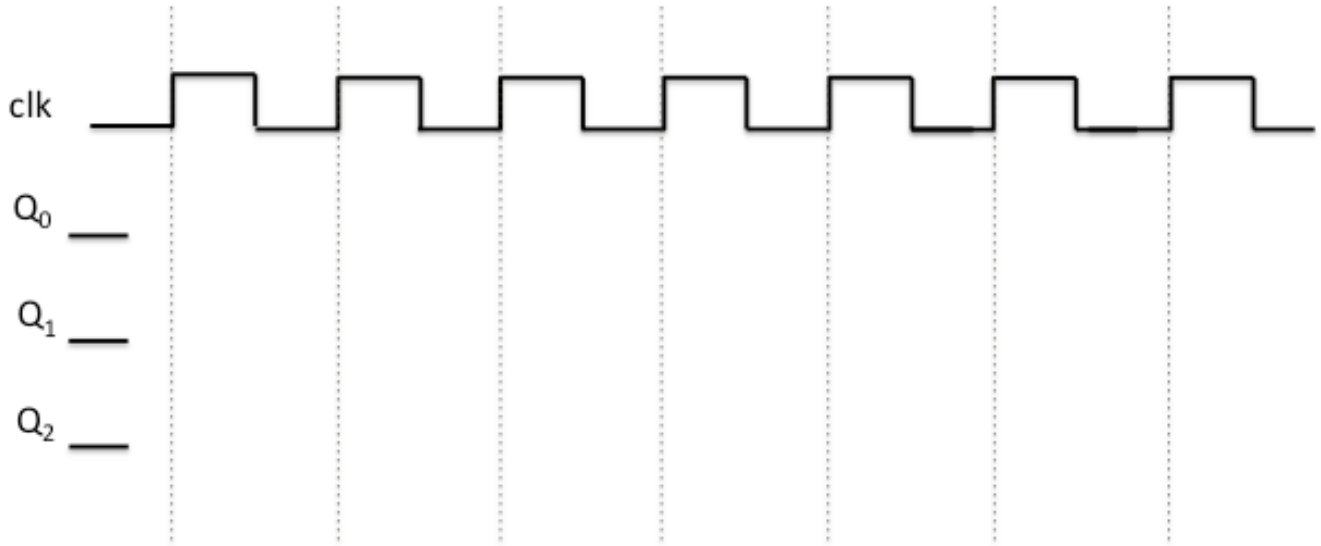
[9] Q6. The left-side of the figure below shows the circuit symbol for a gated D latch (i.e. a transparent latch). A gated D latch can be implemented with the gates shown on the right-side of the figure.

i) Implement a gated D latch using *only* the logic gates provided. You only need to add connections between the gates and label the input and output signals. Your circuit does not need to generate the complemented form of Q. [4]



ii) Complete the timing diagram (see next page) for the circuit below. The flip-flops are positive edge-triggered. You may assume delays are zero. You may further assume that Q_0, Q_1 and Q_2 are all initially logic-0. [4]





iii) Given that $Q_2Q_1Q_0$ represents a 3-bit binary number, what does the above circuit do? [1]

[9] Q7. Consider a circuit with three single-bit inputs S_2, S_1, S_0, and three single-bit outputs Z_2, Z_1, Z_0. The three inputs represent a 3-bit number in binary (S_2 is the most-significant bit), and likewise, the three outputs represent a 3-bit number in binary (Z_2 is the most-significant bit). Design a circuit where, if the binary value of the input is 0, 1, 2 or 3, then the binary value of the output should be one *greater* than the input. If the binary value of the input is 4, 5, 6, or 7, then the binary value of the output should be one *less* than the input.

i) Draw the truth table for your 3-input, 3-output circuit. [3]

ii) Use K-maps to derive minimized logic expressions for the three outputs. [3]

iii) Write procedural Verilog code for the 3-input, 3-output circuit. Your Verilog code must use an *always* block. [3]

[5] Q8.

i) Using a minimum number of 2-to-1 multiplexors, implement a 2-input OR gate. [2]

Solution:

ii) Using a minimum number of 2-to-1 multiplexors, implement a 3-input AND gate. [3]

Solution:

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