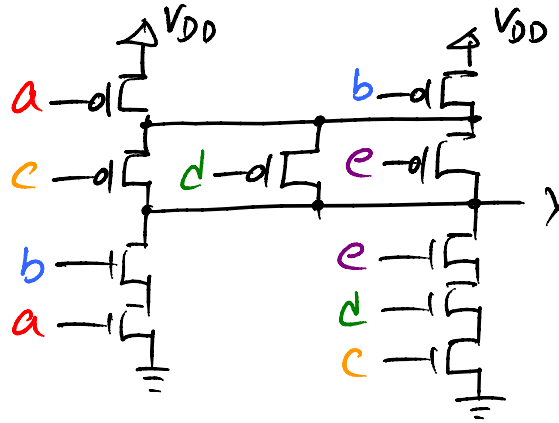
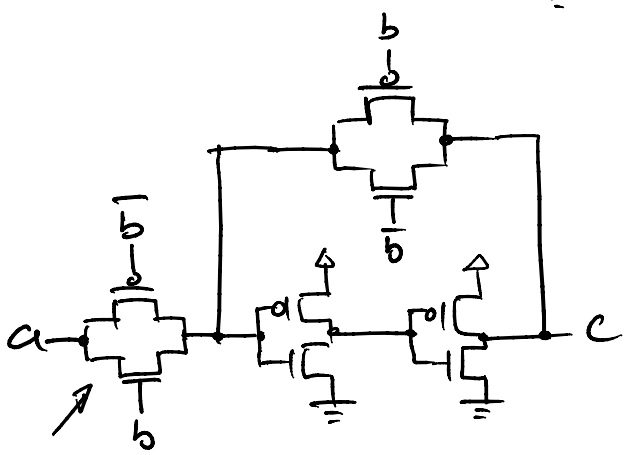
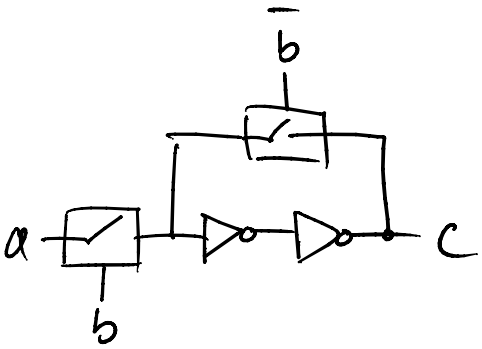
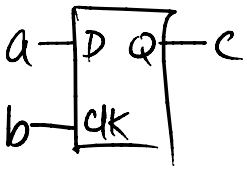
⟹ some interesting CMOS circuits



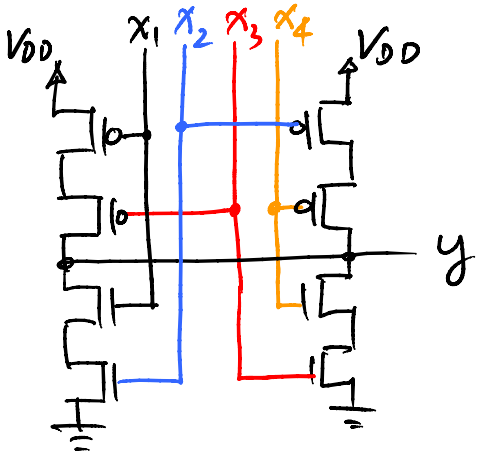
$$Y = \overline{ab + cde}$$







D-latch !



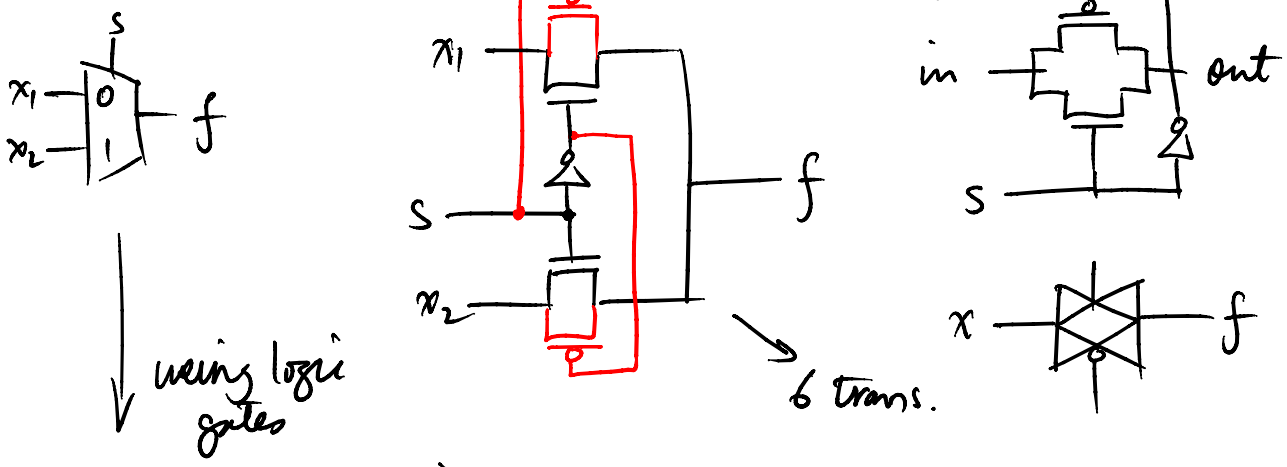
x_1	x_2	x_3	x_4	y	
0	0	0	0	1	
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	0	
0	1	0	0	1	
0	1	0	1	1	
0	1	1	0	z	← high impedance (open ckt.)
0	1	1	1	0	
1	0	0	0	1	
1	0	0	1	z	← (no pull up/pull down path)
1	0	1	0	1	
1	0	1	1	0	
1	1	0	0	0	
1	1	0	1	0	
1	1	1	0	0	
1	1	1	1	0	

① since PUN & PDN are not in dual relationship, there will not be only "0" or "1" output.

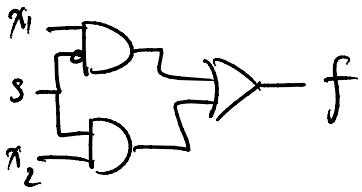
② pull down ($y=0$) if $x_1 \cdot x_2 + x_3 x_4$

③ pull up ($y=1$) if $\bar{x}_1 \cdot \bar{x}_3 + \bar{x}_2 \bar{x}_4$

Transmission Gate

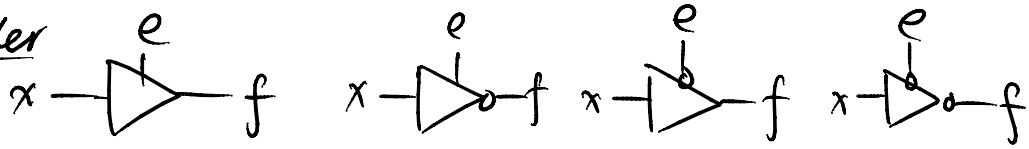


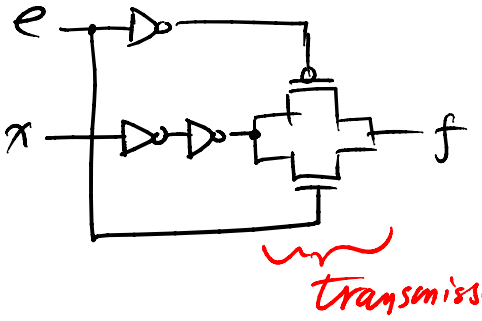
using logic gates



inv → 2 trans.
⇉ → 6 trans
x 2 → 6 trans
⇉ → 6 trans
} 20 trans.

Tri-state buffer

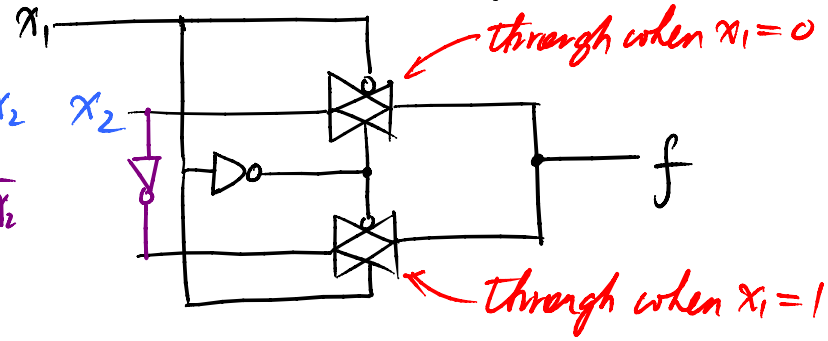




buffer usually has large transistors inside

→ Make an XOR gate out of transmission gates

x_1	x_2	f	
0	0	0	$f = x_2$
0	1	1	
1	0	1	$f = \bar{x}_2$
1	1	0	



→ implement logic function using transmission gates.

$$f = \overline{xyz + \bar{z}(x+y)} = \overline{xyz}\,\overline{\left(\bar{z}(x+y)\right)} = \begin{cases} \overline{xy} & \text{if } z=1 \\ \overline{x+y} & \text{if } z=0 \end{cases}$$