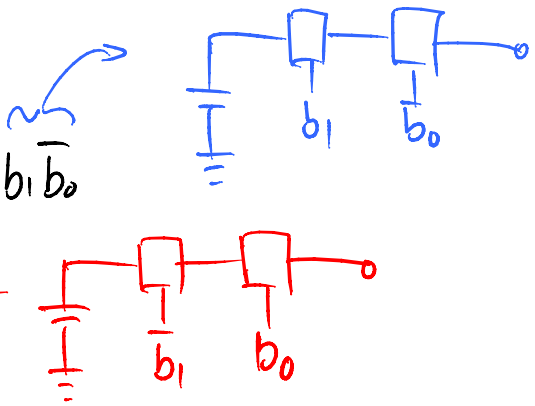
2.4 Logic gates + Logic circuits

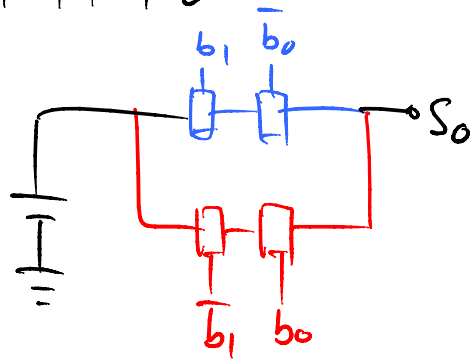
adding 2 bits

$$\begin{array}{r} b_1 \\ + \; b_0 \\ \hline s_1 \; s_0 \end{array}$$

b_1 b_0	s_1 s_0
0 0	0 0
0 1	0 1
1 0	0 1
1 1	1 0

$$s_0 = \bar{b}_1 b_0 + b_1 \bar{b}_0$$



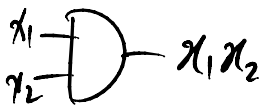


"OR" → parallel connection

"AND" → series connection

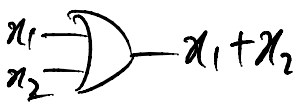
representing logic functions using logic gates:

AND



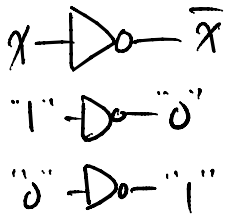
x_1 x_2	AND
0 0	0
0 1	0
1 0	0
1 1	1

OR

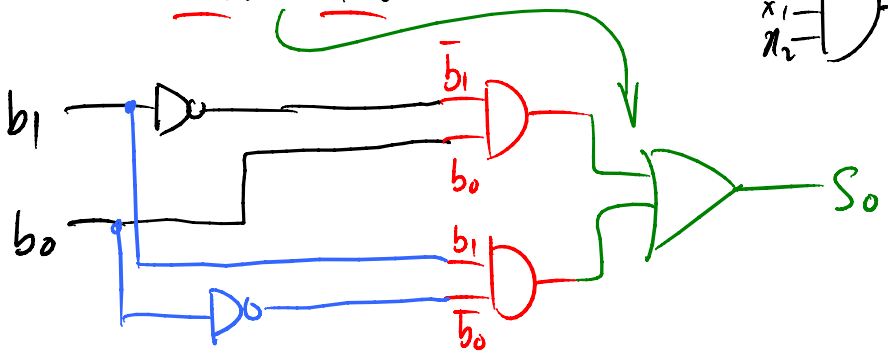


x_1 x_2	OR
0 0	0
0 1	1
1 0	1
1 1	1

NOT



$$s_0 = \bar{b}_1 b_0 + b_1 \bar{b}_0$$



3-variable AND

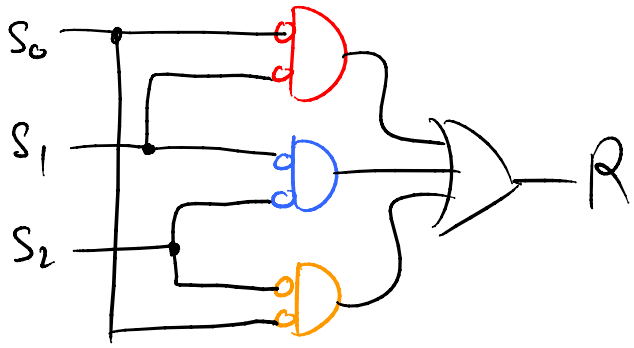
x_0 x_1 x_2	f
0 0 0	0
0 0 1	0
0 1 0	0
0 1 1	0
1 0 0	0
1 0 1	0
1 1 0	0
1 1 1	1

Design example a factory making ball bearings (BB). The three sensors (S_0, S_1, S_2) = S_0 = gives "0" if a BB is too small
S_1 = " " too rough
S_2 = " " Too light

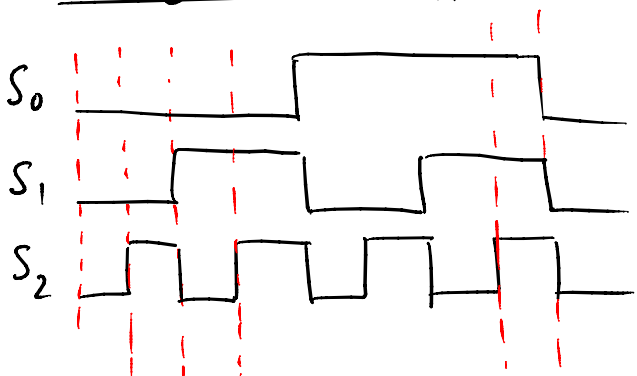
Rejection (R) gives "1" iff at least two sensors give "0"

S_0	S_1	S_2	R
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$$R = \bar{S}_0\bar{S}_1\bar{S}_2 + \bar{S}_0\bar{S}_1S_2 + \bar{S}_0S_1\bar{S}_2 + S_0\bar{S}_1\bar{S}_2$$
$$= \bar{S}_0\bar{S}_1 + \bar{S}_1\bar{S}_2 + \bar{S}_0\bar{S}_2$$



Timing Diagram



$S_0S_1S_2$ 000 001 010 011 100 101 110 111 000

→ Repeats