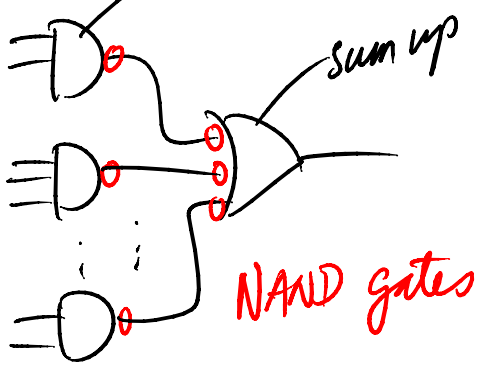
2.7 NAND and NOR networks

⇒Recall demorgan's rule $\overline{xy} = \bar{x} + \bar{y}$ $\qquad \overline{x+y} = \bar{x} \cdot \bar{y}$

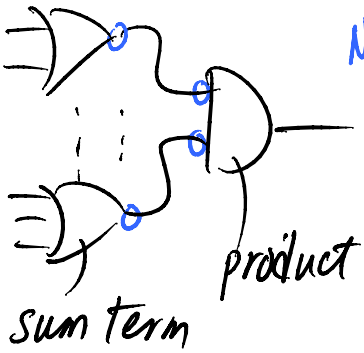
NAND gate

NOR gate

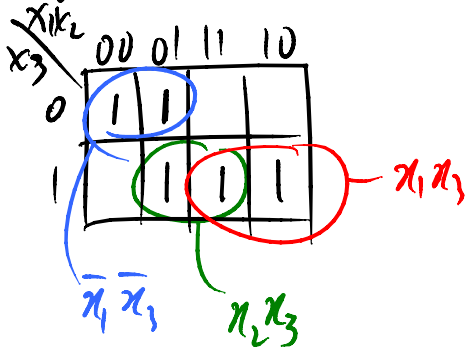
SOP form product term

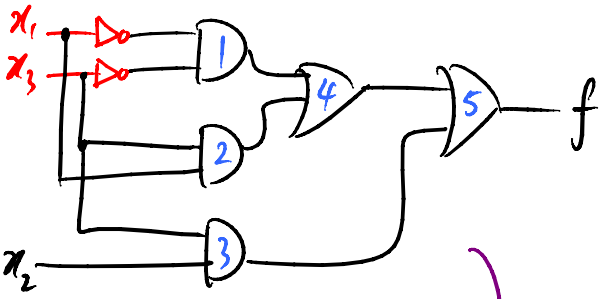


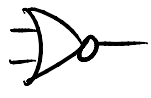
POS form ( )( )

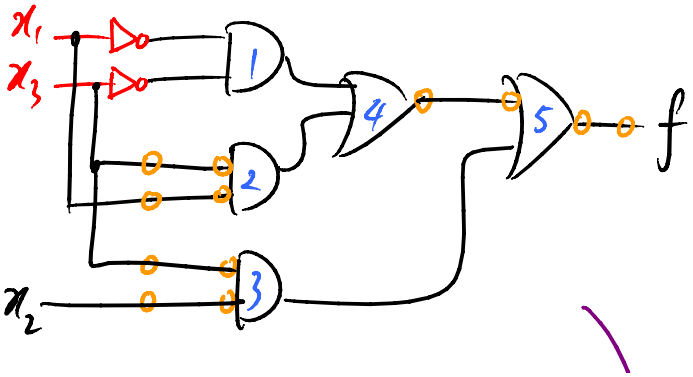


example draw cct. diagram using only 2-input NOR gates for $f = \bar{x}_1 x_2 + x_1 x_3 + \bar{x}_1 \bar{x}_3$ (use as few gates as possible)





make each gate looking like either  or 

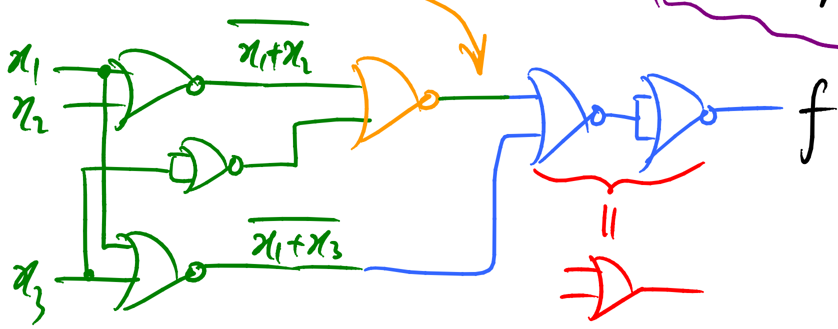


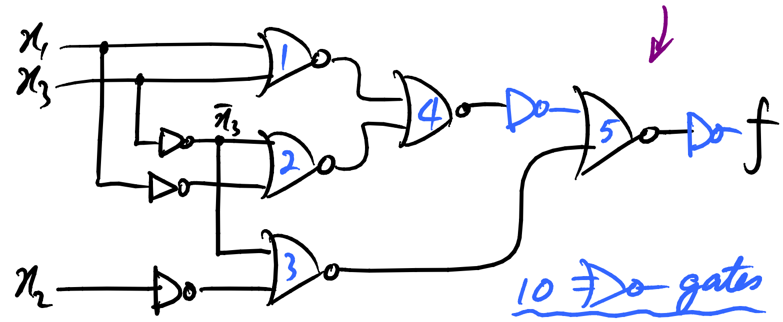
alternative

$$f = x_1 x_3 + x_2 x_3 + \bar{x}_1 \bar{x}_3$$

$$= \overline{\overline{(x_1 + x_2) x_3}} + \bar{x}_1 \bar{x}_3$$

$$= \overline{\overline{x_1 + x_2} + \bar{x}_3} + \overline{x_1 + x_3}$$





10 NOR gates

inverter ( ) can also be implemented using

or

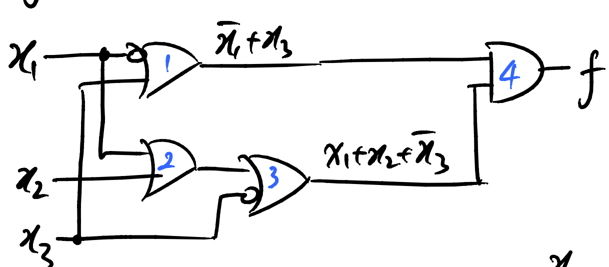
POS form

x_3 \ x_1x_2	00	01	11	10
0			0	0
1	0			

$(\bar{x}_1 + x_3)$

$(x_1 + x_2 + \bar{x}_3)$

$$f = (\bar{x}_1 + x_3)(x_1 + x_2 + \bar{x}_3)$$



Total # of NOR is 7