

CONTENTS

Chapter 1

INTRODUCTION 1

- 1.1 Digital Hardware 2
 - 1.1.1 Standard Chips 4
 - 1.1.2 Programmable Logic Devices 5
 - 1.1.3 Custom-Designed Chips 5
- 1.2 The Design Process 6
- 1.3 Structure of a Computer 8
- 1.4 Logic Circuit Design in This Book 8
- 1.5 Digital Representation of Information 11
 - 1.5.1 Binary Numbers 12
 - 1.5.2 Conversion between Decimal and Binary Systems 13
 - 1.5.3 ASCII Character Code 14
 - 1.5.4 Digital and Analog Information 16
- 1.6 Theory and Practice 16
 - Problems 18
 - References 19

Chapter 2

INTRODUCTION TO LOGIC CIRCUITS 21

- 2.1 Variables and Functions 22
- 2.2 Inversion 25
- 2.3 Truth Tables 26
- 2.4 Logic Gates and Networks 27
 - 2.4.1 Analysis of a Logic Network 29
- 2.5 Boolean Algebra 33
 - 2.5.1 The Venn Diagram 37
 - 2.5.2 Notation and Terminology 42
 - 2.5.3 Precedence of Operations 43
- 2.6 Synthesis Using AND, OR, and NOT Gates 43
 - 2.6.1 Sum-of-Products and Product-of-Sums Forms 48
- 2.7 NAND and NOR Logic Networks 54
- 2.8 Design Examples 59
 - 2.8.1 Three-Way Light Control 59

- 2.8.2 Multiplexer Circuit 60

- 2.8.3 Number Display 63

- 2.9 Introduction to CAD Tools 64

- 2.9.1 Design Entry 64

- 2.9.2 Logic Synthesis 66

- 2.9.3 Functional Simulation 67

- 2.9.4 Physical Design 67

- 2.9.5 Timing Simulation 67

- 2.9.6 Circuit Implementation 68

- 2.9.7 Complete Design Flow 68

- 2.10 Introduction to Verilog 68

- 2.10.1 Structural Specification of Logic Circuits 70

- 2.10.2 Behavioral Specification of Logic Circuits 72

- 2.10.3 Hierarchical Verilog Code 76

- 2.10.4 How *NOT* to Write Verilog Code 78

- 2.11 Minimization and Karnaugh Maps 78

- 2.12 Strategy for Minimization 87

- 2.12.1 Terminology 87

- 2.12.2 Minimization Procedure 89

- 2.13 Minimization of Product-of-Sums Forms 91

- 2.14 Incompletely Specified Functions 94

- 2.15 Multiple-Output Circuits 96

- 2.16 Concluding Remarks 101

- 2.17 Examples of Solved Problems 101

- Problems 111

- References 120

Chapter 3

NUMBER REPRESENTATION AND ARITHMETIC CIRCUITS 121

- 3.1 Positional Number Representation 122

- 3.1.1 Unsigned Integers 122

- 3.1.2 Octal and Hexadecimal Representations 123

- 3.2 Addition of Unsigned Numbers 125

- 3.2.1 Decomposed Full-Adder 129

- 3.2.2 Ripple-Carry Adder 129

- 3.2.3 Design Example 130

3.3	Signed Numbers	132
3.3.1	Negative Numbers	133
3.3.2	Addition and Subtraction	135
3.3.3	Adder and Subtractor Unit	138
3.3.4	Radix-Complement Schemes*	139
3.3.5	Arithmetic Overflow	143
3.3.6	Performance Issues	145
3.4	Fast Adders	145
3.4.1	Carry-Lookahead Adder	146
3.5	Design of Arithmetic Circuits Using CAD Tools	151
3.5.1	Design of Arithmetic Circuits Using Schematic Capture	151
3.5.2	Design of Arithmetic Circuits Using Verilog	152
3.5.3	Using Vectored Signals	155
3.5.4	Using a Generic Specification	156
3.5.5	Nets and Variables in Verilog	158
3.5.6	Arithmetic Assignment Statements	159
3.5.7	Module Hierarchy in Verilog Code	163
3.5.8	Representation of Numbers in Verilog Code	166
3.6	Multiplication	167
3.6.1	Array Multiplier for Unsigned Numbers	167
3.6.2	Multiplication of Signed Numbers	169
3.7	Other Number Representations	170
3.7.1	Fixed-Point Numbers	170
3.7.2	Floating-Point Numbers	172
3.7.3	Binary-Coded-Decimal Representation	174
3.8	Examples of Solved Problems	178
	Problems	184
	References	188

Chapter 4

COMBINATIONAL-CIRCUIT BUILDING BLOCKS 189

4.1	Multiplexers	190
4.1.1	Synthesis of Logic Functions Using Multiplexers	193
4.1.2	Multiplexer Synthesis Using Shannon's Expansion	196
4.2	Decoders	201
4.2.1	Demultiplexers	203

4.3	Encoders	205
4.3.1	Binary Encoders	205
4.3.2	Priority Encoders	205
4.4	Code Converters	208
4.5	Arithmetic Comparison Circuits	208
4.6	Verilog for Combinational Circuits	210
4.6.1	The Conditional Operator	210
4.6.2	The If-Else Statement	212
4.6.3	The Case Statement	215
4.6.4	The For Loop	221
4.6.5	Verilog Operators	223
4.6.6	The Generate Construct	228
4.6.7	Tasks and Functions	229
4.7	Concluding Remarks	232
4.8	Examples of Solved Problems	233
	Problems	243
	References	246

Chapter 5

FLIP-FLOPS, REGISTERS, AND COUNTERS 247

5.1	Basic Latch	249
5.2	Gated SR Latch	251
5.2.1	Gated SR Latch with NAND Gates	253
5.3	Gated D Latch	253
5.3.1	Effects of Propagation Delays	255
5.4	Edge-Triggered D Flip-Flops	256
5.4.1	Master-Slave D Flip-Flop	256
5.4.2	Other Types of Edge-Triggered D Flip-Flops	258
5.4.3	D Flip-Flops with Clear and Preset	260
5.4.4	Flip-Flop Timing Parameters	263
5.5	T Flip-Flop	263
5.6	JK Flip-Flop	264
5.7	Summary of Terminology	266
5.8	Registers	267
5.8.1	Shift Register	267
5.8.2	Parallel-Access Shift Register	267
5.9	Counters	269
5.9.1	Asynchronous Counters	269
5.9.2	Synchronous Counters	272
5.9.3	Counters with Parallel Load	276
5.10	Reset Synchronization	278
5.11	Other Types of Counters	280
5.11.1	BCD Counter	280
5.11.2	Ring Counter	280

5.11.3	Johnson Counter	283
5.11.4	Remarks on Counter Design	283
5.12	Using Storage Elements with CAD Tools	284
5.12.1	Including Storage Elements in Schematics	284
5.12.2	Using Verilog Constructs for Storage Elements	285
5.12.3	Blocking and Non-Blocking Assignments	288
5.12.4	Non-Blocking Assignments for Combinational Circuits	293
5.12.5	Flip-Flops with Clear Capability	293
5.13	Using Verilog Constructs for Registers and Counters	295
5.13.1	Flip-Flops and Registers with Enable Inputs	300
5.13.2	Shift Registers with Enable Inputs	302
5.14	Design Example	302
5.14.1	Reaction Timer	302
5.14.2	Register Transfer Level (RTL) Code	309
5.15	Timing Analysis of Flip-flop Circuits	310
5.15.1	Timing Analysis with Clock Skew	312
5.16	Concluding Remarks	314
5.17	Examples of Solved Problems	315
	Problems	321
	References	329

Chapter 6

SYNCHRONOUS SEQUENTIAL CIRCUITS 331

6.1	Basic Design Steps	333
6.1.1	State Diagram	333
6.1.2	State Table	335
6.1.3	State Assignment	336
6.1.4	Choice of Flip-Flops and Derivation of Next-State and Output Expressions	337
6.1.5	Timing Diagram	339
6.1.6	Summary of Design Steps	340
6.2	State-Assignment Problem	344
6.2.1	One-Hot Encoding	347
6.3	Mealy State Model	349
6.4	Design of Finite State Machines Using CAD Tools	354
6.4.1	Verilog Code for Moore-Type FSMs	355
6.4.2	Synthesis of Verilog Code	356
6.4.3	Simulating and Testing the Circuit	358

6.4.4	Alternative Styles of Verilog Code	359
6.4.5	Summary of Design Steps When Using CAD Tools	360
6.4.6	Specifying the State Assignment in Verilog Code	361
6.4.7	Specification of Mealy FSMs Using Verilog	363
6.5	Serial Adder Example	363
6.5.1	Mealy-Type FSM for Serial Adder	364
6.5.2	Moore-Type FSM for Serial Adder	367
6.5.3	Verilog Code for the Serial Adder	370
6.6	State Minimization	372
6.6.1	Partitioning Minimization Procedure	374
6.6.2	Incompletely Specified FSMs	381
6.7	Design of a Counter Using the Sequential Circuit Approach	383
6.7.1	State Diagram and State Table for a Modulo-8 Counter	383
6.7.2	State Assignment	384
6.7.3	Implementation Using D-Type Flip-Flops	385
6.7.4	Implementation Using JK-Type Flip-Flops	386
6.7.5	Example—A Different Counter	390
6.8	FSM as an Arbiter Circuit	393
6.9	Analysis of Synchronous Sequential Circuits	397
6.10	Algorithmic State Machine (ASM) Charts	401
6.11	Formal Model for Sequential Circuits	405
6.12	Concluding Remarks	407
6.13	Examples of Solved Problems	407
	Problems	416
	References	420

Chapter 7

DIGITAL SYSTEM DESIGN 421

7.1	Bus Structure	422
7.1.1	Using Tri-State Drivers to Implement a Bus	422
7.1.2	Using Multiplexers to Implement a Bus	424
7.1.3	Verilog Code for Specification of Bus Structures	426
7.2	Simple Processor	429

- 7.3 A Bit-Counting Circuit 441
- 7.4 Shift-and-Add Multiplier 446
- 7.5 Divider 455
- 7.6 Arithmetic Mean 466
- 7.7 Sort Operation 470
- 7.8 Clock Synchronization and Timing Issues 478
 - 7.8.1 Clock Distribution 478
 - 7.8.2 Flip-Flop Timing Parameters 481
 - 7.8.3 Asynchronous Inputs to Flip-Flops 482
 - 7.8.4 Switch Debouncing 483
- 7.9 Concluding Remarks 485
 - Problems 485
 - References 489

Chapter 8

OPTIMIZED IMPLEMENTATION OF LOGIC FUNCTIONS 491

- 8.1 Multilevel Synthesis 492
 - 8.1.1 Factoring 493
 - 8.1.2 Functional Decomposition 496
 - 8.1.3 Multilevel NAND and NOR Circuits 502
- 8.2 Analysis of Multilevel Circuits 504
- 8.3 Alternative Representations of Logic Functions 510
 - 8.3.1 Cubical Representation 510
 - 8.3.2 Binary Decision Diagrams 514
- 8.4 Optimization Techniques Based on Cubical Representation 520
 - 8.4.1 A Tabular Method for Minimization 521
 - 8.4.2 A Cubical Technique for Minimization 529
 - 8.4.3 Practical Considerations 536
- 8.5 Concluding Remarks 537
- 8.6 Examples of Solved Problems 537
 - Problems 546
 - References 549

Chapter 9

ASYNCHRONOUS SEQUENTIAL CIRCUITS 551

- 9.1 Asynchronous Behavior 552
- 9.2 Analysis of Asynchronous Circuits 556

- 9.3 Synthesis of Asynchronous Circuits 564
- 9.4 State Reduction 577
- 9.5 State Assignment 592
 - 9.5.1 Transition Diagram 595
 - 9.5.2 Exploiting Unspecified Next-State Entries 598
 - 9.5.3 State Assignment Using Additional State Variables 602
 - 9.5.4 One-Hot State Assignment 607
- 9.6 Hazards 608
 - 9.6.1 Static Hazards 609
 - 9.6.2 Dynamic Hazards 613
 - 9.6.3 Significance of Hazards 614
- 9.7 A Complete Design Example 616
 - 9.7.1 The Vending-Machine Controller 616
- 9.8 Concluding Remarks 621
- 9.9 Examples of Solved Problems 623
 - Problems 631
 - References 635

Chapter 10

COMPUTER AIDED DESIGN TOOLS 637

- 10.1 Synthesis 638
 - 10.1.1 Netlist Generation 638
 - 10.1.2 Gate Optimization 638
 - 10.1.3 Technology Mapping 640
- 10.2 Physical Design 644
 - 10.2.1 Placement 646
 - 10.2.2 Routing 647
 - 10.2.3 Static Timing Analysis 648
- 10.3 Concluding Remarks 650
 - References 651

Chapter 11

TESTING OF LOGIC CIRCUITS 653

- 11.1 Fault Model 654
 - 11.1.1 Stuck-at Model 654
 - 11.1.2 Single and Multiple Faults 655
 - 11.1.3 CMOS Circuits 655
- 11.2 Complexity of a Test Set 655
- 11.3 Path Sensitizing 657
 - 11.3.1 Detection of a Specific Fault 659
- 11.4 Circuits with Tree Structure 661
- 11.5 Random Tests 662

11.6	Testing of Sequential Circuits	665
11.6.1	Design for Testability	665
11.7	Built-in Self-Test	669
11.7.1	Built-in Logic Block Observer	673
11.7.2	Signature Analysis	675
11.7.3	Boundary Scan	676
11.8	Printed Circuit Boards	676
11.8.1	Testing of PCBs	678
11.8.2	Instrumentation	679
11.9	Concluding Remarks	680
	Problems	680
	References	683

Appendix A

VERILOG REFERENCE 685

A.1	Documentation in Verilog Code	686
A.2	White Space	686
A.3	Signals in Verilog Code	686
A.4	Identifier Names	687
A.5	Signal Values, Numbers, and Parameters	687
A.5.1	Parameters	688
A.6	Net and Variable Types	688
A.6.1	Nets	688
A.6.2	Variables	689
A.6.3	Memories	690
A.7	Operators	690
A.8	Verilog Module	692
A.9	Gate Instantiations	694
A.10	Concurrent Statements	696
A.10.1	Continuous Assignments	696
A.10.2	Using Parameters	697
A.11	Procedural Statements	698
A.11.1	Always and Initial Blocks	698
A.11.2	The If-Else Statement	700
A.11.3	Statement Ordering	701
A.11.4	The Case Statement	702
A.11.5	Casez and Casex Statements	703
A.11.6	Loop Statements	704
A.11.7	Blocking versus Non-blocking Assignments for Combinational Circuits	708
A.12	Using Subcircuits	709
A.12.1	Subcircuit Parameters	710
A.12.2	The Generate Capability	712
A.13	Functions and Tasks	713

A.14	Sequential Circuits	716
A.14.1	A Gated D Latch	717
A.14.2	D Flip-Flop	717
A.14.3	Flip-Flops with Reset	718
A.14.4	Registers	718
A.14.5	Shift Registers	720
A.14.6	Counters	721
A.14.7	An Example of a Sequential Circuit	722
A.14.8	Moore-Type Finite State Machines	723
A.14.9	Mealy-Type Finite State Machines	724
A.15	Guidelines for Writing Verilog Code	725
A.16	Concluding Remarks	731
	References	731

Appendix B

IMPLEMENTATION TECHNOLOGY 733

B.1	Transistor Switches	734
B.2	NMOS Logic Gates	736
B.3	CMOS Logic Gates	739
B.3.1	Speed of Logic Gate Circuits	746
B.4	Negative Logic System	747
B.5	Standard Chips	749
B.5.1	7400-Series Standard Chips	749
B.6	Programmable Logic Devices	753
B.6.1	Programmable Logic Array (PLA)	754
B.6.2	Programmable Array Logic (PAL)	757
B.6.3	Programming of PLAs and PALs	759
B.6.4	Complex Programmable Logic Devices (CPLDs)	761
B.6.5	Field-Programmable Gate Arrays	764
B.7	Custom Chips, Standard Cells, and Gate Arrays	769
B.8	Practical Aspects	771
B.8.1	MOSFET Fabrication and Behavior	771
B.8.2	MOSFET On-Resistance	775
B.8.3	Voltage Levels in Logic Gates	776
B.8.4	Noise Margin	778
B.8.5	Dynamic Operation of Logic Gates	779
B.8.6	Power Dissipation in Logic Gates	782
B.8.7	Passing 1s and 0s Through Transistor Switches	784
B.8.8	Transmission Gates	786
B.8.9	Fan-in and Fan-out in Logic Gates	788
B.8.10	Tri-state Drivers	792

B.9	Static Random Access Memory (SRAM)	794	B.12	Examples of Solved Problems	807
B.9.1	SRAM Blocks in PLDs	797		Problems	814
B.10	Implementation Details for SPLDs, CPLDs, and FPGAs	797		References	823
B.10.1	Implementation in FPGAs	804		ANSWERS	825
B.11	Concluding Remarks	806		INDEX	839