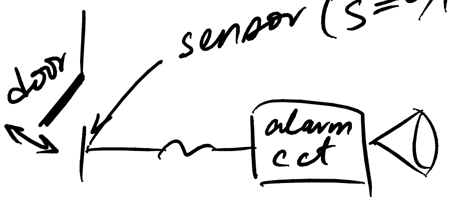
Storage Elements (aka Sequential cct.)

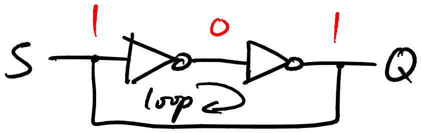
Def'n Combinational cct a logic cct. in which the outputs of the cct. depend only on the present values of the inputs

Def'n Sequential cct a logic cct. in which the outputs depend on both the present values of inputs, and previous values of inputs
→ the cct. incorporate the concept of a stored state.

example (of stored state) – we need to store the value s=1 when the door is opened.

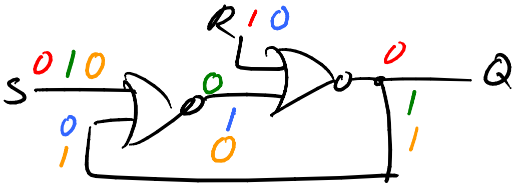


– storage element involves some kind of feedback loop:



– problem is, the cct can't change S value

– let's modify the cct.

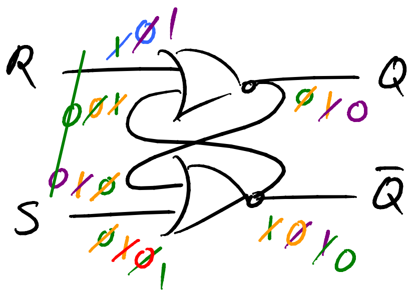


R – reset
S – set
Q – output

Operation:

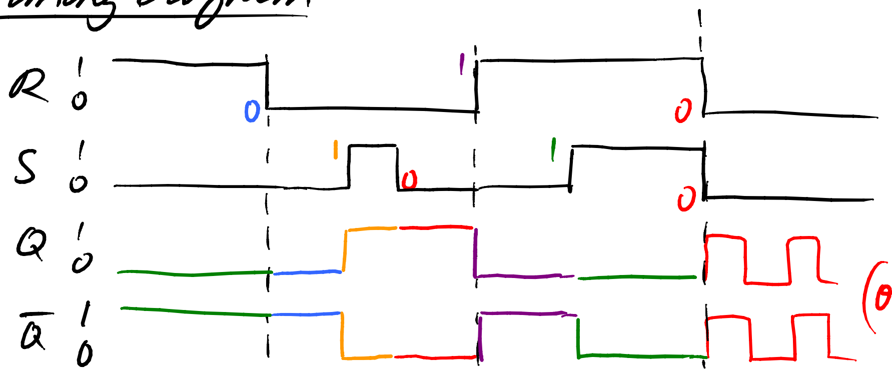
1. we reset the alarm (R=1, Q=0) assuming door is closed at the moment (S=0)
2. let R=0 (device is armed)
3. Door is opened! (S=1, result is Q=1 alarm!)
4. To Take Q=0, we need to reset the alarm (R=1)

RS Latch



"Cross-coupled NOR gates"

Timing Diagram



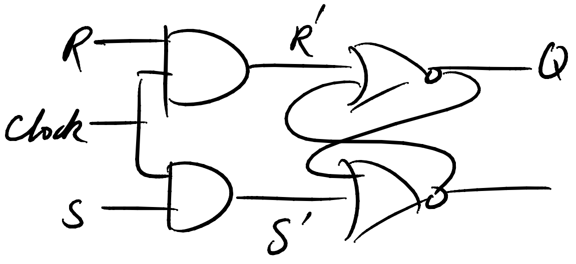
When using a RS latch we should avoid setting R=S=1.

(oscillation)

Truth Table

S	R	Q	$\bar{Q}$	
0	0	x	x	(stored value either 0 or 1)
0	1	0	1	
1	0	1	0	
1	1	0	0	(should not use)

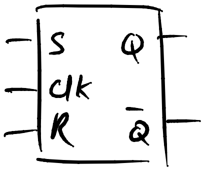
Gated SR latch



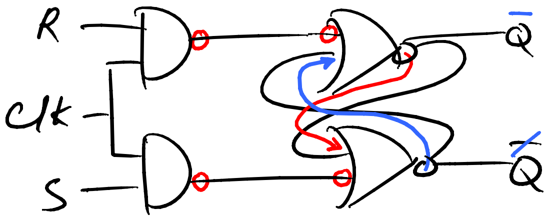
Note: setting Clk=0 means that R'=S'=0, so that Q can't change regardless of R, S.

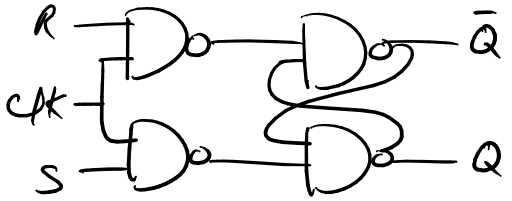
Clk	S	R	Q(t+1)	
0	x	x	Q(t)	(store old value)
1	0	0	Q(t)	(" " ")
1	0	1	0	
1	1	0	1	
1	1	1	?	(not used)

cct. symbol



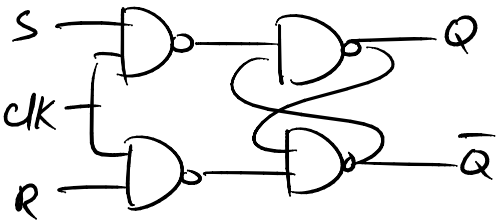
Q: How do we build this gated RS latch using only NAND gates

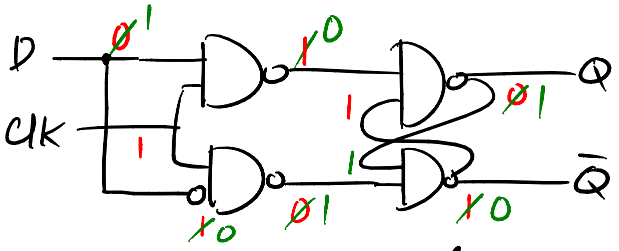




same

NAND version of gated RS latch

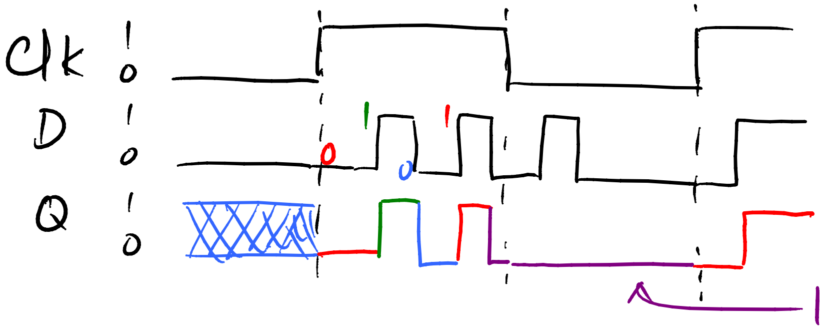




gated D-latch

	Clk	D	Q	
hold old value →	0	X	0/1	(stored)
Q follows D	1	0	0	
	1	1	1	

Timing Diagram

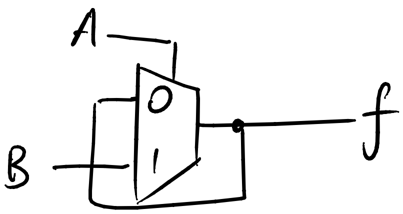


latch holding old value

⇒ Q follows D when clock is "1"

Q holds its value when clock is "0".

Q: what will this cct do?

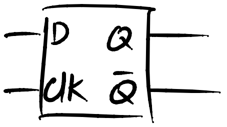


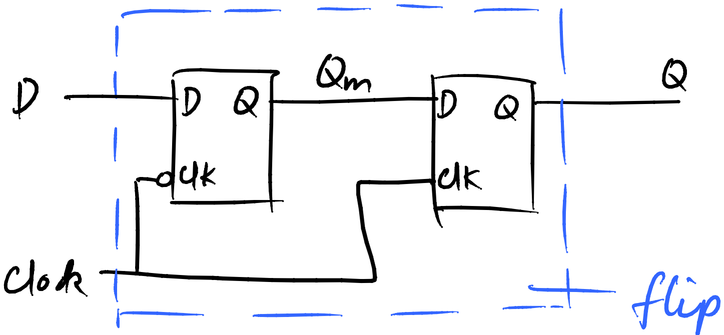
A	B	f	
0	X	0/1	(stored value)
1	0	0	
1	1	1	

clock

D.

this is a gated D latch





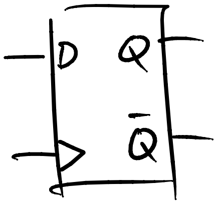
flip-flop (D)

<u>Case 1</u> Clock = 0, $Q_m = D$

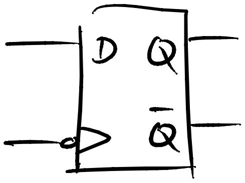
<u>Case 2</u> Clock → 1, Q_m can't make any change. $Q = Q_m$

Note: the flip-flop allows the value of D to be captured and stored on the rising edge of the clock ($_0$⌐^{1}).
+ve edge.

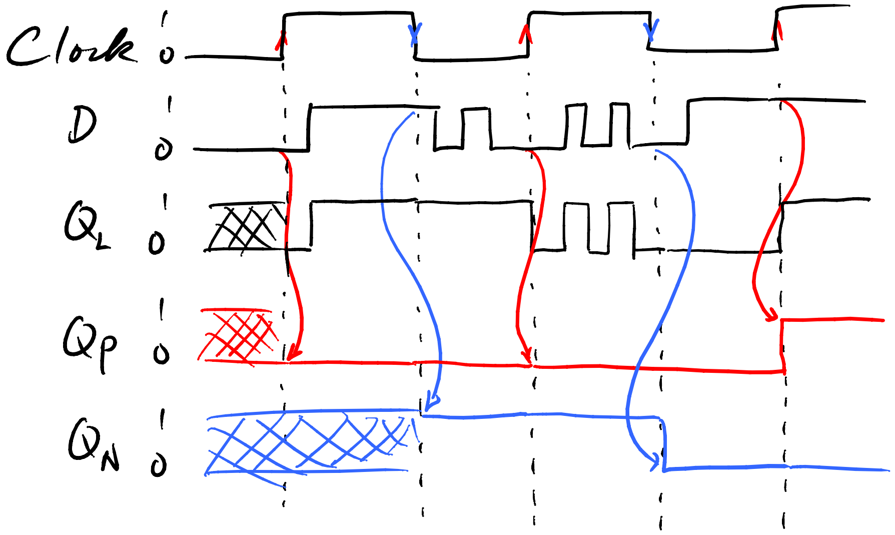
<u>+ve edge triggered f f.</u>

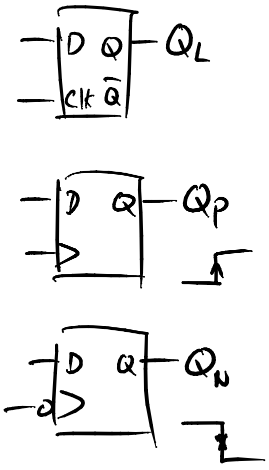


<u>-ve edge triggered f-f</u>



<u>Timing Diagram</u>


Clock 1 0
D 1 0
Q_L 1 0
Q_P 1 0
Q_N 1 0


D Q
clk $\bar{Q}$
Q_L
D Q
Q_P
D Q
Q_N