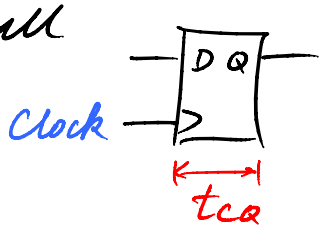
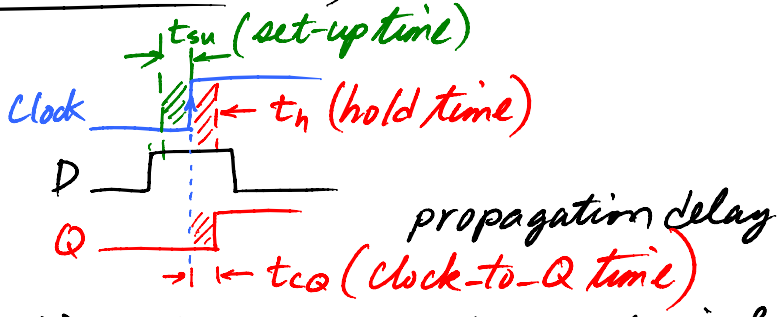
Timing Analysis (revisited)

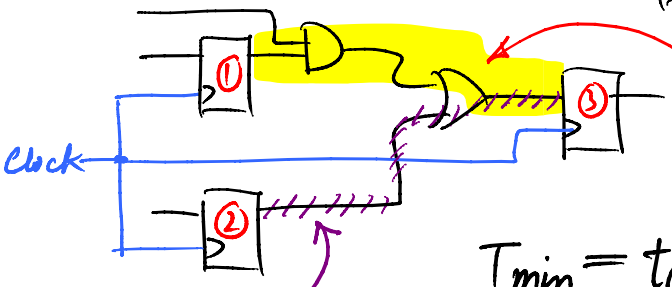
Recall





Note: in datasheets for chips, there are usually both min & max given for t_{CQ} eg.

min	max
0.7 ns	1.0 ns

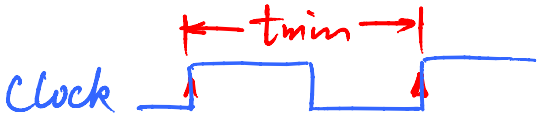


in analysis for f_{max} (T_{min})

the worst case (longest delays)

$$T_{min} = t_{CQ}^{①}(max) + t_{AND} + t_{OR} + t_{su}$$

$$f_{max} = \frac{1}{T_{min}}$$

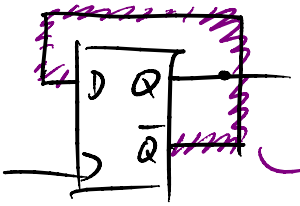


What about hold time?

consider the shortest path. $t_{shortest\ path} = t_{CQ}^{②}(min) + t_{OR}$

if $(t_{CQ}(min) + t_{OR}) \geq t_h$, then there is no violation.

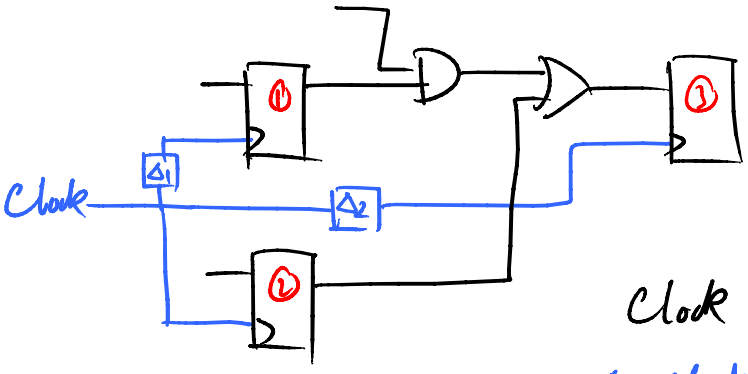
Note: the worst case ckt. for hold time



$t_{shortest\ path} = t_{CQ}(min)$

if $t_{CQ}(min) \geq t_h$, then no hold time violation.

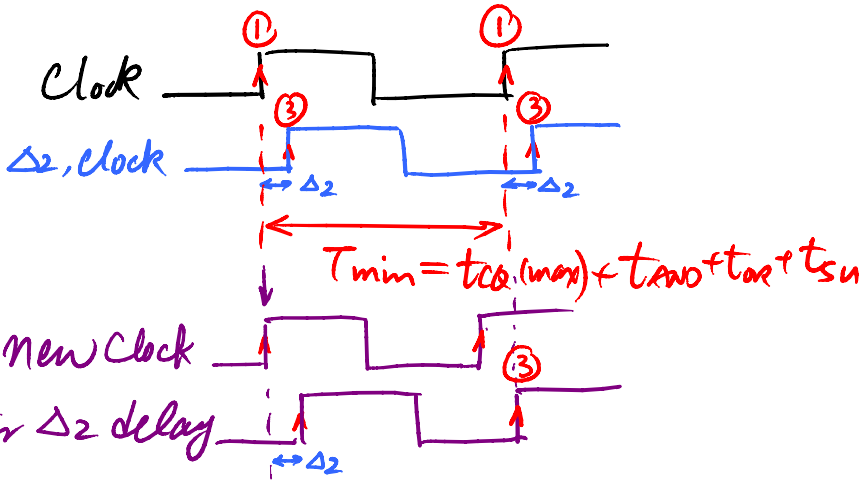
Ⓐ in real chips $t_{CQ}(min)$ is always $\geq t_h$.



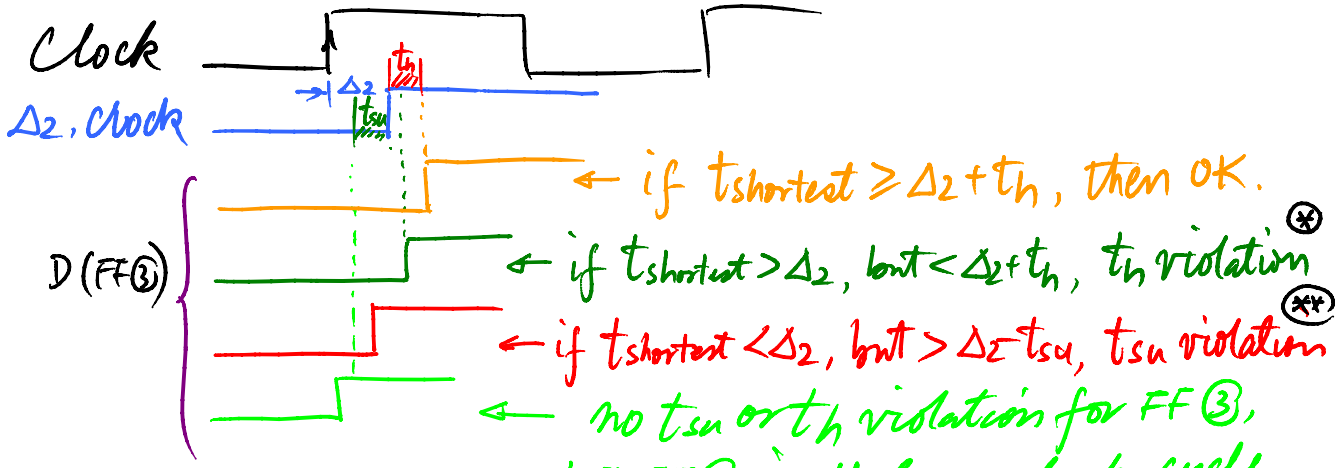
Clock Skew

Clock arrives at FFs at different times

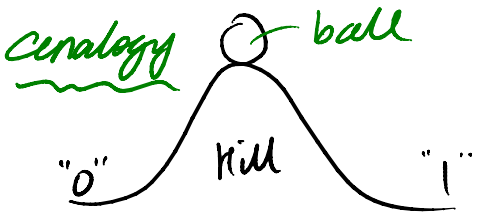
Case 1: $\Delta_1 = 0$, $\Delta_2 > 0$



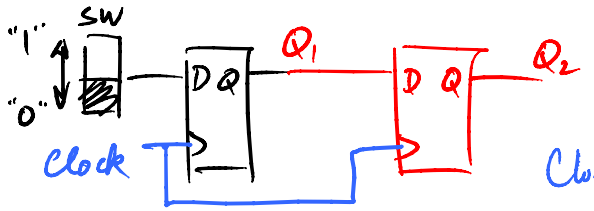
→ Is there a violation of t_h ?



⊛ and ⊛⊛ each violates FF③ parameters (t_{su}, t_h). What happens is that FF③ becomes **metastable**:

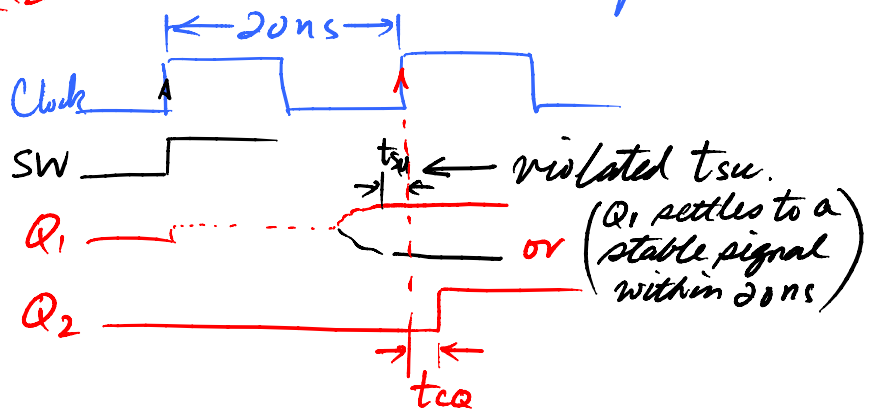


after some random time, the ball will roll down to either "0" or "1"

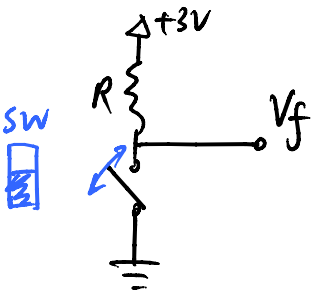


Synchronizer

50 MHz clock. → 20 ns period

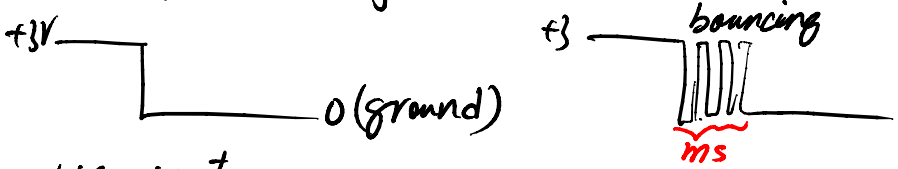


Switch Debouncing



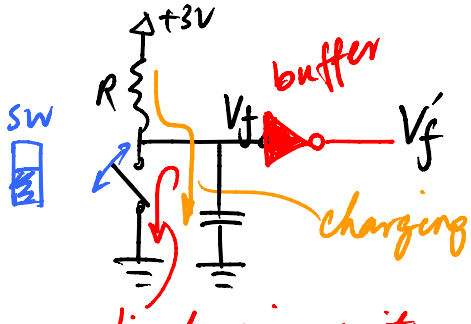
SW – closed. Vf goes to ground ("0")

SW – opens. Vf goes to +3V ("1")



we want.

actual effect.

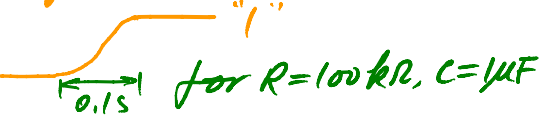


discharging quite fast because of low resistance of the SW
R ≃ 0

SW – closed. capacitor discharge
Vf → "0" Vf' → "1"

SW – opens, capacitor being charged
Vf → "1" Vf' → "0"

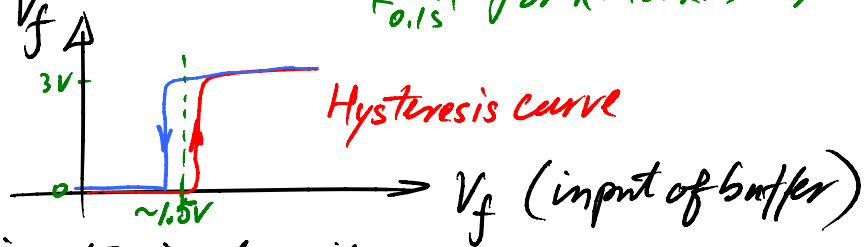
charging speed depends on RC



for R = 100kΩ, C = 1μF

What's the purpose of —▷— buffer?

(output of buffer) Vf'



→ to ensure that FPGA input pin doesn't see a rising signal during the bounce

the buffer has the response shown by the Hysteresis curve

Using FSM to wait out about ms.