```
1   module part4(input [15:0]SW, input [2:0]KEY, output [7:0]LEDR);
2
3      wire [7:0] A, B;
4      wire [2:0] Q;
5
6      assign A = SW[15:8];
7      assign B = SW[7:0];
8      assign Q = KEY;
9      assign LEDR = Z;
10
11     reg [7:0]Z;
12     always@(A, B, Q)
13     case(Q)
14        3'b000: Z = ~A | B;
15        3'b001: Z = A | ~B;
16        3'b010: Z = ~A;
17        3'b011: Z = A & B;
18        3'b100: Z = A + B;
19        3'b101: Z = ~(A | B);
20        3'b110: Z = A[0] + A[1] + A[2] + A[3] + A[4] + A[5] + A[6] + A[7];
21        3'b111: Z = A[0] + A[1] + A[2] + A[3] + A[4] + A[5] + A[6] + A[7] + B[0] + B[1] + B[2]
      + B[3] + B[4] + B[5] + B[6] + B[7];
22     endcase
23
24  endmodule
```