

ci bi as		CitI	Si'
0	00	0	O
0	0	0	
0	10	0	1
0		11	0
1 [OO	O	
1	0	1	0
1 !	10	11	0
1	1 1		

* using ai would have the pame effect. because this value goes through only when both ai and bi have the same value

Verilog for a FA

conditional assignment

endmodue

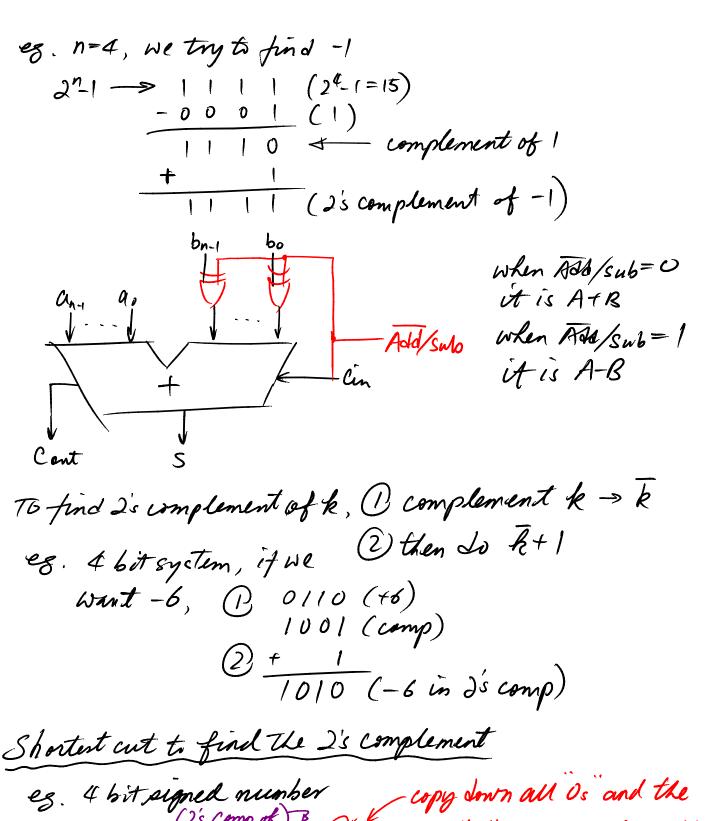
Verilog code for n bit alder usus a for loop

Module addn (Cin, A, B, Cout, S); parameter n=4; input Cin; input [n-1:0] A, B; output reg Cout; output reg [n-1:0]s; reg [o:n]C;

for
$$(k=0; k<0; k=k+1)$$

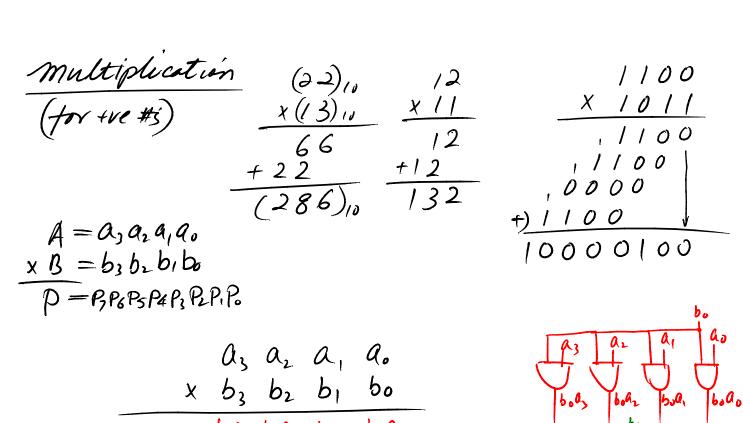
 $\{C[k+1], S[k]\} = A[k] + B[k] + C[k],$

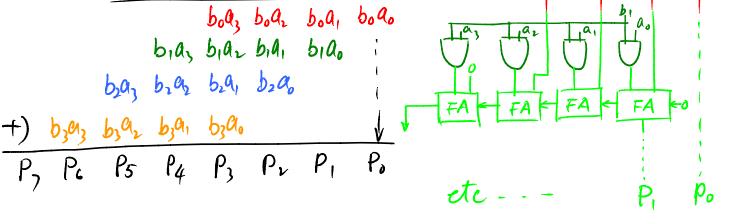
always@ (*); c[o] = Cin; // initialization for (k=0; k<n; k=k+1) begm S[k]=A[k]^B[k]^C[k]; C[k+1] = (A[k] == B[k])? A[k] : C[k];



eg. 4 bit signed number copy down all 0s and the go 110 (2's comp. of) 3 ret 1ct 1 you see from the (4 bit +6) complement the right hand side (ie.

Nemaining bits slanting from the lowest bit)





Finite State Machine (FSM)

