ECE 241 – Digital Systems

Fall 2013 – J. Anderson, P. Chow, K. Truong, B. Wang

Basic Information

Instructors and Lecture Information

Section	1		2		3		4	
Instructor	Jason Anderson		Kevin Truong		Paul Chow		Belinda Wang	
Office	EA 314		Rosebrugh 404B		EA 320		GB 250	
Phone	416-946-7285		416-978-7772		416-978-2402		416-978-5543	
Email	janders@eecg.toronto.edu		kevin.truong@utoronto.ca		pc@eecg.toronto.edu		belinda.wang@utoronto.ca	
Office hours	Arrange with your instructor by email							
Lecture Rooms/Times	M 1-2	RS 211	T 9-10	GB 244	T 2-3	GB 248	M 10-11	GB 220
	W 1-2	GB 248	F 2-3	GB 248	W 9-10	BA 1190	W 1-2	GB 244
	R 1-2	GB 221	F 3-4	GB 248	R 4-5	GB 248	R 2-3	GB 120

Grading

Labs 10%	**Project** 10%	**Midterm** 30%	**Exam** 50%

Web Page: Blackboard Portal

Midterm

Tuesday, October 15 2013 6-8 PM (tentative). Book in your calendar!

Exam

Type D – examiner specified aids: **One single sheet of letter size paper (8.5x11 inch) with your written notes of your choosing**. **No calculators, no cell phones.**

Required Text

Title: Fundamentals of Digital Logic with Verilog Design, **3rd Edition**
Authors: Stephen Brown and Zvonko Vranesic
Publisher: McGraw-Hill
ISBN: 0073380547

Computer Required to Run CAD Software at Home

You'll need a computer running Windows 7, Vista or XP, a 1GHz Processor or better, at least 1GBytes main memory. If you do not have this class of computer, you will be able to use the University's machines instead. See the syllabus page on CAD software to find out how to obtain the software for your computer.

ECE 241 - Digital Systems - Course Outline

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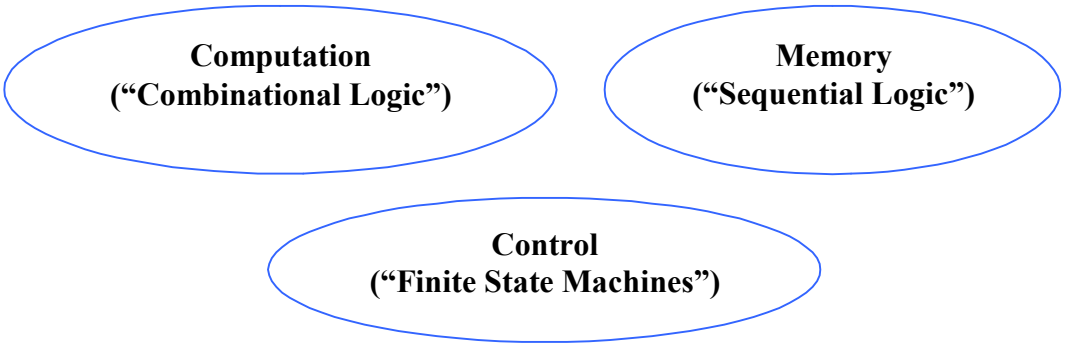

Goals

1. To understand basic digital logic circuit design, optimization and concepts.
2. To become comfortable using Computer-Aided Design (CAD) tools in design.
3. To gain hands-on experience with the design and debug of digital systems, using programmable logic.

1. Introduction to Combinational Logic

- switches and logic gates
- logic functions, truth tables and variables
- Boolean axioms and laws, sum of products, product of sums
- simple algebraic minimization - making things cheaper with a new kind of algebra

2. Technology

- logic voltage levels
- transistors as a switch
- NMOS and CMOS logic gates
- real propagation delay, and timing diagrams, timing analysis of digital circuits
- Field-Programmable Gate Arrays (FPGAs)
- introduction to Verilog (a language for describing hardware) and CAD tools that implement hardware given the Verilog description language

3. Combinational Logic Optimization

- minimization goals - speed and cost
- Karnaugh Map optimization technique
- optimization of logic that have "Don't Care" conditions
- critical path through combinational logic

4. Sequential Logic

- cross-coupled NOR/NAND gates basic latch
- gated latch
- Master-Slave D flip-flop
- shift registers
- counters
- set-up & hold time, clock-to-Q

5. Finite State Machines

- how logic is controlled
- state diagrams
- Moore-type state machines, Mealy-type machines
- state machine synthesis
- state machines in Verilog
- state encoding and optimization

6. Numbers and Arithmetic

- number representation, binary, ones & twos complement representation of negative numbers
- basic adder/subtracter
- carry look-ahead methods for fast addition
- bit serial addition

7. Miscellaneous

- multiplexors & tristate gates
- multiplexors as logic; decoders
- fanout-dependent delay
- power dissipation, I/O devices and FPGAs
- Static Random Access Memory (SRAM);
- controller for digital display
- de-bouncing mechanical switches
- VGA display interface

ECE 241 - Digital Systems - Lab Schedule and Information

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The real learning in this course goes on in the laboratory where you design, build and test and fix real circuits. There are **seven mandatory** labs of three hours each, and so you will have one 3-hour lab every week. You will work in groups of **two**.

There is also a project based on the material of this course that you will also work with your partner on.

There are two parts to the lab experience: preparation, which you must do outside of the lab hours, and the actual implementation of circuits in the lab.

Preparation

Each lab usually requires you to do a significant amount of preparation, and is where you must do much of the work to understand the concepts. Preparation must be complete before the lab begins. Preparation will usually require design using the CAD software supplied. **Each partner in the group of 2 must perform and submit a separate preparation.** While it is acceptable to discuss your preparation with your partner, your work may not be copied from your partner; you will be required to explain your preparation. Please be aware that severe penalties will be imposed for copying of labs, as evidenced by an inability to explain the work given as preparation. It will be graded by the TAs at the beginning of the lab, on the following basis:

Judgement of TA	Grade
Unable to explain any part of preparation	0
Some merit to work	1
Made a legitimate attempt	2
Reasonable job, may be some missing things	3-4
Correct and done well, demonstrated clear knowledge of subject.	5

In-Lab Work

In each lab you will typically have to build a working circuit. Once this is done, for each such circuit, show it to your TA for grading, out of 3:

Judgement of TA	Grade
Did not attend or try	0
Tried, but failed to get much working	1
Most, but not all working	2
Everything worked	3

Note: Although the lab portion of the course is worth only 10%, both the midterm and the final exam will contain questions directly related to skills learned in the lab.

Lab Workstation Number and Maintenance

Each digital workstation that you'll be sitting at has a number. Please use the same station each week. If a piece of equipment is not working, please tell a TA to tag the board with the problem and notify someone to have it repaired. Otherwise it will be broken the next time you need to use it!

Lab Sections, Day Time and Location

Section	Day	Time	Location(s)
1,2	Monday	3pm-6	BA 3135 & 3145
7,8	Thursday	9am-12	BA 3135 & 3145
3,4	Friday	9am-12	BA 3135 & 3145
5,6	Monday	9am-12	BA 3135 & 3145

Lab and Project Schedule for 2013

Date of Monday	Lab
September 9	No lab.
September 16	#1: Building simple logic functions using 7400-series chips.
September 23	#2 Lights, switches, multiplexers (before this lab, you should do the self-guided Quartus tutorial on your own).
September 30	#3 Numbers and displays
October 7	#4 Latches, flip-flops and registers
October 14	**Thanksgiving week – no lab; midterm exam this week!**
October 21	#5 Counters and clocks, arithmetic
October 28	#6 Finite state machines (FSMs)
November 4	#7 FSMs, VGA
November 11	**Project Period 1**
November 18	**Project Period 2**
November 25	**Project Period 3**

ECE 241 - Digital Systems - Access to CAD Software

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The lab in this course depends heavily on the use of Computer-Aided Design (CAD) software to implement the circuits, usually on a programmable logic device. We will be using Field-Programmable Gate Arrays (FPGAs) from Altera, and Altera's **Quartus II** Version 11.1 CAD software. You will be able to access this software in one of three ways:

1. On your own home computer.

If you have a Windows 7, Vista or XP-based home computer with at least 1 GBytes of physical RAM, you can download the Quartus II 11.1 SP2 *Web edition* directly from the Altera web site:

`https://www.altera.com/download/archives/`

In the lab we will be using the full version of the software, but the web edition has all you need as well.

2. On the Windows Machines in the lab – Bahen 3135 and 3145

There are a total of one hundred Windows XP-based machines in these Bahen Centre labs. These will have the latest release of the full license (not the web edition) of Quartus version 11.1 SP2 software installed on them. These machines will have access to your home directory on the ECE network.

ECE 241 Project

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The Task

The purpose of the project is to:

1. Gain experience dealing with the design of a larger digital system, and to deal with the issues in going from a soft simple specification ("make a digital toaster controller") to an actual complete design. There is no substitute for experience!

2. Express your creativity by applying what you have learned in this course to a project of your own choosing.

You will design and implement a project of your own choosing that uses digital logic in some creative way. You may use any of the parts available in the lab, but are restricted to using just one of the Altera DE2 boards. An important part of this lab is the creativity required to think up an interesting project, and then negotiate with a TA or instructor as to the final form of the project.

Originality/Uniqueness Approval

The first step in your project is to come up with an original idea. You must submit your idea, in a 1-3 line description, via email to the ECE241 head TA (email address TBA) for "originality" or "uniqueness" approval (you may also CC your instructor). The head TA will quickly respond to tell you if the idea has already been proposed more than once. If it has, you'll have to come up with something different. Please note that this approval is only the first step and only deals with the basic idea, and not the scope/effort required for the project; that comes next:

Before the First Project lab

You will submit a short project proposal of what your project is about. This should be a short description that gives:

- The basic idea of the project, and the basic function of your circuit.
- Describe the inputs and outputs, and give a simple block diagrams describing how the various parts of your circuit interact.
- Your plan of action for each of the three lab periods - "milestones"
- Present this to your TA to get their opinion on whether the project is viable. Once approved, you should get their signature. This is just a check to make sure that you do not try something overly ambitious.

Demonstration and Report

You will demonstrate your project to your supervising TA in the final lab period, and will be required to provide a short report describing your project.