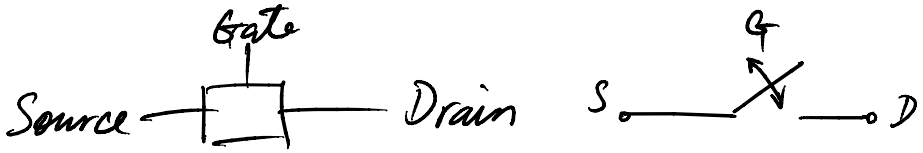
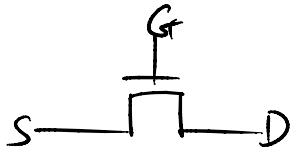
Transistors in logic gates



two variants (opposites):

1. NMOS : n-channel MOSFET (metal-oxide semiconductor field-effect transistor)
2. PMOS p-channel MOSFET

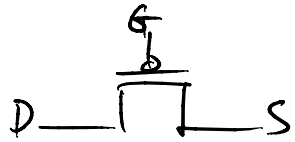
NMOS



G = 1 (~3V) S —— D

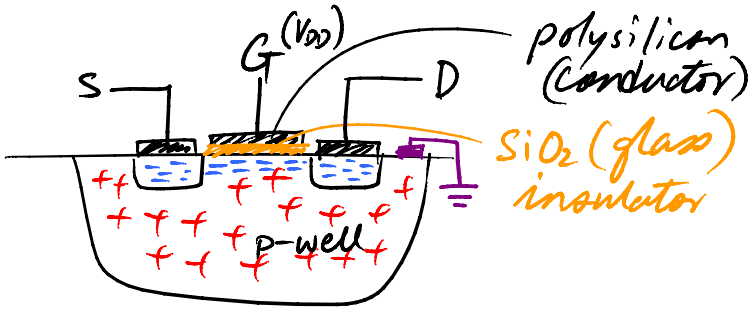
G = 0 (0V) S ⁄ D

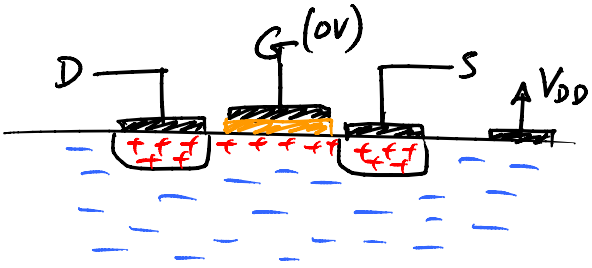
PMOS



G = 0 (Gnd) D —— S

G = 1 (V_{DD}) D ⁄ S





turning on the NMOS transistor

→ G = 3V (logic 1)

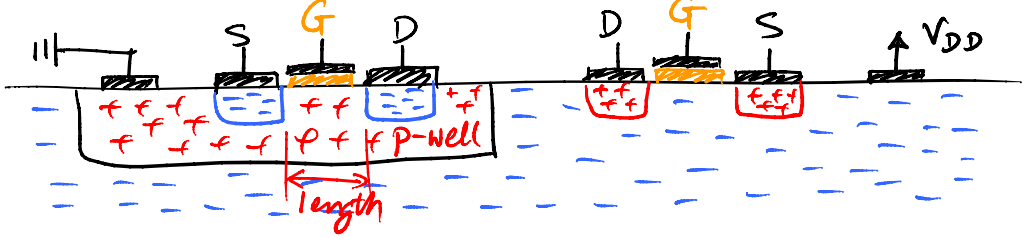
→ ---: channel formed to allow connection between S and D.

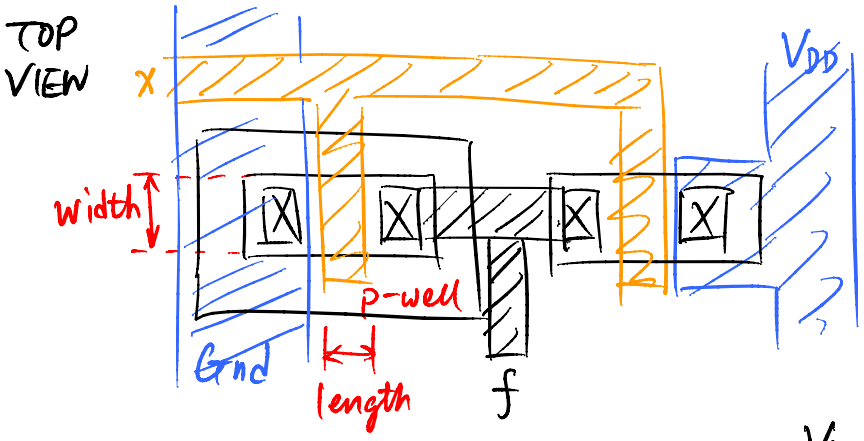
turning on PMOS transistor

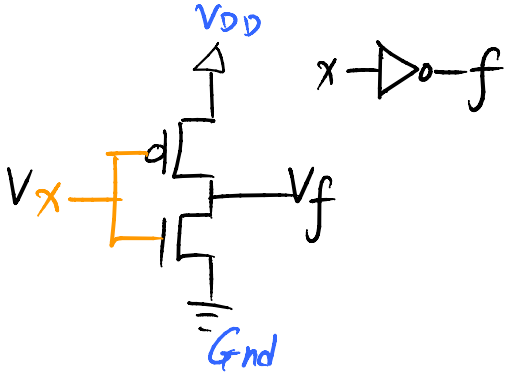
→ G = 0V (logic 0)

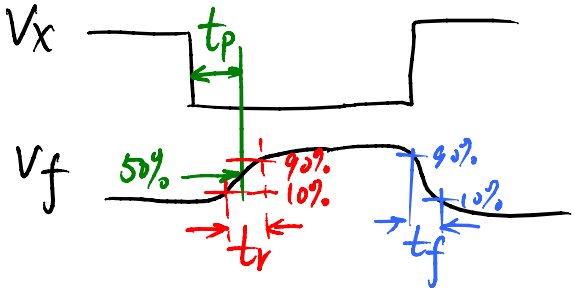
→ +++ channel formed to allow connection between D and S.

CMOS — complementary MOS (we always use an equal number of NMOS and PMOS transistors)

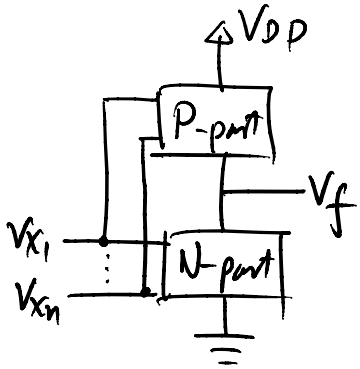




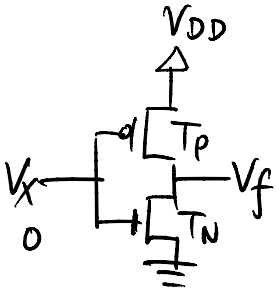




Complex CMOS logic gates

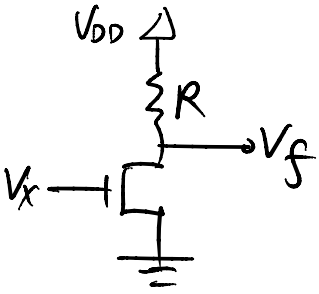


general structure for logic circuit.



Vx	TP	TN	Vf
0	on	off	1
1	off	on	0

alternative



$V_x = 0V$, NMOS off. V_f pulled to V_{DD} through R.

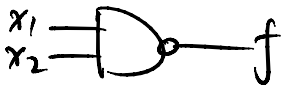
$R = 10k\Omega$, $V_{DD} = 2.5V$

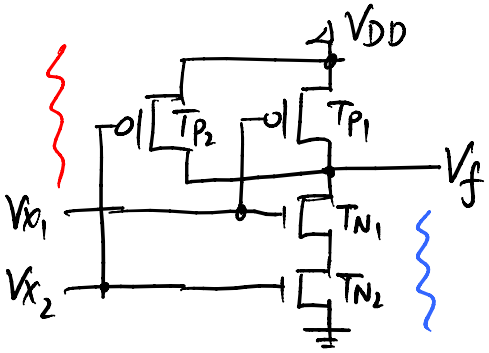
then $I = \frac{2.5V}{10k\Omega} = 0.25mA$

Say 10 million Transistors on a chip. that is $10^7 \times 0.25mA = 2500\ A$

CMOS NAND gate

$f = \overline{x_1 x_2} = \overline{x_1} + \overline{x_2}$

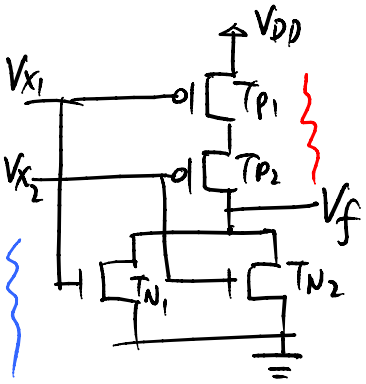




V_{x1}	V_{x2}	T_{P1}	T_{P2}	T_{N1}	T_{N2}	V_f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

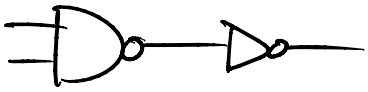
CMOS NOR gate

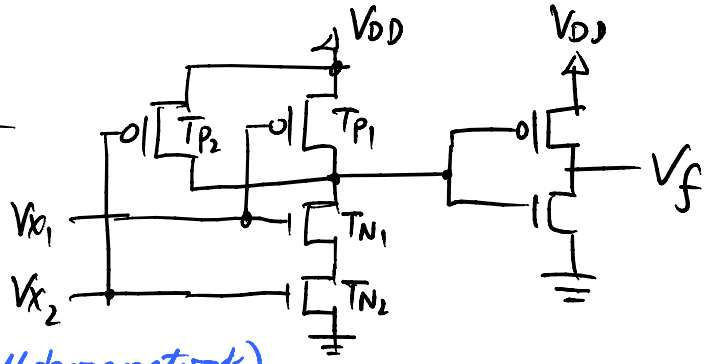
$f = \overline{x_1 + x_2} = \overline{x_1} \cdot \overline{x_2}$



V_{x_1}	V_{x_2}	T_{P_1} T_{P_2} T_{N_1} T_{N_2}	V_f
0	0	on on off off	1
0	1	on off off on	0
1	0	off on on off	0
1	1	off off on on	0

CMOS AND gate





(pull-up network)
PUN

PDN (pull-down network)

→ P-part on top, n-part at the bottom

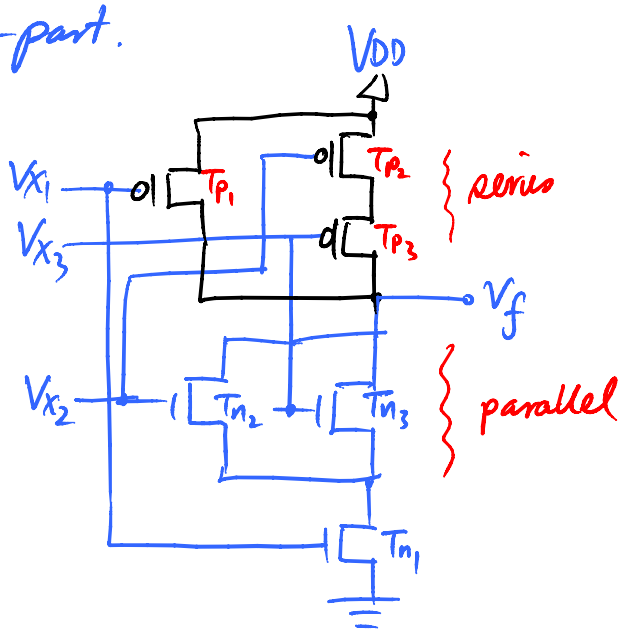
→ if n-part in series, then p-part must be in parallel

" " " parallel, " " " " series

→ $\overline{f(x)}$ → represents n-part.

example: $f = \overline{x_1} + \overline{x_2} \cdot \overline{x_3}$

option 1 — draw PUN first
— then PDN



option 2 — draw PDN first
— then PUN

$f = \overline{x_1} + \overline{x_2} \cdot \overline{x_3} = \overline{x_1} + \overline{x_2 + x_3}$

$= \overline{x_1 (x_2 + x_3)}$ → draw PDN

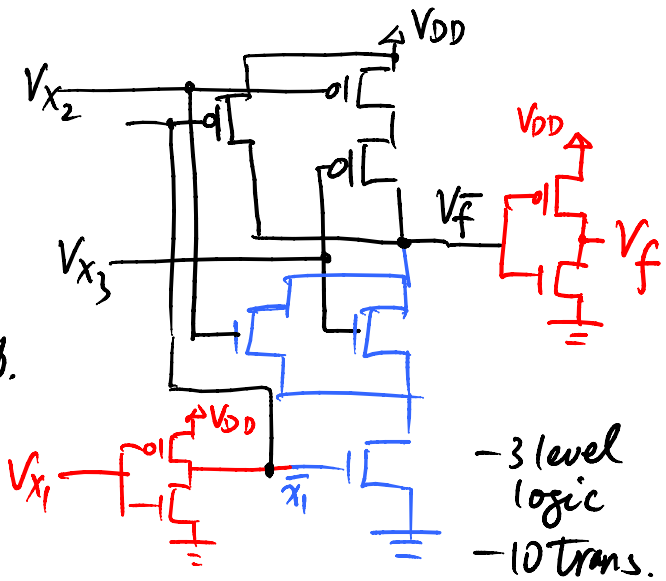
example 2 $f = \overline{x_1}(x_2 + x_3)$

option 1 $\overline{f} = \overline{\overline{x_1}(x_2 + x_3)}$

→ draw PDN first

→ then PUN

→ add an invert at the end.



– 3 level logic

– 10 trans.

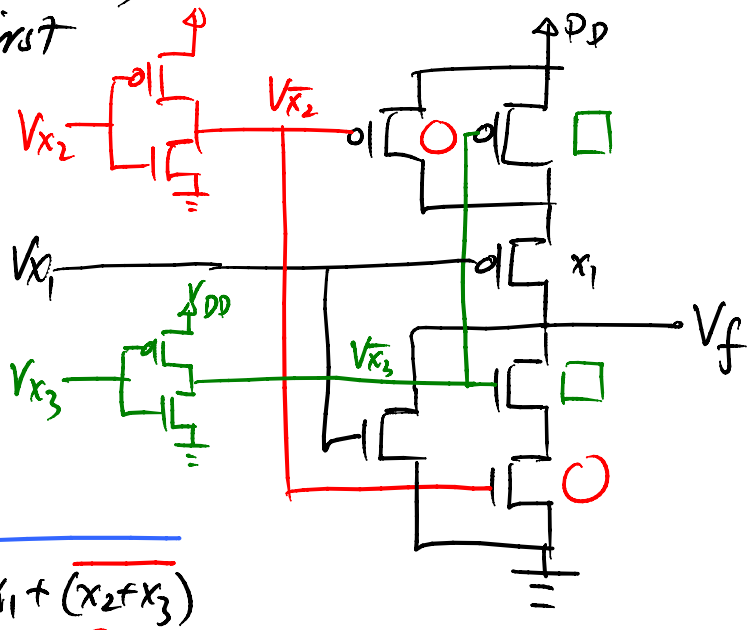
Option 2 $f = \overline{x_1}\left(\overline{\overline{x_2}} + \overline{\overline{x_3}}\right)$

→ draw PUN first

→ then PDN

– 2 level logic

– 10 transistors

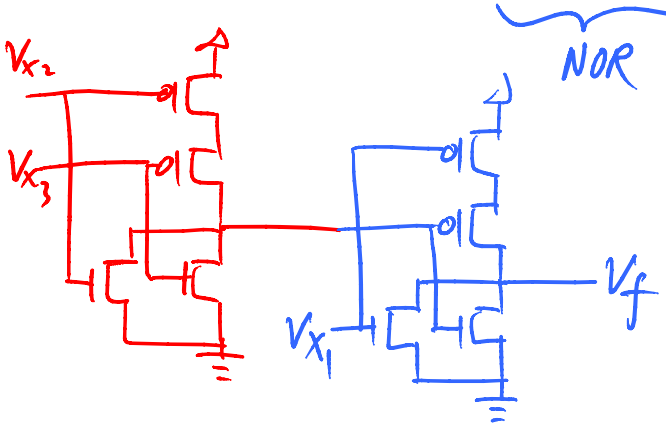


Option 3

$$f = \overline{\overline{x_1}(x_2 + x_3)} = x_1 + \overline{(x_2 + x_3)}$$

NOR

NOR



– 2 level logic

– 8 transistors