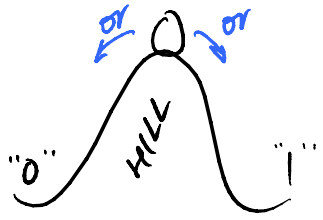
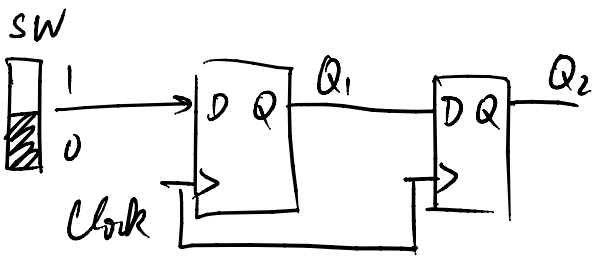
⇒ What happens if there is either a setup time or hold time violation

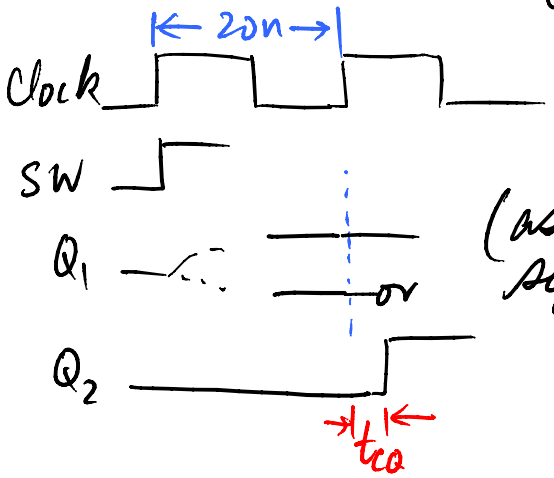


meta stable not certain whether it's "1" or "0"

7.8.3 Synchronizer



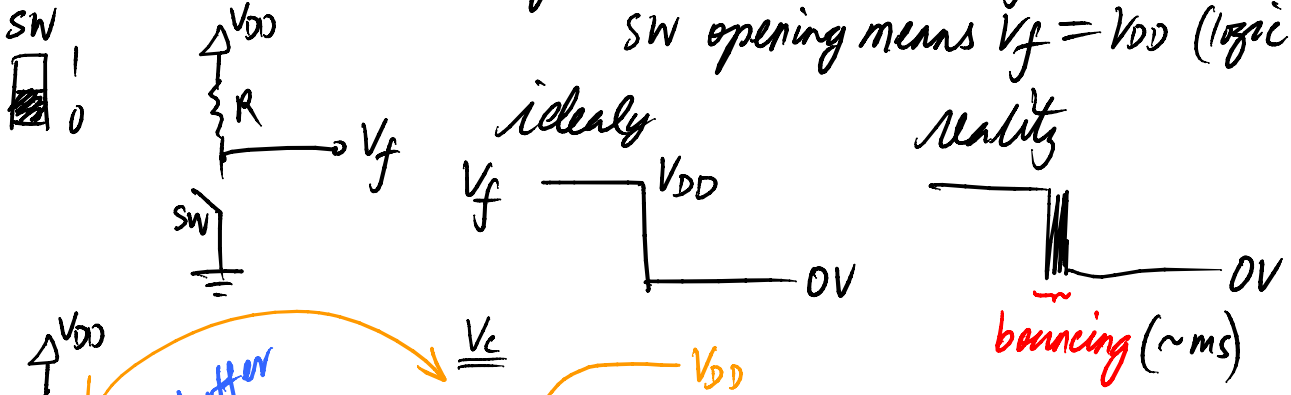
50 MHz, → 20ns period

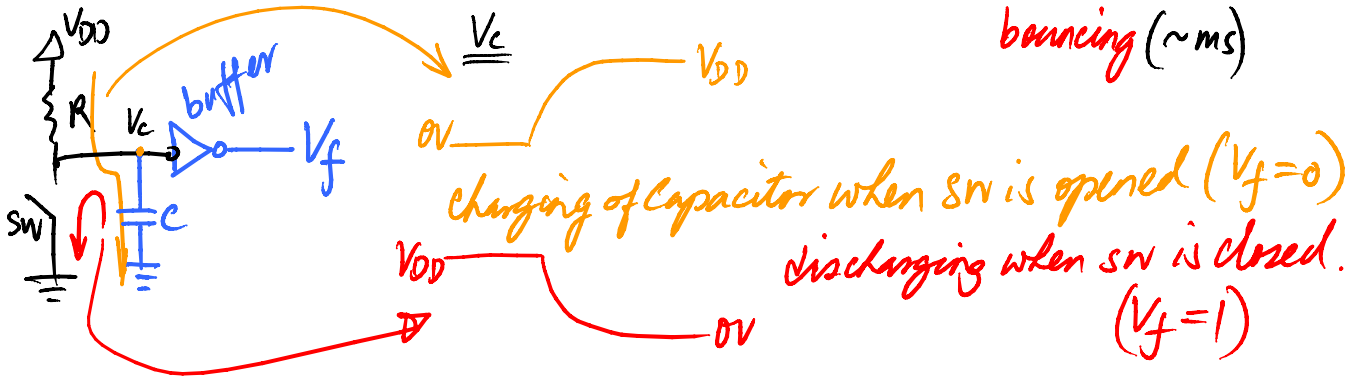


(assuming 20ns is long enough for the signal to settle on either "1" or "0")

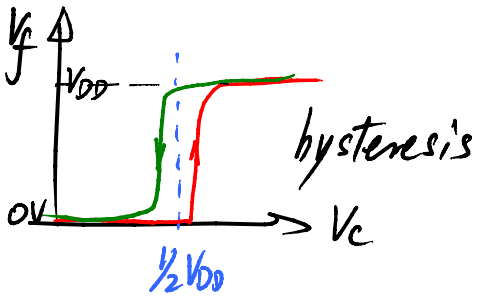
7.8.4 Switch debouncing

SW closing means $V_f = 0V$ (logic 0)
SW opening means $V_f = V_{DD}$ (logic 1)





buffer



- charging speed depends on RC value
- discharging quite fast because of low resistance of the closed SW

→ using FSM to wait out n ms