```verilog
 1    module part3(input [2:0]KEY, input [17:0]SW, output [2:0]LEDG, output [17:0]LEDR);
 2
 3        wire [2:0] s, U, V, W, X, Y, Z, M;
 4
 5        assign s = KEY;
 6        assign U = SW[2:0];
 7        assign V = SW[5:3];
 8        assign W = SW[8:6];
 9        assign X = SW[11:9];
10        assign Y = SW[14:12];
11        assign Z = SW[17:15];
12        assign LEDR = SW;
13        assign LEDG = M;
14
15        mux6to1 call1(s, U[0], V[0], W[0], X[0], Y[0], Z[0], M[0]);
16        mux6to1 call2(s, U[1], V[1], W[1], X[1], Y[1], Z[1], M[1]);
17        mux6to1 call3(s, U[2], V[2], W[2], X[2], Y[2], Z[2], M[2]);
18
19    endmodule
20
21    module mux6to1(input [2:0]s, input u, v, w, x, y, z, output m);
22
23        wire a, b, c, d;
24
25        mux2to1 inst1(u, v, s[0], a);
26        mux2to1 inst2(w, x, s[0], b);
27        mux2to1 inst3(a, b, s[1], c);
28        mux2to1 inst4(y, z, s[0], d);
29        mux2to1 inst5(c, d, s[2], m);
30
31    endmodule
32
33    module mux2to1(input x, y, s, output m);
34
35        assign m = (~s & x) | (s & y);
36
37    endmodule
```