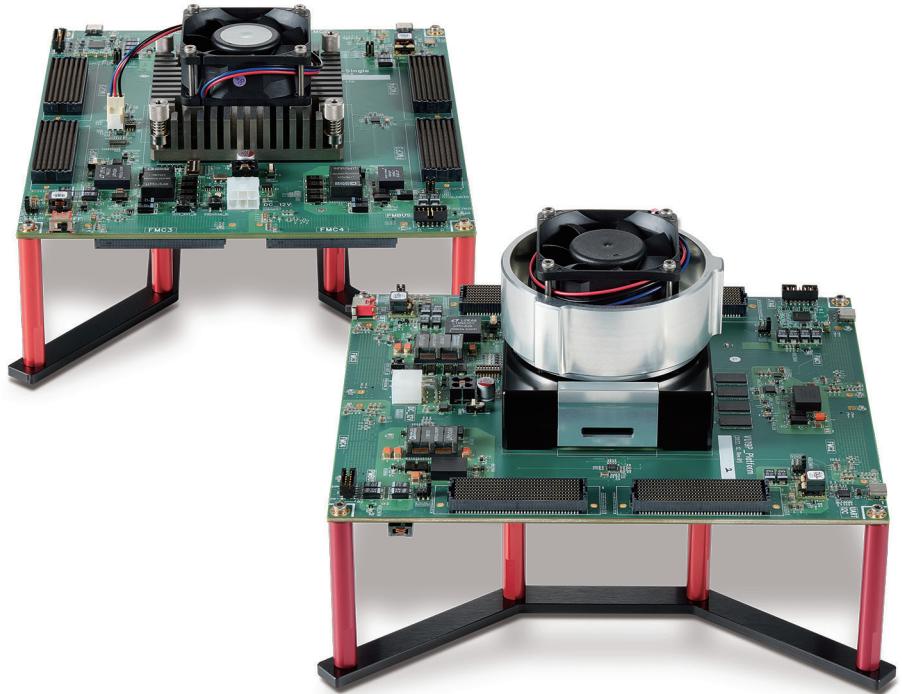


Leo19P-Single

XCVU19P Single FPGA Prototyping System



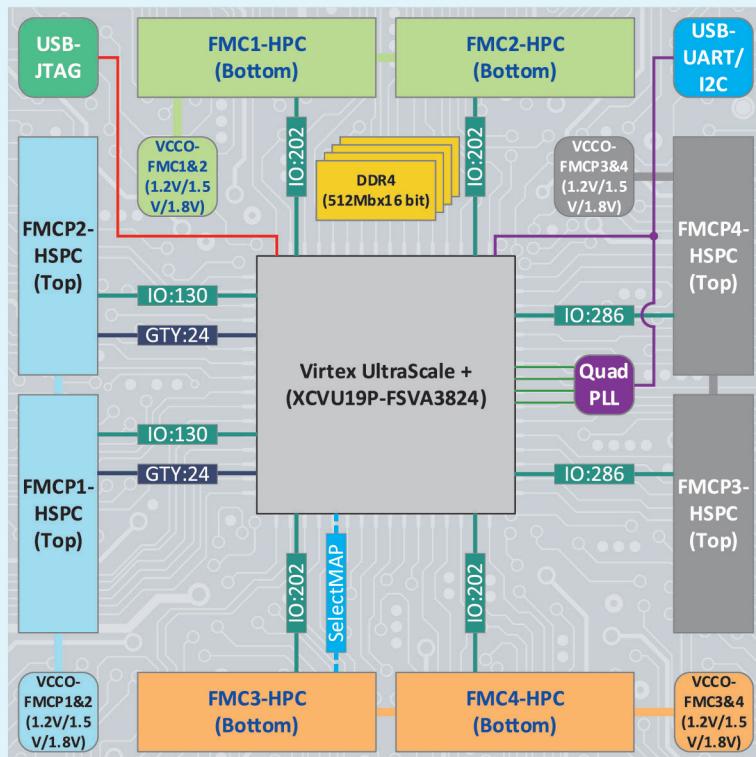
THE LEO19P-SINGLE SYSTEM uses Xilinx® Virtex® UltraScale+™ FPGA XCVU19P-FSVA3824 to support up to 48 million ASIC Gates and 1976(HP) / 96(HD) / 48(GTY) I/O, and 4 GB of DDR4 Component Built-in memory provides design convenience.

JTAG and CLOCK The Leo19P-Single system enables FPGA Configuration and Debugging through the built-in USB-type JTAG Module without the need for a separate JTAG Programmer, and also provides 4 types of basic clock sources for users and 4 separately programmable Design convenience is provided by adding a clock generator with an output.

EXPANDABILITY The Leo19P-Single system has a total of 8 SAMTEC Connectors from Xilinx's Evm. Board-compatible design makes it possible to utilize commercially available Daughter B'd, and in combination with Leo19P-DUO Base Board, it provides multi-FPGA solutions with two XCVU19P, enabling extended ASIC/SoC/AI/NPU/GPU Prototyping.

INDEPENDENT POWER SUPPLY The Leo19P-Single system secures the convenience of daughter board design by allowing the FPGA I/O power to be set through 4 user-configurable power supplies.

BLOCK DIAGRAM



SPECIFICATION

FPGA DEVICE

- Xilinx Virtex UltraScale+ XCVU19P-1FSVA3824 device (PCB Mount or Customized Socket)

MEMORY

- One 4GB DDR4 64-bit component memory interface (four [512 Mb x 16] devices each)

CLOCK(PLL)

- Si5335A quad clock generator
- Si570 I2C programmable LVDS clock generators
- 5P49V5901 quad clock generator

USER I/O

- 2 FMC+ HSPC connector with 24 GTY transceiver and 130 Differential I/O
- 2 FMC+ HSPC connector with 286 Differential I/O
- 4 FMC HPC connector with 202 Differential I/O

DEBUG PORT

- USB to Serial dual channel interface(UART/I2C)

POWER

- Four 1.2V/1.5V/1.8V selectable FPGA I/O power supply
- 12V 200Watts AC Adapter provided

XCVU19P-FSVA3824

- System Logic Cells: 8,937,600
- CLB Flip-Flops: 8,171,520
- CLB LUTs: 4,085,760
- Distributed RAM(Mb): 58.4
- Block RAM Blocks: 2,160
- Block RAM(Mb): 75.9
- UltraRAM Blocks: 320
- UltraRAM(Mb): 90.0
- CMTs(1MMCM & 2PLLs): 40
- HP I/O: 1,976
- HD I/O: 96
- DSP Slices: 3,840
- System Monitor: 4
- GTY Transceivers: 48
- Transceiver Fractional PLLs: 40
- PCIe4C(PCIe Gen3x16/Gen4x8/CCIX): 8

Leo19P-Duo

XCVU19P Duo FPGA Prototyping System



THE LEO19P-DUO SYSTEM uses two Xilinx® Virtex® UltraScale+™ FPGAs XCVU19P-FSVA3824 to support up to 96M ASIC Gates and 1,648(HP)/16(HD)/96(GTY) I/O and up to 8GB of DDR4 Component memory is provided.

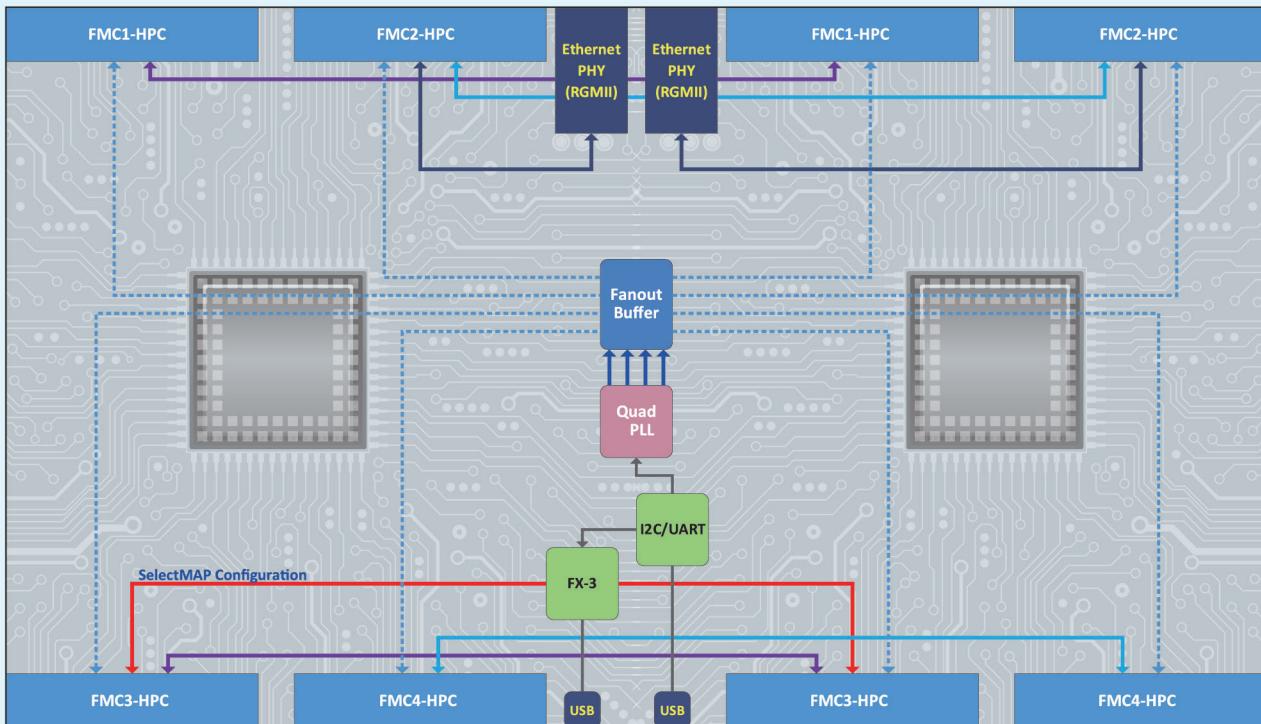
SELECTMAP CONFIGURATION The Leo19P-Duo system not only provides the multi-FPGA solution of the Leo19P-Single system, but also improves user convenience by supporting high-speed SelectMAP Configuration through USB 3.0 Interface and stand-alone SelectMAP Configuration through µ-SD.

INTERFACE The Leo19P-Duo system provides design convenience by adding a separate programmable 4-output clock generator, provides a Gigabit Ethernet PHY for each FPGA, and enables high-speed data communication through the FX3 USB 3.0 interface.

INTERCONNECTION The Leo19P-Duo system facilitates multi-FPGA design by providing a data interface between FPGAs through separate 726 (363pair) I/O interconnections.

STABLE POWER SUPPLY The Leo19P-Duo system has a built-in 750Watts Full Modular ATX Power case that provides sufficient power for system stability and the DUO Base system.

BLOCK DIAGRAM



SPECIFICATION

FPGA Configuration

- SelectMAP Configuration Mode support using FX3

CLOCK(PLL)

- 5P49V5901 quad clock generator

DATA CONNECTION BETWEEN FPGAS

- Over 380 differential I/O, HP-363pair, HD-16pair

ETHERNET

- Two Gigabit Ethernet PHY(RGMII, each FPGA)

DEBUG PORT

- USB to Serial dual channel interface(UART/I2C)
- Support USB3.0 high-speed data interface using FX3

POWER

- Built-in 750Watts Full Modular ATX Power Supply

CASE

- Full Aluminum Anodizing system Case

XCVU19P-FSVA3824

- System Logic Cells:8,937,600
- CLB Flip-Flops:8,171,520
- CLB LUTs:4,085,760
- Distributed RAM(Mb):58.4
- Block RAM Blocks:2,160
- Block RAM(Mb):75.9
- UltraRAM Blocks:320
- UltraRAM(Mb):90.0
- CMTs(1MMCM & 2PLLs):40
- HP I/O:1,976
- HD I/O:96
- DSP Slices:3,840
- System Monitor:4
- GTY Transceivers:48
- Transceiver Fractional PLLs:40
- PCIE4C(PCIE Gen3x16/Gen4x8/CCIX):8