National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Lab 04-1: Verdi
Assigned on Oct 7, 2021
Due day on Oct 14, 2021

Objective

In this lab, you will learn:

1. A simple CPU includes instruction set architecture, dataflow modeling and controller design.
2. Use Verdi to trace and debug legacy RTL codes.

Demo checklist:

- ☐ Show TA your simulation result of fixed CPU.

Environment Setup

Copy lab file packages from ee4292. Decompress the package and enter it. You can check the file list in Appendix.

```
$ cp ~ee4292/iclab2021/lab04.zip .
$ unzip lab04.zip
$ cd lab04/lab4_part1/
```

Note: please run simulation in the ***sim*** directory to maintain a fine data management.

Description

A simple but buggy CPU in RTL is provided in this lab. In these two weeks, we will adapt this CPU and add some functions. But first, you need to trace the legacy verilog code and to understand how the CPU is implemented. As introduced in class, tool *Verdi* can help you trace unfamiliar codes and debug, so finish the lab with Verdi and provided document CPU.

Action Items

I. Use Verdi to debug legacy codes.

1. Use nSchematic to observe the overall CPU.
2. There are some bugs in the CPU, use nWave or nSchematic and the provided testbench to fix these bugs. You will see "*Congradulation! All of the registers are correct.*" if all bugs are cleared.

Appendix

Directory	Filename	Description
sim	run.f	Simulation file list
sim	hdl.f	Pure HDL file list
sim	test_top.f	Test bench for this CPU
sim	golden_register.txt	true gpr state of CPU
sim	golden_register.pat	true gpr state of CPU(hex pattern)
sim	instruction.txt	CPU simulation pattern
source	top.v	Top module for this CPU
source	ID_stage.v	RTL for ID stage
source	controller.v	RTL for control signal
source	regfile.v	RTL for register file
source	ID_EXE.v	RTL for ID EXE flip flop
source	EXE_stage.v	RTL for EXE stage
source	alu.v	RTL for alu
source	CPU_define.v	Define file