National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Lab 11: APR Flow with IC Compiler (Powerplan and Placement)
Assigned on Nov. 25, 2021
Due day in Dec. 2, 2021

Objective

In this lab, you will learn how to use IC Compiler to perform a basic APR flow

Demo checklist:

- ☐ Powerplan result and corresponding IR Drop Map
- ☐ Timing report after placement
- ☐ Questions:
  What's the function of standard cell rails?

Action Items

I. Powerplan

1. In the *icc_run/*, invoke the GUI of ICC by:

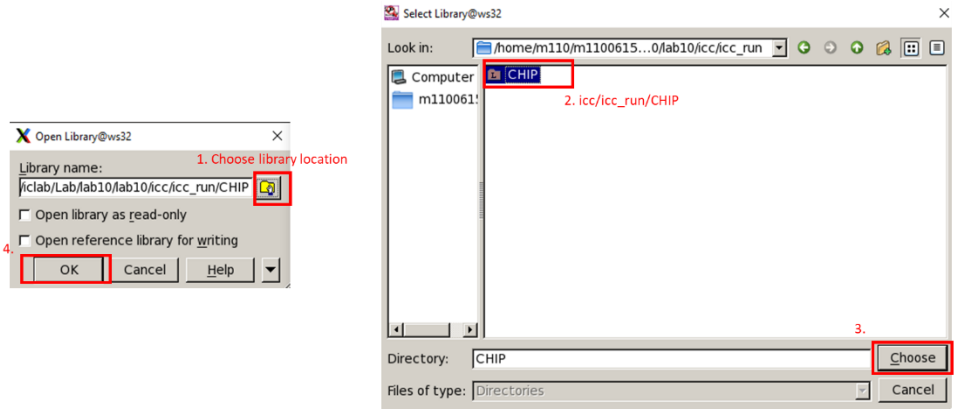
   $ icc_shell -64 -gui

   Set link library and target library:

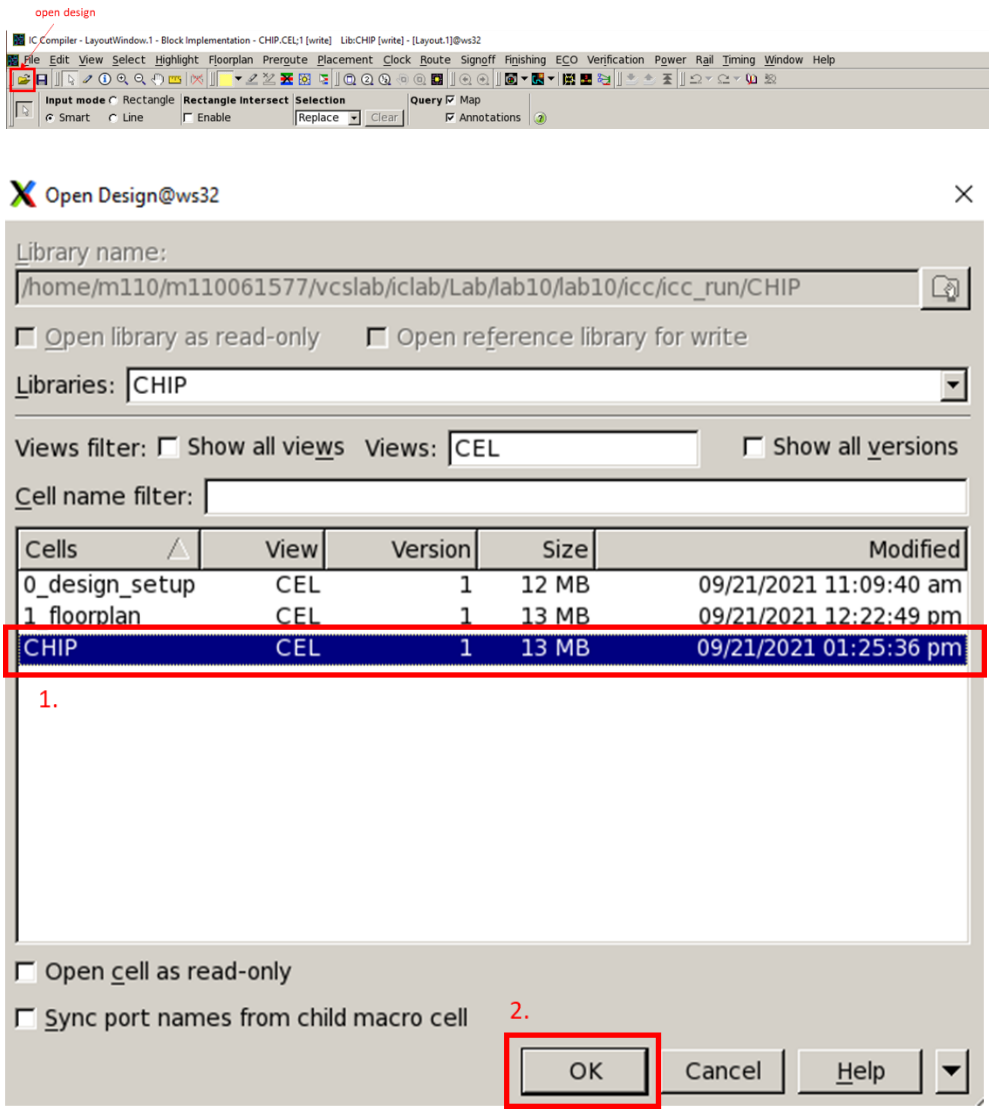
   $ source setup.tcl

2. Open the library and design from the previous step.

   "File->Open Library"



   Click open design icon, then choose open design "CHIP".

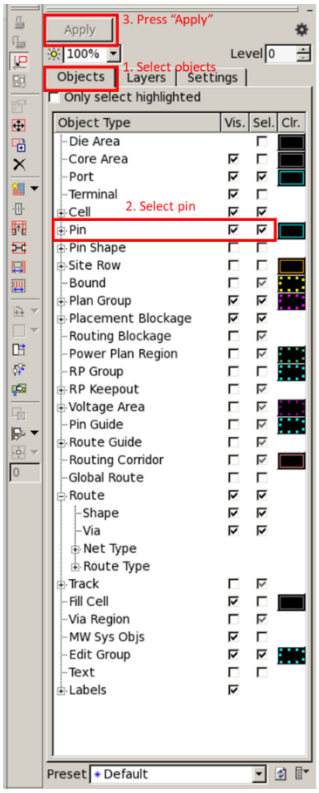


3. Execute the command. Since it has been reset to false when ICC is initialized.

```
$ set power_cg_auto_identify true
```

4. Check the metal directions.

   (1) At panel on the left-hand side. Objects ->turn on Pin ->press “Apply”



(2) Zoom in and you will find the pins (mostly **M1**) of standard cells appears.

Note: You can find the Metal 1 is used for standard cell rails (horizontal).

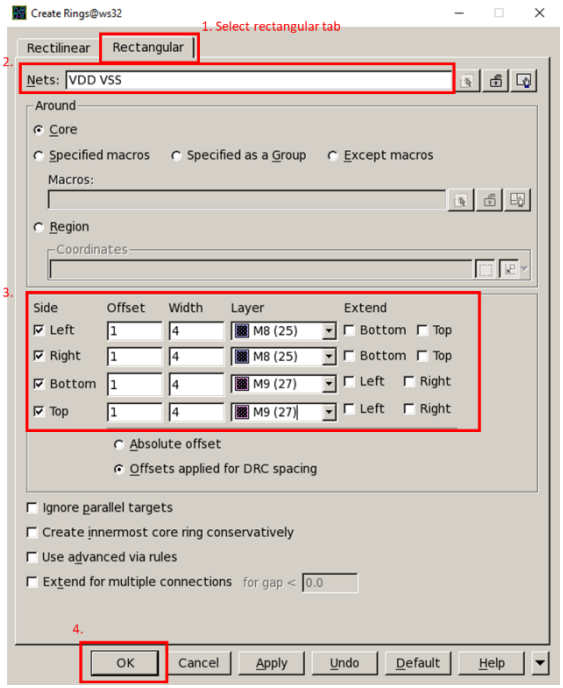
As mentioned in the lecture, standard cells are surrounded by **Power/Ground rail** segments on top and bottom. For routing complexity concern, the direction of each metal layer in the APR flow will follow the rail direction of the standard cells. In our case, we use **odd** layers (M1, M3, ..., M9) for **horizontal** metals and **even** layers (M2, M4, ..., M8) for **vertical** metals. Though this is not a strict rule, violating the metal direction will introduce routing difficulty (more routing resources are required).

Note: This rule will be applied in ring (Core/Macro) and power strap mesh

(3) Turn off "Pin" and click "Apply"

5. Create power rings.

"Preroute->Create Rings," choose **"Rectangular"** tab:



Note: M8 and M9 are used for core rings. Usually upper metal layers are thicker and conduct higher current density.

Note: The spacing is chosen based on **"DRC: Metal spacing rules"**

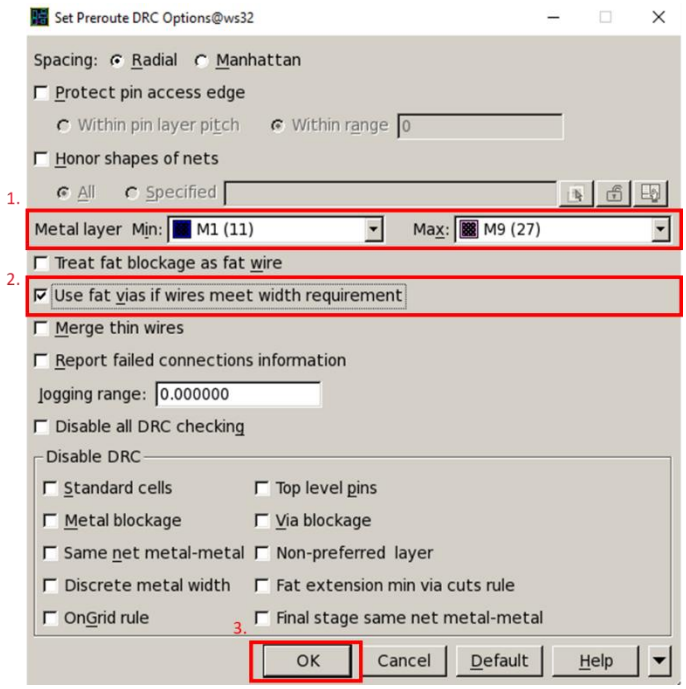
Note: The ring width is chosen based on the power consumption of the chip.

Note: Due to **"DRC: Metal width rules,"** ring width cannot be too large. In such case, you can use multiple pairs to provide enough power supply for your design.

Note: The "Core to xxx" space you set in floor plan should be wide enough for the setting here.

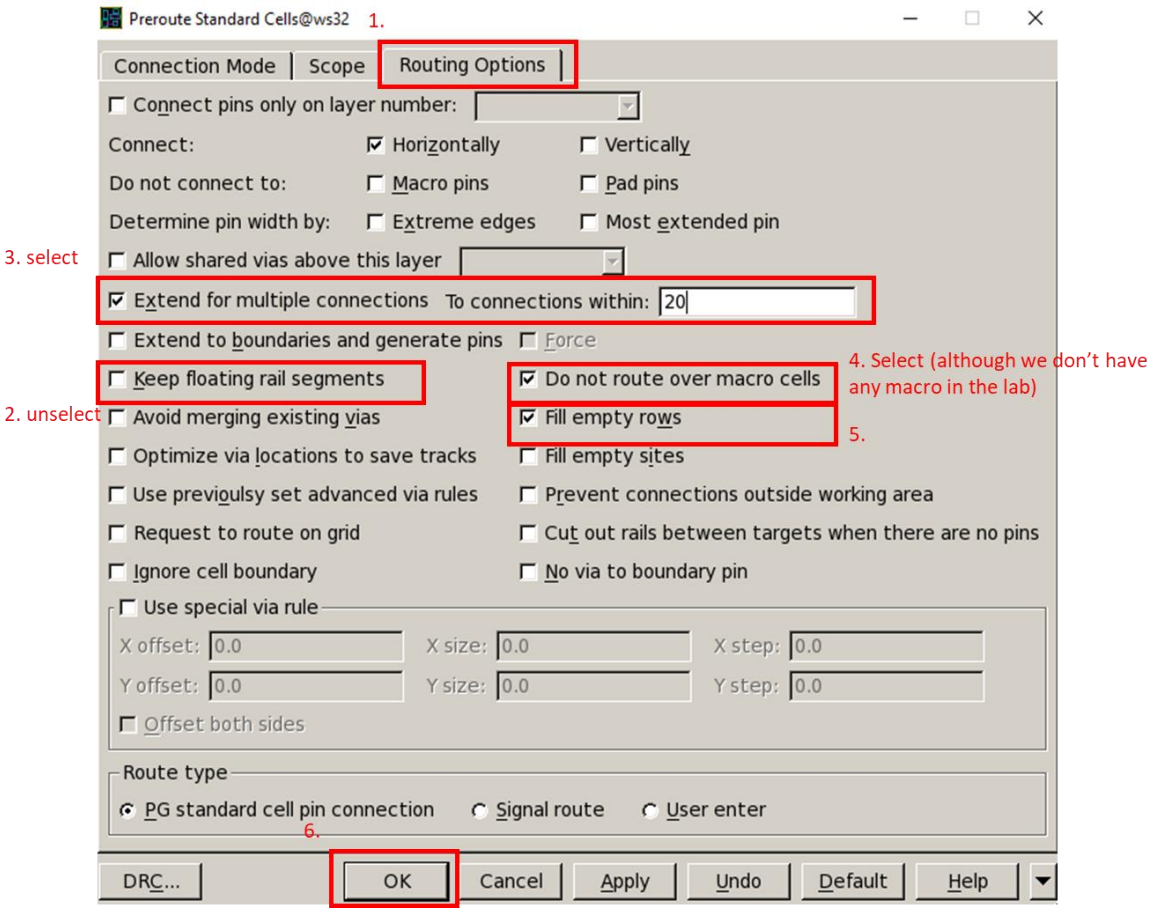
6. Before connecting power rails, we need to set preroute DRC options to prevent ICC using fat vias for connecting rails to power rings/straps, which will cause power rail connection fails.

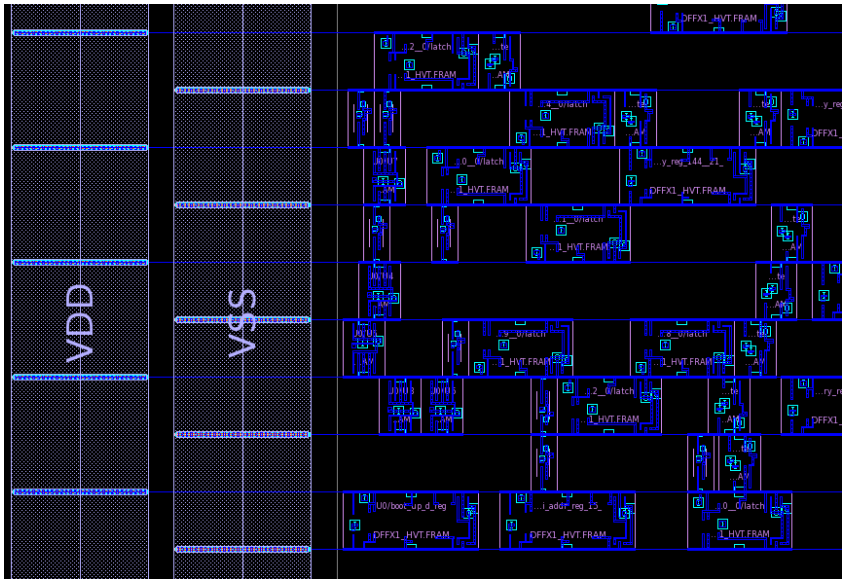
   "Preroute->Set Preroute DRC Options," choose **"Metal layer" with M1~M9**, and select **"Use fat vias if wires meet width requirement"**



7. Create standard cell power rails.

"Preroute->Preroute Standard Cells"

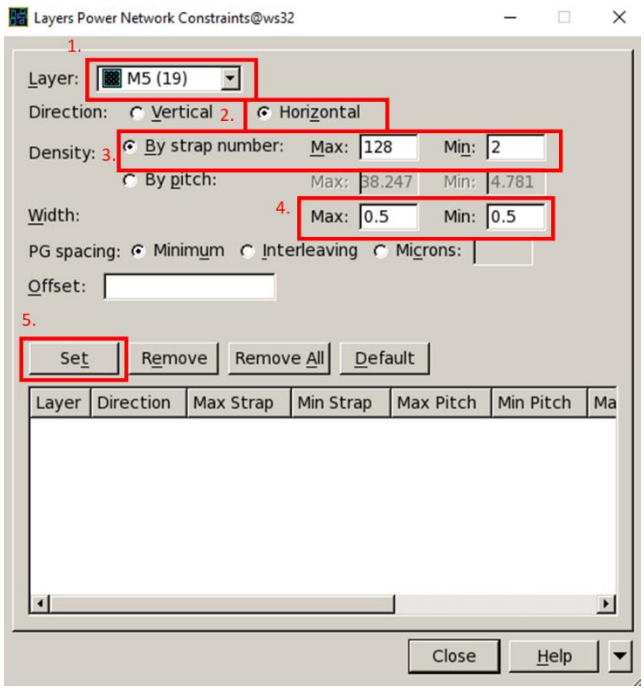


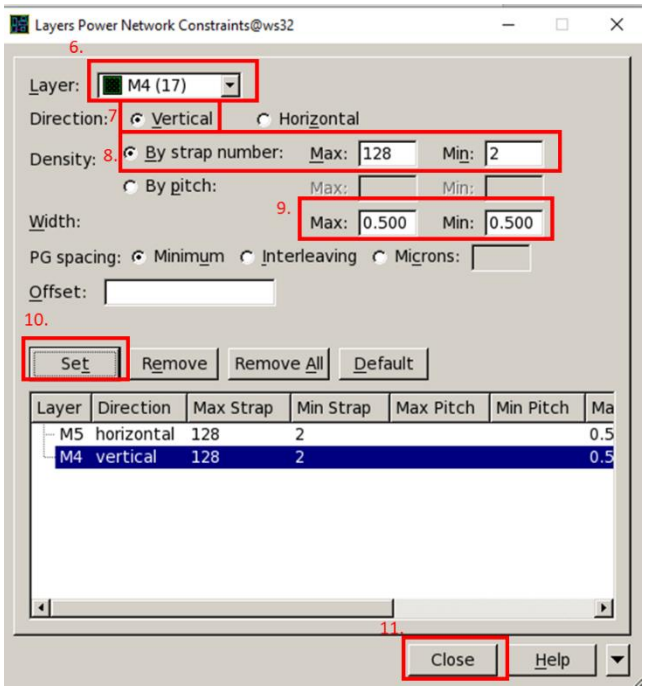


8. Use Power Network Synthesis in ICC to automatically generate power straps.
   Set Power Network Synthesis constraints:

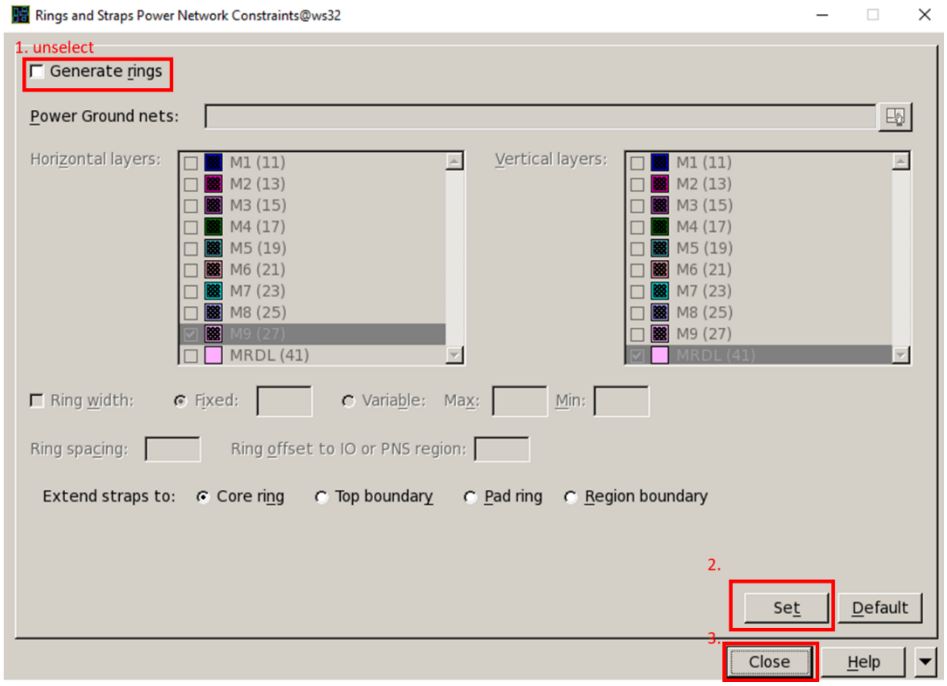
   (1) **"Preroute->Power Network Constraints->Strap Layers Constraints"**

   Note: Mesh-like power straps will be placed to provide near-isotropic power supply for cells. The number of strap are chosen by ICC based on the power consumption.





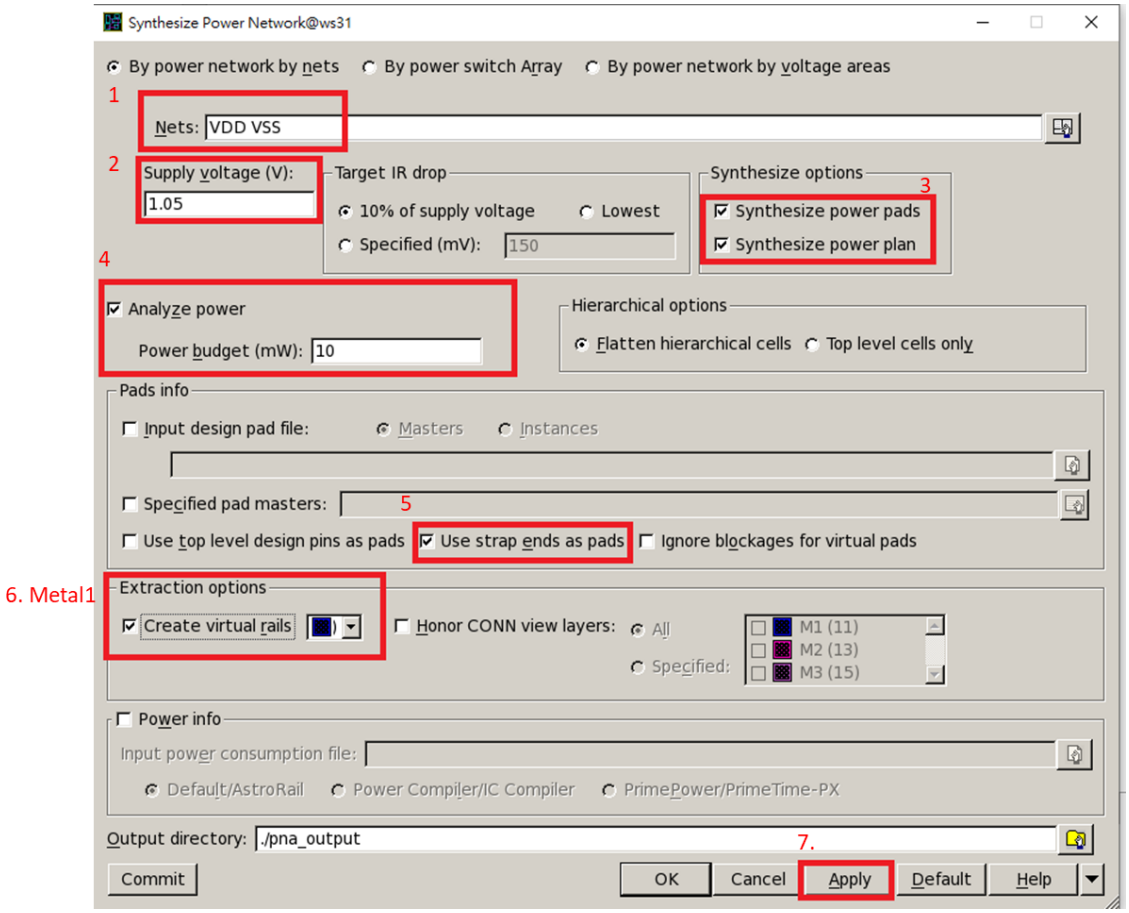
(2) **"Preroute->Power Network Constraints->Ring Constraints,"** and **unselect "Generate rings"** since we have created the power rings in the previous step.



9. Execute PNS.

"Preroute->Synthesize Power Network"

Item	Content
Synthesize Power Network by Nets	VDD VSS
Supply Voltage	1.05 (nominal operating voltage for this library)
Target IR Drop	10% of Supply Voltage
Synthesize Power Pads	Enable
Synthesize Power Plan	Enable
Analyze Power	Enable
Power budget (mW)	10
Use Strap Ends as Pads	Enable (since no real I/O pads used here, we need to identify the source of the current for calculating IR drop)
Extraction options->Create virtual rails	Enable (M1)



Click **"Apply"** to evaluate the PNS result. DO NOT close the window until we are satisfied with the IR drop results.

10. Evaluate the result. Type the following command in **icc_shell** terminal:

```
$ report_power
```

(1) Check the log in the Main Window to find the power analysis result:

Total power: _____(mW)

Total Dynamic power: _____(mW)

Cell Leakage power: _____(mW)

(2) Also check the IR drop result on terminal log messages:

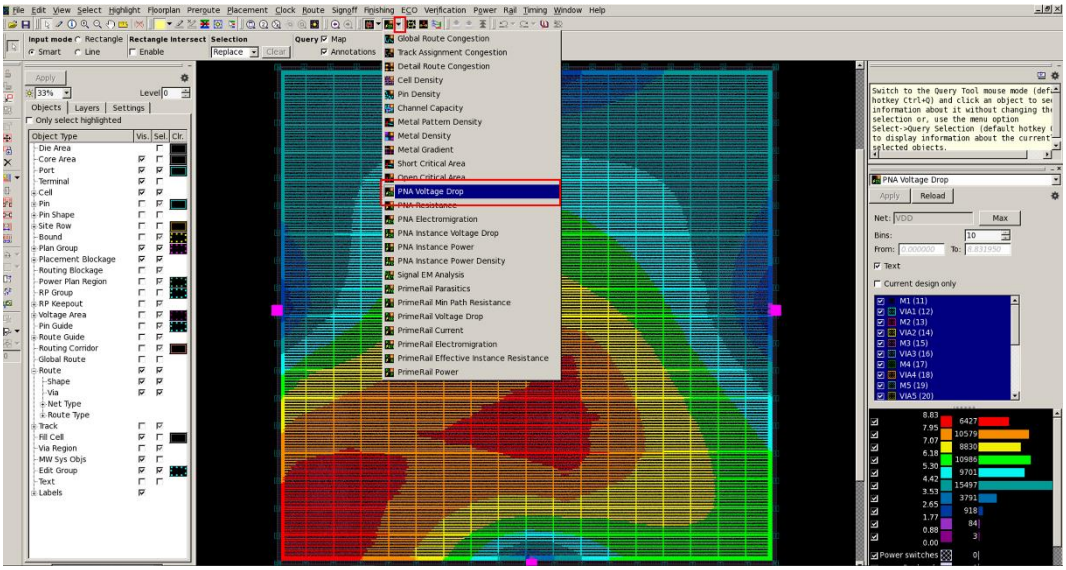
Total Current from Virtual Pads: _____mA

Maximum IR drop in 1_floorplan (or in CHIP): _____mV

Maximum current in 1_floorplan (or in CHIP): _____mA

```
Virtual Pad at (595.982 627.452) layer M4 Supplies     0.03 mA Current (0.31%)
Virtual Pad at (323.336 632.952) layer MRDL Supplies     0.02 mA Current (0.25%)
Total Current from Straps Ends:     0.00 mA (0.00%)
Total Current from Virtual Pads:     9.53 mA (100.00%)
Maximum IR drop in CHIP : 4.04 mV
Maximum current in CHIP : 0.360 mA
Maximum EM of wires in CHIP : 7.204641e+00 A/cm, layer M5
Maximum EM of vias in CHIP : 3.654911e+05 A/cm_square, layer VIA1
The PNS synthesizes the net VDD successfully
The maximum IR drop of the synthesized net VDD is   4.044 mV
Processing net VSS ...
Average power dissipation in CHIP :     10.00 mW
Power supply voltage :     1.05 V
Average current in CHIP :     9.52 mA
Performing Wire Cutting of net VSS for Honoring Blockage Constraints
Processing virtual rail for net VSS
Number of power pads reaching to the power ports of the leaf cells or blocks: 72
Total assigned virtual connection port current is 0.000000
Total assigned connected port current is 9.527406
Total assigned current is 9.527406
Total floating virtual connection port current is 0.000000
Total floating connected port current is 0.000000
```

(3) View the IR drop map in the Layout Window and the histogram on the right. Which region has the worst IR drop?



Note: On the left hand side is the IR drop distribution of the CHIP, and on

the right hand side is the histogram of IR drop.

Note: The IR drop can be turned on by clicking the **"PNA Voltage Drop,"** the icon under ECO.

11. Commit the PNS result.

Since the worst IR drop is much smaller than our target and the power ring can offer sufficient power for the core, we can accept this power plan by clicking the **"Commit"** button in the Synthesis Power Network Window and leave by clicking **"Cancel."** Then the power ring and strap will show in the Layout Window. **Do not click "OK," or ICC will crash.**

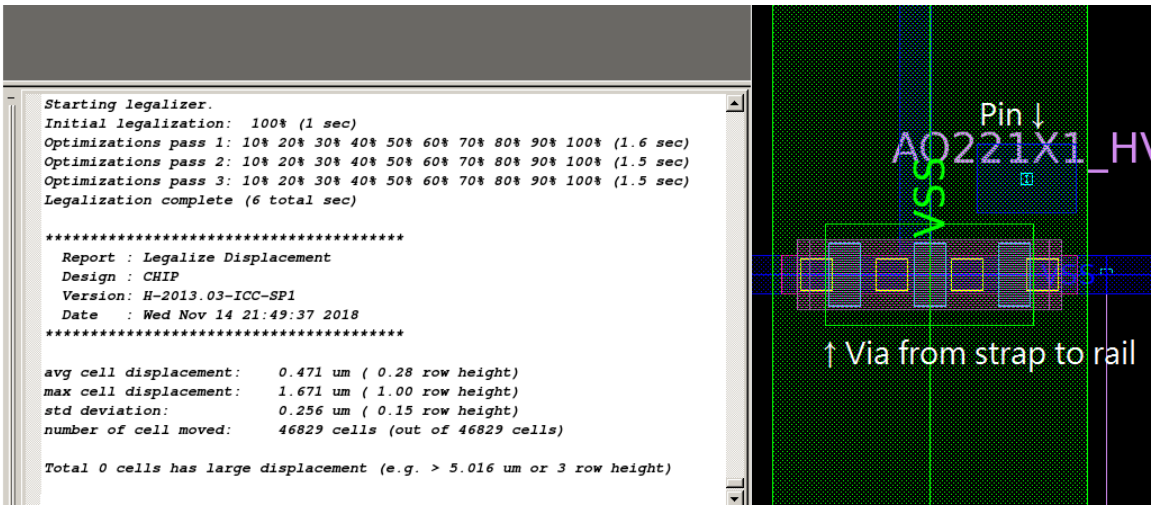
12. Move standard cells to avoid pins of the standard cells being placed under the straps (short or routing difficult).

Execute these two commands in the Command Line:

```
$ set_pnet_options -partial "M4 M5"
$ create_fp_placement -incremental all
```

Note: The report on the left hand side shows the statistics of the moved cells

Note: The layout on the right hand side shows that cells are moved to avoid shorting with power straps.



13. Save your design.

"File->Save Design" and click **"Save all."** Or you can save your design with command line interface.

```
$ save_mw_cel CHIP
```

14. Save your design as new file for backup.

    "File->Save Design" and check **"Show advanced options".**

Item	Content
Save as	Enable
Save as name	2_powerplan

    Or you can save your design with command line interface.

    $ save_mw_cel -as 2_powerplan

    Note: You may add power ring and straps manually by verifying the power density by yourself.

II. Placement

1. Check the power numbers of the current virtual flat placement by executing:

    $ report_power

    Total power: _____(mW)

    Total Dynamic power: _____(mW)

    Cell Leakage power: _____(mW)

2. Set Power Optimization Constraint by executing

    $ set_optimize_pre_cts_power_options

3. **(Optional)** Set separate process options for placement.

    Due to some network problems, placement will fail if ICC uses RPC (Remote Process Call) technique. We need to set separate process options for placement to "false" to prevent ICC using RPC to run placement optimization. Type the following command in **icc_shell** terminal:

    $ set_separate_process_options -placement false

4. Run full placement by executing:

    $ identify_clock_gating

    $ place_opt -power

5. Check the power numbers again to see the improvement **(mostly on dynamic power).**

$ report_power

Total power: _____(mW)

Total Dynamic power: _____(mW)

Cell Leakage power: _____(mW)

6. Check the timing report by executing:

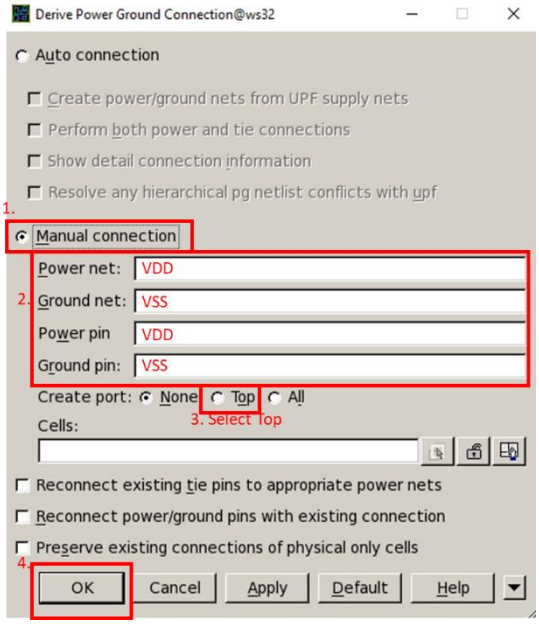
$ report_timing

Is the timing met in this phase? If not, many iterations of placement refinement should be executed.

7. Power/Ground connection.

"Preroute->Derive PG Connection" (in Layout window)

Item	**Content**
Manual connection	Selected
Power net	VDD
Ground net	VSS
Power pin	VDD
Ground pin	VSS
Create port	Top



Note: This step **needs to be re-executed** whenever power nets are modified or new cells are added.

8. Save your design.

   "File->Save Design" and click **"Save all."**

   Or you can save your design with command line interface.

   ```
   $ save_mw_cel CHIP
   ```

9. Save your design as new file for backup.

   "File->Save Design" and check **"Show advanced options."**

Item	Content
Save as	Enable
Save as name	3_placement

   Or you can save your design with command line interface.

   ```
   $ save_mw_cel -as 3_placement
   ```

10. Close ICC. (copy lab10)

    "File->Close Design," "File->Close Library," and then type **exit** in the icc_shell terminal **(make sure to close library before you leave)**

Appendix

Here is the file list of the lab package. Please check if anything missing!

Directory	Filename	Description
icc/icc_run	setup.tcl	Environment setup
icc/pre_layout/dc	top_pipe_syn.sdc	Synthesis SDC
icc/pre_layout/dc	top_pipe_syn.v	Synthesized
icc/pre_layout/design_data	add_tie.tcl	Tie cells insertion
icc/pre_layout/design_data	addCoreFiller.tcl	Core filler insertion
icc/pre_layout/design_data	CHIP_syn.f	Filelist for simulation
icc/pre_layout/design_data	CHIP_syn.sdc	SDC for ICC
icc/pre_layout/design_data	CHIP_syn_app.v	Netlist wrapper
icc/pre_layout/design_data	get_pnr_netlist.bat	Batch file for merging netlist
icc/pre_layout/design_data	io_pin.tdf	Pin Constraint
sim	instruction.txt	CPU simulation pattern
sim	presim.f	Filelist for pre-simulation
sim	test_top.v	Testbench for the CPU
sim	top.f	Filelist for the CPU

source	top.v	Top module for this CPU
source	top_pipe.v	Pipelined design for this CPU
source	ID_stage.v	RTL for ID stage
source	IF_stage.v	RTL for IF stage
source	controller.v	RTL for control signal
source	regfile.v	RTL for register file
source	ID_EXE.v	RTL for ID to EXE flip flop
source	EXE_stage.v	RTL for EXE stage
source	alu.v	RTL for alu module
source	CPU_define.v	Definition file
source	dsram.v	RTL for memory
source	PC.v	RTL for program counter
source	IF_ID.v	RTL for IF to ID flip flop
syn	.synopsys_dc.setup	DC setup file
syn	*.tcl	Synthesis scripts
syn	*.log	Log file
syn	run_dc.bat	Batch file for running synthesis
syn/report	*.out	Report files
syn/report	*.log	Log files
syn/netlist	top_pipe_syn.ddc	Netlist & constraints can be read by DC
syn/netlist	top_pipe_syn.saif	Switching activity interchange format (for power)
syn/netlist	top_pipe_syn.sdc	Synopsys design constrains format
syn/netlist	top_pipe_syn.sdf	Standard delay format
syn/netlist	top_pipe_syn.v	Netlist in verilog