National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Homework Assignment #3 **(5%)**
Logic Synthesis for Enigma
Assigned on Oct 21, 2021
Due by **Nov 04, 2021**

Assignment Description

Perform logic synthesis for the Enigma you designed in Homework #2. An RTL redesign to improve the performance is allowed and encouraged. Be sure that your RTL code can pass all the test pattern in Homework #2. The grading will be based on the following performance index:

A: Total area (shown in report/report_area_enigma.out, e.g. **Total area**: 10000)
T: Timing (your timing constraint, e.g. 3.0 for a nice implementation)

$$Performance\ index(PI) = A \times T\ (e.g.\ 3 \times 10^4\ for\ the\ above\ example)$$

For this problem, you need to complete the following missions:

1. Show the logic correctness and synthesizability functional module by delivering a functional module **enigma_part2.v** and its spyglass report **spyglass.rpt.** You will get 0% if failing to achieve this requirement.

2. Perform logic synthesis with the provided scripts. Only two script files can be modified: 0_readfile.tcl for adding your self-defined RTL files, and synthesis.tcl for changing the clock timing constraint TEST_CYCLE (e.g. 10 for 10 ns). Your timing slack should not be negative.

Grading policy

1. For this assignment, we have the following three grading ranks:
   The grading will be based on your performance index in enigma_part2:

   (Modified in v2)

   $$\begin{cases} Rank\ A\ (5\%)\colon & if\ PI \le 8.00 \times 10^4 \\ Rank\ B\ (3\%)\colon & if\ 1.33 \times 10^5 \ge PI > 8.00 \times 10^4 \\ Rank\ C\ (2\%)\colon & if\ PI > 1.33 \times 10^5 \end{cases}$$

2. **Bonus**. For Rank A works, **2%** will be given to **the best work** in terms of the performance index, and **1%** given to the second best.

   Notice: Late assignments will not be counted in the ranking!

3. A text file **misc.txt** summarizing your Rank, performance index and your A, and T as well.

Deliverable

Note: 1% punishment for wrong file delivery

File Organization

Directory	Filename	Description
HW3.1_10XXXXXXX/hdl/	enigma_part2.v (or others if any)	Enigma with rotorA & rotorB & rotorC & reflector
HW3.1_10XXXXXXX/hdl/	spyglass.rpt	Spyglass report
HW3.1_10XXXXXXX/syn/	0_readfile.tcl	Synthesis script
HW3.1_10XXXXXXX/syn/	synthesis.tcl	Synthesis script
HW3.1_10XXXXXXX/syn/	report_area_enigma.out	Area report
HW3.1_10XXXXXXX/syn/	report_time_enigma.out	Timing report
HW3.1_10XXXXXXX/	misc.txt	Your rank and performance