National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Lab 04-2: Finite State Machine (1%)
Assigned on Oct 7, 2021
Due day on Oct 14, 2021

Objective

In this lab, you will learn:

1. Design a **Moore Finite State Machine (FSM)** control unit.

Demo checklist:

- ☐ Show TA your state diagram of FSM.
- ☐ Show TA your simulation result of traffic light.

Environment Setup

Copy lab file packages from ee4292. Decompress the package and enter it. You can check the file list in Appendix.

```
$ cp ~ee4292/iclab2021/lab4.zip .
$ unzip lab4.zip
$ cd lab4/lab4_part2/
```

Note: please run simulation in the ***sim*** directory to maintain a fine data management.

Description

Traffic light is a road signal for directing vehicular traffic by means of colored lights, typically red for stop, green for go, and yellow for proceed with caution. Now consider a simple traffic light with only three light signals (red, green, and yellow) and the behavior of the traffic light depends only on its current light signal, and how long it stays (i.e. a Moore Machine).

The traffic light is originally idle before it receives the enable signal. Then it turns to red, and starts its circle. **It stays in red for 3 cycles ⇨ in green for 2 cycles ⇨ in yellow for 1 cycles ⇨ back to red and repeats**. **Note that no matter which state it stays, it will turn to idle when the enable signal or the reset signal is off.**

Action Items

I. FSM Design.

1. Design and draw a finite state machine and describe the behavior of traffic light. Please reference figure.1.

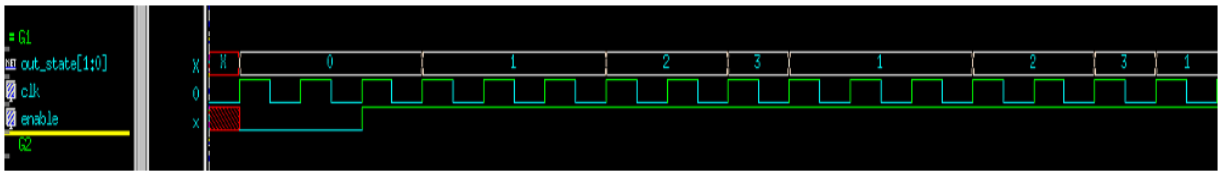

Figure 1. Waveform of FSM.

Note: Traffic light may need a counter to record the staying periods.

2. Write Verilog RTL code to construct the traffic light and verify the state of traffic light with provided testbench. The circuit should have one *clk* input, one *enable* input, one *rst_n* input, and one *state* output.
Note: You can start with *trafficlight.v*

Appendix

Directory	Filename	Description
hdl	trafficlight.v	Top module for traffic light
sim	run.f	Simulation file list
sim	tf_tb.v	Test bench for traffic light
sim	golden_state.pat	reference pattern