National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Homework Assignment #3.1 **(1%)**
Logic Synthesis for ROP3
Assigned on Oct 21, 2021
Due by **Nov 04, 2021**

Assignment Description

In HW1, you've implemented the ROP3 function using different methods. Now you are going to **synthesize** this design using ***Design Compiler*** and examine the synthesis result

I. Synthesize rop3_smart.v and rop3_lut256.v

Do logic synthesis on the verilog RTLs (rop3_smart.v and rop3_lut256.v) you implemented in homework 1. You can use the tcl-scripts you wrote in lab 6 to run the ***Design Compiler***. Remember that some settings should be changed (e.x. top design name, RTLs file name). Synthesize both your designs with clock period = 1.8ns for fair comparison and record the performance result under report/.

- **Important : Before synthesis, modify the default parameter setting from N=4 to N=32 in both files! (rop3_smart.v and rop3_lut256.v)**

II. Performance Comparison

Please compare the synthesis result of both designs, including timing, area and power, and summarize your observation in **README.txt**.

Deliverable

Directory	Filename	Description
HW3.1_10XXXXXXX/hdl/	rop3_smart.v	HW1 module
HW3.1_10XXXXXXX /hdl/	rop3_lut256.v	HW1 module
HW3.1_10XXXXXXX /hdl/	spyglass_smart.rpt	Spyglass report
HW3.1_10XXXXXXX /hdl/	spyglass_ lut256.rpt	Spyglass report
HW3.1_10XXXXXXX /report_smart/	report_area_smart.out	Area report
HW3.1_10XXXXXXX /report_smart/	report_time_smart.out	Timing report
HW3.1_10XXXXXXX /report_smart/	report_power_smart.out	Power report
HW3.1_10XXXXXXX /report_lut256/	report_area_lut256.out	Area report
HW3.1_10XXXXXXX /report_lut256/	report_time_lut256.out	Timing report
HW3.1_10XXXXXXX /report_lut256/	report_power_lut256.out	Power report
HW3.1_10XXXXXXX /	README.txt	Your discovery and summary