National Tsing Hua University
Department of Electrical Engineering
EE429200 IC Design Laboratory, Fall 2021

Lab 09-1: Conformal check with LEC

Assigned on Nov 11, 2021

Due day on Nov 18, 2021

Objective

In this lab, you will learn:

1. How to use Conformal LEC.

Demo checklist:

- ☐ Answer the questions in Action items.

Environment Setup

Copy lab file packages from ee4292. Decompress the package and enter it. You can check the file list in Appendix.

```
$ cp ~ ee4292/iclab2021/lab09.zip .
$ unzip lab09.zip
$ cd lab09_part1/
```

Note: please run simulation in the ***sim*** directory to maintain a fine data management.

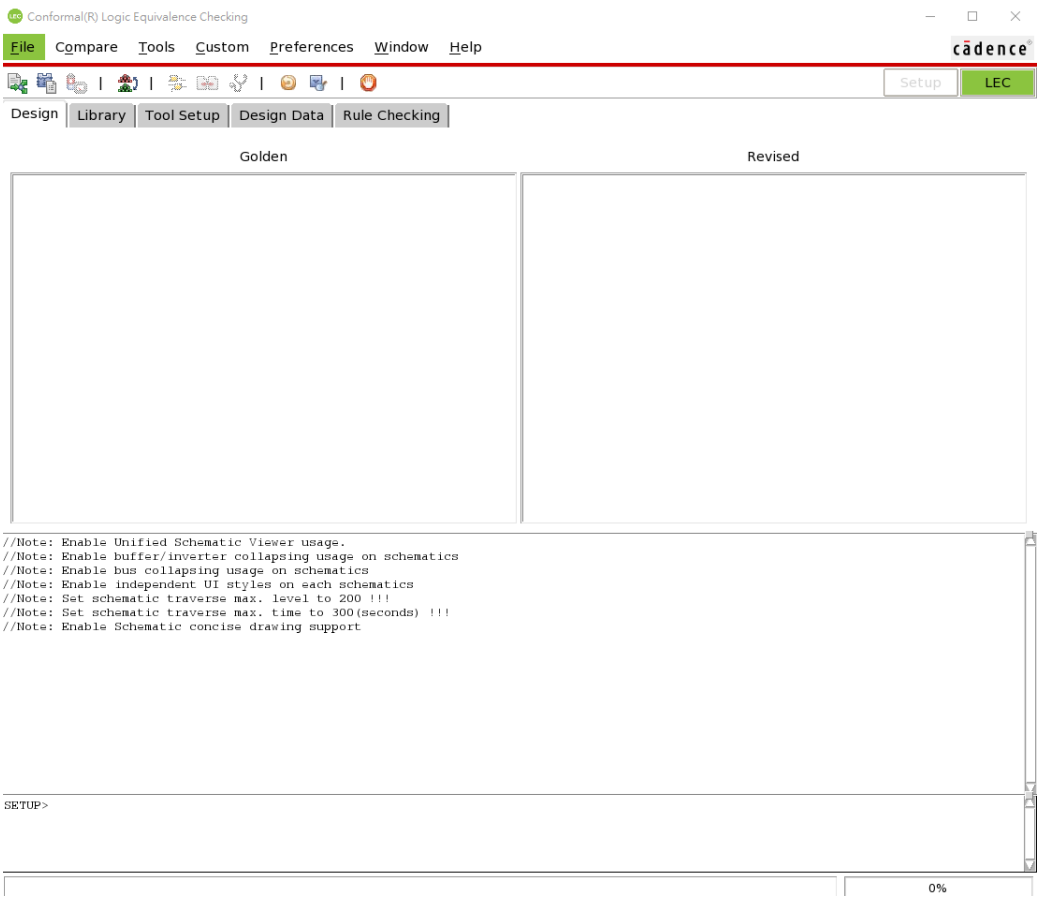
Description

In previous labs, we have synthesized our RTL design. However, we haven't checked the correctness of the synthesized result. Rather than directly do the gate-level simulation, we adopt the conformal tool LEC to check the logic equivalence between our RTL design and the synthesized netlist. Note that, we can also use the same tool to check the logic equivalence between synthesized netlist with P&R's result.

Action Items

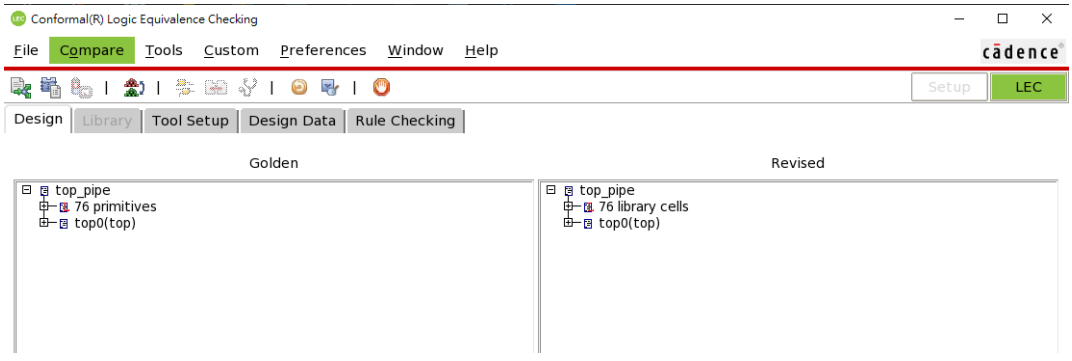
I. Flat Compare：

1. In the lec/, open the GUI of LEC(lec -xl -gui &)



2. **"File->Do dofile"** and choose **0_lec_setup_top_pipe.do** to set up the LEC environment, including setting **SRAM as black block**, setting **flatten models**, and read Verilog files.

   Read the script and understand what you are doing.



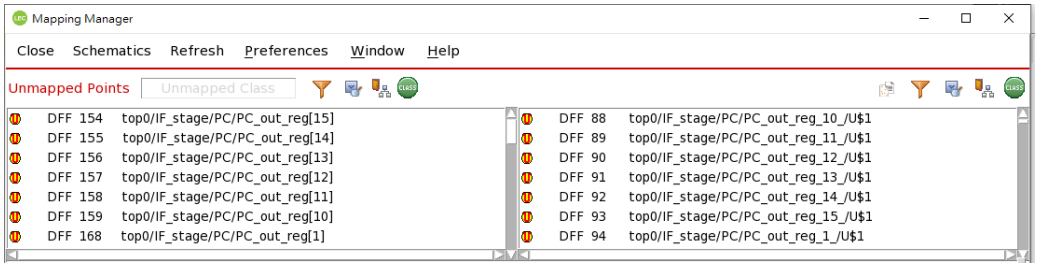
3. Click the LEC button (top right click) for changing to the LEC mode and mapping key points.

   Find out how many key points are mapped：

   PI：_____ ; PO：_____ ; DFF：_____ ; BBOX：_____ ; Total：_____.

4. There are 35 **unreachable(unmapped)** points in the RTL(Golden). Is this OK? Why? _____.

   [Hint：Investigate the problem using **"Tools > Mapping Manager"**.]



5. There are additional 1160 **unreachable points** for **DLAT**(latch) in the netlist(Revised). Why? _____

6. **"File->Do dofile"** and choose **0_lec_compare_top_pipe.do** for comparing the golden and revised circuits. Read the script and understand what you are doing.

   How many key points are compared and claimed **equivalent**? _____

7. **"File->Reset Design"** for resetting the LEC GUI.

II. Hierarchical Compare：

1. **"File->Do dofile"** and choose **0_lec_setup_top_pipe.do**.

2. **"File->Do dofile"** and choose **1_lec_hier_compare_top_pipe.do** for hierarchical comparison.

   How many modules are compared separately? _____

3. **LEC without GUI (optional)：**

   You can run LEC without GUI by executing the batch file(./run_lec.bat).

Appendix

Directory	Description
source/	RTL codes of CPU
sim/	Test bench for this CPU
netlist/	Synthesized CPU
lec/	Referenced LEC scripts