5.2. Single port SRAM

5.2.1. Basic pins

Basic pins of single port SRAMnxm_1rw are shown in Figure 5.7, and their descriptions are in Table 5.6.

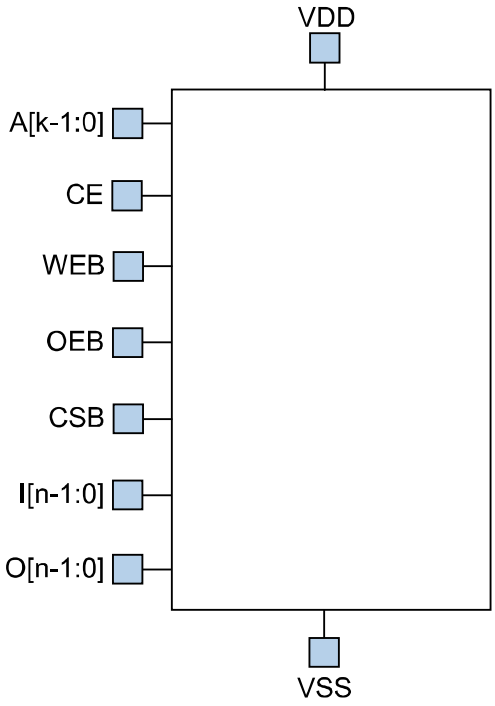

Figure 5.7. Single port SRAMnxm_1rw Basic Pins

Table 5.6. Single port SRAMnxm_1rw Pin Definition

Pin Symbol	Width(bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CE	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
VDD	Power supply		
VSS	Power ground		

5.2.2. Description

The general block-diagram of single port SRAMnxm_1rw is shown in Figure 5.8. and its basic operations are shown in Table 5.7.

Single port SRAMnxm_1rw access is synchronous and triggered by the rising edge of the clock signals (CE1). Read/Write addresses (A1), Input data (I1), Write enable signals (WEB1), and Chip select signals (CSB1) are latched by the rising edge of the clocks (CE).

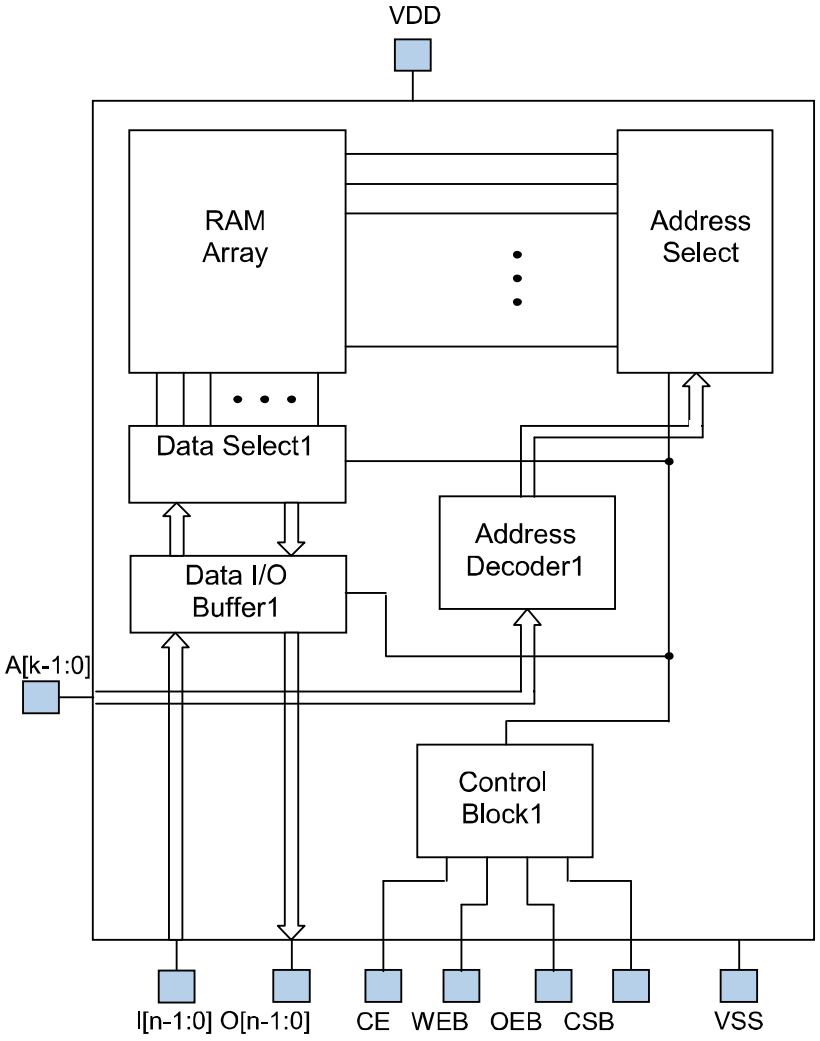

Figure 5.8. Single port SRAMnxm_1rw block diagram

The value of Chip Select signal is low (CS=0) for read/write operation. The single port SRAMnxm_1rw enter read mode when CS=0 and WEB=1. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Single port SRAMnxm_1rw enter write mode when CSB=0 and WEB=0. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].

If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continue. When OEB=0, the data appear on the output bus O[n-a:0].

Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Table 5.7. Single port SRAMnxm_1rw Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A[k-1:0]	WEB	OEB	CSB	I[n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)		
X	X	0	1	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I[n-1:0]	I[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A[k-1:0]) (t)	D(A[k-1:0]) (t)	No	Read
		1			Z			

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.
O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

Address contention will occur when both ports simultaneously access the same address. In this case, both ports will read the same data.
The list of expressions to be used in this section and their meanings is presented in Table 5.7.

5.2.3. Timing Waveforms

Single port SRAMnxm_1rw functions according to the block-diagrams shown in Figures 5.9. – 5.11.

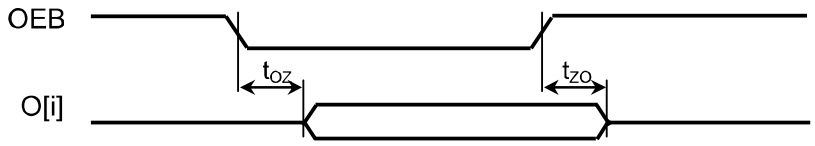

Figure 5.9. Single port SRAMnxm_1rw Output-Enable Timing Waveforms

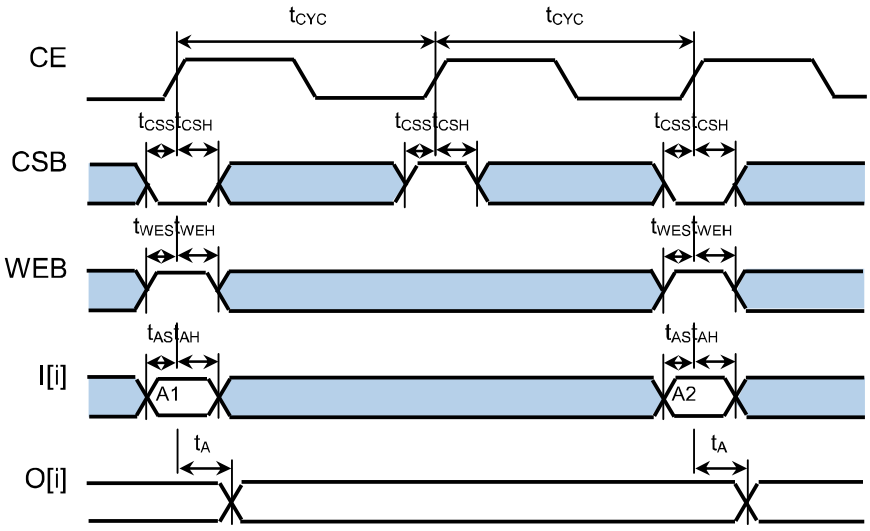

Figure 5.10. Single port SRAMnxm_1rw Read-Cycle Timing Waveforms

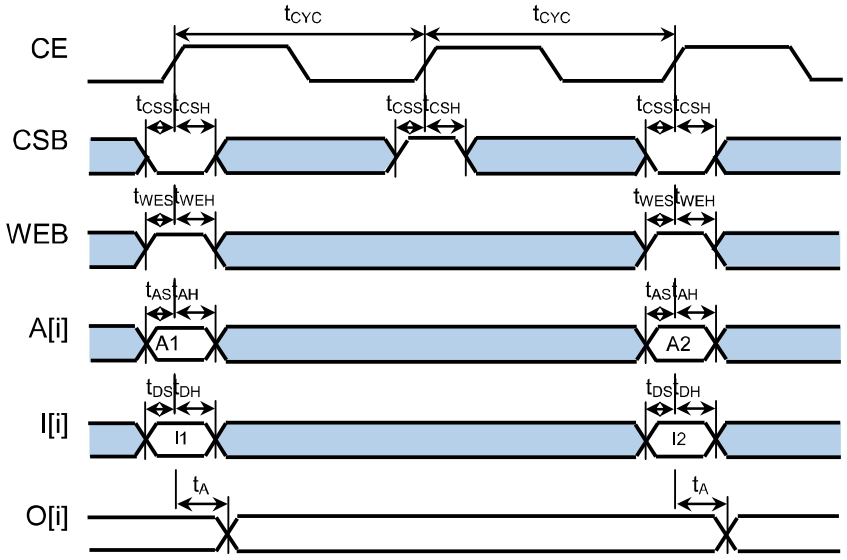

Figure 5.11. Single port SRAMnxm_1rw Write-Cycle Timing Waveforms