SPI_BASIC

REVISION HISTORY

Revision Number	Date	Description of Change	Author
V0.0	8/12/2022	Draft version	Shaoqiang
V0.1	9/21/2022	Add SPI_RDY	Shaoqiang
V1.0	10/09/2022	Change to design SPEC	Shaoqiang

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SPI_BASIC

Introduction

SPI (Serial Peripheral Interface) is a synchronous communication protocol, which is always a slave device to the host. The main function is to allow communication between the host and daisy chain. Communication between the host and the device via SCK, CSB, MOSI, MISO and SPI_RDY pins.

Main features

The SPI module has the following features:

- •Support full duplex (HWR007_SPI_BASIC)
- • Internal SOF detection based on CSB falling edge (HWR001_SPI_BASIC)
- • Bit captured on low to high clock transitions and propagated on high to low clock transition (HWR002_SPI_BASIC)
- •For each byte at SPI interface, MSB transmitted first (HWR002_SPI_BASIC)
- •In command frame, MISO will remain "1" (HWR002_SPI_BASIC)
- •Take over the daisy chain communication (except tone communication) of either south or north (HWR002_SPI_BASIC)
- •Extract rx_data[8:0] into RX FIFO from A2D_SPI_SCLK and A2D_SPI_MOSI, MSB is SOF bit (HWR001_SPI_BASIC)
- •Propagate frame in TX FIFO on A2D_SPI_SCLK and D2A_SPI_MISO(HWR005_SPI_BASIC)
- • Internal communication clear pattern detection, reset TX FIFO and RX FIFO when COMM_CLEAR is detected (HWR001_SPI_BASIC)
- •Transmit next RX FIFO data and SPI_SOF bit when COPY_NXT is detected (HWR005_SPI_BASIC)
- •Internal 60us timer start to count by entering response frame or receiving tx_data[7:0] (HWR007_SPI_BASIC)
- •Additional SPI_RDY interface to inform the host that it can be written or read (HWR009_SPI_BASIC)
- •Internal FIFO overflow and underflow fault detection
- •The SCLK frequency of SPI interface support 2-6MHz (TR096)
- •Transmit FIFO depth is 4 bytes*2

•Receive FIFO depth is8 bytes

Functional Details

Block Diagram

The SPI allows communication between host and daisy chain. In the command frame, the command sent by the host is stored in the Receive FIFO (RX FIFO) after being received by the RX shift register, and then sent to the daisy chain. Response frame of daisy chain will be stored in the Transmit FIFO (TX FIFO) and then sent to the MISO via the TX shift register.

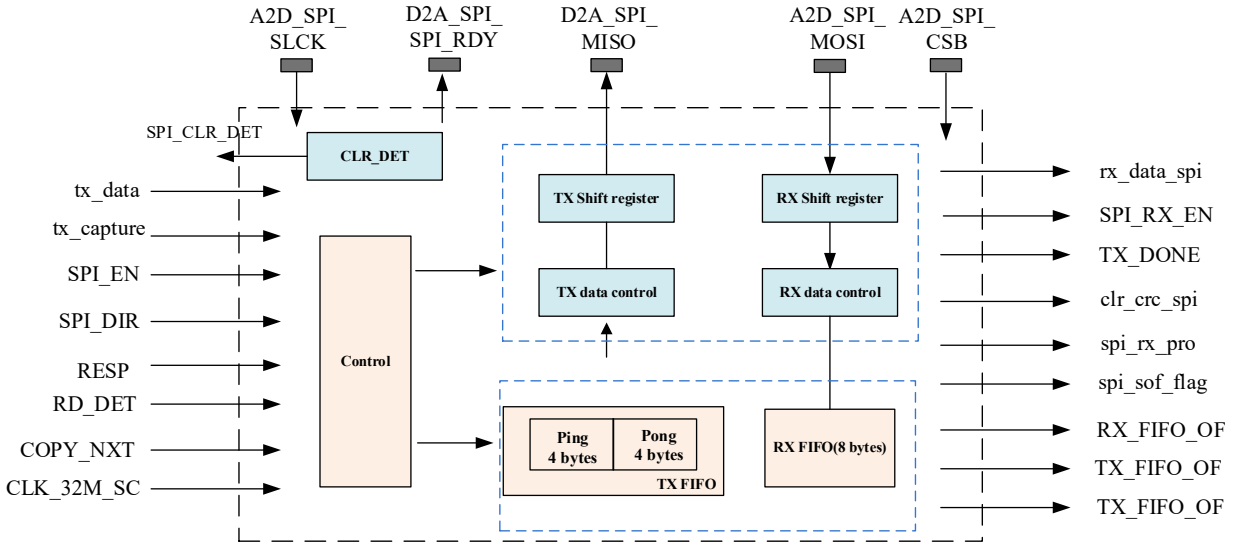

Fig 1SPI block diagram

I/O description

Table 1 SPI I/O description

Pin Name	Direction	Width	Duration	Description
A2D_SPI_SCLK	I	1'b	N/A	Clock input
A2D_SPI_MOSI	I	1'b	N/A	Master output slave input, MSB first
A2D_SPI_CSB	I	1'b	N/A	Chip selection input
COPY_NXT	I	1'b	N/A	SPI to send next data to COMM_CTRL
RD_DET	I	1'b	N/A	D2A_SPI_SPI_RDY (h -> l), indicate is read command
SPI_RESP	I	1'b	N/A	RESP =1, indicate is maser read state RESP = 0 , indicate is master write state
tx_data	I	8'b	N/A	Dasiy chain input data, store to TX FIFO
tx_capture	I	1'b	N/A	Tx_data enable
SPI_EN	I	1'b	N/A	Enable SPI
SPI_DIR	I	1'b	N/A	"1" for north interface, "0" for south interface
D2A_TX_EN_N	I	1'b	N/A	North interface enable
D2A_TX_EN_S	I	1'b	N/A	South interface enable
CLK_32M_SC	I	1'b	N/A	System clock
CLK_SLOW_SC	I	1'b	N/A	Used to count RX timeout
resetb_CLK	I	1'b	N/A	Power on reset of CLK_32M_SC
CLK_REG_SC	I	1'b	N/A	8M clock

CLK_REG	I	1'b	N/A	8M timer
resetb_SR_CLK	I	1'b	N/A	Reset signal for CLK_32M_SC
D2A_SPI_SPI_RDY	O	1'b	N/A	Indicate slave can be read or write by master
D2A_SPI_MISO	O	1'b	N/A	Master input slave output, MSB first
rx_data_spi	O	9'b	> CLK_REG_SC	Read from RX_FIFO，MSB is SOF(if MSB is 1)，SOF(1bit)+ DATA(8bit)
SPI_RX_EN	O	1'b	1 CLK_REG_SC	Indicate RX_DATA_SPI is update
SPI_CLR_DET	O	1'b	1 CLK_REG_SC	CLR_DET module detect COMM_CLEAR command after detect falling edge and then receive 8'h00
TX_FIFO_OF	O	1'b	1 CLK_REG_SC	TX FIFO overflow, when TX FIFO is full and daisy chain still write to TX FIFO
RX_FIFO_OF	O	1'b	1 CLK_REG_SC	RXFIFO overflow, when RXFIFO is full and host still write to RXFIFO
TX_FIFO_UF	O	1'b	1 CLK_REG_SC	TXFIFO underflow, when FIFO is empty and read from FIFO
clr_crc_spi	O	1'b	1 CLK_REG_SC	In RX state when the falling edge of A2D_SPI_CSB
spi_rx_pro	O	1'b	1 CLK_REG_SC	Indicate SPI is In RX State
TX_DONE	O	1'b	1 CLK_REG_SC	All TX FIFOis empty and timeout

State Machine

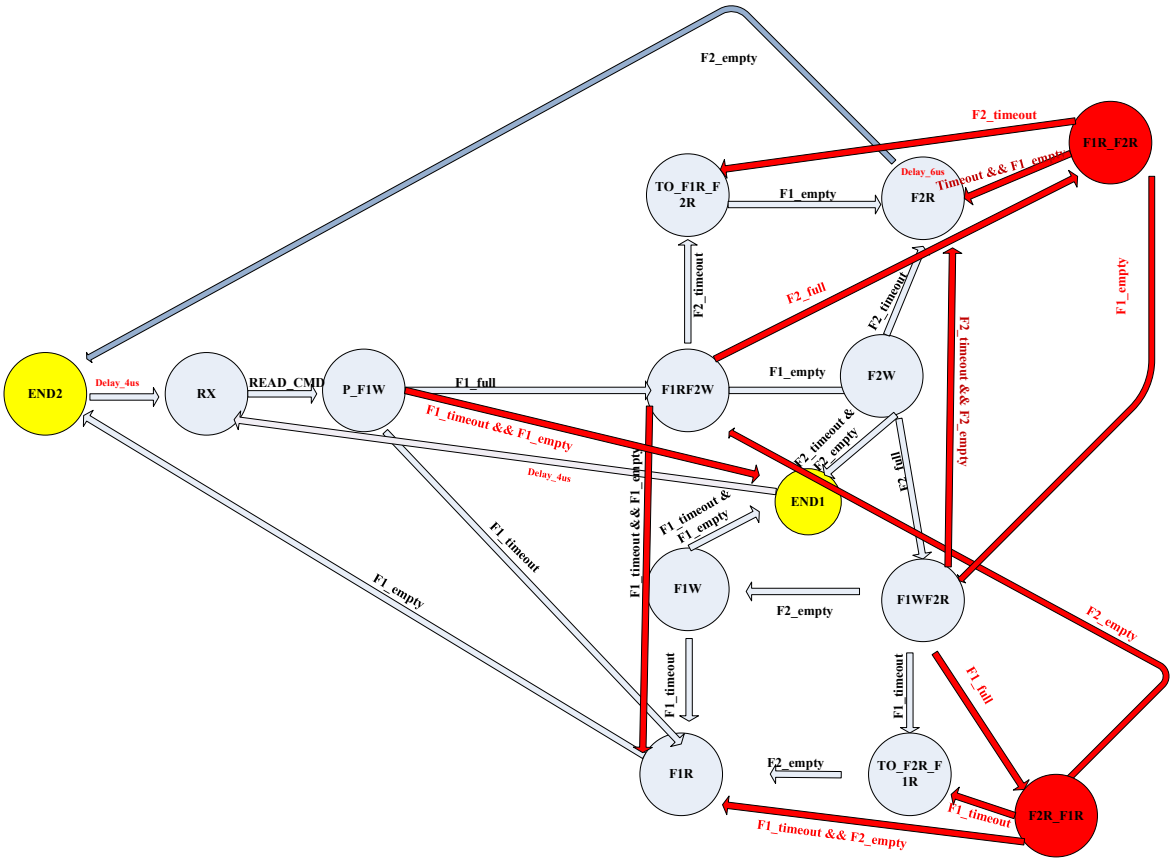

Fig 2 State machine of SPI_BASIC

The state machine of SPI_BASIC has 14 states in total. The following describes the meaning of these states:

•RX: Receive command state

•P_F1W: Enter the write TX FIFO1 state from the RX state

•F1RR2W: Read TX FIFO1 and write TX FIFO2

•TO_F1R_F2R: TX FIFO1 is not empty while TX FIFO2 is timeout

•F2R: Read TX FIFO2 only

•F1R_F2R: TX FIFO1 is not empty while TX FIFO2 is full

•F2W: Write TX FIFO2 only

•F1W: Write TX FIFO1 only

•F1WF2R: Read TX FIFO2 and write TX FIFO1

•TO_F2R_F1R: TX FIFO2 is not empty while TX FIFO1 is timeout

•F1R: Read TX FIFO1 only

•F2R_F1R: TX FIFO1 is not empty while TX FIFO2 is full

•END1: F1W/P_F1W state but TX FIFO1 empty & TX FIFO1 timeout or enter F2W state but TX FIFO2 empty & TX FIFO2 timeout

•END2: F1R state and FIFO1 is empty or F2R state and FIFO2 is empty

Internal SOF detection

(HWR001_SPI_BASIC)

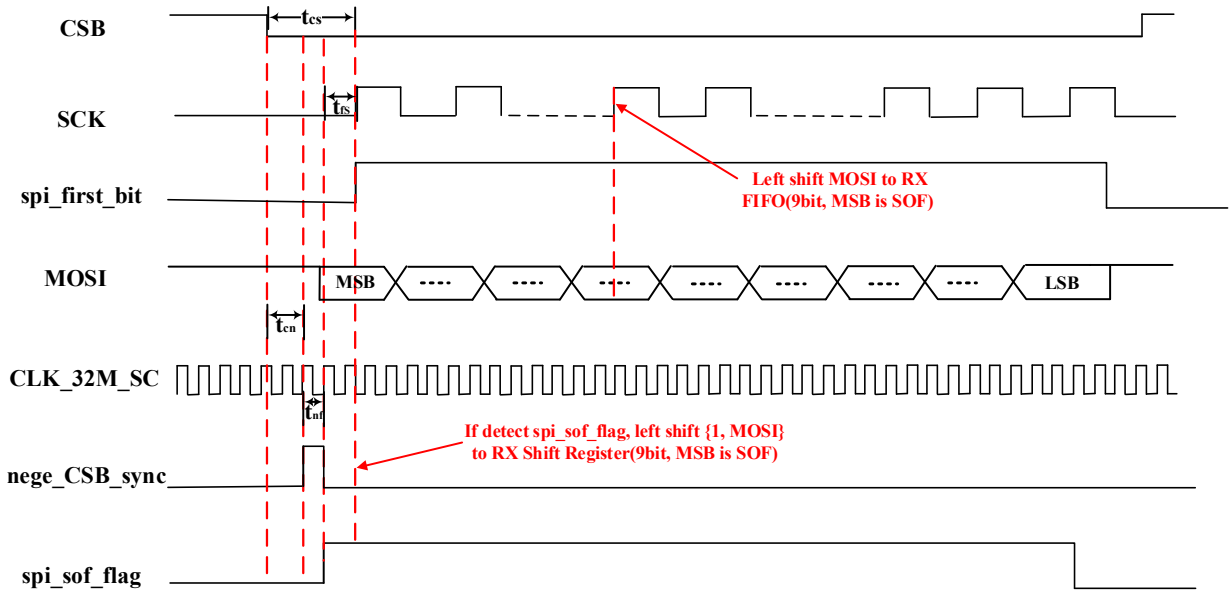

Fig 3 Schematic diagram of internal SOF detection

The calculation formula of t_{cs} is as follows:

$$t_{cs} = t_{cn} + t_{nf} + t_{fs}$$

t_{cn} is the time between the falling edge of CSB and the rising edge of CSB_sync obtained by internal synchronization, with a minimum of 2 CLK_32M_SC. The next clock cycle produces spi_sof_flag, t_{nf} =1

CLK_32M_SC. To ensure spi_sof_flag stably sampled on the SCK rising edge, t_{fs}> 1 CLK_32M_SC is required, so t_{cs}>4 CLK_32M_SC(125ns) is obtained. To broaden the time, t_{cs}>= 200ns.

The RX shift register and RX FIFO have a storage unit of 9bit, bit[8] stores the SOF flag, and bit[7:0] is one byte of data received. At each SCLK rising edge, the MOSI is shifted left from the lowest position into the shift register. When the first bit(MSB) of each byte detects spi_sof_flag, it shifts {1, MOSI} left into the shift register.For other non-MSB bits, only the MOSI is shifted.

SPI Communication Formats

(HWR007_SPI_BASIC, HWR005_SPI_BASIC, HWR002_SPI_BASIC)

Although the SPI interface supports full duplex, since the daisy chain only supports half duplex, it is actually half duplex. It means that only command frame or response frame is transmitted between the MCU and the device at a given time. During master reading mode, MOSI is ignored by the device. SPI will capture data on low to high clock transitions and propagate on high to low clock transition. For each byte at SPI interface, MSB transmitted first. The communication timing diagram is shown in Figure 4.

Command Frame

When command is sent from the MCU to the device, the MISO will remain 1. In command frame, the interval between the falling edge of CSB and the first rising edge of the SCK (t_{cs}) must be greater than 200ns.Pulling CSB high during the transmission of a command frame is not allowed, if this is done, the frame command will be considered an invalid command.

Response Frame

In response frame, the host must send 8 SCK clock cycles when it detects that SPI_RDY is 1, otherwise it may receive an incomplete response frame. MISO is wrong when SPI_RDY is low. If host sends SCK when SPI_RDY is low, SPI_BASIC will generate a TX_FIFO_OF error.

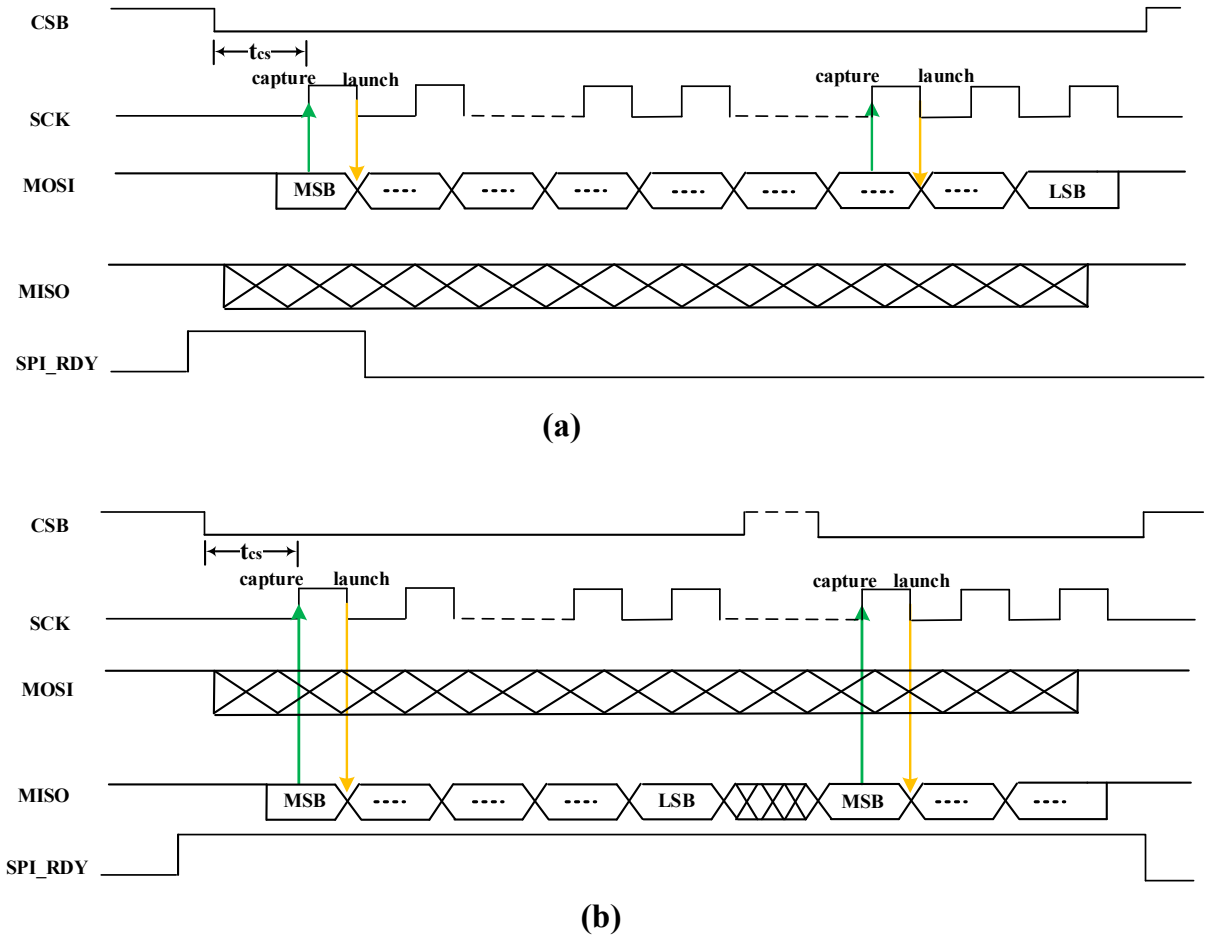

Fig 4SPI communication timing diagram of (a) command frame, and (b) response frame.

TX timeout timer

(HWR002_SPI_BASIC, HWR007_SPI_BASIC)

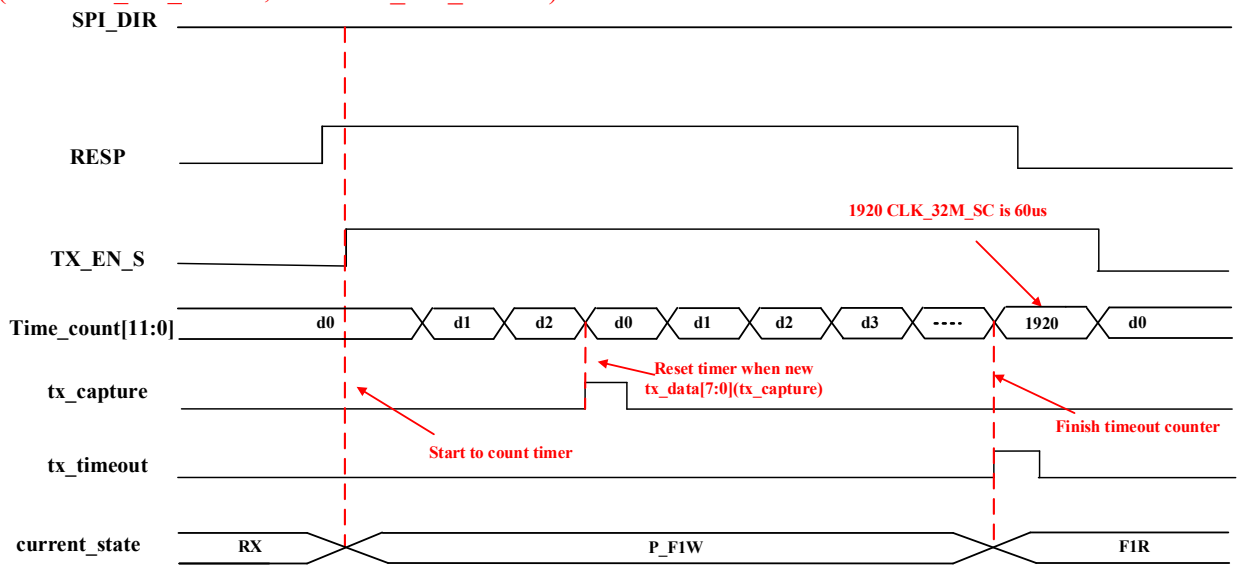

Fig 5 The timing diagram of TX timeout timer

The condition for SPI_BASIC to enter TX from RX is:

TX_state = SPI_EN & (SPI_DIR ? TX_EN_N : TX_EN_S) & RESP

When SPI_EN is 1 and RESP is 1, SPI_ DIR is required. If SPI_DIR is 0, SPI receives data from the south port of the daisy chain. When TX_EN_S is 1, SPI enters TX. In contrast, if SPI_DIR is 1, SPI receives data from the north port of the daisy chain. When TX_EN_N is 1, SPI enters TX.

The counter starts counting at the beginning of entering TX. When a new tx_data [7:0] is received the counter will restart counting. When the counter reaches 1920, the timeout flag will be generated and exit the write TX FIFO mode.

COMM_CLEAR Command

The COMM_CLEAR command is defined as: eight consecutive bits of 0 are detected after the falling edge of the CSB as shown in Fig 3. COMM_CLEAR command will be detected during the entire process when CSB is low, if detected, will reset TX and RX FIFO. After receiving the COMM_CLEAR command, the SPI immediately enters the receive command mode, which means that the host must send a new command but cannot receive the response frame at this time.

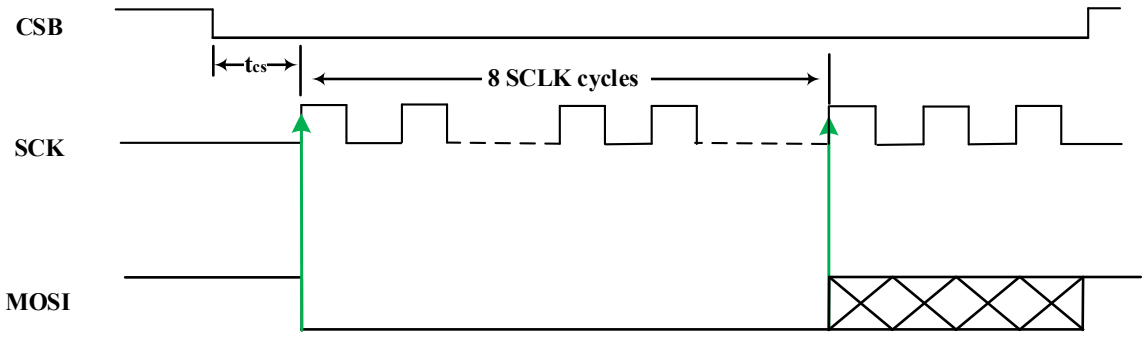

Fig 6 SPI COMM_CLEAR command

SPI_RDY Behavior

(HWR010_SPI_BASIC, HWR011_SPI_BASIC)

SPI_RDY is required because the depth of the TX FIFO is limited. Data overflow occurs if the host requests more than 256 bytes and the host does not service (read data) the device in time. SPI_RDY indicates to the host that a certain amount of data is ready to be read or written.

In the command frame, when the data in the RX FIFO is no more than2 bytes, SPI_RDY will become high. When the data in the RX FIFO is greater than 4 bytes, SPI_RDY will become low.When the SPI

receives the COMM_CLEAR command, it will enter the receive command mode, and SPI_RDY will become high regardless of the previous state.

In the response frame, SPI will receive the data sent by the daisy chain. When TX FIFO (ping or pong FIFO)is full or the TX timeout timer is expired (TX timeout is defined as no response from the daisy chain within 60us in response frame), SPI_RDY will be pulled high, indicating that host can read the response frame stored by the SPI.SPI_RDY will continue be high until the current FIFO is empty.Note that if another TX FIFO is full before the current FIFO is empty, TX_FIFO_OF error will be generated when daisy chain sends new data.When the TX FIFOs are all empty, the SPI will automatically enter the receive command mode and SPI_RDY will become high after 6us.The behavior of SPI_RDY is summarized in Table 1.

Note:

When SPI_RDY is low, it lasts at least 2us before it becomes high.

Table1. SPI_RDY Behavior Summary

	HIGH -> LOW	LOW -> HIGH
Host write	RX FIFO has >4 bytes	RX FIFO has <=2 bytes
Host read	Device receive first byte of read command	Ping or Pong FIFO is full
	Ping or Pong FIFO being read becomes empty(the last byte in the FIFO is read)	TX FIFO time out happened
		TX FIFO timeout and TX FIFO are all read empty, after 6us

Error Detection

(HWR009_SPI_BASIC)

SPI_BASIC will detect three kinds of errors. Errors include the following:

RX_FIFO_OF: in command frame, when RX FIFO is full but host still writes data to SPI_BASIC. lpspi_rx_full && lpspi_end_byte

TX_FIFO_OF: in response frame, host did not read the data from the TX FIFO in time, when the TX FIFOs are all full but the daisy chain still writes data to SPI_BASIC.

(lpspi_tx_full && lpspi_tx_full2 && tx_capture) ||

((current_state == F2R_F1R || current_state == F1RF2R) && tx_capture)

TX_FIFO_UF: in response frame, hostsends SCK clocks when SPI_RDY is low.

(~D2A_SPI_SPI_RDY)&& (current_state != RX) && pose_SCLK