RSTGEN IP SPEC

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Introduction

The RSTGEN module is used to generate reset signals for other digital modules.

Feature

Output reset signals include hardware reset, hardware and software reset. Both reset signals are scan-muxed by SCAN_MODE.

Functional Details

Block Diagram

The following diagram shows the main inputs and outputs of RSTGEN.

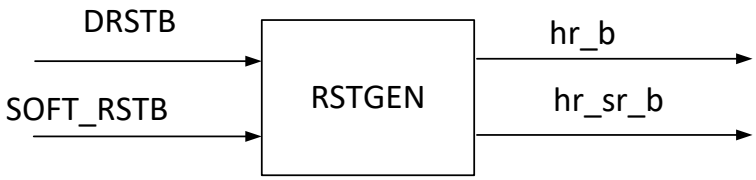

Figure1 RSTGEN diagram

Module input/output list

Name	Dir	Width	Discirption	duration
resetb_CLK_256K	O	1	Scan-muxed resetb for CLK_256K domain	level
resetb_CLK_OUT	O	1	Scan_muxed resetb for CLK_OUT domain	level
resetb_SR_CLK_OUT	O	1	Scan_muxed resetb and soft resetb for CLK_OUT domain	level
resetb_SR_CLK_SLOW	O	1	Scan_muxed resetb and soft resetb for CLK_SLOW domain	level
resetb_CLK	O	1	Scan_muxed resetb for CLK_32M domain	level
resetb_SR_CLK_I2C	O	1	Scan_muxed resetb and soft resetb for CLK_I2C domain	level
rstb_32M_OK	O	1		
rstb_32M_ok_and_sr	O	1	CLK_32M_OK high and SOFT_RSTB high	level(CLK_32M domain)
SOFT_RSTB_32M	O	1	SOFT_RSTB_REG synchronized to CLK_32M domain	level
resetb_32M_no_sc	O	1	Resetb for CLK_32M domain(no scan-mux)	level
SCAN_MODE	I	1	DFT scan mode	
SCAN_RSTB	I	1	DFT scan resetb	
CLK_32M	I	1	Main clock from analog	
CLK_256K_SC	I	1	Scan_muxed CLK_256K	
DRSTB	I	1	Async digital reset	
CLK_OUT_SC	I	1	Scan_muxed CLK_OUT	

CLK_SLOW_SC	I	1	Scan_muxed CLK_SLOW	
SOFT_RSTB_REG	I	1	SOFT_RSTB register bit	
SOFT_RSTB	I	1	SOFT_RSTB in CLK_SLOW domain	
CLK_32M_ORG_SC	I	1	Scan_muxed original CLK_32M	
CLK_32M_SC	I	1	Scan_muxed CLK_32M	
I2C_MAS_EN	I	1	I2C master enable register bit	
CLK_32M_OK	I	1	CLK_32M status from analog	Level(async)

Clock Definition

The following table describes clocks defined in Figure 1 block diagram and other sections of this document.

Clock Name	Definition
resetb_CLK_256K	CLK_256 domain
resetb_CLK_OUT	CLK_OUT domain
resetb_SR_CLK_OUT	CLK_OUT domain
resetb_SR_CLK_SLOW	CLK_SLOW domain
resetb_CLK	CLK_32M domain
resetb_SR_CLK_I2C	CLK_32M domain
rstb_32M_ok_and_sr	CLK_32M domain
SOFT_RSTB_32M	CLK_32M domain
resetb_32M_no_sc	CLK_32M domain

Table1 clock definitions

RSTGEN function description

For different sub-modules, reset signals are generated for corresponding clock domain.
Hr_b change to 0 synchronously when DRSTB low and released synchronously when DRSTB high. Hr_b is a group of reset signals, include resetb_CLK, resetb_CLK_OUT and resetb_CLK_SLOW. (HWR001_RSTGEN)

Hr_sr_b change to 0 synchronously when DRSTB low, change to 0 synchronously when SOFT_RSTB_REG low, released synchronously when DRSTB and SOFT_RSTB_REG high. Hr_sr_b is a group of reset signals, include resetb_SR_CLK_OUT, resetb_SR_CLK_SLOW and resetb_SR_CLK_I2C. (HWR002_RSTGEN, HWR003_RSTGEN)

All signals in hr_b and hr_sr_b are scan-muxed. When SCAN_MODE high, they all connected to SCAN_RSTB. (HWR004_RSTGEN)