CKGEN IP SPEC

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Introduction

The CKGEN module is used to generate clocks for digital part of the chip.

Feature

Consist of CKGEN1 and CKGEN2.
Sub-module CKGEN1 generates clocks for normal logic.
Sub-module CKGEN2 generates clocks for safety requirements.

Functional Details

Block Diagram

The following diagram shows the main inputs and outputs of CKGEN.

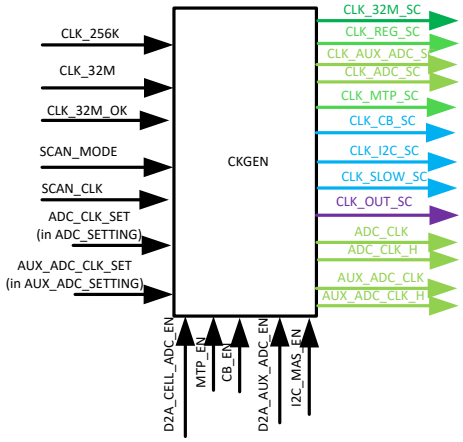

Figure1 CKGEN diagram

Module input/output list

Name	Dir	Width	Discirption	duration
CLK_256K_SC	O	1	Scan-muxed CLK_256K	1.952us(50% duty)
CLK_32M_SC	O	1	Scan_muxed CLK_32M	15.625ns
CLK_32M_EN	O	1	Real gate for CLK_32M	Level(CLK_32M domain)
CLK_32M_ORG_SC	O	1	Scan_muxed original CLK_32M	15.625ns
CLK_OUT_SC	O	1	Scan_muxed CLK_OUT	15.625ns or 1.952us
CLK_8M_256K_SC	O	1	Scan_muxed CLK_8M_256K	15.625ns or 62.5ns
CLK_REG_SC	O	1	Scan_muxed CLK_REG	62.5ns
CLK_REG	O	1	8MHz divided from CLK_32M	62.5ns
pulse_2M	O	1	2MHz pulse divided from CLK_32M	125ns
pulse_1M	O	1	1MHz pulse divided from CLK_32M	125ns

ADC_CLK_H	O	1	2 timers frequency clock of ADC_CLK	
ADC_CLK	O	1	Clock set by ADC_CLK_SET[1:0]	
CLK_ADC_SC	O	1	Scan_muxed ADC_CLK_H	
AUX_ADC_CLK_H	O	1	2 timers frequency clock of ADC_AUX_CLK	
AUX_ADC_CLK	O	1	Clock set by ADC_CLK_SET[1:0]	
CLK_AUX_ADC_SC	O	1	Scan_muxed AUX_ADC_CLK_H	
CLK_I2C_SC	O	1	Gated CLK_400K_SC by I2C_MAS_EN	
CLK_MTP_SC	O	1	Gated CLK_400K_SC by MTP_EN	
CLK_CB_SC	O	1	Gated CLK_SLOW_SC by CB_EN	
CLK_SLOW_SC	O	1	Scan_muxed CLK_SLOW	
CLK_SLOW2_SC	O	1	Scan_muxed CLK_SLOW2	
pulse_SLOW2_2ms	O	1	2ms period pulse divided from CLK_SLOW2_SC	3.9us
resetb_CLK	I	1	Asynchronous reset signal(synchronously released)	Level(CLK_32M domain)
resetb_CLK_256K	I	1	Asynchronous reset signal(synchronously released by CLK_256K)	Level(CLK_256K domain)
resetb_SR_CLK_SLOW	I	1	Scan_muxed resetb and soft resetb for CLK_SLOW domain	Level
SCAN_MODE	I	1	For DFT test	
SCAN_CLK	I	1	Clock for DFT test	
CLK_32M	I	1	Main clock. When A2D_SLEEP_1P8 high, after 4us, CLK_32M is off	31.25ns period
CLK_256K	I	1	Always on low clock	3.90625us period
CLK_32M_OK	I	1	CLK_32M_OK high means CLK_32M is accurate and can be used	
ADC_CLK_SET	I	2	From reg, ADC clock selection	Level(CLK_REG domain)
CB_EN	I	1	From reg, Cell balance enable	Level(CLK_REG domain)
D2A_CELL_ADC_EN	I	1	CELL_ADC enable	Level(CLK_REG domain)
D2A_AUX_ADC_EN	I	1	AUX_ADC enable	Level(CLK_REG domain)
SOFT_RSTB_REG	I	1	From reg, soft reset (low reset)	Level(CLK_REG domain)
I2C_MAS_EN	I	1	I2C_MAS enable	Level(CLK_REG domain)
MTP_EN	I	1	MTP interface enable	Level(CLK_REG domain)

Clock Definition

The following table describes clocks defined in Figure 1 clock block diagram and other sections of this document.

Clock Name	Definition
CLK_32M_SC	For u_BASIC_CTRL
CLK_REG_SC	For u_COMM_CTRL, u_FRAME_COUNTER, u_COMM_TO, u_COMM_REG
ADC_CLK	For analog part

ADC_CLK_H	For analog part
AUX_ADC_CLK	For analog part
AUX_ADC_CLK_H	For analog part
CLK_ADC_SC	For u_ADC_CTRL
CLK_AUX_ADC_SC	For u_AUX_ADC_CTRL
CLK_I2C_SC	For u_I2C_MAS
CLK_MTP_SC	For u_MTP_TOP
CLK_CB_SC	For u_CB_CTRL
CLK_SLOW_SC	For u_CYC_WAKE, u_OVUV_OTUT_CMP, u_FLT_LOGIC, u_TO_SLP_sync, u_TO_SD_sync, u_SOFT_RSTB_sync
CLK_SLOW2_SC	For u_GAP_CMP, u_CONF_REG_CRC_DET, u_MTP_REG_CRC_DET
CLK_OUT_SC	For u_DS_BASIC
CLK_8M_256K_SC	For u_CB_CTRL, u_FLT_REG

Table1 clock definitions

CKGEN function description

The following diagram shows the clock architecture and various clock sources for this chip.

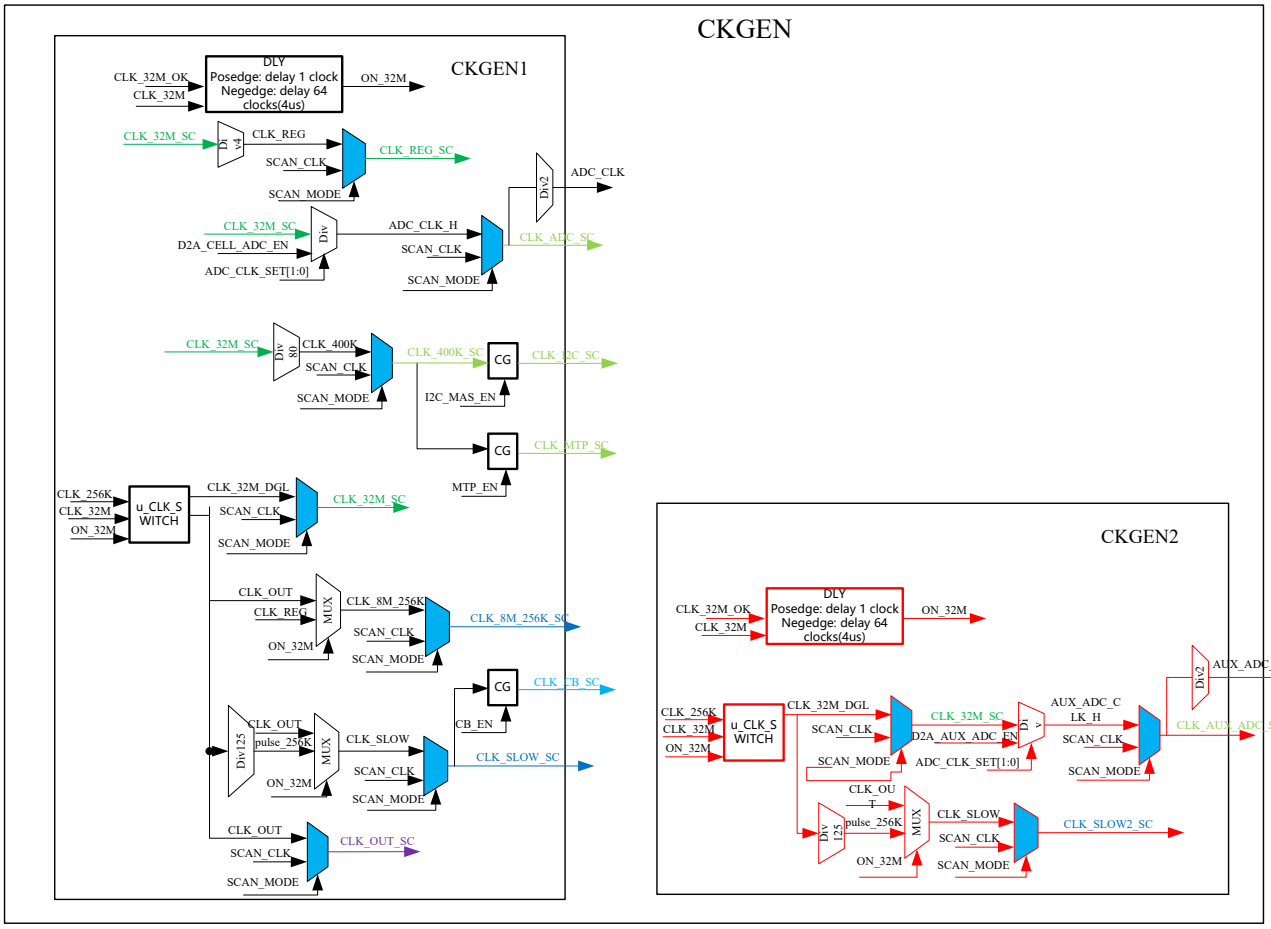

Figure2 clock diagram(HWR003/004/005/006/007_CKGEN1)

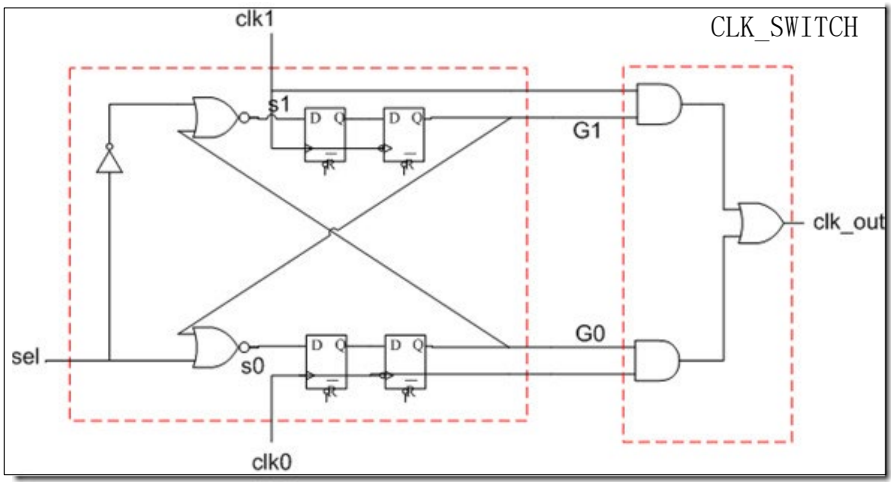

Figure3 CLK_SWITCH diagram

CLK_32M_SC

When CLK_32M_OK turns high from low, CLK_32M is stable.

When CLK_32M_OK turns high from low, CLK_32M is still useable within 4us.

Thus ON_32M is generated. ON_32M's posedge is 1 clock later than CLK_32M_OK, but its negedge is 4us later than CLK_32M_OK.

CLK_32M_DGL is the gated clock of CLK_32M, gated by ON_32M.

CLK_32M_SC is the scan-muxed result of CLK_32M_DGL.

CLK_REG_SC

8MHz clock divided form CLK_32M_SC. (HWR006_CKGEN1)

ADC_CLK, ADC_CLK_H

(HWR007_CKGEN1)

ADC_CLK freq setting：ADC_CLK_SET[1:0]

2'b00 : ADC_CLK 250k

2'b01: ADC_CLK 500k

2'b10 : ADC_CLK 1M

2'b11 : ADC_CLK 1.5M

Frequency of ADC_CLK_H is 2 times of ADC_CLK with 7/16 duty.

AUX_ADC_CLK,AUX_ ADC_CLK_H

(HWSR003_CKGEN2)

AUX_ADC_CLK freq setting：ADC_CLK_SET[1:0]

2'b00 : ADC_CLK 250k

2'b01: ADC_CLK 500k

2'b10 : ADC_CLK 1M

2'b11 : ADC_CLK 1.5M

Frequency of AUX_ADC_CLK_H is 2 times of ADC_CLK with 7/16 duty.

CLK_ADC_SC

Scan-muxed result of ADC_CLK_H. (HWSR001/002_CKGEN2)

CLK_AUX_ADC_SC

Scan-muxed result of AUX_ADC_CLK_H.

CLK_I2C_SC

CLK_400K is the divided clock of CLK_32M, divided by 80.

CLK_400K_SC is the scan-muxed result of CLK_400K.

CLK_I2C_SC is the gated clock of CLK_400K_SC, gated by I2C_MAS_EN.(HWR004_CKGEN1)

CLK_MTP_SC

CLK_MTP_SC is the gated clock of CLK_400K_SC, gated by MTP_EN. (HWR004_CKGEN1)

CLK_OUT_SC

(HWR001_CKGEN1)

When ON_32M is high, CLK_OUT is from CLK_32M.

When ON_32M is low, CLK_OUT is from CLK_256K.

Glitch-free logic is used for CLK_OUT.

CLK_OUT_SC is the scan-muxed result of CLK_OUT.

CLK_8M_256K_SC

When ON_32M is high, CLK_8M_256K is from CLK_REG.

When ON_32M is low, CLK_8M_256K is from CLK_OUT.

Glitch-free logic is used for CLK_8M_256K.

CLK_8M_256K_SC is the scan-muxed result of CLK_8M_256K.

CLK_SLOW_SC

(HWR001_CKGEN1)

Pulse_256K is the divided signal CLK_32M, divided by 125, with duty 1/125.

When ON_32M is high, CLK_SLOW is from pulse_125K.

When ON_32M is low, CLK_SLOW is from CLK_OUT(from CLK_256K).

CLK_SLOW_SC is the scan-muxed result of CLK_SLOW.

CLK_SLOW2_SC

(HWSR001/002_CKGEN2)

Redundant copy of CLK_SLOW_SC for safety use, using separate path with CLK_SLOW_SC.

CLK_CB_SC

CLK_CB_SC is the gated clock of CLK_SLOW_SC, gated by CB_EN. (HWR004_CKGEN1)

Operating Modes

To save power, most of clock source can be gated in low power mode.
The following table shows the clock availability in low power modes.

Clock Name	Sleep	active	shutdown
CLK_32M_SC	No (by ON_32M)	Yes	No
CLK_REG_SC	No (by ON_32M)	Yes	No

Clock Name	Sleep	active	shutdown
ADC_CLK	No (by D2A_CELL_ADC_EN)	Yes (by D2A_CELL_ADC_EN)	No
ADC_CLK_H	No (by D2A_CELL_ADC_EN)	Yes (by D2A_CELL_ADC_EN)	No
AUX_ADC_CLK	No (by D2A_AUX_ADC_EN)	Yes (by D2A_AUX_ADC_EN)	No
AUX_ADC_CLK_H	No (by D2A_AUX_ADC_EN)	Yes (by D2A_AUX_ADC_EN)	No
CLK_ADC_SC	No (by D2A_CELL_ADC_EN)	Yes (by D2A_CELL_ADC_EN)	No
CLK_AUX_ADC_SC	No (by D2A_AUX_ADC_EN)	Yes (by D2A_AUX_ADC_EN)	No
CLK_I2C_SC	No (by I2C_MAS_EN)	Yes (by I2C_MAS_EN)	No
CLK_MTP_SC	No (by MTP_EN)	Yes (by MTP_EN)	No
CLK_CB_SC	Yes (by CB_EN)	Yes (by CB_EN)	No
CLK_SLOW_SC	Yes (from CLK_256K)	Yes (from pulse_125K)	No
CLK_OUT_SC	Yes (from CLK_256K)	Yes (from CLK_32M)	No

Table 2 clock availability in different modes