

# ADC\_CTRL

## REVISION HISTORY

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## ADC

### Introduction

A 16-bit high accuracy ADC is applied inside BM20A to do the data acquisition. ADC supports 18 CELLS single conversion and continuous conversion. Besides ADC also supports 12 GPIO channels and 3 other(VPTAT, VBG and VBG2) channels single conversion.

BM20A's full scale range for CELL ADC is -6.5536V to +6.5536V, LSB is 200uv, but the recommended sampling range for each cell is -5V to +5V. The negative range is mostly for bus bar monitoring, which can be +/-0.7V at most. This sampling result will be used to calculate the total voltage of the whole battery pack.

The ADC measurement result will use 2's complement code.

#### Main Features

- Configurable ADC conversion modes (four modes)
- Configurable sample clock from 250KHz to 1.5MHz(four speed)
- Programmable ADC Analog dead time and settling time
- Optional chopper conversion to reduce system offset
- Supports single conversion and continuous conversion
- Supports 18 CELLS conversion, 12 GPIOs conversion and 3 others conversion
- Controllable data freezing function
- Configurable data low-pass filter

### Functional Description

#### Block Diagram

As show in the Fig 1, High-voltage measurement objects are first converted to low-voltage objects by the path of HV-MUXn and level-shift blocks, and then all measurement objects are fed to ADCs through LV-MUX and level-shift blocks. HV-MUXn are powered by VDC, and LV-MUXn is powered by VAA1.

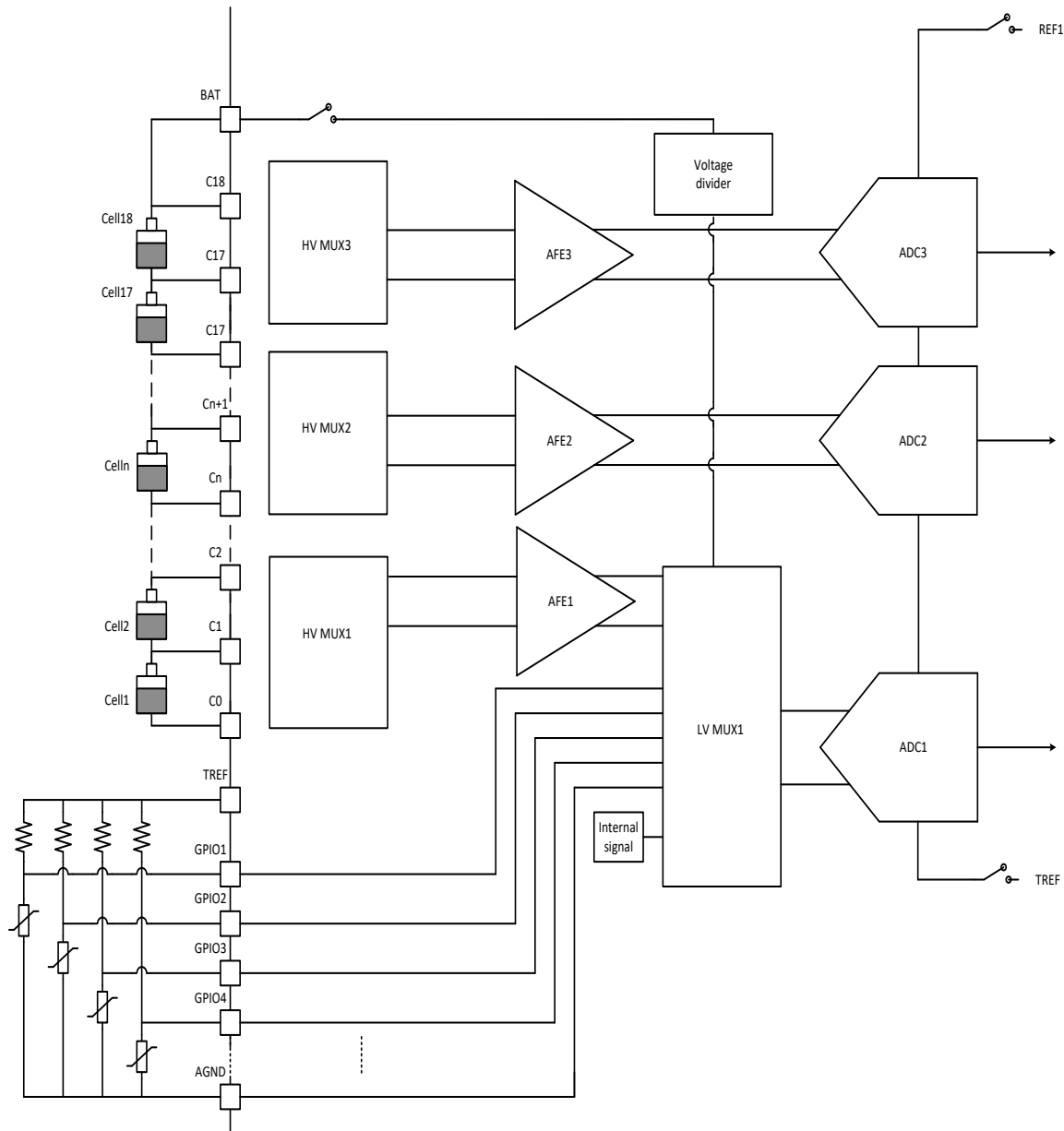


Fig 1 ADC Block Diagram

### ADC Clock

ADC clock frequency is controlled by ADC\_CLK\_SET bits to generate frequency of 250KHz, 500KHz, 1MHz and 1.5MHz clock. ADC\_CLK\_SET shall be updated by ADC\_CLK\_SET\_REG in ADC\_SETTING\_REG when ADC\_GO\_DLY is detected high[HWR006\_CH\_SEL\_GEN], and ADC\_CLK\_SET need to output to CLKGEN to generate ADC\_CLK and ADC\_CLK\_H.

Besides ADC clock setting, ADC\_SETTING\_REG also include ADC mode setting(ADC\_MODE\_REG), chopper conversion control(ADC\_CHP\_EN\_REG), channel dead time setting(CH\_DT\_REG), channel set up time setting(CH\_STL\_REG, CH\_TOP\_STL\_REG), data low-pass filtering setting(DLPF\_FC\_REG) and GPIO reference selection setting(GPIO\_REF\_SEL\_REG). ADC\_SETTING\_REG can only be refreshed when ADC\_GO\_DLY is high[HWR006\_CH\_SEL\_GEN].

## ADC Sequence Setting

ADC sequence setting mainly includes dead time and settling time setting. ADC dead time is configured by CH\_DT\_REG to control the blank time for channel switching, settling time controls the duration between the conversion channel enable asserts and ADC reset active, the settling time of CELL18 is configured by CH\_TOP\_STL\_REG, and the settling time of CELL1 is configured by CH\_BOT\_STL\_REG, the others channel is configured by CH\_STL\_REG.

## ADC Mode

The ADC has four work modes which can be configured by ADC\_MODE\_REG. For different mode, ADC has different effective bits of SDM data and ALG data from analog to digital, and the conversion time is different. As shown in table1.

ADC MODE and Conversion Time Calculation				
ADC_MODE	00	01 (Default)	10	11
ADC_CHP_EN	1			
ADC Clock Frequency(Mhz)	1			
Resolution_Final(Bits)	15	15	15	15
Resolution_Original(Bits)	16	17	17	17
Effective bits of SDM+ALG	4+12	6+11	7+10	9+8
First integration( $2^N+1$ )	17	65	129	513
First Algorithmic	12	11	10	8
2nd integration( $2^N+1$ )	17	65	129	513
2nd Algorithmic	12	11	10	8
Actual Conversion time(cycle) (ADC only)	58	152	278	1042
Actual Conversion time(uS) (ADC only)	58.00	152.00	278.00	1,042.00

Besides the output data format of SDM and ALG are also affected by ADC mode as shown in table1.

(1) The ADC data in all modes should be 17Bit format, from mode 00 to 11. In mode "00" the LSB bit D0 is empty, can be set to a random number.

(2) DATA[17] only use to judge "overflow" of input range, not use for data calculation.

ADC_MODE	DATA[17:0]
0	{SDM[4:0], ALG[11:0], 1'b0}
1	{SDM[6:0], ALG[10:0]}
2	{SDM[7:0], ALG[11:1]}
3	{SDM[9:0], ALG[11:4]}

## Conversion Mode

- Single Conversion

In single conversion mode, the ADC performs a big round-robin conversion of CELL conversion(from CELL18 to CELL1), GPIO conversion(from GPIO12-GPIO1) and 3 others(VPTAT,VBG and VBG2)conversion.

#### ● Continuous Conversion

In continuous conversion mode, ADC performs a little round-robin of 18 CELLS periodically, ADC will not stop converting by itself until been interrupted by single conversion start(ADC\_SGLE\_GO or MON\_ADC\_GO or C\_OW\_ADC\_GO).

### ADC Start

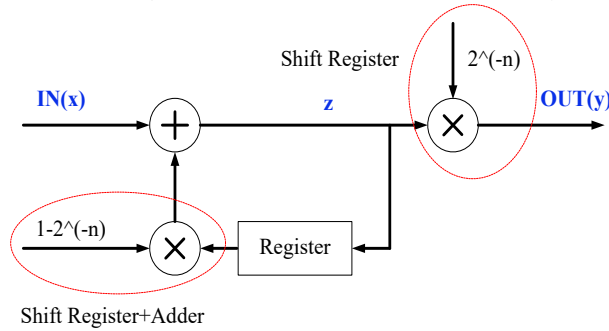
ADC has four kinds start control signals include ADC\_SGLE\_GO, ADC\_CNTI\_GO, MON\_ADC\_GO and C\_OW\_ADC\_GO, when any of the four ADC\_GO is detected high, ADC clock gating signal will be asserted to generate ADC measurement clocks, then ADC start to convert[HWR001\_ADC\_CTRL]. After all channels of single round-robin are finished, the clock gating signal will be invalid to stop ADC clock.

ADC\_CNTI\_GO is used to initiate CELLS continuous round-robin conversion, the other start control signals are used to start a single round-robin conversion. When ADC\_CNTI\_GO and ADC\_SGLE\_GO asserts at the same time, ADC only goes into continuous conversion and the ADC\_SGLE\_GO will be ignored[HWR003\_ADC\_CTRL].

ADC also generates a clear signal to prepare for the next start and the clr\_ADC\_GO shall be kept high at least for 8us allow for clock domain crossing[HWR005\_CH\_SEL\_GEN].

### ADC Data Filtering

Besides the RC filter added to the Cn pin to reduce aliasing effects, an additional single pole digital low pass filter(DLPF) is supplied to avoid that too big external RC filter will affect accuracy.



$$z(i) = x(i) + (1 - 2^{(-n)}) * z(i-1)$$

$$y(i) = 2^{(-n)} * z(i), \text{ 同时 } y(i-1) = 2^{(-n)} * z(i-1)$$

So,

$$y(i) = 2^{(-n)} * x(i) + (1 - 2^{(-n)}) * y(i-1)$$

So, the corner frequency is:

$$f_c = \frac{f_s}{2\pi(2^n - 1)}, \text{ } f_s \text{ is the sample frequency from the ADC}(f_{IN}).$$

The corner frequency of DLPF can be adjust by ADC\_CONF[DLPF\_FC<2:0>].

Since there is a obvious step response of DLPF, it is highly recommended that DLPF is enabled with ADC\_CTRL[MODE<1:0>]=CONTI, and a waiting delay is necessary before first reading the ADC results after DLPF is enabled.

CELLs conversion results are calculated by calibration algorithm and then output to ADC\_DATA\_LFP registers through the low-pass filter. The filtering frequency ranges from 10Hz to 1KHz, which is divided

into 8 steps. User can set the filtering frequency according to the needs, or turn off the filter by configuring the DLPF\_FC\_REG[HWR001\_DLPF].

## ADC Freezing

CONTROL1[FREEZE] bit is asserted to freeze all ADC measurement results and round-robin numbers(RR\_COUNTER) instead of stopping ADC measurement and RR\_COUNTER counting. Write CONTROL1[FREEZE] to 0 to allow ADC measurement results and round-robin numbers updating.

Normally ADC measurement result registers are not be refreshed until new converted data is available[HWR004\_ADC\_CTRL]. When FREEZE\_DLY(the delay of CONTROL1[FREEZE]) is detected high, all ADC measurement result registers will be temporarily locked, even if there is a new converted data, it will not be loaded into the result register[HWR005\_ADC\_CTRL].

## Functional Detail

ADC\_CTRL block diagram shows in Fig2. RECLK\_COMP controls the delay of FREEZE and ADC\_GO from CONTROL2[FREEZE], CONTROL2[ADC\_SGLE\_GO] and CONTROL2[ADC\_CNTI\_GO], the delay length is decided by device number and CB\_SETTLE\_REG[4:0].

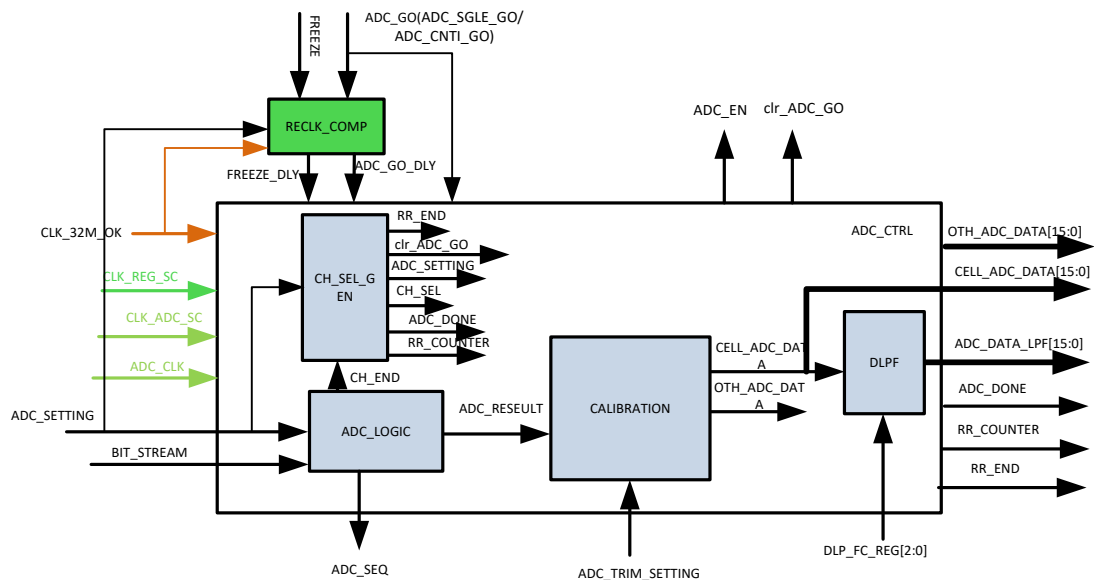


Fig 2 ADC\_CTRL block diagram

The ADC\_CTRL consists of the following units:

- ADC sequence generation
- ADC analog data combination logic
- ADC data calibration calculation
- ADC CELL DATA low-pass filtering

When CLK\_32M\_OK is low, it means the source clock 32MHz will stop soon. Before ADC clock disappears, all the counters and temporary registers in ADC\_CTRL need to be reset to initial state (except result registers CELL\_ADC\_DATA, OTH\_ADC\_DATA and ADC\_DATA\_LPF) to make prepare for the new conversion later[HWR002\_ADC\_CTRL].

CH\_SEL\_GEN refreshes values of ADC\_SETTING\_REG to ADC\_SETTING register when ADC\_GO\_DLY is detected high, it uses several counters to generate ADC sequence control signals. At end of each channel(except last channel), CH\_COUNTER(the number of converted channels) will be incremented by one[HWR002\_CH\_SEL\_GEN]. At end of each round-robin, RR\_COUNTER is added by 1, while CH\_COUNTER is cleared to zero for next cycle, and a RR\_END flag will be set to 1 to announce that all the converted data are available, allow for the latency of clock domain crossing process, RR\_END need to keep high at least 8us[HWR001\_CH\_SEL\_GEN].

ADC\_LOGIC convert analog bit stream to parallel data according to the ADC\_MODE setting. Besides ADC\_LOGIC use counters to generate channel end flag (CH\_END) to CH\_SEL\_GEN[HWR001\_ADC\_LOGIC].

ADC I/O signals description shows in the following table.

Signal	Width (bits)	I/O	Default value	Duration	DESCRIPTION
ADC_POLAR	1	output	0	N/A	Polarity control of ADC, "H" polarity is positive, "L" polarity is negative
ADC_RST_INT	1	output	0	2 CLK_ADC_SC	Reset signal of ADC, when "RST_INT" is "high", integrator is in reset mode, the integration capacitor will be reset in every cycle.
ADC_EN_SH_VIN	1	output	0	N/A	Enable signal of input sample of integrator. The integrator will sample Vshunt or Vbus only if EN_SH_VIN is "high"
ADC_EN_SH_VRFEF	1	output	0	N/A	Enable signal of reference feedback in ADC. The integrator will feedback reference voltage only if EN_SH_VREF is "high"
ADC_EN_ALG	1	output	0	N/A	Enable signal of ADC gain2 function. EN_ALG is "high", the integrator is in GAIN2 mode, the redundant signal in INT_CAP will amplified by 2X.
ADC_CMP_OUT_POS	1	input	0	N/A	Output data of positive comparator
ADC_CMP_OUT_NEG	1	input	0	N/A	Output data of negative comparator
ADC_CELL_CH_SEL	18	output	18'h0	N/A	ADC CELL18-CELL1 channel enable
ADC_GPIO_CH_SEL	12	output	12'h0	N/A	ADC GPIO12-GPIO1 channel enable
ADC_VPTAT_SEL	1	output	0	N/A	ADC VPTAT channel enable
ADC_VBG_SEL	1	output	0	N/A	ADC VBG channel enable
ADC_VBG2_SEL	1	output	0	N/A	ADC VBG2 channel enable
D2A_CELL_ADC_EN	1	output	0	N/A	ADC clock gating enable
D2A_ADC_DONE	1	output	0	N/A	ADC_DONE is high when 1st round-robin ends.

RR_END	1	output	0	8us	Round-robin end flag
ADC_CLK_SET	2	output	0	N/A	ADC CLK frequency setting
clr_ADC_GO	1	output	0	8us	Output to clear 4 kinds of ADC_GO
RR_COUNTER	16	output	0	N/A	Round-robin number, RR_COUNTER is frozen when FREEZE_DLY is detected, is cleared by ADC_GO_DLY is high .
GPIO_REF_SEL	12	output	0	N/A	GPIO reference voltage selection
CELL_ADC_DATA_CHx	16	output	0	N/A	CELL18-CELL1 battery convert result
ADC_DATA_LPF_CHx	16	output	0	N/A	CELL18-CELL1 convert result with filter
ADC_DATA_GPIOx	16	output	0	N/A	GPIO12-GPIO1 convert result
ADC_DATA_OTH	16	output	0	N/A	VPAT,VBG,VBG2 convert result
CLK_REG_SC	1	input	0	8MHz	Frequency is 8MHz, is divided from CLK_32M
CLK_ADC_SC	1	input	0	ADC CLK HIGH	generated from CLK_32M divided by ADC_CLK_SET
ADC_CLK	1	input	0	ADC CLK	generated from CLK_32M divided by ADC_CLK_SET, half the frequency of CLK_ADC_SC
resetb_CLK	1	input	1	N/A	Asynchronous power on reset
rstb_32M_ok_and_sr	1	input	1	N/A	Power reset and CLK_32M_OK reset CLK_32M_OK is low, ADC_CTRL shall be reset to initial state
SOFT_RSTB_REG	1	input	1	N/A	Soft reset, release synchronously in CLK_32M domain.
MON_ADC_GO	1	input	0	N/A	ADC single conversion go to work
C_OW_ADC_GO	1	input	0	N/A	ADC single conversion go to work
ADC_SGLE_GO	1	input	0	N/A	ADC single conversion go to work
ADC_CNTI_GO	1	input	0	N/A	ADC continuous conversion go to work
ADC_SGLE_GO_DLY	1	input	0	N/A	ADC single conversion go with delay
ADC_CNTI_GO_DLY	1	input	0	N/A	ADC continuous conversion go with delay
FREEZE_DLY	1	input	0	N/A	ADC FREEZE flag with delay
ADC_SETTING	92	input		N/A	



ADC sequence signals contain ADC\_POLAR, ADC\_RST\_INT, ADC\_EN\_SH\_VIN, AC\_EN\_SH\_VREF and ADC\_EN\_ALG.

### ADC Calibration

ADC calibrates the converted results from analog ADC with TRIM\_ADC[HWR001\_CALIBRATION]. As shown in Fig3, ADC\_CHP\_EN bit is set to 1, conversion process contains POLAR high and low stage. Each stage includes SDM phase and ALG phase. In SDM phase, total data length is  $2^N$ , ADC\_LOGIC needs to count number of all '1' of the serial compared result and save data to SDM\_POS/SDM\_NEG register. In ALG phase, total data length is M, the first data is MSB and the last data is LSB. All data are shift into ALG\_POS/ALG\_NEG register.

ADC\_POS is the 18bits data combined by SDM\_POS and ALG\_POS which is controlled by ADC\_MODE\_REG, ADC\_NEG is the 18bits data combined by SDM\_NEG and ALG\_NEG. ADC\_OUT1/ADC\_OUT0 is the difference between ADC\_POS and ADC\_NEG of POLAR high/low stage. ADC\_OUT\_F is the mean of the difference between ADC\_OUT1 and ADC\_OUT0. ADC\_OUT\_ORG is the product of ADC\_OUT\_F and scale factors. ADC\_OUT\_FL is the result of ADC\_OUT\_ORG calibrated with gain and offset coefficients. The final results ADC\_OUT\_FL\_ED is 16 bits signed binary complement data(CELL\_ADC\_DATA[15:0] and OTH\_ADC\_DATA[15:0]) will be saved into registers, and the CELL\_ADC\_DATA need to output to DLPF separately to do filtering[HWR002\_CALIBRATION].

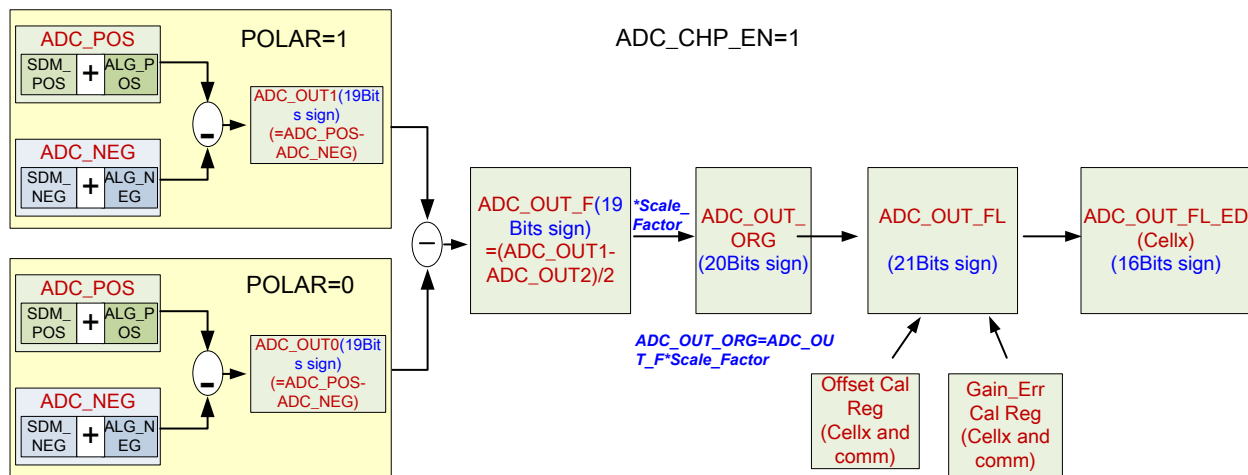


Fig 3 ADC Calibration algorithm(ADC\_CHP\_EN=1)

Different from the situation of ADC\_CHP\_EN bit is set to 1, ADC\_OUT is always zero, as ADC only converts when POLAR is high. As a result, ADC\_OUT\_F is equal to ADC\_OUT1.

ADC data calibrations totally takes 8 ADC\_CLK periods(16 CLK\_ADC\_SC periods) after the last serial data is available, analog ADC outputs results at the rising edge of ADC\_CLK, ADC\_CTRL captures data at the opposite edge of ADC\_CLK. The implementation of ADC\_CTRL calibration is shown in Fig4.

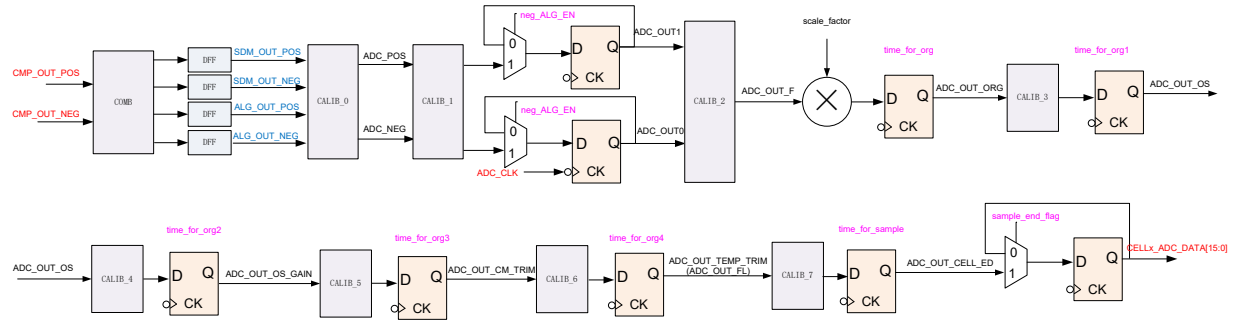


Fig 4 ADC Calibration flow

As shown in Fig4, all result registers are equivalent to be driven by the falling edge of ADC\_CLK, each step result is locked into D Flip-Flop only when the control signal(neg\_ALG\_EN/time\_for\_org/.../sample\_end\_flag) is valid. The ADC\_CTRL calibration timing is shown in Fig5.

### ADC Timing for Digital

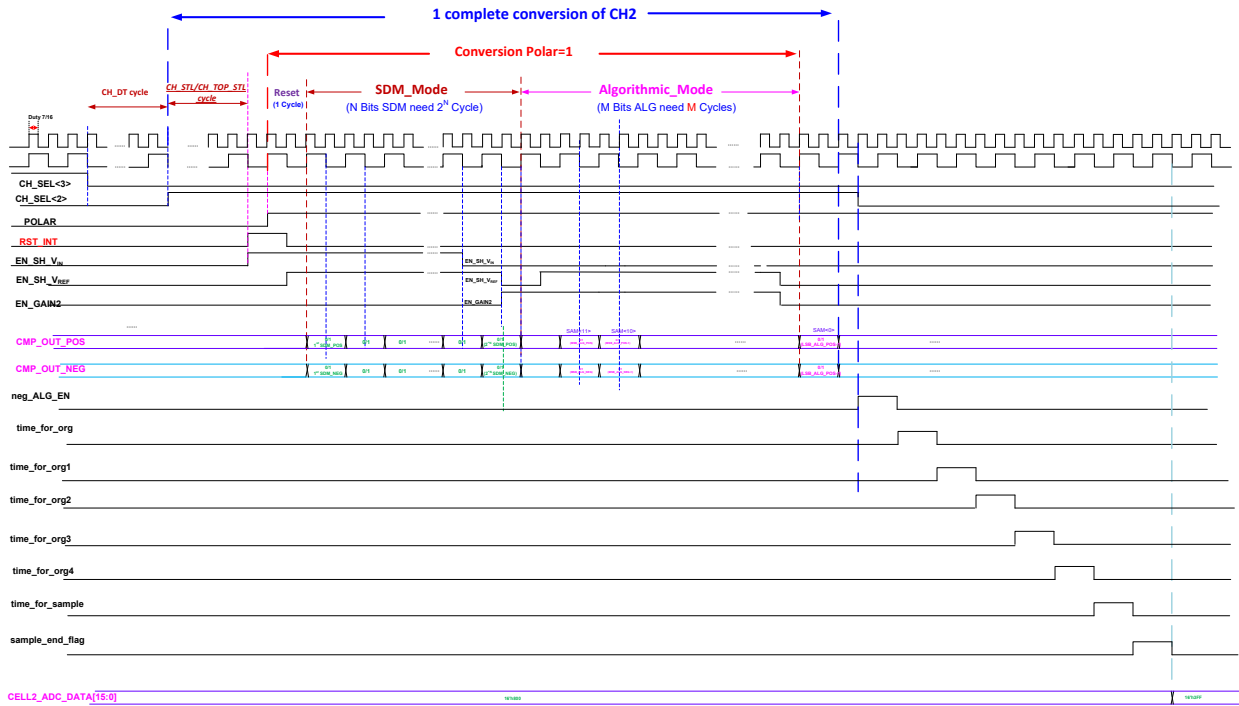


Fig 5 ADC Calibration timing

### ADC DLPF

According to the simplified filter formula:

$$y(i)=2^{-(n)}*x(i)+(1-2^{-(n)})*y(i-1)$$

It can be seen that

$$2^n * Y_i = X_i + 2^n * Y_{i-1} - Y_{i-1}, \text{ that is}$$

$$2^n * Y_0 = X_0$$

$$2^n * Y_1 = X_1 + 2^n * Y_0 - Y_0$$

$$2^n * Y_2 = X_2 + 2^n * Y_1 - Y_1$$

$2^n * Y_i$  is the sum data, and the  $Y_i$  is the average of sum. Data low-pass filter circuit implemented as shown in Fig6. DLPF circuits only need a 16bits register to save the average data in real time, as the converted data is achieved by sequence, so that it can reuse the adder and subtractor resource.

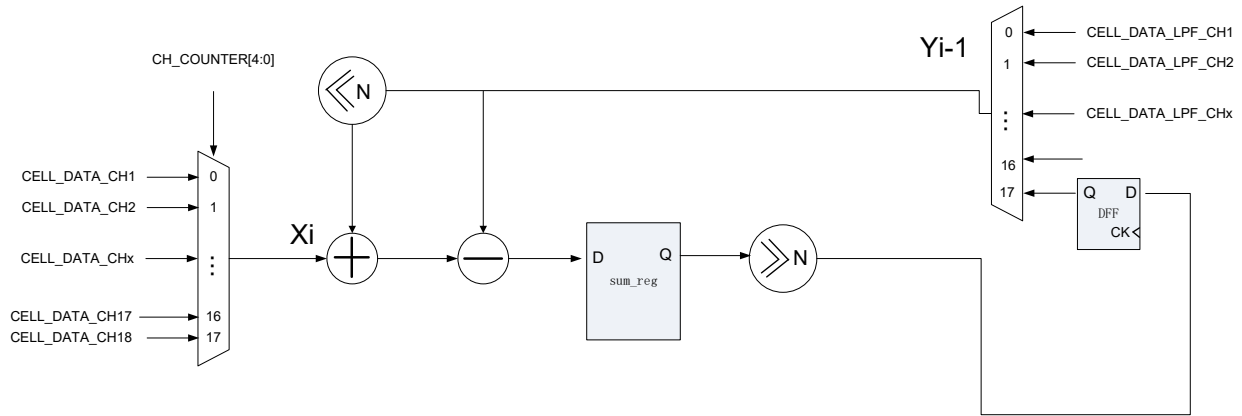


Fig 6 ADC DLPF implementation

## ADC Sequence Timing

ADC Sequence timing shows in the Fig7.

CH\_DT[4:0] controls dead time between different channel enable signal, time unit is ADC\_CLK period.

CH\_TOP\_STL[4:0] controls settling time for ADC after top channel enable is high, time unit is  $4*ADC\_CLK$  period.

CH\_STL[4:0] controls settling time for ADC after channel enable is high, time unit is  $2*ADC\_CLK$  period.

CH\_BOT\_STL[4:0] controls settling time for ADC after bottle channel enable is high, time unit is  $4*ADC\_CLK$  period.

As shown in Fig5, ADC sequence signals include CH\_SEL, POLAR, RST\_INT, EN\_SH\_VIN, EN\_SH\_VREF and EN\_GAIN2. All sequence signals are generated by CLK\_ADC\_H. CLK\_ADC is half of the CLK\_ADC\_H. Both POLAR and compared results(CMP\_OUT\_POS/CMP\_OUT\_NEG) are aligned with rising edge of CLK\_ADC. RST\_INT keeps asserting one CLK\_ADC period to reset the integration capacitor. ADC\_CHP\_EN also affects the ADC conversion time.

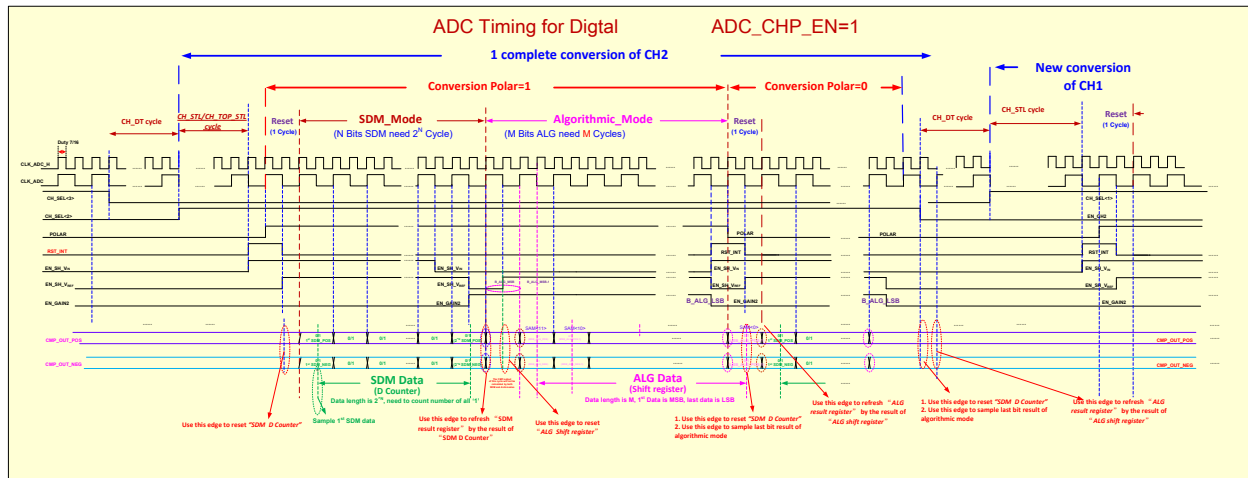


Fig 7 ADC Sequence timing(ADC\_CHP\_EN=1)



## ADC Continuous Conversion Timing

As shown in Fig11, when ADC\_CNTI\_GO asserts high, ADC goes into continuous conversion mode, each time the last channel conversion is done, RR\_COUNTER is automatically increased by 1. ADC can not stop automatically.

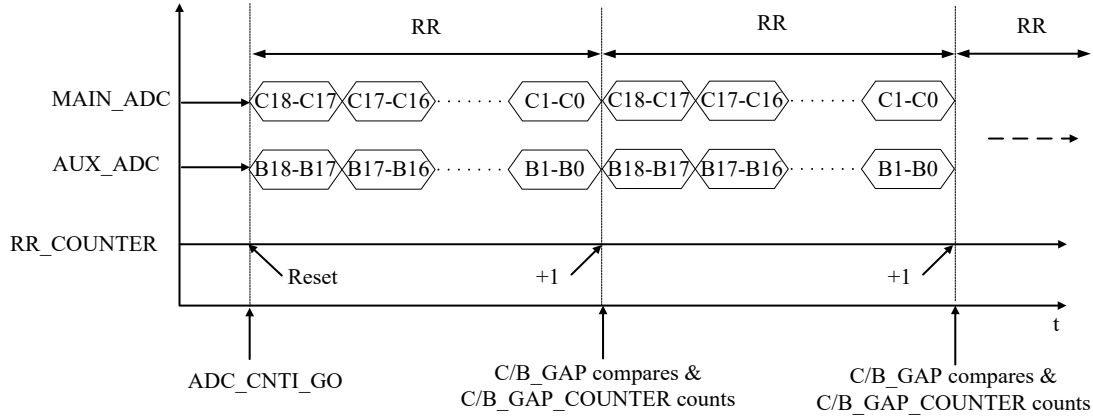


Fig 11 ADC continuous conversion without ADC\_SGLE\_GO

As shown in Fig12, during ADC continuous conversion, even that `ADC_SGLE_GO` asserts high, it can not terminate continuous conversion immediately, ADC starts to single conversion after current round-robin finished, `RR_COUNTER` is reset to zero at same time. After single conversion round-robin is finished, ADC will stop.

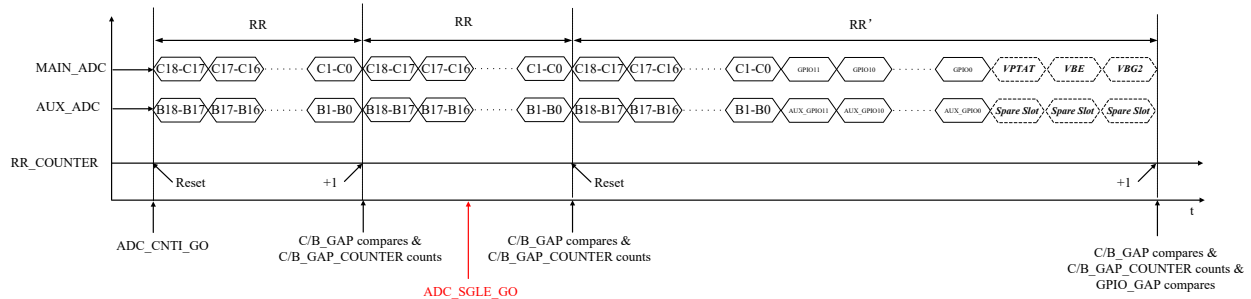


Fig 12 ADC continuous conversion with ADC\_SGLE\_GO

## ADC Counter Timing

As shown in Fig13, `cnt_STL` counts for settling time controlled by `CH_STL_TOP` or `CH_STL_REG`, `COUNTER` counts the conversion time firstly and counts the dead time later, `CH_COUNTER` mainly counts the number of converted channel except for the end of round-robin, `RR_COUNTER` counts the number of round-robin and cleared by `ADC_GO_DLY`. All counters increment one by the `CLK_ADC_H` and be cleared to 0 when `CLK_32M_OK` is low.

