Hardware Safety Requirement

WP as Prerequisites	Author of HWSR
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TSR ID	HWSR ID	Description	Note
TSR001	HWSR1_AUX_ADC HWSR1_AUX_ADC_CTRL	AUX_ADC and AUX_ADC_CTRL shall reuse ADC and ADC_CTRL IP	
	HWSR1_CKGEN2	CKGEN2 shall generate CLK_AUX_ADC_SC and CLK_SLOW2_SC CLK_AUX_ADC_SC is same loigc as CLK_ADC_SC CLK_SLOW2_SC is same loigc as CLK_SLOW_SC CLK_AUX_ADC_SC shall use separate path from CLK_ADC_SC CLK_SLOW2_SC shall use separate path from CLK_SLOW_SC CLK_AUX_ADC_SC shall be used for AUX_ADC and AUX_ADC_CTRL	
	HWSR2_CKGEN2	CKGEN2 shall mux all clocks with scanmux. Each scanmux shall output functional clock when SCAN_NODE is low, and output SCAN_CLK when SCAN_MODE is high. The clock outputs of CKGEN2 shall be CLK_AUX_ADC_SC, CLK_SLOW2_SC	
	HWSR3_CKGEN2	CKGEN2 shall output AUX_ADC_CLK, AUX_ADC_CLK_H according to AUX_ADC_CLK_SET.	
	HWSR1_COMM_REG	CELL_GAP_THRESH_REG[4:0], OTH_GAP_THRESH_REG[2:0], CELL_GAP_DEGL_REG[4:0] shall be defined in COMM_REG	
	HWSR1_GAP_CMP	CELL_GAP_THRESH_REG, OTH_GAP_THRESH_REG, CELL_GAP_DEGL_REG shall be updated into CELL_GAP_THRESH, OTH_GAP_THRESH, CELL_GAP_DEGL when ADC_GO_DLY or MON_WAKE_GO is high	
	HWSR2_GAP_CMP	GAP_CMP shall compare the gap between AUX_ADC_DATA_LPF and ADC_DATA_LPF with CELL_GAP_THRESH when RR_END is high Once over range, the counter in GAP_CMP shall increase by 1, once not over range, the counter in GAP_CMP shall decrease by 1, until the counter reaches CELL_GAP_DEGL, GAP_CMP output CELL_GAP_FLT CELL_GAP_THRESH shall cover from 20mV to 180mV, 5mV step CELL_GAP_DEGL shall cover from 1 to 32	
	HWSR3_GAP_CMP	GAP_CMP shall compare the gap between AUX_OTH_ADC_DATA_LPF and OTH_ADC_DATA_LPF with OTH_GAP_THRESH when RR_END is high Once over range, GAP_CMP output OTH_GAP_FLT OTH_GAP_THRESH shall cover from 1% to 8%, 1% step	
	HWSR4_GAP_CMP	CLK_SLOW2_SC shall be used for GAP_CMP	
	HWSR1_FLT_REG	CELL_GAP_FLT[17:0] and OTH_GAP_FLT[11:0] shall be defined in FLT_REG	
	HWSR2_DS_BASIC	When FLT_WAKE is high, F_COMM_GEN shall set the SOF bits of device address byte and register address bytes in its own response frame	
	HWSR3_DS_BASIC	When any SOF bit of received response frame is detected in device address byte and register address bytes, FCOMM_DET shall output FCOMM_FLT	
	HWSR2_FLT_REG	FCOMM_FLT shall be defined in FLT_REG	
TSR002	/		
TSR003	HWSR2_COMM_REG	TWARN_THRESH_REG[2:0] shall be defined in COMM_REG	

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	HWSR1_OVUV_OTUT_CMP	TWARN_THRESH_REG shall be updated into TWARN_THRESH when ADC_GO_DLY or MON_WAKE_GO is high	
	HWSR2_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall compare the gap between OTH_ADC_DATA with TWARN_THRESH when RR_END is high Once over range, OVUV_OTUT_CMP shall output TWARN TWARN_THRESH shall cover from 110℃ to 145℃, 5℃ step	
	HWSR3_OVUV_OTUT_CMP	TWARN comparison shall ignore OVUV_OTUT_EN	
	HWSR3_FLT_REG	TWARN_FLT shall be defined in FLT_REG	
TSR004	HWSR1_CMP_BIAS	VCC_FS shall generate 5V from BAT VCC_FS current capacity shall support 1mA CMP_BIAS shall be off when SD	
	HWSR2_CMP_BIAS	CMP_BIAS shall output BIAS_OK_DLY after SD is low after xxms	
	HWSR1_BG2	BG2 shall output VBG2	
	HWSR1_IREF2	IREF2 shall output IREF2	
	HWSR1_CP_CMP	CP_CMP shall only work when BIAS_OK_DLY high CP_CMP shall work when any of ACT, MON_WAKE, CB_EN is high CP_CMP shall compare CP-BAT with VBG2, when CP-BAT>7V, CP_CMP shall output CP_OV at CP_OVUV, when CP-BAT<3V, CP_CMP shall output CP_UV at CP_OVUV CP_CMP shall have 25us deglitch time	
	HWSR4_FLT_REG	CP_OV_FLT, CP_UV_FLT shall be defined in FLT_REG	
TSR005	HWSR1_VAA_CMP	VAA_CMP shall only work when BIAS_OK_DLY high VAA_CMP shall compare VAA with VBG2, when VAA>5.5V, VAA_CMP shall output VAA_OV at VAA_OVUV, when VAA<4.5V, VAA_CMP shall output VAA_UV at VAA_OVUV VAA_CMP shall have 25us deglitch time	
	HWSR5_FLT_REG	VAA_OV_FLT, VAA_UV_FLT shall be defined in FLT_REG	
TSR006	HWSR1_VDD_CMP	VDD_CMP shall only work when BIAS_OK_DLY high VDD_CMP shall compare VDD with VBG2 and compare DGND with VBG2, when VDD>1.98V, VDD_CMP shall output VDD_OV at VDD_OVUV and VDD_OV_BIST at VDD_OVUV_BIST, when VDD<1.62V or DGND>0.3V, VDD_CMP shall output VDD_UV at VDD_OVUV and VDD_UV_BIST at VDD_OVUV_BIST When BIST_REF_EN is high, the VDD_OVUV shall be blanked and only output VDD_OVUV_BIST VDD_CMP shall have 25us deglitch time	
	HWSR1_SEQ	DRSTB **shall** be L when VDD_OV is L DRSTB **shall** be L when VDD_UV is L	
	HWSR1_RST_REG	When the VDD_OV is a rising edge, VDD_OV_LATCH **shall** output H When the VDD_UV is a rising edge, VDD_UV_LATCH **shall** output H	

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TSR007	HWSR1_ADC	VBG shall be measured by REFP VBG2 shall be measured by TREF VBG accuracy should be better than VBG2	
TSR008	HWSR1_CH_SEL_GEN	RR_COUNTER **shall** be frozen when FREEZE_DLY is detected	
TSR009, ETSR001	HWSR1_FRAME_COUNTER	FR_CNT[15:0] shall increase by 1 when FRAME_DONE is detected by FRAME_COUNTER FR_CNT shall be readable by COMM_DIG through COMM_REG	
	HWSR1_LOW_BYTE_BUF	The low byte of FR_CNT shall be buffered when read by COMM_DIG	
	HWSR1_FR_CRC_DET	FR_CRC_DET shall output FRAME_DONE when each command and response frame is received (without CRC fault). FR_CRC_DET shall not output FRAME_DONE when frame is interrupted by new frame	
TSR010, ETSR002	HWSR1_FR_CRC_GEN	FR_CRC_GEN shall generate 2 CRC bytes in response frame	
TSR011, ETSR003	HWSR2_FR_CRC_DET	FR_CRC_DET shall detect the CRC fault in received frame (command and response), when detected, set FR_CRC_FLT and not set FRAME_DONE	
	HWSR6_FLT_REG	FR_CRC_FLT shall be defined in FLT_REG	
	HWSR1_COMM_CTRL	When FR_CRC_FLT is set, writing/reading by this frame shall be ignored, propagation shall still go on	
TSR012	HWSR1_CONF_REG_CRC_DET	CONF_REG_CRC_DET shall compare the calculated 16-bit CRC of configuration registers and MTP shadow registers with CONF_REG_CRC every 2ms, once fault detected, output CONF_REG_CRC_FLT	
	HWSR2_CONF_REG_CRC_DET	CLK_SLOW2_SC shall be used for CONF_REG_CRC_DET	
	HWSR3_COMM_REG	CONF_REG_CRC[15:0] shall be defined in COMM_REG	
	HWSR7_FLT_REG	CONF_REG_CRC_FLT shall be defined in FLT_REG	
TSR013	HWSR1_MTP_REG_CRC_DET	MTP_REG_CRC_DET shall compare the calculated 16-bit CRC of MTP shadow registers (except MTP CRC) with this MTP CRC every 2ms, once fault detected, output MTP_REG_CRC_FLT	
	HWSR5_CKGEN2	CLK_SLOW2_SC shall be used for MTP_REG_CRC_DET	
	HWSR8_FLT_REG	MTP_REG_CRC_FLT shall be defined in FLT_REG	
TSR014	HWSR1_AGND_OW_DET	AGND_OW_DET shall only work when BIAS_OK_DLY high AGND_OW_DET shall compare both B0-AGND and B1-ANGD with -0.4V, when any is over range, AGND_OW_DET shall output AGND_OW AGND_OW_DET shall have 25us deglitch time	

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	HWSR9_FLT_REG	AGND_OW_FLT shall be defined in FLT_REG	
TSR016	HWSR1_CS	CS shall use IREF to generate current sinks/source There shall be 500uA(+-10%) current sinks from each Cn(n=1-18) to AGND There shall be 500uA(+-10%) current source from VAA to C0 For current sink at C1, the resistance should <1k	
	HWSR2_CS	All current sinks/source shall be off when ACT is not high	
	HWSR3_CS	All current sinks shall be enabled when current sinks are selected in CS_EN_AUTO Current source shall be enabled when current source is selected in CS_EN_AUTO	
	HWSR4_COMM_REG	C_OW_DET_GO, C_OW_TDIS_REG[3:0] shall be defined in COMM_REG	
	HWSR1_C_OW_CTRL	C_OW_CTRL shall latch C_OW_TDIS_REG to C_OW_TDIS once C_OW_DET_GO is high.	
	HWSR2_C_OW_CTRL	C_OW_TDIS_REG shall cover from 2ms to 32ms	
	HWSR3_C_OW_CTRL	C_OW_CTRL shall output twice C_OW_ADC_GO(ADC_SINGLE_GO_DLY) to start Cn open wire detection when C_OW_DET_GO is high C_OW_CTRL shall clear C_OW_ADC_GO when clr_ADC_GO is detected C_OW_CTRL shall output clr_C_OW_DET_GO after C_OW_DET_GO high is detected	seq diagram
	HWSR4_C_OW_CTRL	C_OW_CTRL shall be reset when CLK_32M_OK is low	
	HWSR5_C_OW_CTRL	C_OW_CTRL shall compare CELL_ADC_DATA with -0.4V (C0-18 except C1) or 0.1V (C1) when RR_END high Once over range, C_OW_CTRL shall output C_OW[18:0]	
	HWSR10_FLT_REG	C_OW_FLT[18:0] shall be defined in FLT_REG	
TSR021	HWSR5_COMM_REG	CS_EN_MANU[18:0] shall be defined in COMM_REG	
	HWSR4_CS	Each current sink/source shall be enabled respectively when selected in CS_EN_MANU	
	HWSR6_COMM_REG	WEAK_PUPD_EN[11:0] and WEAK_PUPD[11:0] shall be defined in COMM_REG	
	HWSR1_10K_20UA_PUPD	There shall be 10K resistor between each GPIOn_ANA(n=0-11) and AUX_GPIOn_ANA(n=0-11) For each AUX_GPIOn_ANA(n=0-11), there is 20uA PU to VAA, 20uA PD to AGND When WEAK_PUPD_EN is high and WEAK_PUPD is low, 20uA PU shall be enabled When WEAK_PUPD_EN is high and WEAK_PUPD is high, 20uA PD shall be enabled When WEAK_PUPD_EN is low, both 20uA PU and PD shall be disabled	
TSR022	HWSR2_VAA_CMP	VAA_CMP shall switch the comparison reference (which can toggle VAA_CMP output) based on VBG2 when BIST_REF_EN is high	

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	HWSR2_VDD_CMP	VDD_CMP shall switch the comparison reference (which can toggle VDD_CMP output) based on VBG2 when BIST_REF_EN is high	
	HWSR2_CP_CMP	CP_CMP shall switch the comparison reference (which can toggle CP_CMP output) based on VBG2 when BIST_REF_EN is high	
	HWSR2_AGND_OW_DET	AGND_OW_DET shall switch the comparison reference (which can toggle AGND_OW_DET output) based on VBG2 when BIST_REF_EN is high	switch B0/B1?
	HWSR1_CMP_BIST_CTRL	CMP_BIST_CTRL shall be reset when CLK_32M_OK is low	
	HWSR7_COMM_REG	BIST_GO shall be defined in COMM_REG	
	HWSR2_CMP_BIST_CTRL	CMP_BIST_CTRL shall output 400us BIST_REF_EN high pulse and 200us BIST_REF_EN_EARLY high pulse when BIST_GO is detected	
	HWSR3_CMP_BIST_CTRL	CMP_BIST_CTRL shall output clr_BIST_GO after BIST_GO is detected	
	HWSR4_CMP_BIST_CTRL	before BIST_REF_EN_EARLY turns low, CMP_BIST_CTRL shall check if VAA_OVUV, VDD_OVUV_BIST, CP_OVUV, AGND_OW are all 1 within 50us, if any is 0, output CMP_FLT	
	HWSR11_FLT_REG	CMP_FLT shall be defined in FLT_REG	
TSR025	HWSR1_FLT_SUM	SYS_FLT, POWER_FLT, CELL_OVUV_FLT, GPIO_OTUT_FLT, COMM_FLT,GAP_FLT,C_OW_FLT shall be defined in FLT_SUM	
	HWSR2_FLT_SUM	Each fault flag in FLT_SUM shall combine corresponding inputs	
	HWSR3_FLT_SUM	Inputs for FLT_SUM shall support being masked by separate mask control from MSK	
TSR028	HWSR1_COMS_TONE_RX	**COMS** _TONE_RX shall output HB_TONE_DET when HB TONE is received. HB Tone should only be detected during SLEEP mode. HB Tone should be detected after 20-30 couplets of logic-0 are detected. COMS_TONE_RX shall not output HB_TONE_DET before make sure all the tones is received.	
	HWSR1_TONE_CTRL	TONE_CTRL shall detect the period timing of HB_TONE_DET when SLEEP is high and output HB_TONE_TO if >800ms or HB_TONE_FAST if <200ms at HB_TONE_FLT	
	HWSR12_FLT_REG	HB_TONE_TO and HB_TONE_FAST shall be defined in FLT_REG	

TSR ID	HWSR ID	Description	Note
TSR030	HWSR1_TBYTE_DET	There shall be a TBYTE counter based on 32M in TBYTE_DET to count the period (8.375+STACK_RESP_CMD) of received communication frame bytes The TBYTE counter shall count for both command frame and response frame The TBYTE counter shall re-count byte by byte The TBYTE counter shall be reset when FRAME_DONE or FR_CRC_FLT is high Once TBYTE <0.875(8.375+STACK_RESP_CMD)/CLK_32M, output TBYTE_FAST high pulse at TBYTE_FLT Once TBYTE >1.125(8.375+STACK_RESP_CMD)/CLK_32M, output TBYTE_TO high pulse at TBYTE_FLT	
	HWSR13_FLT_REG	TBYTE_FLT shall be defined in FLT_REG	