

Technical Requirement

WP as Prerequisites	Author of TR
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ITEM	TR ID	Description
Compatibility	TR000	BM02A should have pin to pin compatibility with xx718 (BB pin can be NC)

ITEM	TR ID	Description
Operation Mode	TR001	<p>BM02A shall have 3 operating modes:</p> <p>The average current consumption of BM02A and its BOM from PACK+ during active mode shall <10mA at full temp</p> <p>The average current consumption of BM02A with OVUV&OTUT detection every 1s and its BOM from PACK+ during sleep mode shall <100uA at full temp</p> <p>The average current consumption of BM02A and its BOM from PACK+ during shutdown mode should <10uA at room temp</p>
Operation Mode	TR002	The time from opearating mode switching signal received to operating mode switching done of BM02A shall <10ms at full temp
Operation Mode	TR003	The direct operating mode switching of BM02A shall support: shutdown mode<-sleep mode, shutdown mode<->active mode, sleep mode<->active mode
Operation Mode	TR004	12 daisy-chained BM02As shall support being switched to active mode from sleep or shutdown mode within 100ms with signal pattern received from MCU at full temp
Operation Mode	TR005	12 daisy-chained BM02As shall support being switched to shutdown mode from sleep or active mode within 100ms with signal pattern received from MCU at full temp
Operation Mode	TR006	12 daisy-chained BM02As shall support being switched to sleep mode from active mode within 100ms with signal pattern received from MCU at full temp
Operation Mode	TR007	<p>The active mode entrance signal pattern detection of BM02A shall reuse communication port</p> <p>The active mode entrance detection of BM02A shall use noise free signal pattern w.r.t 50% magnitude and 10% occurrence</p> <p>The active mode entrance signal pattern detection of BM02A shall support both north and south communication direction</p>
Operation Mode	TR008	<p>The shutdown mode entrance signal pattern detection of BM02A shall reuse communication port</p> <p>The shutdown mode entrance detection of BM02A shall use noise free signal pattern w.r.t 50% magnitude and 10% occurrence</p> <p>The shutdown mode entrance signal pattern detection of BM02A shall support both north and south communication direction</p> <p>The shutdown mode entrance signal pattern detection of BM02A should be based on the edge detection of register bit</p>

ITEM	TR ID	Description
Operation Mode	TR009	<p>The sleep mode entrance signal pattern detection of BM02A shall reuse communication port</p> <p>The sleep mode entrance detection of BM02A shall use noise free signal pattern w.r.t 50% magnitude and 10% occurrence</p> <p>The sleep mode entrance signal pattern detection of BM02A shall support both north and south communication direction</p> <p>The sleep mode entrance signal pattern detection of BM02A should be based on the edge detection of register bit</p>
Operation Mode	TR010	<p>BM02A shall support hard digital reset signal pattern detection without digital core engagement during sleep/active mode</p> <p>The digital core of BM02A shall be reset when hard digital reset signal pattern is detected</p>
Operation Mode	TR011	<p>The time from hard and soft digital reset signal pattern received to digital core reset done of BM02A shall <10ms at full temp</p>
Operation Mode	TR012	<p>The hard and soft digital reset signal pattern detection of BM02A shall reuse communication port</p> <p>The hard and soft digital reset signal pattern detection of BM02A shall use noise free signal pattern w.r.t 50% magnitude and 10% occurrence</p> <p>The hard and soft digital reset signal pattern detection of BM02A shall support both north and south communication direction</p> <p>The soft digital reset signal pattern detection of BM02A should be based on the edge detection of register bit</p>
Operation Mode	TR013	<p>BM02A shall set fault flag in register bit when a programmable short frame communication timer timeout</p> <p>The fault flag register bit shall support being written to clear</p> <p>The fault flag shall support being masked from being set by register bit</p> <p>The timer shall support being programmed from 100ms to 1h with 8 steps, accuracy 5%, by register bit</p> <p>The timer shall start to count only during active mode</p> <p>The timer shall be reset when a frame is received</p>
Operation Mode	TR014	<p>BM02A shall enter shutdown mode(default)/sleep mode/or keep in active mode when a programmable long frame communication timer timeout</p> <p>The target operating mode when frame communication timer timeout shall support being selected by register bit</p> <p>The timer shall support being programmed from 100ms to 1h(default) with 8 steps, accuracy 5%, by register bit</p> <p>The timer shall start to count only during active mode</p> <p>The timer shall be reset when a frame is received</p>

ITEM	TR ID	Description
Operation Mode	TR015	BM02A shall enter active mode after digital core reset done The cause of digital reset excluding MCU's intention shall be recorded by register bit The register bit shall support being written to clear The fault flag shall support being masked from being set by register bit
Power Supply Capability	TR016	The power rail voltage of BM02A for thermal sensors shall have accuracy 10% during sleep/active mode at full temp The power rail for thermal sensors shall support 0-12 resistor dividers' as load (10k-200k)
Operation Voltage Range	TR017	BM02A shall support 9-100V DC input as power input for functional operation
Measurement	TR018	BM02A shall support the ADC measurement of 6-18 channel voltages (consists of 6-18 battery cell voltages plus 0-2 bus bar voltages), 0-12 thermal sensor voltage ratios, 0-12 auxiliary input voltages, die temperature during active mode The thermal sensor voltage ratios measurement should reuse digital IO pin The auxiliary input voltages measurement should reuse digital IO pin
Measurement	TR019	The connection of busbar shall support random location selected by register bit except top/bottom and adjacent 2 busbars for BM02A
Measurement	TR020	The spared channel without connection of battery cell shall support random location except bottom for BM02A
Measurement	TR021	The differential leakage into each measurement pin couplet (battery cells, busbars, thermal sensors, auxiliary inputs) of BM02A during measurement shall <1uA at full temp
Measurement	TR022	ADC accuracy of BM02A shall meet the spec under default measurement time (should <150us) as below: battery cell voltage and bus bar voltage measurement: <input type="checkbox"/> ±1mV accuracy (1.5V to 4.5V, 25°C) <input type="checkbox"/> ±3mV accuracy (1.5V to 4.5V, 0°C to +65°C) <input type="checkbox"/> ±5mV accuracy (1.5V to 4.5V, -20°C to +65°C) <input type="checkbox"/> ±5mV accuracy (3.3V, -40°C to +125°C) <input type="checkbox"/> ±10mV accuracy (-2V to 5V, -40°C to +125°C) (shall be guaranteed within 10 years) thermal sensor voltage ratio measurement <input type="checkbox"/> ±0.2% accuracy (10% to 90% VTREF, -20°C to +65°C) <input type="checkbox"/> ±0.48% accuracy (0 to 100% VTREF, -40°C to +125°C) auxiliary input voltage measurement: <input type="checkbox"/> ±5mV accuracy (1.5V to 4.5V, -20°C to +65°C) <input type="checkbox"/> ±12mV accuracy (0V to 5V, -40°C to +125°C) die temperature measurement: <input type="checkbox"/> ±5°C accuracy (-40°C to +125°C)

ITEM	TR ID	Description
Measurement	TR023	The skew time of all stack 216(18x12) channel voltages' ADC measurement when one command received from MCU should <200us and shall <1ms at full temp ADC accuracy of battery cell voltage and bus bar voltage measurement shall meet the spec under the <1ms skew time: $\pm 3\text{mV}$ accuracy (1.5V to 4.5V, 25°C)
Measurement	TR024	The skew time of all stack 144(12x12) thermal sensor voltage ratios' ADC measurement with one command received from MCU should <200us and shall <12ms at full temp
Measurement	TR025	The duration time from single measurement starting command of all 12 daisy-chained BM02As' 216(18x12) channel voltages is received from MCU to all these ADC measurement data are received by MCU shall <10ms at full temp The duration time from continuous measurement freeze command of all 12 daisy-chained BM02As' 216(18x12) channel voltages is received from MCU to all these ADC measurement data are received by MCU shall <10ms at full temp
Measurement	TR026	The ADC measurement data of each channel of BM02A shall only be updated till new measurement data of this channel is available
Measurement	TR027	The all ADC measurement data of BM02A shall support being read with one command received from MCU
Measurement	TR028	There shall be information for MCU to judge if the read ADC measurement data is newly updated
Measurement	TR029	The measurement data stored in registers of BM02A should be filtered to <-3dB from battery cell voltage noise those frequencies > f_c The f_c should be programmable from typical 10Hz to 1kHz with 8 steps by register bit
Communication	TR030	The communication of BM02A shall support xx600 communication protocol
Communication	TR031	The communication of BM02A shall support daisy-chained BM02As isolated by typical 2.2nF capacitors and min 150uH max 1.4mH transformer

ITEM	TR ID	Description
Communication	TR032	<p>The error rate of communication should <0.001% during communication burn-in test</p> <p>For the communication burn-in test, BM02A devices shall be isolated by 2m communication cable plus caps only, transformers only, or cap+choke</p> <p>6 daisy-chained BM02A devices shall burn-in 8h at -40°C, 25°C, 125°C</p> <p>12 or 24 daisy-chained BM02A devices shall burn-in 24h at 25°C</p>
Communication	TR033	The specified single BM02A device shall support being read at least 128 bytes registers with continuous addresses by one command received from MCU
Communication	TR034	The specified single BM02A device shall support being written at least 16 bytes writable registers with continuous addresses by one command received from MCU
Communication	TR035	The whole stack BM02A devices shall support being read at least 128 bytes registers with continuous addresses by one command received from MCU
Communication	TR036	The whole stack BM02A devices shall support being written at least 16 bytes writable registers with continuous addresses by one command received from MCU
Communication	TR037	The device addresses of 12 daisy-chained BM02As shall support being identified by MCU
Communication	TR038	The identified device addresses of BM02A should be kept during all operating mode unless being identified by MCU again or power off
Communication	TR039	The communication between adjacent BM02As shall pass BCI 300mA test (no communication fault)
Communication	TR040	When ring architecture is used, if one any communication node is open among 12 daisy-chained BM02As and transceiver, all daisy-chained BM02As shall still support being written and read by MCU
Communication	TR041	When the isolators configuration are same for each BM02A, the difference of average communication current consumption among all 12 daisy-chained BM02As should <1mA
Cell Balance	TR042	Passive cell balance for each battery cell of BM02A shall be available when MCU requests during both active and sleep mode, no matter battery cell/busbar use separate balance channels or busbar+battery cell share two adjacent balance channels

ITEM	TR ID	Description
Cell Balance	TR043	<p>BM02A shall support at least 9 battery cell channels' balance at the same time when MCU requests</p> <p>Only enabled channel can be balanced, BM02A should support both automatic channel selection and manual channel selection by register bit</p> <p>For automatic mode, the enabled channels should be default odd or even channels group, during manual mode, each channel should support being selected by register bit</p>
Cell Balance	TR044	<p>Maximum passive cell balance current of BM02A should >300mA and shall >240mA for each battery cell channel when no adjacent cells balancing, $R_B=10\Omega$, $V_{cell}=5V$, $T_a=85^\circ C$</p> <p>Delta Tc of BM02A with 9 channels' 240mA balance current shall <20°C at $T_a=85^\circ C$</p>
Cell Balance	TR045	<p>Cell balance of BM02A shall start (timer shall start to count and the balance current shall be on) by register bit</p>
Cell Balance	TR046	<p>BM02A shall provide programmable cell balance time threshold by register bit for each battery cell channel, the biggest value of threshold shall >12h, step 1s-1min, accuracy 5% at full temp</p> <p>The default value of time threshold for each battery cell channel shall be the biggest</p> <p>When timer touches any programed time threshold, the balance of this channel shall be stopped (timer shall go on to count and the balance current shall be off)</p>
Cell Balance	TR047	<p>Cell balance of BM02A shall support being paused (timer shall hold and the balance current shall be off) when junction temperature is over programmable CB_TWARN threshold by register bit, 100°C-150°C, 5°C step, accuracy 5°C</p> <p>When junction temperature is under the hys 10°C, the balance shall be resumed (timer shall go on to count and the balance current shall be on)</p>
Cell Balance	TR048	<p>Cell balance of BM02A shall support being paused (timer shall hold and the balance current shall be off) when any thermal sensor channel is over programmable CB_OT threshold by register bit, 5%-36%, 1% step, 1% accuracy at full temp</p> <p>The detection period of CB_OT should share same configuration with OTUT detection</p> <p>BM02A shall have two programmable CB_OT thresholds sharing same threshold range to be selected by register bit for each thermal sensing channel</p> <p>When all thermal sensor temperatures are under the hys 2%, the balance shall be resumed (timer shall go on to count and the balance current shall be on)</p>

ITEM	TR ID	Description
Cell Balance	TR049	Cell balance of BM02A shall support being paused (timer shall hold and the balance current shall be off) manually by register bit When this register bit is toggled, the balance shall be resumed (timer shall go on to count and the balance current shall be on)
Cell Balance	TR050	Cell balance of BM02A shall support being paused (timer shall hold and the balance current shall be off) when channel voltage ADC measurement is ongoing When channel voltage ADC measurement is not ongoing, the balance shall be resumed (timer shall go on to count and the balance current shall be on)
Cell Balance	TR051	Cell balance of BM02A shall support being stopped (timer shall clear and the balance current shall be off) when any unmasked fault flag is set in register
Cell Balance	TR052	The odd group and even group of battery cell channels shall be switched alternately during automatic mode The switching period should be programmable by register bit, range 5s-30min, 8 steps, accuracy 5% at full temp
Cell Balance	TR053	BM02A shall support programmable average cell balance current by register bit, range 12.5%-100% maximum cell balance current value, step 12.5%, accuracy 5% at full temp The cell balance current should be averaged within every 0.2s duration
Cell Balance	TR054	BM02A shall provide information about remaining balance time for each channel by register bit BM02A shall provide balance current on/off indication (excluding on/off due to averaging) for each channel by register bit BM02A shall provide the cell balance pause/stop status (excluding MCU's intention) in register bit
Reversely Wake Up	TR055	The OVUV for each battery cell channel shall be detected by BM02A periodically during sleep mode The period of OVUV detection shall support being programmable by register bit, from 200ms to 8s, 200ms step, accuracy 5% at full temp
Reversely Wake Up	TR056	The OTUT for each thermal sensor channel shall be detected by BM02A periodically during sleep mode The period of OTUT detection shall support being programmable by register bit, from 200ms to 8s, 200ms step, accuracy 5% at full temp
Reversely Wake Up	TR057	The OVUV detection period and OTUT detection period shall support being programmed respectively

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Reversely Wake Up	TR058	<p>The detected OVUV&OTUT fault for each channel shall be recored in register bit</p> <p>The fault flag register bit shall support being written to clear</p> <p>The fault flag shall support being masked from being set by register bit</p>
Reversely Wake Up	TR059	<p>The OVUV and OTUT detection of BM02A for each channel shall have fixed typical 150us deglitch time which counts from fault occurs to fault flag set in register</p>
Reversely Wake Up	TR060	<p>Battery cell channel OVUV detection of BM02A shall meet 60mV accuracy at full temp</p> <p>Battery cell channel OVUV detection threshold shall be programmable by register bit, OV:2V-5V, 25mV step and UV: 0.7V-3.875V, 25mV step</p>
Reversely Wake Up	TR062	<p>Thermal sensor OTUT detection of BM02A shall meet 1% accuracy at full temp</p> <p>Thermal sensor OTUT detection threshold shall be programmable by register bit, OT:5%-36%, 1% step and UT:76%-90%, 2% step</p>
Reversely Wake Up	TR063	<p>BM02A shall have two groups of OTUT programmable thresholds sharing same threshold range for each thermal sensing channel</p> <p>For each thermal sensing channel, the threshold group shall support being selected by register bit</p>
Reversely Wake Up	TR064	<p>The differentail leakage into each OVUV&OTUT comparison pin couplet (battery cells, thermal sensors) of BM02A during comparison shall <1uA at full temp</p>
Reversely Wake Up	TR065	<p>Among 12 daisy-chianed BM02As, any BM02A with any OVUV&OTUT fault flag set in registers shall actively send out wake signal to MCU only during sleep mode</p> <p>The time from any OVUV&OTUT fault flag is set in registers to wake signal is received by transceiver shall <100ms at full temp</p>
Digital IO	TR067	<p>BM02A shall have 12 digital IO channels</p>
Digital IO	TR068	<p>The each digital IO of BM02A shall support being selected as push-pull output or digital input by register bit during active mode</p>
Digital IO	TR069	<p>When the digital IO of BM02A is configured as push-pull output:</p> <p>Digital IO shall be pulled to >4V at 1mA load current within 1ms when logic high enabled and pulled to <0.4V at 1mA sink current within 1ms when logic low enabled by register bit at full temp</p> <p>The output current limit of each digital IO shall have typ 8mA at full temp</p>

ITEM	TR ID	Description
Digital IO	TR070	<p>When the digital IO of BM02A is configured as digital input: The input of digital IO shall be detected as logic low when <1V within 1ms and logic high when >2.5V within 1ms at full temp The logic input detection result of each digital IO shall be indicated in register bit The leakage of digital IO shall <1uA at full temp</p>
I2C Master	TR071	<p>BM02A shall support reading and writing the I2C slave 24C02 (E2PROM) of during active mode The reading and writing of I2C slave 24C02 should reuse digital IO pin</p>
Others	TR072	<p>The die X-Y location on wafer and lot information during production for each BM02A chip shall be stored in NVM for customer read ONLY The version ID should be read ONLY for customer</p>
Others	TR073	BM02A shall pass AEC-Q100 Grade1 qualification
Others	TR074	BM02A shall pass ESD HBM: 2kV ESD CDM: 750V for corner pins, 500V for other pins Latch-up: ±200mA
Others	TR075	Maximum die size of BM02A shall <25mm ²
Others	TR076	Package of BM02A shall be LQPF 10x10-64 with thermal pad
Others	TR077	FT time @ room temp for BM02A shall <6s
Others	TR078	BM02A shall survive during 80V(5Vx16) battery pack random hot-plug
Maintain	TR079	<p>If the number of open wire faults for FPC (including channel harness and thermal sensor harness) <=2, the fault flag in register bit shall provide the accurate location information The register bit shall support being masked from being set by register bit The register bit shall support being written to clear</p>
Measurement	TR080	The measurement accuracy of battery cell voltage shall be kept when -2V<VBAT-VC18
Balance	TR081	The mismatch of balance current for each separately enabled channel shall <10mA at 4.25V under same temp
Measurement	TR082	The measurement of both cell voltage and auxiliary input voltage shall pass 300mA BCI test (error<10mV)
Operation Mode	TR083	<p>BM02A shall support soft digital reset signal pattern detection during active mode The digital core of BM02A shall be soft reset (The identified device addresses shall be kept) when soft digital reset signal pattern is detected</p>

ITEM	TR ID	Description
Operation Mode	TR084	12 daisy-chained BM02As should support being hard digital reset from sleep or active mode to active mode within 20ms with signal pattern received from MCU at full temp
Bridge Interface	TR085	Half-duplex SPI(MISO/MOSI/SCLK/CSB/SPI_RDY/FLTb) interface reusing GPIO pins shall be provided by BM02A
Bridge Interface	TR086	The voltage level of SPI shall support 3.3V.
Bridge Interface	TR087	BM02A shall support being waked up into active mode from shutdown mode by MOSI wake up pattern detection (as bridge)
Bridge Interface	TR088	Once BM02A is waked up into active mode from shutdown mode by active mode entrance signal pattern detection from daisy chain communication port, all MOSI pattern detection shall be disabled
Bridge Interface	TR089	SPI interface shall take over the daisy chain communication (except tone communication) of either south (default) or north (shall support being selected by register bit) port once BM02A is waked up by MOSI wake up pattern detection
Bridge Interface	TR090	When BM02A is waked up by MOSI wake up pattern detection, FLTb pin shall be asserted when any unmasked fault flag is set in register
Bridge Interface	TR091	Only bridge BM02A shall support being hard digital reset by MOSI wake up pattern detection during shutdown mode or sleep mode or active mode
Bridge Interface	TR092	Only bridge BM02A shall support being shutoff into shutdown mode from active mode or sleep mode by MOSI shutdown pattern detection
Bridge Interface	TR093	Only bridge BM02A shall support being waked up into active mode from sleep mode by MOSI sleep to active pattern detection
Bridge Interface	TR094	The bridge BM02A shall support wake up whole 12 daisy-chained BM02As from shutdown mode
Bridge Interface	TR095	The bridge BM02A shall support hard digital reset whole 12 daisy-chained BM02As
Bridge Interface	TR096	The SCLK frequency of SPI interface shall support 2-6MHz
Bridge Interface	TR097	The new command frame identification of SPI interface should be based on falling edge of CSB TX FIFO and TX FIFO should be reset after SPI communication clear pattern is detected

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Communication	TR098	The command frame propagation of top device defined in the daisy-chained BM02As shall support being disabled by register bit.
Bridge Interface	TR099	The bridge BM02A shall support wake up whole 12 daisy-chained BM02As from sleep mode
Bridge Interface	TR100	SPI_RDY shall be high to inform host that TX FIFO is ready for reading to avoid overflow and underflow internal 8-byte TX FIFO SPI_RDY shall be high to inform host that RX FIFO is ready for writing to avoid overflow of internal 8-byte RX FIFO
Bridge Interface	TR101	During device reading mode, MOSI shall be ignored by BM02A During device writing mode, MISO shall be ignored by host SPI interface of BM02A shall be default device writing after the detection of communication clear pattern Once valid read command is detected, SPI interface of BM02A shall turn to device reading Once TX FIFO is empty and reading timeout, SPI interface of BM02A shall turn back to device writing
Bridge Interface	TR102	BM02A shall start propagate received first byte of command frame in RX FIFO from host's SPI to BM02A's daisy-chain UART within 1us The extra delay time between characters shall be programmable from 0.25us-15.75us with 64 steps BM02A shall only store received bytes of response frame from BM02A's daisy-chain UART into TX FIFO, and only propagate data in TX FIFO to host's SPI until read command is detected by BM02A, SPI_RDY is high and SCLK is toggled
Bridge Interface	TR103	Each bit should be captured on low to high clock transitions and propagated on high to low clock transition Default SCLK shall be logic-0, MOSI and MISO shall be logic-1 For each byte at SPI interface, MSB shall be transmitted first