CONF_REG_CRC_DET IP SPEC

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Introduction

Check the CRC value of configure registers and MTP shadow registers every 2ms, if no right, output CONF_REG_CRC_FLT is high.

Feature

Monitor the configure registers and MTP shadow register to ensure all values are right.

Register Definition

Register Map

Table 1 1CONF_REG_CRC_DET Register Map

Name	Add	D7	D6	D5	D4	D3	D2	D1	D0	default
CONF_ CRC_H	0x2000	CONF_CRC[15:8]								0x00
CONF_ CRC_L	0x2001	CONF_CRC[7:0]								0x00
SYS_FLT2	0x5114			CONF_ CRC						0x00

Functional Details

Block Diagram

The following diagram shows the CONF_REG_CRC_DET inputs and outputs.

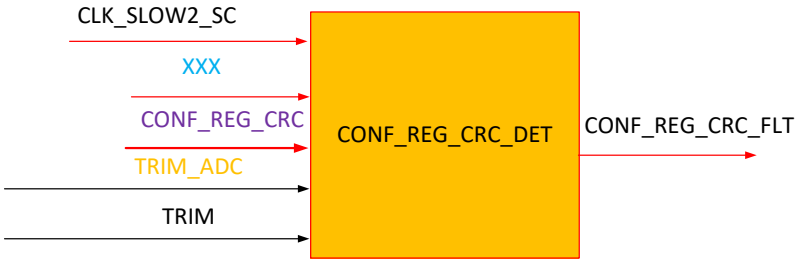

Figure1 CONF_REG_CRC_DET diagram

Module input/output list

Name	Dir	Width	Discirption	duration
CONF_REG_CRC_FLT	O	1	Configuration register crc fault bit	Level(CLK_SLOW2 domain)
CLK_SLOW2_SC	I	1	Redundant CLK_SLOW	256KHz, 50%duty
resetb_SR_CLK_SLOW	I	1	Scan_muxed resetb and soft resetb for CLK_SLOW domain	level

load_done	I	1	MTP load done	Level(CLK_MTP domain)
pulse_SLOW2_2ms	I	1	2ms pulse in CLK_SLOW2 domain	1 CLK_SLOW2
reg0000~001E	I	8*31	Configuration registers 0000~001E	Level(CLK_REG domain)
reg0100~0117	I	8*24	Configuration registers 0100~0117	Level(CLK_REG domain)
TM_REG1~TM_REG10	I	8*10	Configuration registers 0800~0809	Level(CLK_REG domain)
reg1000~107F	I	8*128	Configuration registers 1000~107F (MTP shadow registers)	Level(CLK_REG domain)
CONF_CRC	I	16	Configuration registers 2000~2001	Level(CLK_REG domain)

Clock Domain

The clock for CONF_REG_CRC_DET is CLK_SLOW2_SC. (HWSR2_CONF_REG_CRC_DET)

CONF_REG_CRC_DET function description

IBM algorithm with polynomial (x16+x15+x2+1) and default value 16'hFFFF is used for CRC.
CONFIG_adr[13:0] is defined that goes through all configuration registers and MTP shadow registers, i.e., 16'h0000~16'h001E, 16'h0100~0117, 16'h0800~0809, 16'h1000~107F and 16'h 2000~2001.
CONFIG_data[7:0] changes to corresponding register value every time CONFIG_adr changes.
CRC calculator updates every time CONFIG_data[7:0] changes. Once CONFIG_adr[13:0] went through all the registers, check the calculator result, if not 0, CONF_REG_CRC_FLT is high.
(HWSR1_CONF_REG_CRC_DET)