C_OW_CTRL

REVISION HISTORY

Revision Number	Date	Description of Change	Author
V0.0	10/12/2022	Draft version	Taoli

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C_OW_CTRL

Introduction

C_OW_CTRL generates current control signals CS_EN_AUTO_SINK and CS_EN_AUTO_SOURCE, outputs twice ADC single conversion start(C_OW_ADC_GO) and monitors whether ADC measurement results exceed the specified voltage range.

Main features

The C_OW_CTRL module has the following features:

- Programmable current time up to 32ms by 2ms per step
- Independent over range flag for each CELL

Functional Details

Block Diagram

C_OW_CTRL block diagram shows in Fig1.

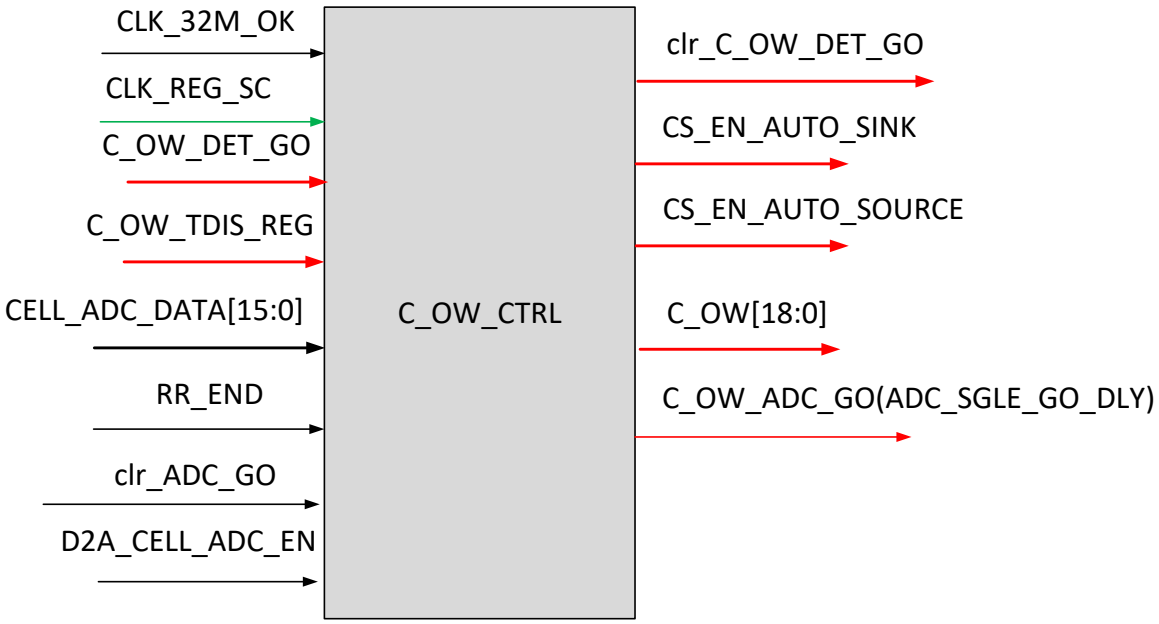

Fig 1 C_OW_CTRL control flow Diagram

C_OW_CTRL I/O signals description shows in table.

Pin Name	Direction	Width	Default Value	Duration	Description
resetb_SR_CLK	Input	1b'	1'b1	N/A	Asynchronous power on reset, release synchronously in CLK_32M domain.

rstb_32M_ok_and _sr	Input	1b'	1'b1	N/A	soft reset, CLK_32M_OK low reset
SOFT_RSTB_REG	Input	1b'	1'b1	N/A	soft reset; release synchronously in CLK_32M domain.
CLK_REG_SC	Input	1b'	1'b0	125ns	8MHZ
CLK_32M_OK	Input	1b'	1'b0	N/A	CLK_32M_OK
C_OW_DET_GO	Input	1b'	1'b0	N/A	C_OW_CTRL star
clr_ADC_GO	Input	1b'	1'b0	8us	ADC_GO clear
RR_END	Input	1b'	1'b0	8us	Round-robin end flag
C_OW_TDIS_REG	Input	4b'	4'h0	N/A	C_OW_TDIS_REG shall cover from 2ms to 32ms 4'h0: 2ms 4'h1: 4ms 4'h2: 8ms … 4'h15: 32ms
CELL_ADC_DATA_CH1 - CELL_ADC_DATA_CH18	Input	16b'	16'h8000	N/A	ADC converted data of CELL1-CELL18 without DLPF
C_OW_FLT	Output	19b'	19'h0	N/A	Over range flags
clr_C_OW_DET_GO	Output	1b'	1'b0	1 CLK_REG	C_OW_DET_GO clear signal
CS_EN_AUTO_SINK	Output	1b'	1'b0	3*TDIS	
CS_EN_AUTO_SOURCE	Output	1b'	1'b0	1*TDIS	
C_OW_ADC_GO	Output	1b'	1'b0		ADC single conversion go, it is cleared by clr_ADC_GO

Control flow

C_OW_CTRL work control flow shows in Fig2. C_OW_CTR only loads C_OW_TDIS_REG to C_OW_TDIS when C_OW_DET_GO is high and keep the value. Besides, CS_EN_AUTO_SINK is set to 1 when C_OW_DET_GO is detected high. After 3*(C_OW_TDIS+1)*2ms time delay, C_OW_ADC_GO is set to 1 the first time to start Cn open wire detection. C_OW_ADC_GO is cleared to 0 by clr_ADC_GO generated by ADC_CTRL. Until a single round-robin conversion is finished(RR_END from ADC_CTRL is asserted), CS_EN_AUTO_SINK can be cleared to 0 and CS_EN_AUTO_SOURCE will be asserted. When the first RR_END is high, it compares measurement result of CELL1 with 0.1V, the other CELL results compare with -0.4V, any CELL measurement result over range will be recorded to C_OW[18:1], After a delay of C_OW_TDIS*2ms time, C_OW_ADC_GO is set to 1 the second time. Until a single round-robin conversion is finished(RR_END from ADC_CTRL is asserted), CS_EN_AUTO_SOURCE can be cleared to 0. When the second RR_END is high, it only compares measurement result of CELL1 with -0.4V, if the measurement over range C_OW[0] will be asserted high.

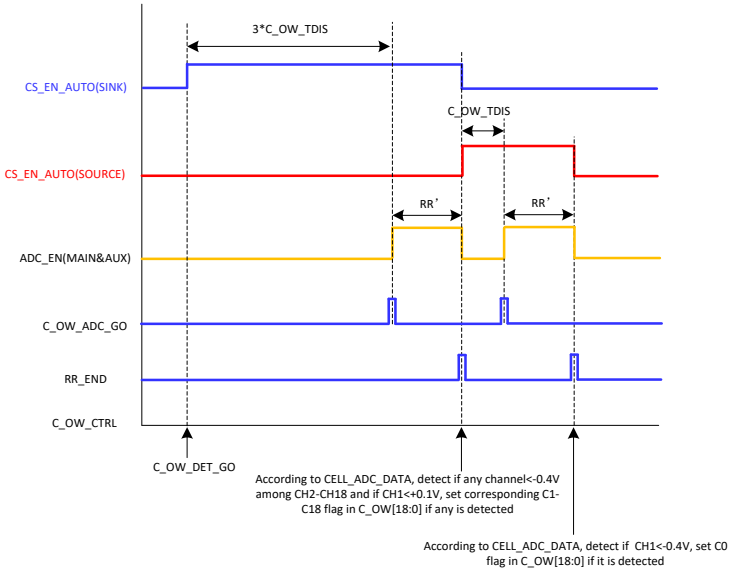

Fig 2 C_OW_CTRL control flow Diagram

State Machine

C_OW_CTRL is mainly implemented by a state machine shows in Fig3.

As shown in Fig3, C_OW_AUTO1_STAT controls to generate CS_EN_AUTO_SINK and the first C_OW_ADC_GO, C_OW_AUTO2_STAT controls to generate CS_EN_AUTO_SOURCE and the second C_OW_ADC_GO. The c_ow_cnt is the delay counter, which is automatically incremented by one when another counter(counter_2ms) reaches 14'd16000. The c_ow_cnt is cleared to 0 when RR_END is high or CLK_32M_OK is low.

C_OW_CTRL state machine will be reset when CLK_32M_OK is low. The state machine switches to C_OW_AUTO1_STAT state from IDLE state when C_OW_DET_GO is high, and exit from C_OW_AUTO1_STAT state to C_OW_AUTO2_STAT state by swap1 is valid(c_ow_cnt more than 3*C_OW_TDIS and RR_END is high), then return to IDLE state by swap2 is valid(c_ow_cnt more than C_OW_TDIS and RR_END is high). When the state machine enters the C_OW_AUTO1_STAT state, a clr_C_OW_DET_GO signal is generated to clear clr_C_OW_DET_GO to 0.

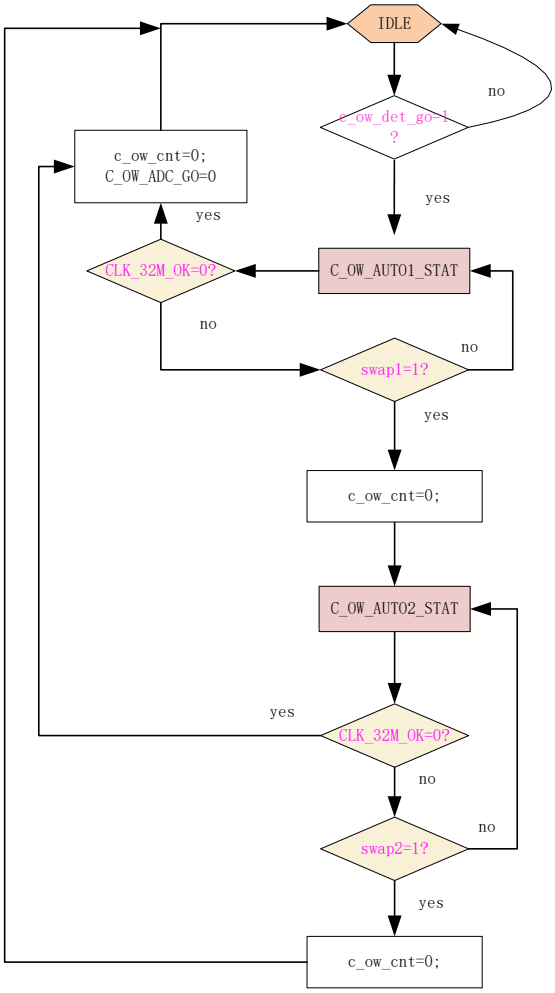

Fig 3 C_OW_CTRL state machine flow

If ADC is busy, in order to obtain correct Cn open wire measurement results, it is advised to disable ADC before write 1 to the DLAG_CTRL1[C_OW_DET_GO] bit.