Hardware Requirement

WP as Prerequisites
TR_v0.3
ARCH_v0.1

Author of HWR
Sean Wu, Snow Wang, Lei Nie, Lei Cao

TR ID	HWR ID	Description	Note
TR0_00, TR2_00, TR4_00, TR5_00, TR10_01	HWR_00_DRIVE	LDOIN pin **shall** be powered by external BJT, which is drived by DRIVE from PACK+	
TR2_00, TR4_00, TR5_00	HWR_01_DRIVE	LDOIN pin **shall** be powered to 5.7V with 5% accuracy at full temp	
TR1_00	HWR_02_DRIVE	The current consumption of DRIVE **shall** <4uA at room temp	
TR2_00, TR4_00, TR5_00, TR5_01	HWR_03_DRIVE	The current-limiting of DRIVE pin **shall** be 2mA(typ), 1mA(min) considering beta of BJT=200	
TR1_02	HWR_04_DRIVE	DRIVE block **shall** be always on during all operating modes	
TR3_00	HWR_05_DRIVE	The UVLO threshold of BAT in DRIVE block **shall** <9V at full temp	
TR1_01, TR1_02	HWR_06_DRIVE	When LDOIN is set up, DRIVE block **shall** output LDOIN_OK to H The LDOIN_OK threshold **shall** <5.3V at room temp The hysteresis of LDOIN_OK threshold **shall** be 100mV The deglitch time of LDOIN_OK **shall** be typ 600us	
TR1_01, TR1_02	HWR_07_DRIVE	When LDOIN is set up, DRIVE block **shall** output current source I_START with 30% accuracy	
TR2_00, TR4_00, TR5_00, TR5_01	HWR_08_DRIVE	When jucntion temperature >150℃, DRIVE **shall** output short DRIVE to GND When jucntion temperature >150℃, DRIVE **shall** output TSD high The thermal sensor in DRIVE **shall** be next DRIVE and VAA in layout	
TR5_00, TR5_01	HWR_09_DRIVE	DRIVE **shall** output 1/2xLDOIN as LDOIN_HALF	
TR4_04	HWR_01_DRIVE	DRIVE **shall** output PREREF	
TR0_00, TR4_04	HWR_00_VAA	VAA **shall** be powered from LDOIN The bias current of VAA **shall** be I_START The refer voltage of VAA **shall** be PREREF when BG_OK is L, and **shall** switch to BG when BG_OK is H	
TR4_04	HWR_01_VAA	VAA pin **shall** be regulated to 5V with 2% accuracy at full temp	
TR1_00	HWR_02_VAA	The current consumption of VAA **shall** <5uA at full temp	

TR ID	HWR ID	Description	Note
TR4_04	HWR_03_VAA	The current-limiting of VAA **shall** >20mA at full temp	
TR1_00	HWR_04_VAA	VAA **shall** be off when SDB is low	
TR1_01, TR1_02	HWR_05_VAA	VAA **shall** build within 0.5ms when LDOIN_OK is H	
TR1_02	HWR_06_VAA	When VAA is set up, VAA **shall** output VAA_OK to H	
TR0_00, TR4_00, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_00_VDD	VDD **shall** be powered from LDOIN The bias current of VDD **shall** be I_REF The refer voltage of VDD **shall** be BG	
TR4_00, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_01_VDD	VDD pin **shall** be regulated to 1.8V with 5% accuracy at full temp	
TR1_00	HWR_02_VDD	The current consumption of VDD **shall** < 5uA at full temp	
TR4_00, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_03_VDD	The current-limiting of VDD **shall** >10mA at full temp	
TR1_00	HWR_04_VDD	VDD **shall** be off when SDB is low	
TR1_01, TR1_02	HWR_05_VDD	VDD **shall** build within 0.5ms when LDOIN_OK is H and IREF_OK is H	
TR1_02	HWR_06_VDD	When VDD is set up, VDD block **shall** output VDD_OK to H	
TR4_12, TR6_00	HWR_00_CP	CP **shall** be powered from BAT The bias current of CP **shall** be I_REF CP **shall** use CLK_256K to generate a delay, which is used for high side floating power rail building	

TR ID	HWR ID	Description	Note
TR4_04, TR4_12, TR6_00	HWR_01_CP	CP **shall** output VCP to typ BAT+5V when no-load VCP **shall** >BAT+3V when the load is 300uA The ripple of VCP **shall** <300 mV when the load is 300uA	
TR1_00	HWR_02_CP	The current consumption of a block named CP **shall** <50uA at full temp	
TR1_00	HWR_03_CP	CP **shall** be off when all of ACT, MON_WAKE and CB_EN is L	
TR1_02	HWR_04_CP	CP **shall** start work when IREF_OK is H and CLK_256K_OK is H	
TR0_00, TR4_04	HWR_00_REFP	REFP **shall** be powered from VAA REFP **shall** output REFP ref to REFN The bias current of REFP **shall** be I_REF	
TR4_04	HWR_01_REFP	REFP-REFN **shall** be typ 2.5V with 0.5‰ accuracy at room temp REFP-REFN **shall** be trimmed by TRIM REFP **shall** use CLK_256K as the clock for auto-zero and sample hold The temp drift of REFP-REFN **shall** <5ppm/℃ The long term drift of REFP-REFN **shall** <20ppm/sqr(khr)	
TR1_00	HWR_02_REFP	The current consumption of REFP **shall** <90uA at full temp	
TR4_04	HWR_03_REFP	The current-limiting of REFP **shall** >10mA at full temp	
TR1_00	HWR_04_REFP	REFP **shall** be off when all of ACT, MON_WAKE is L	
TR1_02	HWR_05_REFP	REFP **shall** start work when IIREF_OK is H, CLK_256K is H and IREF_OK is H	
TR1_02	HWR_06_REFP	When REFP is set up, REFP block **shall** output REFP_OK to H	
TR2_00, TR4_00, TR4_04, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_00_BG	BG **shall** be powered from VAA The bias current of BG **shall** be I_START	

TR ID	HWR ID	Description	Note
TR2_00, TR4_00, TR4_04, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_01_BG	BG **shall** be typ 1.22V with 0.5% accuracy at room temp BG **shall** be trimmed by TRIM The temp drift of VBG **shall** <50ppm/℃	
TR1_00	HWR_02_BG	The current consumption of BG **shall** <20uA at full temp	
TR1_00	HWR_03_BG	BG **shall** be off when SDB is low	
TR1_02	HWR_04_BG	BG **shall** start work when VAA_OK is H	
TR1_02	HWR_05_BG	When BG is set up, BG block **shall** output BG_OK to H	
TR0_00, TR2_00	HWR_00_TREF	TREF **shall** be powered from VAA The bias current of TREF **shall** be I_REF	
TR2_00	HWR_01_TREF	TREF pin **shall** be regulated to 2.5V with 10% accuracy at (10/12)kOhm ~200kOhm load at full temp	
TR1_00	HWR_02_TREF	The current consumption of TREF **shall** <20uA	
TR2_00	HWR_07_TREF	The current-limiting of TREF **shall** >10mA at full temp	
TR1_00	HWR_04_TREF	TREF **shall** be off when ACT is L and MON_WAKE is L	
TR1_01, TR1_02, TR7_00	HWR_05_TREF	TREF **shall** build within 0.5ms at full load range at 2.2uF when IIREF_OK is H	
TR1_02	HWR_06_TREF	When TREF is set up, TREF **shall** output TIREF_OK to H	
TR2_00, TR4_00, TR4_04, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_00_IREF	IREF **shall** powered by VAA Bias current of IREF **shall** be I_START The input refer voltage of IREF **shall** be VBG	

TR ID	HWR ID	Description	Note
TR2_00, TR4_00, TR4_04, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_01_IREF	The accuracy of IREF **shall** <10% at full temp The output of IREF **shall** be trimmed by TRIM	
TR1_00	HWR_02_IREF	The current consumption of IREF **shall** <3uA at full temp	
TR1_00	HWR_03_IREF	IREF **shall** be off when SDB is L	
TR1_02	HWR_04_IREF	IREF **shall** start work when BG_OK is H	
TR1_02	HWR_05_IREF	When IREF is set up, IREF **shall** output IIREF_OK to H	
TR4_04	HWR_00_VPTAT	VPTAT accuracy **shall** meet k(T+-4) (T is the absolute temperature of junction, Kelvin), T=233K-400K	
TR6_05	HWR_00_BE	The current source of BE block **shall** be I_REF	
TR6_05	HWR_01_BE	There **shall** be have 9 BE blocks on layout, each BE is placed near every two groups of CBFETs	
TR6_05	HWR_00_JOT_DAC	JOT_DAC shall output JOT_REF selected CB_TWARN_THRESH[3:0] by based on VBG	
TR6_05	HWR_01_JOT_DAC	JOT_REF **shall** meet the range and accuracy of CB_TWARN,100℃-150℃, accuracy is 5℃, step is 5℃	
TR4_00, TR4_04, TR5_00, TR6_00, TR7_00, TR8_00, TR9_00, TR10_00, TR11_00	HWR_00_CLK	CLK **shall** be powered by VDD Bias current of CLK **shall** be I_REF The refer voltage of CLK **shall** be VBG	
TR1_12, TR1_13, TR4_04, TR5_00, TR5_02	HWR_01_CLK	LCLK **shall** output CLK_256K with 5% accuracy at full temp The duty of CLK_256K **shall** be typ 50% CLK_256K **shall** be trimmed by TRIM	

TR ID	HWR ID	Description	Note
TR4_04, TR5_02	HWR_02_CLK	HCLK **shall** output CLK_32M with 5% accuracy at full temp CLK_32MHz **shall** be PLL based on CLK_256K	
TR6_05	HWR_03_CLK	LCLK block **shall** output JOT_CLK to JOT_CMP for periodical JOT check	
TR1_00	HWR_04_CLK	The current consumption of LCLK **shall** <10uA at full temp The current consumption of HCLK **shall** <150uA at full temp	
TR1_02	HWR_05_CLK	CLK **shall** work when IREF_OK and VDD_OK is H	
TR1_00	HWR_06_CLK	LCLK **shall** be off when SDB is L	
TR1_00	HWR_07_CLK	HCLK **shall** be off when all ACT and MON_WAKE is L	
TR1_02	HWR_08_CLK	When CLK_32M is established, CLK block **shall** output CLK_32M_OK	
TR1_02	HWR_09_CLK	When CLK_256K is established, CLK block **shall** output CLK_256K_OK	
TR1_02	HWR_10_CLK	CLK_256K, CLK_32M and CLK_32M_OK signal **shall** work as seq predefined	
TR1_02, TR1_06, TR1_10, TR5_00	HWR_00_SEQ	When WAKE_TONE_DET is H (rise edge), ACT **shall** be H, DRSTB **shall** be L last 8us and then set to H, SLEEP **shall** be L, SDB **shall** be H When STA_TONE_DET is H (rise edge) and SLEEP is H, ACT **shall** be H, SLEEP **shall** be L, SDB **shall** be H	
TR1_02, TR1_04, TR1_07, TR5_00	HWR_01_SEQ	When SD_TONE_DET is H (rise edge), SDB **shall** be L, ACT and SLEEP **shall** be L When D2A_TO_SD is H (rise edge), SDB **shall** be L, ACT and SLEEP **shall** be L	
TR1_02, TR1_05, TR1_08, TR5_00	HWR_02_SEQ	When D2A_TO_SLEEP is H (rise edge), SLEEP **shall** be H, ACT **shall** be L, SDB **shall** be H	
TR1_09, TR5_00	HWR_03_SEQ	DRSTB **shall** be L when CLK_256K_OK is L DRSTB **shall** be L when VAA_OK is L DRSTB **shall** be L when VDD_OK is L When DRSTB rises from L to H, ACT **shall** be H, SLEEP **shall** be L, SDB **shall** be H	

TR ID	HWR ID	Description	Note
TR1_13	HWR_04_SEQ	When LCTO_SET is H (rise edge) and LCTO_SEL[1:0]=ACT, ACT **shall** be H, SLEEP **shall** be L, SDB **shall** be H When LCTO_SET is H (rise edge) and LCTO_SEL=SLEEP, SLEEP **shall** be H, SLEEP **shall** be L, SDB **shall** be H When LCTO_SET is H (rise edge) and LCTO_SEL=SD, SDB **shall** be L, SLEEP and ACT **shall** be L， LCTO_SD **shall** be H	
TR1_02	HWR_05_SEQ	SEQ **shall** start work when LDOIN_OK is H The default value of SEQ **shall** be: ACT is L; SLEEP is L; SDB is H; DRSTB is L	
TR4_00	HWR_00_ADC	ADC **shall** be shut down when IREF_OK or REFP_OK is low Bias current of ADC **shall** be IREF	
TR4_00	HWR_00_MUX_HV	MUX_HV **shall** choose one pair among Cn-Cn-1(n=1-18) and gnd as MUX_OUT_HV according to CH_SEL	
TR4_12	HWR_01_MUX_HV	MUX_HV **shall** be powered from VCP	
TR1_00	HWR_02_MUX_HV	MUX_HV block **shall** only be enabled by D2A_CELL_ADC_EN	
TR4_00	HWR_00_MUX_LV	MUX_LV **shall** choose one pair among BAT_FB, VPTAT/GPIOn(n=0-11) and gnd as MUX_OUT_LV according to CH_SEL	
TR4_03	HWR_01_MUX_LV	Current flows into MUX_LV through BAT_FB, GPIO/VPTAT **shall** <0.1uA	
TR4_04	HWR_02_MUX_LV	MUX_LV **shall** support 0-5V / 0-100%* TREF input voltage range MUX_OUT_LV **shall** <REFP-REFN/TREF (according to GPIO_REF_SEL)	
TR1_00	HWR_03_MUX_LV	MUX_LV block **shall** only be enabled by D2A_CELL_ADC_EN	
TR4_04	HWR_04_MUX_LV	Accoding to GPIO_REF_SEL and CH_SEL to output ADC_REF: the reference voltage ADC_MODU used for Cn-Cn-1 /VPTAT/BAT_FB **shall** be REFP-REFN , typical value **shall** be 2.5V the reference voltage ADC_MODU used for GPIO absolute voltage measurement **shall** be REFP-REFN the reference voltage ADC_MODU used for GPIO voltage ratio measurement **shall** be TREF	

TR ID	HWR ID	Description	Note
TR4_00, TR4_04	HWR_00_BAT_VCM_GEN	BAT_VCM_GEN **shall** generate 1/2xVBAT (BAT_VCM) and 1/32xVBAT (BAT_FB) with less than 0.1% gain error	
TR4_00, TR4_04	HWR_01_BAT_VCM_GEN	BAT_VCM_GEN **shall** only be enabled by D2A_CELL_ADC_EN	
TR4_00, TR4_04	HWR_00_ADC_LV_SHT	ADC_LV_SHT **shall** use switching capacitors structure Input sampling switch **shall** be powered from VCP ADC_LV_SHT **shall** use ADC_CLK for switching caps	
TR4_00, TR4_04, TR4_13	HWR_01_ADC_LV_SHT	ADC_LV_SHT **shall** shift the common voltage of MUX_OUT_HV to BAT_VCM as ADC_INPUT_LV	
TR4_00, TR4_04	HWR_02_ADC_LV_SHT	ADC_LV_SHT **shall** scale the differential voltage of MUX_OUT_HV down to 1/2 as ADC_INPUT_LV	
TR4_12	HWR_03_ADC_LV_SHT	ADC_LV_SHT **shall** support VBAT+2V as input signal's max voltage	
TR4_03, TR7_07	HWR_04_ADC_LV_SHT	The differential input current at MUX_OUT_HV **shall** <1uA for ADC_LV_SHT	
TR4_04	HWR_05_ADC_LV_SHT	The offset of ADC_LV_SHT (output differential voltage -input differential voltage *0.5) **shall** <3mV (4 sigma) The offset variation **shall** <0.5mV at full temp	
TR4_04	HWR_06_ADC_LV_SHT	The gain error of ADC_LV_SHT(output differential voltage /input differential voltage /0.5*100%) **shall** <0.5/1000 (4 sigma) The gain error variation **shall** <0.1/1000 at full temp	
TR1_00	HWR_07_ADC_LV_SHT	ADC_LV_SHT block **shall** only be enabled by D2A_CELL_ADC_EN	
TR4_04, TR4_05	HWR_00_ADC_MODU	ADC_MODU and ADC_LOGIC **shall** constitute a 6-bit SDM + 10-bit algorithm hybrid ADC with system level chopper(300us for 1 chennel) or 4-bit SDM + 12-bit algorithm hybrid ADC without system level chopper(30us for 1 channel)	
TR4_04	HWR_01_ADC_MODU	ADC_MODU **shall** transfer selected input voltage into BIT_STREAM under the control of ADC_SEQ	
TR4_04	HWR_02_ADC_MODU	The reference voltage ADC_MODU **shall** be ADC_REF	

TR ID	HWR ID	Description	Note
TR4_04	HWR_03_ADC_MODU	The LSB for Cn-Cn-1 **shall** be typical 200uV The LSB for GPIO input voltage measurement **shall** be 200uV The LSB for GPIO voltage ratio measurement **shall** be 100uV /2.5V The LSB for die temperature **shall** be 0.05 degree The LSB for BAT input voltage measurement **shall** be 200uVx16=3.2mV	
TR4_04	HWR_04_ADC_MODU	ENOB of Hybrid architecture ADC **shall** >14 bit (300us for 1 channel)	
TR1_00	HWR_05_ADC_MODU	ADC_MODU block **shall** only be enabled by D2A_CELL_ADC_EN	
TR4_04	HWR_06_ADC_MODU	The sample clock of ADC_MODU **shall** be ADC_CLK	
TR1_00	HWR_00_COMS_VCM	COMS_VCM **shall** be powered from LDOIN	
TR1_00	HWR_01_COMS_VCM	COMS_VCM **shall** always on When SDB is L,the bias current for COMS_VCM **shall** be I_START; the total current consumption for COMS_VCM **shall** <1uA When SLEEP is H,the bias current for COMS_VCM **shall** be IREF; the total current consumption for COMS_VCM **shall** <2.5uA When SLEEP is L and SDB is H,the bias current for COMS_VCM **shall** be IREF	
TR5_00	HWR_02_COMS_VCM	The RX of COMS_VCM **shall** be off when D2A_RX_EN is L and ACT is H	
TR5_00, TR5_09	HWR_03_COMS_VCM	COMS_VCM **shall** shift the +/- 20V common mode voltage of differential communication signals from COMS pins to typical LDOIN_HALF (COMS_SHAPE) The logic H threshold of differential communication signals for COMS_TONE_RX and COMS_COMM_RX **shall** <1.2V The logic L threshold of differential communication signals for COMS_TONE_RX and COMS_COMM_RX **shall** >0.4V The default output of COMS_VCM **shall** be logic 0	
TR5_00	HWR_04_COMS_VCM	When SLEEP is H or SDB is L, the delay time from COM pins to A2D_RX_S **shall** <500ns When SLEEP is L and SDB is H, the delay time from COM pins to A2D_RX_S **shall** <30ns	
TR5_00	HWR_06_COMS_VCM	COMS_VCM **shall** keep voltage of COMS pins LDOIN_HALF with typical 45Kohm when D2A_TX_EN is low and no COMM signals incoming from COMS pins	

TR ID	HWR ID	Description	Note
TR1_00	HWR_00_COMN_VCM	COMN_VCM **shall** be powered from LDOIN	
TR1_00	HWR_01_COMN_VCM	COMN_VCM **shall** always on When SDB is L,the bias current for COMN_VCM **shall** be I_START; the total current consumption for COMN_VCM **shall** <1uA When SLEEP is H,the bias current for COMS_VCM **shall** be IREF; the total current consumption for COMN_VCM **shall** <2.5uA When SLEEP is L and SDB is H,the bias current for COMN_VCM **shall** be IREF	
TR5_00	HWR_02_COMN_VCM	The RX of COMN_VCM **shall** be off when D2A_RX_EN is L and ACT is H	
TR5_00, TR5_09	HWR_03_COMN_VCM	COMN_VCM **shall** shift the +/- 20V common mode voltage of differential communication signals from COMN pins to typical LDOIN_HALF (COMN_SHAPE) The logic H threshold of differential communication signals for COMN_TONE_RX and COMN_COMM_RX **shall** <1.2V The logic L threshold of differential communication signals for COMN_TONE_RX and COMN_COMM_RX **shall** >0.4V The default output of COMN_VCM **shall** be logic 0	
TR5_00	HWR_04_COMN_VCM	When SLEEP is H or SDB is L, the delay time from COM pins to A2D_RX_N **shall** <500ns When SLEEP is L and SDB is H, the delay time from COM pins to A2D_RX_N **shall** <30ns	
TR5_00	HWR_06_COMN_VCM	COMN_VCM **shall** keep voltage of COMN pins LDOIN_HALF with typical 45Kohm when D2A_TX_EN is low and no COMM signals incoming from COMN pins	
TR5_01	HWR_00_COMS_TX	The driver resistance of COMS_TX **shall** <15ohm Delay time from D2A_TX to COMS pins **shall** <10ns	
TR5_00, TR5_02, TR5_09	HWR_01_COMS_TX	When D2A_TX_EN is high, COMS_TX **shall** output differential signal to COMS pins according to D2A_TX	
TR5_01	HWR_02_COMS_TX	When D2A_TX_EN and TONE_TRANS_EN are L, COMS_TX **shall** output high-z when voltage of COMN pins is during -20V-20V	

TR ID	HWR ID	Description	Note
TR1_03, TR5_00	HWR_03_COMS_TX	When TONE_TRANS_EN is H, if TONE_POLAR is low , COMS_TX **shall** output logic 0 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal if TONE_POLAR is high , COMS_TX **shall** output logic 1 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal	
TR5_01	HWR_00_COMN_TX	The driver resistance of COMN_TX **shall** <15ohm Delay time from D2A_TX to COMN pins **shall** <10ns	
TR5_00, TR5_02, TR5_09	HWR_01_COMN_TX	When D2A_TX_EN is high, COMN_TX **shall** output differential signal to COMN pins according to D2A_TX	
TR5_01	HWR_02_COMN_TX	When D2A_TX_EN and TONE_TRANS_EN are L, COMN_TX **shall** output high-z when voltage of COMN pins is during -20V-20V	
TR1_03, TR5_00	HWR_03_COMN_TX	When TONE_TRANS_EN is H, if TONE_POLAR is low , COMN_TX **shall** output logic 0 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal if TONE_POLAR is high , COMN_TX **shall** output logic 1 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal	
TR5_00	HWR_00_COMS_TONE_RX	COMS_TONE_RX **shall** be powered from LDOIN	
TR1_02	HWR_01_COMS_TONE_RX	COMS_TONE_RX **shall** work when LDOIN_OK is H	
TR1_00	HWR_02_COMS_TONE_RX	When SDB is L or SLEEP is H, the current consumption of COMS_TONE_RX **shall** <50nA at full temp	
TR1_02, TR1_03, TR1_06, TR1_09, TR1_10, TR1_11, TR5_00, TR5_10	HWR_04_COMS_TONE_RX	COMS_TONE_RX **shall** output WAKE_TONE_DET when WAKE TONE is received. WAKE_TONE_DET **shall** be low when D2A_CLR_WAKEUP is received. WAKE Tone **shall** be detected after >60 couplets of logic-1 are detected. COMS_TONE_RX does not need receiving all the tones to output WAKE_TONE_DET H.	

TR ID	HWR ID	Description	Note
TR1_02, TR1_03, TR1_06, TR5_00, TR5_10	HWR_05_COMS_TONE_RX	COMS_TONE_RX **shall** output STA_TONE_DET when STA TONE is received . STA Tone **shall** be detected after 20-30 couplets of logic-1 are detected. STA Tone **shall** only be detected when SLEEP is H. COMS_TONE_RX **shall** not output STA_TONE_DET before make sure all the tones is received.	
TR1_02, TR1_07, TR5_00	HWR_06_COMS_TONE_RX	COMS_TONE_RX **shall** output SD_TONE_DET when SD TONE is received. SD Tone **shall** be detected after >180 couplets of logic-0 are detected. COMS_TONE_RX does not need receiving all the tones to output SD_TONE_DET H.	
TR5_00, TR7_08	HWR_07_COMS_TONE_RX	COMS _TONE_RX **shall** output FLT_TONE_DET when FLT TONE is received. FLT Tone **shall** only be detected during SLEEP mode. FLT Tone **shall** be detected after 60-90 couplets of logic-0 are detected. COMS_TONE_RX **shall** not output FLT_TONE_DET before make sure all the tones is received.	
TR1_02, TR1_03, TR1_06, TR1_07, TR1_09, TR1_11, TR5_00, TR5_10, TR7_08	HWR_08_COMS_TONE_RX	COMS_TONE_RX **shall** have typical 720us (min 360us max 1080us) tone time out timer for logic 1 tone. COMS_TONE_RX **shall** have typical 1200us (min 1100us max 1300us) tone time out timer based on CLK_256K for logic 0 tone. Before timeout, no tone **shall** be detected	
TR1_02, TR1_03, TR1_06, TR1_09, TR1_11, TR5_00, TR5_10	HWR_09_COMS_TONE_RX	For COMS_TONE_RX, the detection of logic-0 tone **shall** not blank the detection of logic-1 tone when SLEEP is H	
TR5_00	HWR_00_COMN_TONE_RX	COMN_TONE_RX **shall** be powered from LDOIN	
TR1_02	HWR_01_COMN_TONE_RX	COMN_TONE_RX **shall** work when LDOIN_OK is H	
TR1_00	HWR_02_COMN_TONE_RX	When SDB is L or SLEEP is H, the current consumption of COMN_TONE_RX **shall** <50nA at full temp	

TR ID	HWR ID	Description	Note
TR1_02, TR1_03, TR1_06, TR1_09, TR1_10, TR1_11, TR5_00, TR5_10	HWR_04_COMN_TONE_RX	COMN_TONE_RX **shall** output WAKE_TONE_DET when WAKE TONE is received. WAKE_TONE_DET **shall** be low when D2A_CLR_WAKEUP is received. WAKE Tone **shall** be detected after >60 couplets of logic-1 are detected. COMN_TONE_RX does not need receiving all the tones to output WAKE_TONE_DET H.	
TR1_02, TR1_03, TR1_06, TR5_00, TR5_10	HWR_05_COMN_TONE_RX	COMN_TONE_RX **shall** output STA_TONE_DET when STA TONE is received . STA Tone **shall** be detected after 20-30 couplets of logic-1 are detected. STA Tone **shall** only be detected when SLEEP is H. COMN_TONE_RX **shall** not output STA_TONE_DET before make sure all the tones is received.	
TR1_02, TR1_07, TR5_00	HWR_06_COMN_TONE_RX	COMN_TONE_RX **shall** output SD_TONE_DET when SD TONE is received. SD Tone **shall** be detected after >180 couplets of logic-0 are detected. COMN_TONE_RX does not need receiving all the tones to output SD_TONE_DET H.	
TR1_02, TR1_03, TR1_06, TR1_07, TR1_09, TR1_11, TR5_00, TR5_10, TR7_08	HWR_07_COMN_TONE_RX	COMN_TONE_RX **shall** have typical 720us (min 360us max 1080us) tone time out timer for logic 1 tone. COMN_TONE_RX **shall** have typical 1200us (min 1100us max 1300us) tone time out timer based on CLK_256K for logic 0 tone. Before timeout, no tone **shall** be detected	
TR1_02, TR1_03, TR1_06, TR1_09, TR1_11, TR5_00, TR5_10	HWR_08_COMN_TONE_RX	For COMN_TONE_RX, the detection of logic-0 tone **shall** not blank the detection of logic-1 tone when SLEEP is H	
TR9_00	HWR_00_3P3	3P3 **shall** be powered from LDOIN The bias current of 3P3 **shall** be I_REF	
TR9_00	HWR_01_3P3	3P3 **shall** output typical 3.3V	
TR1_02	HWR_02_3P3	3P3 **shall** work when IREF_OK is H,	
TR9_00	HWR_00_I2C_MAS_INTER	I2C_MAS_INTER **shall** only be enabled by I2C_MAS_EN	
TR9_00	HWR_01_I2C_MAS_INTER	I2C_MAS_INTER **shall** only pull up/down SCL pin according to SCL	

TR ID	HWR ID	Description	Note
TR9_00	HWR_02_I2C_MAS_INTER	I2C_MAS_INTER **shall** only pull down SDA pin according to SDA_OUT with 100ohm I2C_MAS_INTER **shall** only pull up SCL to **3.3V** with 10k typical resistor	
TR9_00	HWR_03_I2C_MAS_INTER	I2C_MAS_INTER **shall** output SDA_IN H/L as SDA_IN according to SDA H/L status	
TR8_00, TR8_01, TR8_02	HWR_00_IO_INTER	When GPIO_PUPD_EN or LDOIN_OK is low , IO_INTER **shall** output high-z When GPIO_PUPD_EN is high, GPIO pins is configured as digital output with 0.4/4V voltage threshold and at least 1mA current ability according to GPIO_PUPD.	
TR8_00, TR8_01, TR8_03	HWR_01_IO_INTER	When GPIO_ASDIN_EN is high, IO_INTER **shall** compare the GPIO pin's voltage with 1V/2.5V threshold and output corresponding H/L signal to GPIO_HL When GPIO_ASDIN_EN is low, GPIO_HL **shall** keeps low Leakage on GPIO pins into IO_INTER **shall** <1uA when configured as digital input	
TR4_00	HWR_02_IO_INTER	GPIOn_ANA(n=0-11) **shall** be buffered from GPIOn(n=0-11) when any GPIO_PUPD_EN, GPIO_ASDIN_EN, I2C_MAS_EN are 1, otherwise, corresponding GPIOn_ANA(n=0-11) **shall** be pulled down to DGND	
TR6_02	HWR_00_CBFET	Rdson of CBFET **shall** be typ 2.5ohm @85 degree with NMOS switch	
TR6_00	HWR_01_CBFET	The switch **shall** only be on when the corresponding CB_CH_EN is high The switch **shall** only be off when the corresponding CB_CH_EN is low	
TR6_01	HWR_02_CBFET	The max operating voltage of the CB switch **shall** >16V	
TR10_06	HWR_03_CBFET	The shutdown resistor at gs of CBFET **shall** be small enough to prevent CB switch turned on by coupling of parasitic capacitors during hot-plug	
TR6_13	HWR_04_CBFET	The mismatch of balance current for all CBFET channels **shall** <10mA at 4.25V	
TR6_05	HWR000_JOT_CMP	JOT_CMP **shall** compare VBE with JOT_REF to output JOT signal to CB_CTRL with 20us deglitch Hys of JOT_CMP **shall** be 5℃	
TR6_05	HWR001_JOT_CMP	JOT_CMP **shall** use one CMP to monitor all the junction temp sensors through time-sharing reusing the CMP	

TR ID	HWR ID	Description	Note
TR1_00	HWR002_JOT_CMP	JOT_CMP **shall** only be enabled when CB_EN is H JOT **shall** keep low when JOT_CMP is not enabled	
TR1_02, TR1_14, TR1_15, TR5_08	HWR_00_RST_REG	RST_REG **shall** be powered from LDOIN RST_REG **shall** work when LDOIN_OK is H RST_REG **shall** be reset when LDOIN_OK is L	
TR1_14	HWR_01_RST_REG	When the LCTO_SD is a rise edge, LCTO_SD_LATCH **shall** output H When the CLK_256K_OK is a falling edge, CLK_256K_OKB_LATCH **shall** output H When the VAA_OK is a falling edge, VAA_OKB_LATCH **shall** output H When the VDD_OK is a falling edge, VDD_OKB_LATCH **shall** output H	
TR1_14	HWR_02_RST_REG	RST_REG **shall** be reset by RST_XXX_LATCH, when it is written to 1.	
TR1_15, TR5_08	HWR_03_RST_REG	COMM_DIG_SETTING **shall** include TOP_DEV, DIR_SEL, DEV_ADD, DEV_NUM COMM_DIG_SETTING **shall** be latched in RST_REG when ADD_W_EN falling edge RST_REG **shall** output default values included by COMM_DIG_SETTING_LATCH	
TR1_15, TR5_08	HWR_04_RST_REG	The default value of XXX_LATCH and COMM_DIG_SETTING_LATCH **shall** be same as corresponding register in digital core	
TR1_14	HWR_05_RST_REG	When SDB is H, CLK_256K_OKB, VDD_OKB and VAA_OKB **shall** be blanked by RST_REG	
TR1_00	HWR_00_CKGEN1	CKGEN1 **shall** generate CLK_8M_256K. CLK_8M_256K **shall** be from CLK_32M when CLK_32M_OK is high, and from CLK_256K when CLK_32M_OK is low.	
TR1_00	HWR_01_CKGEN1	CKGEN1 **shall** generate CLK_SLOW. CLK_SLOW **shall** be from divided CLK_32M when CLK_32M_OK high, and from CLK_256K when CLK_32M_OK low.	
TR1_00	HWR_05_CKGEN1	CKGEN1 **shall** generate CLK_REG. CLK_REG **shall** be divided clock from CLK_32M. CLK_REG **shall** be 8MHz.	
TR4_04, TR7_00	HWR_07_CKGEN1	CKGEN1 **shall** generate ADC_CLK, ADC_CLK_H according to ADC_CLK_SET.	

TR ID	HWR ID	Description	Note
TR1_00	HWR_02_CKGEN1	Higher clock gatings **shall** be used in CKGEN1. The gate signals in higher clock gatings are CLK_32M_OK (for CLK_REG) , D2A_CELL_ADC_EN(for CLK_ADC, ADC_CLK_H, ADC_CLK), MTP_EN(for CLK_MTP), CB_EN(for CLK_CB), I2C_MAS_EN(for CLK_I2C)	
TR10_01, TR10_05	HWR_06_CKGEN1	CKGEN1 **shall** mux all clocks with scanmux. Each scanmux **shall** output functional clock when SCAN_MODE is low, and output SCAN_CLK when SCAN_MODE is high. The clock outputs of CKGEN1 **shall** be CLK_32M_SC,CLK_REG_SC, CLK_ADC_SC, CLK_MTP_SC, CLK_CB_SC, CLK_I2C_SC, CLK_SLOW_SC, CLK_8M_256K_SC.	
TR1_09, TR1_11	HWR_00_RSTGEN	RSTGEN **shall** output hr_b low to asynchrously reset digital core when DRSTB low is detected. Hr_b **shall** be released synchronously. Hr_b **shall** include resetb_CLK(CLK_32M domain), resetb_CLK_OUT(mixed: CLK_32M domain when CLK_32M_OK high, CLK_256`K domain when CLK_32M_OK low) and resetb_CLK_SLOW(CLK_SLOW domain).	
TR1_10, TR1_11, TR1_15	HWR_01_RSTGEN	RSTGEN **shall** output hr_sr_b low to asynchrously reset partial logic of digital core when DRSTB low or SOFT_RSTB is low. Hr_sr_b **shall** be released synchronously. Hr_sr_b **shall** include resetb_SR_CLK(CLK_32M domain), resetb_SR_CLK_OUT(mixed: CLK_32M domain when CLK_32M_OK high, CLK_256K domain when CLK_32M_OK low) and resetb_SR_CLK_SLOW(CLK_SLOW domain).	
TR1_10, TR1_11, TR1_15	HWR_02_RSTGEN	When SOFT_RSTB is written to 0 via COMM_CTRL, RSTGEN **shall** output hr_sr_b to low	
TR10_01, TR10_05	HWR_03_RSTGEN	Hr_b and Hr_sr_b **shall** all be scan-muxed. When SCAN_MODE high, CKGEN **shall** switch all registers' asynchronous reset to SCAN_RSTB.	
TR1_10, TR4_04	HWR_00_MTP_TOP	Data in MTP **shall** be loaded to DS_REG via DOUT after reset(DRSTB posedge or SOFT_RSTB posedge) done.	
TR1_14, TR1_15, TR5_08	HWR_01_MTP_TOP	load_done **shall** be high after MTP load done.	

TR ID	HWR ID	Description	Note
TR1_02, TR1_03, TR1_06, TR1_09, TR1_10, TR1_11, TR1_16, TR5_00, TR5_01, TR5_10	HWR_00_TONE_CTRL	When WAKE_TONE_DET is high, TONE_CTRL **shall** output WAKEUP TONE(consist of 90 logic-1 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN TONE_TRANS_EN **shall** include TONE_TRANS_EN_N and TONE_TRANS_EN_S. TONE_TRANS_EN_N or TONE_TRANS_EN_S **shall** be the opposite direction of WAKE_TONE_DET	
TR1_02, TR1_03, TR1_06, TR1_09, TR1_10, TR1_11, TR1_16, TR5_00, TR5_01, TR5_10	HWR_01_TONE_CTRL	TONE_CTRL **shall** output a high pulse on D2A_CLR_WAKEUP when WAKE_TONE_DET is high and WAKE TONE is already generated completely at the opposite direction of WAKE_TONE_DET	
TR1_02, TR1_03, TR1_06, TR5_00, TR5_01, TR5_10	HWR_02_TONE_CTRL	When STA_TONE_DET is high, TONE_CTRL **shall** output STA TONE(consist of 30 logic-1 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN TONE_TRANS_EN **shall** include TONE_TRANS_EN_N and TONE_TRANS_EN_S. TONE_TRANS_EN_N or TONE_TRANS_EN_S **shall** be the opposite direction of STA_TONE_DET	
TR5_00, TR7_08	HWR_03_TONE_CTRL	Only when SLEEP is high and FLT_WAKE high, TONE_CTRL **shall** output FLT TONE(consist of 90 logic-0 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N every 50ms.	
TR5_00	HWR_04_TONE_CTRL	When WAKE_TONE_GEN is high, TONE_CTRL **shall** generate wake tone Direction in TONE_TRANS_EN **shall** base on TONE_GEN_DIR	
TR5_00	HWR_05_TONE_CTRL	TONE_CTRL **shall** output clr_WAKE_TONE_GEN high after WAKE_TONE_GEN is detected as high	
TR5_00	HWR_06_TONE_CTRL	When STA_TONE_GEN is high, TONE_CTRL **shall** generate STA tone Direction in TONE_TRANS_EN **shall** base on TONE_GEN_DIR	
TR5_00	HWR_07_TONE_CTRL	TONE_CTRL **shall** output clr_STA_TONE_GEN high after STA_TONE_GEN is detected as high	
TR5_00	HWR_08_TONE_CTRL	When SD_TONE_GEN is high, TONE_CTRL **shall** generate SD TONE(consist of 270 logic-0 couplets) Direction in TONE_TRANS_EN **shall** base on TONE_GEN_DIR	
TR5_00	HWR_09_TONE_CTRL	TONE_CTRL **shall** output clr_SD_TONE_GEN high after SD_TONE_GEN is detected as high	

TR ID	HWR ID	Description	Note
TR5_00	HWR_10_TONE_CTRL	The period of TONE_CLK for all tones **shall** be typ 11us.	
TR5_00	HWR_11_TONE_CTRL	TONE_TRANS_EN **shall** be clear to 0 when D2A_TX_EN_S or D2A_TX_EN_N (in D2A_TX) is high.	
TR5_00	HWR_12_TONE_CTRL	About tone generation priority, WAKE TONE and STA TONE **shall** have higher priority to HB TONE and FLT TONE.	
TR5_00	HWR_00_DS_BASIC	DS_BASIC **shall** extract rx_data[8:0] (1 SOF bit+ 8 data bits) from A2D_RX.	
TR5_02	HWR_01_DS_BASIC	DS_BASIC **shall** sample A2D_RX using CLK_32M DS_BASIC **shall** transmit D2A_TX using CLK_32M	
TR5_02	HWR_02_DS_BASIC	DS_BASIC **shall** use majority vote (10%) to sample A2D_RX with +-10% sampling clock accuracy.	
TR5_01	HWR_03_DS_BASIC	After (0.5us+STACK_RESP_CMD) bus short blank time from the complete reception of last byte, the new preamable **shall** not be identified by DS_BASIC until a 0.5us bus idle (logic-0) is detected to avoid faulty preamable identification due to ring of communication bus	
TR5_00	HWR_04_DS_BASIC	For each byte, only after preamable + SYNC[1:0] are received correctly(timing and data), the following bits **shall** start to be extracted	
TR5_00	HWR_05_DS_BASIC	After preamable + SYNC[1:0] are received correctly(timing and data), the opposite A2D_RX data **shall** be blanked	
TR5_10, TR5_11	HWR_06_DS_BASIC	DS_BASIC **shall** propagate frame on D2A_TX in the opposite direction of A2D_RX.	
TR5_00	HWR_07_DS_BASIC	D2A_RX_EN **shall** be default high D2A_TX_EN and D2A_RX_EN **shall** not be high at the same time at same port TONE_TRANS_EN and D2A_RX_EN **shall** not be high at the same time at same port	
TR5_12	HWR_08_DS_BASIC	The output D2A_TX_EN (N) of DS_BASIC **shall** only be high when COMN_TX_DIS is low The output D2A_TX_EN (S) of DS_BASIC **shall** only be high when COMN_TX_DIS is low	
TR1_02	HWR_02_BASIC_CTRL	When CLK_32M_OK is low, BASIC_CTRL **shall** be synchronously-reset to initial state.	
TR5_00	HWR_00_COMM_CTRL	A new frame is identified by COMM_CTRL when SOF bit is recognised high in rx_data	

TR ID	HWR ID	Description	Note
TR5_10	HWR_01_COMM_CTRL	COMM_CTRL **shall** support frame propagation from rx_data to tx_data.	
TR5_04, TR5_06	HWR_02_COMM_CTRL	COMM_CTRL **shall** support writing register bit. COMM_CTRL distinguish device_addr, bytes_num, ini_reg_addr and data from rx_data, and then write to DS_REG via W. Reg_addr **shall** automatically add by 1 when bytes_num > 1 for continuous writing. If device_addr not match with DEV_ADD(in COMM_DIG_SETTING), no register **shall** be written. If received direction not match with DIR_SEL(in COMM_DIG_SETTING), no register **shall** be written.	
TR5_03, TR5_05	HWR_03_COMM_CTRL	COMM_CTRL **shall** support reading register bit. COMM_CTRL distinguish device_addr, bytes_num, and ini_reg_addr from rx_data, and then send reg_addr via W to DS_REG(preparing to response register data). If device_addr not match with DEV_ADD(in COMM_DIG_SETTING), no register **shall** be read. If received direction not match with DIR_SEL(in COMM_DIG_SETTING), no register **shall** be read.	
TR5_03, TR5_05	HWR_04_COMM_CTRL	When responsing, COMM_CTRL **shall** extract data(corresponding to reg_addr) from COMM_REG via R, then send device_addr, bytes_num, ini_reg_addr and data to BASIC_CTRL via tx_data. Reg_addr **shall** automatically add by 1 when bytes_num > 1 for continuous reading.	
TR4_07, TR5_00	HWR_05_COMM_CTRL	Data format in D2A_TX and A2D_RX **shall** be as described : The character **shall** consist of 0.5-bit preamble bit, 2-bit SYNC bits,1-bit SOF bit, 8-bit DATA bit,1-bit CERR bit,0.5-bit postable bit SOF bit **shall** represent the start of frame. The DATA of character **shall** send LSB then MSB Before each character, there **shall** be 1.375us idle time. After each character,0.5us short time **shall** be present. The baud rate of DATA communication **shall** be 2Mbps. The logic 1 of bit **shall** consist of 1 differential couplet: positive half-bit first, negative half-bit then The logic 0 of bit **shall** consist of 1 differential couplet: negative half-bit first, positive half-bit then	
TR5_00	HWR_06_COMM_CTRL	Data format in D2A_TX and A2D_RX **shall** be as described : INIT byte in D2A_TX and A2D_RX **shall**: bit 7 define the frame type: 1 is command, 0 is response for command, bit6-bit4: 000 is Single Read, 001 is Single Write, 010 is Stack Read, 011 is Stack Write; bit3-bit0: represent the number of DATA bytes (max 16 bytes) for response, bit6-bit0: represent the number of DATA bytes (max 128 bytes)	

TR ID	HWR ID	Description	Note
TR5_00	HWR_07_COMM_CTRL	Data format in D2A_TX and A2D_RX **shall** be as described : DATA byte in D2A_TX and A2D_RX **shall**: define the data value to be written for write command define the byte number to be read for read command	
TR5_00	HWR_08_COMM_CTRL	Data format in D2A_TX and A2D_RX **shall** be as described : CRC bytes **shall** use CRC-16-IBM polynomial (x^16+x^15+x^2+1) with 0xFFFF initialization	
TR5_00	HWR_09_COMM_CTRL	Data format in D2A_TX and A2D_RX **shall** be as described : Single Write command frame **shall** consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes Stack Write command frame **shall** consist of 1 INIT byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes Single Read command frame **shall** consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, 1 DATA byte, 2 CRC bytes Stack Read command frame **shall** consist of 1 INIT byte, 2 REG_ADD bytes, 1 DATA byte, 2 CRC bytes Response frame of each device **shall** consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes	
TR5_00	HWR_10_COMM_CTRL	After receiving Stack Read Command: If TOP_DEV is low, COMM_CTRL **shall** send itselfs' response frame in tx_data only when response frame from +1 device address is propagated. If TOP_DEV is high, COMM_CTRL **shall** send itselfs' response frame in tx_data to BASIC_CTRL.	
TR5_00, TR5_01	HWR_11_COMM_CTRL	COMM_CTRL **shall** program the delay time(from 0.25us-15.75us) between characters by STACK_RESP_CMD. STACK_RESP_CMD **shall** program the self-generated response delay only	
TR5_07	HWR_12_COMM_CTRL	COMM_CTRL **shall** identify Broadcast Read Command as Addressing Identification Command	
TR5_07	HWR_13_COMM_CTRL	If frame type is address identification, frame propagation **shall** be canceled. If frame type is not address identification, frame propagation **shall** start after a byte is completely received from rx_data.	
TR1_12, TR1_13	HWR_19_COMM_CTRL	FRAME_DONE **shall** be generated when a frame is received completely (no matter CRC). FRAME_DONE **shall** be a pulse.	
TR1_02	HWR_20_COMM_CTRL	When CLK_32M_OK is low, COMM_CTRL **shall** be synchronously-reset to initial state.	

TR ID	HWR ID	Description	Note
TR1_12, TR1_13	HWR_00_COMM_TO	COMM_TO **shall** contain a watchdog counter The counter **shall** be reset when FRAME_DONE is high, or when ACT is low. The timer **shall** support being programmed from 100ms to 1h with 8 steps, by PROG_SCTO or PROG_LCTO.	
TR1_12	HWR_01_COMM_TO	COMM_TO **shall** output SET_SCTO when counter reach the the threshold programmed by the PROG_SCTO[2:0].	
TR1_13	HWR_02_COMM_TO	COMM_TO **shall** output SET_LCTO when counter reach the the threshold programmed by PROG_LCTO[2:0].	
TR1_04, TR1_07	HWR_00_DS_REG	TO_SD **shall** be defined in DS_REG.	
TR1_05, TR1_08	HWR_01_DS_REG	TO_SLEEP **shall** be defined in DS_REG. TO_SLEEP **shall** be low when clr_TO_SLEEP is high.	
TR1_10, TR1_15	HWR_02_DS_REG	SOFT_RSTB_REG **shall** be defined in DS_REG. SOFT_RSTB_REG **shall** be default high. SOFT_RSTB_REG **shall** be high when clr_SOFT_RSTB is high	
TR1_12	HWR_03_DS_REG	PROG_SCTO[2:0] **shall** be defined in DS_REG.	
TR1_13	HWR_04_DS_REG	PROG_LCTO[2:0] **shall** be defined in DS_REG.	
TR1_13	HWR_05_DS_REG	LCTO_SEL[1:0] **shall** be defined in DS_REG	
TR4_04	HWR_06_DS_REG	TRIM_ADC bits(92 bytes) **shall** be defined in DS_REG. TRIM_ADC **shall** only be written when TRIM_EN is high.	
TR4_00, TR4_04	HWR_07_DS_REG	ADC_DATA_LPF (including ADC_LPF_CH1-18[15:0]) **shall** be readable via DS_REG.	
TR4_00, TR4_04	HWR_08_DS_REG	ADC_SETTING_REG **shall** be defined in DS_REG. ADC_SETTING_REG **shall** include ADC_MODE_REG[1:0], ADC_CHP_EN_REG, ADC_CLK_SET_REG[1:0], CH_DT_REG[1:0], CH_STL_REG[3:0], CH_TOP_STL_REG[3:0], DLPF_FC_REG[2:0] (including disable option), GPIO_REF_SEL_REG[11:0].	
TR4_05, TR4_06, TR4_11	HWR_09_DS_REG	ADC_GO including ADC_SGLE_GO and ADC_CNTI_GO **shall** be defined in DS_REG. ADC_GO **shall** be cleared when clr_ADC_GO is high or CLK_32M_OK is low. ADC_GO high pulse width **shall** >8us.	
TR6_08	HWR_10_DS_REG	CB_SETTLE[4:0] **shall** be defined in DS_REG	

TR ID	HWR ID	Description	Note
TR4_05, TR4_06, TR4_11	HWR_11_DS_REG	FREEZE bit **shall** be defined DS_REG.	
TR4_00, TR4_04	HWR_12_DS_REG	CELL_ADC_DATA(including ADC_CH1-18[15:0]) and OTH_ADC_DATA(including ADC_GPIO0-11[15:0], ADC_VPTAT[15:0], ADC_BAT[15:0], xxx) **shall** be readable via DS_REG.	
TR4_10	HWR_13_DS_REG	RR_COUNTER[15:0] **shall** be readable via DS_REG.	
TR4_09	HWR_14_DS_REG	RR_COUNTER, ADC_DATA_LPF and OTH_ADC_DATA **shall** all be stored in DS_REG with continuous addresses.	
TR5_07	HWR_15_DS_REG	ADD_W_EN **shall** be defined in DS_REG ADD_W_EN **shall** only be set 1 when address identify starts. ADD_W_EN **shall** support only being cleared to 0 via COMM_CTRL.	
TR5_07, TR5_08	HWR_16_DS_REG	COMM_DIG_SETTING (including TOP_DEV, DIR_SEL, DEV_ADD[6:0]) **shall** be defined in DS_REG The default values of COMM_DIG_SETTING come from XXX_LATCH when load done is high COMM_DIG_SETTING **shall** not be changed when ADD_W_EN is low.	
TR4_05, TR4_06 TR5_07	HWR_17_DS_REG	DEV_NUM[6:0] **shall** be defined in DS_REG DEV_NUM is changed by COMM_CTRL address identifying or written via COMM_CTRL when ADD_W_EN high. When address identify starts, DEV_NUM is clear to 0. DEV_NUM adds by step 1 when a response is received . DEV_NUM **shall** not be changed when ADD_W_EN is low.	
TR5_12	HWR_18_DS_REG	COMN_TX_DIS and COMN_TX_DIS **shall** be defined in DS_REG, default 0	
TR5_00	HWR_19_DS_REG	TONE_GEN_DIR **shall** be defined in DS_REG, default south.	
TR5_00	HWR_20_DS_REG	STACK_RESP_CMD[5:0] **shall** be defined in DS_REG.	
TR6_03	HWR_21_DS_REG	CB_GO **shall** be defined in DS_REG. CB_GO **shall** be cleared when clr_CB_GO is high.	
TR6_00	HWR_22_DS_REG	CB_CTRL_SETTING_REG **shall** be defined in DS_REG.	
TR6_01	HWR_23_DS_REG	CB_CTRL_SETTING_REG **shall** include CBFET_EN_REG1-18, CB_MANUAL_REG.	

TR ID	HWR ID	Description	Note
TR6_04	HWR_24_DS_REG	CB_CTRL_SETTING_REG **shall** include CB_TO_THRESH_REG1-18[9:0] and CB_UNIT_REG[17:0]. Default value of CB_TO_THRESH_REG1-18[9:0] **shall** be 10'h3FF and default CB_UNIT is 1.	
TR6_05	HWR_25_DS_REG	CB_CTRL_SETTING_REG **shall** include CB_TWARN_THRESH_REG[3:0]	
TR6_06	HWR_26_DS_REG	CB_OT_PACK_THRESH_REG[4:0] and CB_OT_PCB_THRESH_REG[4:0] **shall** be defined in DS_REG.	
TR6_05	HWR_27_DS_REG	CB_CTRL_SETTING_REG **shall** include JOT_EN_REG, with default value 1.	
TR6_06	HWR_28_DS_REG	CB_CTRL_SETTING_REG **shall** include GPIO_CBOT_EN_REG, with default value 1.	
TR6_07	HWR_29_DS_REG	CB_CTRL_SETTING_REG **shall** include CB_MANU_PAUSE, with default value 0.	
TR6_08	HWR_30_DS_REG	CB_CTRL_SETTING_REG **shall** include ADC_PAUSE_EN_REG, with default value 1.	
TR6_09	HWR_31_DS_REG	CB_CTRL_SETTING_REG **shall** include FLT_STOP_EN_REG, with default value 1.	
TR6_10	HWR_32_DS_REG	CB_CTRL_SETTING_REG **shall** include CB_PERIOD_REG[2:0].	
TR6_11	HWR_33_DS_REG	CB_CTRL_SETTING_REG **shall** include CB_DUTY_REG[2:0].	
TR6_12	HWR_34_DS_REG	CB_ODD_CNT[15:0] and CB_EVEN_CNT[15:0] **shall** be readable via DS_REG.	
TR6_12	HWR_35_DS_REG	CB_CH_EN_FULL_DUTY[17:0] **shall** be readable via DS_REG.	
TR1_00, TR7_00, TR7_01	HWR_36_DS_REG	MON_WAKE_EN_REG **shall** be defined in DS_REG.	
TR1_00, TR7_00, TR7_01	HWR_37_DS_REG	OVUV_OTUT_EN_REG **shall** be defined in DS_REG.	
TR7_00, TR7_01	HWR_38_DS_REG	MON_WAKE_GO **shall** be defined in DS_REG. MON_WAKE_GO **shall** be cleared when clr_MON_WAKE_GO is high.	
TR7_00, TR7_01, TR7_02	HWR_39_DS_REG	MON_WAKE_PERIOD_REG[5:0] **shall** be defined in DS_REG	
TR7_04	HWR_40_DS_REG	CELL_OV_THRESH_REG[6:0], CELL_UV_THRESH_REG[6:0] **shall** be defined in DS_REG.	
TR7_09	HWR_41_DS_REG	OVUV_DEGL_REG[4:0] **shall** be defined in DS_REG.	

TR ID	HWR ID	Description	Note
TR7_05, TR7_06	HWR_42_DS_REG	GPIO_OT_PACK_THRESH_REG[4:0], GPIO_UT_PACK_THRESH_REG[2:0], GPIO_OT_PCB_THRESH_REG[4:0], GPIO_UT_PCB_THRESH_REG[2:0] **shall** be defined in DS_REG.	
TR7_06	HWR_43_DS_REG	GPIO_OTUT_THRESH_SEL_REG[11:0] **shall** be defined in DS_REG	
TR9_00	HWR_44_DS_REG	I2C_CTRL, I2C_MAS_EN **shall** be defined in DS_REG. I2C_CTRL **shall** include WR_DATA[7:0], WR_GO. RD_DATA[7:0] and ACK_BIT RD_DATA[7:0] from i2c_slave **shall** be readable via DS_REG. ACK_BIT from i2c_slave **shall** be readable via DS_REG.	
TR4_04	HWR_45_DS_REG	TRIM_ANA(32 bytes) **shall** be defined in DS_REG. TRIM_ANA **shall** only be written when TRIM_EN is high. In TRIM_ANA: TRIM_L_CLK[x:0] **shall** be in one byte address. TRIM_H_CLK[x:0] **shall** be in one byte address. TRIM_BG[x:0] **shall** be in one byte address. TRIM_IREF[x:0] **shall** be in one byte address.	x TBD
TR4_04	HWR_46_DS_REG	MTP_CTRL_BITS(including WR_MTP) **shall** be defined in DS_REG. MTP_CTRL_BITS in DS_REG **shall** only be written when TRIM_EN is H.	
TR10_00	HWR_47_DS_REG	X-Y and lot information **shall** be defined in DS_REG as the shadow register of MTP, and **shall** be read only for customer.	
TR5_00	HWR_48_DS_REG	WAKE_TONE_GEN **shall** be defined in DS_REG WAKE_TONE_GEN **shall** be reset when clr_WAKE_TONE_GEN is high	
TR5_00	HWR_49_DS_REG	STA_TONE_GEN **shall** be defined in DS_REG STA_TONE_GEN **shall** be reset when clr_STA_TONE_GEN is high	
TR5_00	HWR_50_DS_REG	SD_TONE_GEN and SD_TONE_DIR **shall** be defined in DS_REG. SD_TONE_GEN **shall** be low when clr_SD_TONE_GEN is high.	
TR8_01, TR8_02	HWR_51_DS_REG	GPIO_PUPD[11:0], GPIO_PUPD_EN[11:0], GPIO_ASDIN_EN[11:0] **shall** be defined in DS_REG to output H/L/HZ to IO.	
TR8_01, TR8_03	HWR_52_DS_REG	GPIO_HL[11:0] **shall** be readable via DS_REG.	

TR ID	HWR ID	Description	Note
TR1_12, TR1_14, TR4_01, TR4_02, TR6_09, TR7_03, TR11_00	HWR_53_DS_REG	All fault bits **shall** have corresponding mask bit defined in DS_REG.	
TR4_00, TR4_04, TR4_10, TR6_12	HWR_00_LOW_BYTE_BUF	Low bytes of ADC_DATA_LPF, CELL_ADC_DATA, OTH_ADC_DATA, CB_ODD_CNT, CB_EVEN_CNT, RR_COUNTER **shall** be buffered in LOW_BYTE_BUF, and when reading, the buffered bits **shall** be output to COMM_CTRL.	
TR1_10, TR1_15	HWR_00_SOFT_RSTB_sync	SOFT_RSTB **shall** be synchronized in SOFT_RSTB_sync. Output clr_SOFT_RSTB **shall** be high when synchronized SOFT_RSTB is low, clr_SOFT_RSTB **shall** be low when synchronized SOFT_RSTB is high.	
TR1_04, TR1_07	HWR_00_TO_SD_sync	TO_SD **shall** be synchronized in TO_SD_sync.	
TR1_05, TR1_08	HWR_00_TO_SLP_sync	TO_SLEEP **shall** be synchronized in TO_SLP_sync to output D2A_TO_SLEEP (Pulse high width **shall** > 8us) Output clr_TO_SLEEP **shall** be high when synchronized TO_SLEEP is high, clr_TO_SLEEP **shall** be low when synchronized TO_SLEEP is low.	
TR1_12	HWR_00_FLT_REG	SCTO **shall** be defined in FLT_REG SCTO **shall** be set by SET_SCTO.	
TR1_13, TR1_14	HWR_01_FLT_REG	LCTO **shall** be defined in FLT_REG LCTO **shall** be set by SET_LCTO or LCTO_LATCH (when load done is high)	
TR1_14	HWR_02_FLT_REG	XXX (including LCTO_SD, VAA_OKB, VDD_OKB, CLK_256K_OKB, VDD_OV, VDD_UV) **shall** be defined in FLT_REG These bits **shall** only be set by XXX_LATCH (when load done is high). FLT_REG **shall** output RST_XXX_LATCH when corresponding register bit among these bits is written to 1.	

TR ID	HWR ID	Description	Note
TR7_08	HWR_03_FLT_REG	FLT_TONE_DET_REG **shall** be defined in FLT_REG FLT_TONE_DET_REG **shall** be set by FLT_TONE_DET	
TR7_03, TR7_08	HWR_04_FLT_REG	GPIO_OTUT (including GPIO_OT[11:0], GPIO_UT[11:0]) **shall** be defined in FLT_REG	
TR7_03, TR7_08	HWR_05_FLT_REG	CELL_OVUV (including CELL_OV[17:0] and CELL_UV[17:0]) **shall** be defined in FLT_REG	
TR11_00	HWR_06_FLT_REG	COW[18:0] **shall** be defined in FLT_REG.	
TR6_00, TR6_01	HWR_07_FLT_REG	CB_CONF_FLT **shall** be defined in FLT_REG.	
TR1_12, TR1_14, TR7_03, TR11_00	HWR_10_FLT_REG	All fault bits **shall** not be written to 1 via COMM_CTRL. All fault bits **shall** be cleared to 0 when written 0 via COMM_CTRL.	
TR1_12, TR1_14, TR6_09, TR7_03, TR11_00	HWR_11_FLT_REG	All fault bits **shall** not be set to 1 when corresponding mask bit is 1.	
TR6_09, TR7_08	HWR_00_FLT_LOGIC	FLT_LOGIC **shall** combine all fault regs as logic-OR and output FLT_WAKE.	
TR1_00	HWR_00_MTP_INTERF	MTP_EN **shall** be generated in MTP_INTERF. MTP_EN **shall** be high when MTP write or MTP read starts, and **shall** be low when MTP write and MTP read ends. MTP_EN **shall** be initially high for MTP loading.	
TR4_04	HWR_01_MTP_INTERF	MTP_INTERF **shall** support writing MTP via MTP_CTRL_BITS in DS_REG. MTP write starts when WR_MTP is high. MTP write ends when all MTP address are covered.	
TR1_10, TR4_04	HWR_02_MTP_INTERF	MTP_INTERF **shall** support reading MTP after reset. MTP read starts after reset(DRSTB posedge or SOFT_RSTB posedge) when CLK_32M_OK is high. MTP read ends when all MTP address are covered.	
TR4_04	HWR_00_TRIM_LOGIC	TRIM **shall** be the AND results of TRIM_ANA and load_done.	

TR ID	HWR ID	Description	Note
TR4_05, TR4_06, TR6_08	HWR_00_RECLK_COMP	A delay **shall** be added between ADC_GO and ADC_GO_DLY. The delay time **shall** be: Tdelay = (DEV_NUM+CB_SETTLE+1) * 8.375us A delay **shall** be added between FREEZE and FREEZE_DLY. The delay time **shall** be: Tdelay = DEV_NUM * 8.375us	
TR4_05, TR4_06, TR6_08	HWR_01_RECLK_COMP	RECLK_COMP **shall** be reset when CLK_32M_OK is 0.	
TR1_00	HWR_00_ADC_CTRL	Higher clock gating signal D2A_CELL_ADC_EN **shall** be generated in ADC_CTRL. D2A_CELL_ADC_EN **shall** be high when ADC measurement starts(ADC_GO high), and **shall** be low when ADC measurement ends.	
TR1_02	HWR_01_ADC_CTRL	When CLK_32M_OK is low, ADC_CTRL **shall** be reset to initial state (except CELL_ADC_DATA, OTH_ADC_DATA and ADC_DATA_LPF)	
TR4_05, TR4_06, TR4_11	HWR_02_ADC_CTRL	ADC_CTRL **shall** only execute one cycle only when ADC_SGLE_GO or MON_ADC_GO is detected. ADC_CTRL **shall** only execute continously when ADC_CNTI_GO is detected. ADC_CNTI_GO **shall** has higher priority to ADC_SGLE_GO(ADC_CTRL only execute ADC_CNTI_GO when both are detected at the same time).	
TR4_08	HWR_03_ADC_CTRL	ADC_CTRL **shall** only update till new measurement data is available.	
TR4_05, TR4_06	HWR_04_ADC_CTRL	When FREEZE_DLY is high, CELL_ADC_DATA, ADC_DATA_LPF and OTH_ADC_DATA **shall** all be freezed. When FREEZE_DLY is low, CELL_ADC_DATA, ADC_DATA_LPF and OTH_ADC_DATA **shall** be allowed updating.	
TR4_00	HWR_00_ADC_LOGIC	ADC_LOGIC **shall** convert BIT_STREAM to ADC_RESULT. ADC_LOGIC **shall** output CH_END, ADC_SEQ according to ADC_SETTING.	
TR4_09, TR4_10, TR7_00, TR7_01	HWR_00_CH_SEL_GEN	RR_END **shall** be defined in CH_SEL_GEN. RR_END generate high pulse(>8us) when round-robin ends.	

TR ID	HWR ID	Description	Note
TR4_00, TR4_10	HWR_01_CH_SEL_GEN	CH_COUNTER **shall** be defined in CH_SEL_GEN. CH_COUNTER **shall** add by step 1 when CH_END is high. CH_COUNTER **shall** be cleared to 0 when current round-robin ends.	
TR4_05, TR4_06, TR4_11	HWR_02_CH_SEL_GEN	Clr_ADC_GO **shall** be high when ADC_GO_DLY(including ADC_SGLE_GO_DLY and ADC_CNTI_GO_DLY) or MON_ADC_GO is synchronized by CLK_REG_SC and ADC_CTRL starts to work. High time of clr_ADC_GO **shall** >8us.	
TR4_00	HWR_03_CH_SEL_GEN	CH_SEL_GEN **shall** update ADC_SETTING_REG to ADC_SETTING when ADC_GO_DLY is high.	
TR4_10	HWR_00_RR_CNT	RR_COUNTER **shall** add by step 1 when current round-robin ends. RR_COUNTER **shall** clear to 0 when ADC_GO_DLY is high.	
TR4_04	HWR_00_CALIBRATION	CALIBRATION **shall** calibrate ADC_RESULT into ADC_DATA by TRIM_ADC.	
TR4_04	HWR_01_CALIBRATION	CALIBRATION **shall** output signed complementary code results including CELL_ADC_DATA and OTH_ADC_DATA.	
TR4_11	HWR_00_DLPF	DLPF **shall** filter CELL_ADC_DATA to ADC_DATA_LFP with stage defined according to DLPF_FC (in ADC_SETTING).	
TR6_00	HWR_00_CB_CTRL	CB_CH_EN **shall** be default 0	
TR6_00, TR6_01, TR6_04, TR6_05, TR6_06, TR6_08, TR6_09, TR6_10, TR6_11	HWR_01_CB_CTRL	CB_CTRL_SETTING (except CBFET_EN1-18 and CB_MANU_PAUSE) in CB_CTRL **shall** be updated directly from CB_CTRL_SETTING_REG when CB_GO is high. When CB_GO is detected at CB_MANUAL_REG is high, if >2 consecutive channels are enabled in CBFET_EN_REG1-18, CBFET_EN1-18 **shall** not be updated, and CB_CTRL **shall** output CB_CONF_FLT to high. CB_CTRL **shall** output updated CB_TWARN_THRESH.	
TR1_00	HWR_02_CB_CTRL	Higher clock gating signal CB_EN **shall** be generated in CB_CTRL. CB_EN **shall** be high when CB_GO high is detected by CB_CTRL, and **shall** be low when 1.internal counter reaches each channel's target threshold; or 2.CBFET_EN1-18 are all 0.	

TR ID	HWR ID	Description	Note
TR6_04	HWR_03_CB_CTRL	There **shall** be 2 timers (ODD/EVEN) in CB_CTRL, max 12h The timer **shall** only count when CB_GO is detected CB_CTRL **shall** output CB_CH_EN to H only if the timer does not touch the CB_TO_THRESH. CB_TO_THRESH_REG **shall** cover 12h, step 1s-1min and CB_UNIT_REG **shall** be: 0 means second and 1 means minute).	
TR6_01, TR6_10	HWR_04_CB_CTRL	When CB_MANUAL=0, CB_CH_EN **shall** support switching between odd/even (logic AND with CBFET_EN1-18) group every CB_PERIOD automatically CB_PERIOD **shall** cover typical 5s-30min, 8steps. When CB_MANUAL=1, CB_CH_EN **shall** support being selected by CBFET_EN1-18	
TR6_11	HWR_05_CB_CTRL	CB_CTRL **shall** output CB_CH_EN with duty as defined by CB_DUTY every typical 200ms. CB_DUTY **shall** cover 12.5%-100%, 8steps.	
TR6_05	HWR_06_CB_CTRL	CB_CTRL **shall** outputs CB_CH_EN L if the JOT is high when JOT_EN is high. Timer of balance **shall** be held if the JOT is H when JOT_EN is high.	
TR6_06	HWR_07_CB_CTRL	CB_CTRL **shall** outputs CB_CH_EN L if the GPIO_CBOT is H when GPIO_CBOT_EN is high. Timer of balance **shall** be held if the GPIO_CBOT is H when GPIO_CBOT_EN is high.	
TR6_07	HWR_08_CB_CTRL	CB_CTRL **shall** outputs CB_CH_EN L if the CB_MANU_PAUSE is H. Timer of balance **shall** be held if the CB_MANU_PAUSE is H.	
TR6_08	HWR_09_CB_CTRL	CB_CTRL **shall** outputs CB_CH_EN L only if the D2A_CELL_ADC_EN is H when ADC_PAUSE_EN is high. Timer of balance **shall** be held if the D2A_CELL_ADC_EN when ADC_PAUSE_EN is high.	
TR6_09	HWR_10_CB_CTRL	CB_CTRL **shall** outputs CB_CH_EN L if the FLT_WAKE is H when FLT_STOP_EN is high. Timer of balance **shall** be cleared if the FLT_WAKE is H when FLT_STOP_EN is high.	
TR6_12	HWR_11_CB_CTRL	CB_CTRL **shall** output CB_ODD_CNT and CB_EVEN_CNT.	
TR6_12	HWR_12_CB_CTRL	CB_CTRL **shall** output CB_CH_EN_FULL_DUTY (CB_CH_EN excluding CB_DUTY).	
TR7_00, TR7_01	HWR_00_CYC_WAKE	Once MON_WAKE_GO is high, CYC_WAKE **shall** latch and update MON_EN_REG, MON_WAKE_PERIOD_REG to MON_EN, MON_WAKE_PERIOD	

TR ID	HWR ID	Description	Note
TR7_00, TR7_01	HWR_01_CYC_WAKE	clr_MON_WAKE_GO **shall** be high when MON_ADC_GO is synchronized High time of clr_MON_WAKE_GO **shall** >8us(after reg latch done).	
TR7_00, TR7_01, TR7_02	HWR_02_CYC_WAKE	CYC_WAKE **shall** output MON_ADC_GO according to MON_WAKE_PERIOD MON_WAKE_PERIOD **shall** cover 200ms-3.2s, step 200ms, 3.2s-156.8s, step 3.2s When D2A_CELL_ADC_EN is high, MON_ADC_GO **shall** be low MON_ADC_GO **shall** be cleared by clr_ADC_GO	
TR7_00, TR7_01, TR7_02	HWR_03_CYC_WAKE	CYC_WAKE **shall** output MON_WAKE according to MON_WAKE_PERIOD MON_WAKE **shall** be cleared by RR_END MON_WAKE **shall** be high earlier 10ms than MON_ADC_GO	
TR7_00	HWR_00_OVUV_OTUT_CMP	Once MON_WAKE_GO or ADC_GO_DLY is high, OVUV_OTUT_CMP **shall** latch and update OVUV_OTUT_EN_REG, CELL_OV_THRESH_REG, CELL_UV_THRESH_REG, GPIO_OTUT_THRESH_SEL_REG, GPIO_OT_PACK_THRESH_REG, GPIO_OT_PCB_THRESH_REG, GPIO_UT_PACK_THRESH_REG, GPIO_UT_PCB_THRESH_REG, CB_OT_PACK_THRESH_REG, CB_OT_PCB_THRESH_REG, OVUV_DEGL_REG to OVUV_OTUT_EN, CELL_OV_THRESH, CELL_UV_THRESH, GPIO_OTUT_THRESH_SEL, GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH, OVUV_DEGL	
TR7_00, TR7_03, TR7_04	HWR_01_OVUV_OTUT_CMP	OVUV_OTUT_CMP **shall** compare ADC_DATA_LPF with CELL_OV_THRESH and CELL_UV_THRESH when RR_END is high, and output CELL_OVUV according to OVUV_DEGL when OVUV_OTUT_EN is high.	
TR7_00, TR7_03, TR7_05, TR7_06	HWR_02_OVUV_OTUT_CMP	OVUV_OTUT_CMP **shall** compare OTH_ADC_DATA(only GPIO measurement result) with GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH according to GPIO_OTUT_THRESH_SEL when RR_END is high, and output GPIO_OTUT, GPIO_CBOT when OVUV_OTUT_EN is high	
TR7_00	HWR_03_OVUV_OTUT_CMP	OVUV_OTUT_CMP **shall** be reset when OVUV_OTUT_EN is low.	

TR ID	HWR ID	Description	Note
TR7_09	HWR_04_OVUV_OTUT_CMP	OVUV_OTUT_CMP **shall** output CELL_OVUV until counter=OVUV_DEGL The counter **shall** +1 when fault is detected The max of counter **shall** be OVUV_DEGL The counter **shall** -1 when fault is not detected	
TR9_00	HWR_00_I2C_MAS	I2C_MAS **shall** output SCL and SDA_OUT according to I2C_MAS_EN and I2C_CTRL. I2C_MAS **shall** support i2c master writing command.	
TR9_00	HWR_01_I2C_MAS	I2C_MAS **shall** output RD_DATA and ACK_BIT to DS_REG according to SDA_IN	
TR10_05	HWR_00_TM_KEY_CHECK	TM_KEY_CHECK **shall** check the TM_KEY using register bits pattern and timing pattern to output TRIM_EN and TMREG_EN TM_KEY_CHECK **shall** use TMREG_EN to protect TRIM_EN	
TR10_01	HWR_00_DFT	All internal power supplies **shall** support output HZ	
TR10_01	HWR_00_DFT	DFT mode **shall** be supported in Digital Core to detect stuck-at faults. Scan related signals **shall** be defined(SCAN_EN, SCAN_CLK, SCAN_RSTB, SCAN_MODE, SCAN_INx are inputs, SCAN_OUTx are outputs, x are integers that >= 1). Maximum value of x(scan chain number) **shall** be as big as possible.	
TR1_15	HWR_00_Digital_Core	When hr_sr_b is low, digital core(except identified device address) **shall** be reset	
TR10_01	HWR_00_CHIP	BM21A **shall** pass AEC-Q100 Grade1 qualification	
TR10_02	HWR_01_CHIP	BM21A **shall** pass ESD HBM: 2kV ESD CDM: 750V for corner pins, 500V for other pins Latch-up: ±200mA	
TR10_03	HWR_02_CHIP	Maximum die size of BM21A **shall** <22mm^2	
TR10_04	HWR_03_CHIP	Package of BM21A **shall** be LQPF 10x10-64E	
TR10_05	HWR_04_CHIP	FT time @ room temp for BM21A **shall**<6s	
TR10_06	HWR_05_CHIP	BM21A **shall** survive during 90V(5Vx18) battery pack random hot-plug	