Hardware Requirement

WP as Prerequisites	Author of HWR
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TR ID	HWR ID	Description	Note
TR001	HWR001_ADC	all blocks shall be shut down when REF_OK is low all blocks' bias current shall be IREF	
TR018	HWR_001_MUX_HV	MUX_HV **shall** choose one pair of Cn-Cn-1(n=1-18) or gnd as output MUX_OUT_HV according to CH_SEL	
TR080	HWR_002_MUX_HV	MUX_HV's power supply **shall** be CP	
TR001	HWR_003_MUX_HV	MUX_HV block **shall** only be enabled by D2A_CELL_ADC_EN	
TR018	HWR_001_MUX_LV	MUX_LV **shall** choose one channel between VPTAT/GPIOn(n=0-11) or gnd as output MUX_OUT_LV according to CH_SEL	
TR021	HWR_002_MUX_LV	Current flows into MUX_LV through GPIO/VPTAT **shall** <0.1uA	
TR022	HWR_003_MUX_LV	MUX_LV **shall** support 0-5V / 0-100%* TREF input voltage range MUX_LV's output voltage **shall**<REFP-REFN/ TREF (according to GPIO_REF_SEL)	
TR001	HWR_004_MUX_LV	MUX_LV block **shall** only be enabled by D2A_CELL_ADC_EN	
TR022	HWR_008_ADC_LV_SHT	ADC_LV_SHT shall use switching capacitors structure power suply for input sampling switch shall be CP the CLK signal for switching caps shall be ADC_CLK	
TR022	HWR_001_ADC_LV_SHT	ADC_LV_SHT **shall** shift the common voltage of MUX_OUT_HV to 1/2 VAA in output ADC_INPUT_LV	
TR018 TR022	HWR_002_ADC_LV_SHT	ADC_LV_SHT **shall** scale the differential voltage of MUX_OUT_HV down to 1/2 in output ADC_INPUT_LV	
TR080	HWR_003_ADC_LV_SHT	ADC_LV_SHT **shall** support VBAT+2V as input signal's max voltage	
TR021	HWR_004_ADC_LV_SHT	for ADC_LV_SHT , the differential input current at MUX_OUT_HV **shall** <1uA	
TR022	HWR_005_ADC_LV_SHT	the offset of ADC_LV_SHT(output differential voltage -input differential voltage *0.5) **shall** <3mV (4 sigma) the offset variation with temperature from -40 degree to 125 degree **shall** <0.5mV	
TR022	HWR_006_ADC_LV_SHT	the gain error of ADC_LV_SHT(output differential voltage /input differential voltage /0.5*100%) **shall** <0.5/1000 (4 sigma) the gain error variation with temperature from -40 degree to 125 degree **should** <0.1/1000	
TR001	HWR_007_ADC_LV_SHT	ADC_LV_SHT block **shall** only be enabled in active mode(D2A_CELL_ADC_EN is high)	
TR022 TR023	HWR_001_ADC_MODU	according to "XX.xls"ADC_MODU and ADC_LOGIC constitute a 6-bit SDM + 10-bit algorithm hybrid ADC with system level chopper(300us for 1 chennel) or 4-bit SDM + 12-bit algorithm hybrid ADC without system level chopper(30us for 1 channel)	
TR022	HWR_002_ADC_MODU	ADC_MODU **shall** choose ADC_INPUT_LV or MUX_OUT_LV as modulator's input voltage according to CH_SEL ADC_MODU shall transfer selected input voltage into BIT_STREAM under the control of ADC_SEQ	

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TR022	HWR_003_ADC_MODU	the reference voltage ADC_MODU use for Cn-Cn-1 /VPTAT **shall** be REFP-REFN , typical value **should** be 2.5V the reference voltage ADC_MODU use for GPIO input voltage measurement **shall** be REFP-REFN (accoding to GPIO_REF_SEL) the reference voltage ADC_MODU use for GPIO voltage ratio measurement **shall** be TREF (accoding to GPIO_REF_SEL)	
TR022	HWR_004_ADC_MODU	the LSB for Cn-Cn-1 **should** be typical 200uV The LSB for GPIO input voltage measurement **shall** be 200uV The LSB for GPIO voltage ratio measurement **shall** be 100uV /2.5V The LSB for die temperature **shall** be 200uV*2/k degree, the unit for k is degree/mV. the exact value of "k" is relative to the exact BG's schematic	
TR022	HWR_005_ADC_MODU	ENOB of Hybrid architecture ADC **shall** >14 bit (300us for 1 channel)	
TR001	HWR_006_ADC_MODU	ADC_LV_SHT block **shall** only be enabled in active mode(D2A_CELL_ADC_EN is high)	
TR055	HWR_007_ADC_MODU	the sample CLK of ADC_MODU shall be ADC_CLK	
TR030	HWR001_COMS_VCM HWR001_COMN_VCM	The RX of COMS/N_VCM shall be turned off when D2A_RX_EN is low and ACT is high	
TR030	HWR001_COMS_VCM HWR001_COMN_VCM	COMS/N_VCM **should** shift the +/- 20V common mode voltage of differential communication signals from COMS/N pins to typical 2.5V (COMS/N_SHAPE) The logic H threshold of differential communication signals for COMS/N_TONE_RX and COMS/N_COMM_RX **should** <1.2V The logic L threshold of differential communication signals for COMS/N_TONE_RX and COMS/N_COMM_RX **should** >0.4V The default output of COMN/S_VCM **shall** be logic 0	
TR001	HWR002_COMS_VCM HWR002_COMN_VCM	COMS/N_VCM **shall** always keep alive in both SD/sleep/active mode In shut down mode,the bias current for COMS/N_VCM **shall** be Istart; the total current consumption for COM_VCM **should**<2uA In sleep mode,the bias current for COMS/N_VCM **shall** be IREF; the total current consumption for COM_VCM **should**<5uA In active mode,the bias current for COMS/N_VCM **shall** be IREF	
TR030	HWR002_COMS_VCM HWR002_COMN_VCM	In sleep/SD mode, the delay time from COM pins to A2D_RX_S/N **should** < 500ns In active mode , the delay time from COM pins to A2D_RX_S/N **should** < 30ns	
TR039	HWR003_COMS_VCM HWR003_COMN_VCM	COMS/N_VCM should support converting differential signals with +-20V common mode voltage into differential signals with 2.5V common mode voltage	
TR001	HWR004_COMS_VCM HWR004_COMN_VCM	COMS/N_VCM **shall** be powered by LDOIN	
TR030	HWR005_COMS_VCM HWR005_COMN_VCM	COMS/N_VCM should keep voltage of COMMS/N pins 2.5V with typical 45Kohm when D2A_TX_EN is low and no COMM signals incoming from COMM pins	

TR ID	HWR ID	Description	Note
TR031	HWR001_COMN/S_TX	The typical value of driver resistor of COMN/S_TX **should** < 15ohm Delay time from D2A_TX to COMM pins **shall** <10ns	
TR032	HWR002_COMN/S_TX	COMN/S_TX **shall** output differential signal to COMN/S pins according to D2A_TX when D2A_TX_EN is high	
TR039	HWR003_COMN/S_TX	COMN/S_TX **shall** be enabled by D2A_TX_EN or TONE_TRANS_EN When not enabled, COMN/S_TX **shall** output high-z when voltage of COMM pins is during -20V-20V	
TR030	HWR004_COMN/S_TX	When TONE_TRANS_EN is H, if TONE_POLAR is low , HWR004_COMN/S_TX shall output logic 0 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal . if TONE_POLAR is high , HWR004_COMN/S_TX shall output logic 1 tone with typical 1us (min 700ns , max 2.5us) pules width at the rising edge of TONE_CLK signal .	
	HWR001_COMN/S_TONE_RX	When SPI_EN is high, COMS_TONE_RX shall not detect wake tone, S2A tone and SD tone When SPI_EN is high, COMN_TONE_RX shall not detect wake tone, S2A tone and SD tone	
TR030	HWR001_COMN/S_TONE_RX	COMN/S_TONE_RX shall output WAKE_TONE_DET when WAKE TONE is received. WAKE_TONE_DET shall be low when D2A_CLR_WAKEUP is received. WAKE Tone should be detected after >60 couplets of logic-1 are detected. COMN/S_TONE_RX does not need receiving all the tones to output WAKE_TONE_DET H.	
TR030	HWR002_COMN/S_TONE_RX	COMN/S_TONE_RX shall output STA_TONE_DET when STA TONE is received . STA Tone should be detected after 20-30 couplets of logic-1 are detected. STA Tone should only be detected during SLEEP mode. COMN/S_TONE_RX shall not output STA_TONE_DET before make sure all the tones is received.	
TR030	HWR003_COMN/S_TONE_RX	COMN/S_TONE_RX shall output SD_TONE_DET when SD TONE is received. SD Tone should be detected after >180 couplets of logic-0 are detected. COMN/S_TONE_RX does not need receiving all the tones to output SD_TONE_DET H.	
TR030	HWR004_ **COMS** _TONE_RX	**COMS** _TONE_RX shall output FLT_TONE_DET when FLT TONE is received. FLT Tone should only be detected during SLEEP mode. FLT Tone should be detected after 60-90 couplets of logic-0 are detected. COMN/S_TONE_RX shall not output FLT_TONE_DET before make sure all the tones is received.	
TR001	HWR005_COMN/S_TONE_RX	COMN/S_TONE_RX **shall** be powered by LDOIN COMN/S_TONE_RX **shall** be alive once LDOIN_OK is high COMN/S_TONE_RX **should** cost less than 100nA current during SD/sleep mode	

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TR030	HWR005_COMN/S_TONE_RX	COMN/S_TONE_RX shall have typical 720us (min 360us max 1080us) tone time out timer for logic 1 tone.	
TR030	HWR006_COMN/S_TONE_RX	COMN/S_TONE_RX shall have typical 1200us (min 1100us max 1300us) tone time out timer for logic 0 tone.	
	HWR007_COMN/S_TONE_RX	after timer reaches tone time out threshold , tone deglitch timer starts to count, before it reaches tone deglitch threshold(5ms typical), no tone should be detected .	
	HWR008_COMN/S_TONE_RX	The detection of logic-0 tone shall not blank the detection of logic-1 tone when SLEEP is high	
TR087, TR091	HWR006_PING_DET	PING_DET shall output WAKE_PING_DET when WAKE_PING is identified from A2D_SPI_MOSI and A2D_SPI_CSB WAKE_PING detection should monitor both the falling edge and rising edge to avoid faultly detection during power up	
TR093	HWR006_PING_DET	PING_DET shall output STA_PING_DET when STA_PING is identified from A2D_SPI_MOSI and A2D_SPI_CSB when SLEEP is high	
TR092	HWR006_PING_DET	PING_DET shall output SD_PING_DET when SD_PING is identified from A2D_SPI_MOSI and A2D_SPI_CSB	
TR088	HWR006_SPI Communication	When WAKE_TONE_DET is high, SPI Communication shall be off	
TR089	HWR006_SPI_EN_LOGIC	When WAKE_PING_DET is high, SPI_EN_LOGIC shall output SPI_EN high	
TR047	HWR001_JOT_CMP	JOT_CMP **should** compare VBE with JOT_REF to output JOT signal to CB_CTRL with 20us deglitch Hys of JOT_CMP **should** be 5℃	
TR047	HWR002_JOT_CMP	JOT_CMP **should** use one CMP to monitor all the junction temp sensors through time-sharing reusing the CMP	
TR001	HWR003_JOT_CMP	JOT_CMP **shall** only be enabled when CB_ON is high JOT **shall** keep low when JOT_CMP is not enabled	
TR086	HWR006_3P3	3P3 shall output V3P3 at typical 3.3V from LDOIN 3P3 shall use I_START and I_REF When LDOIN_OK is low, 3P3 shall be off	
TR085	HWR006_MOSI_INTER	MOSI_INTER shall convert MOSI in 3.3V domain into A2D_SPI_MOSI in 6V domain When MOSI>2.5V, MOSI_INTER shall output A2D_SPI_MOSI as high When MOSI<0.4V, MOSI_INTER shall output A2D_SPI_MOSI as low	
	HWR006_MOSI_INTER	When WAKE_TONE_DET is high, MOSI_INTER shall be off	
TR085	HWR006_MISO_INTER	When D2A_SPI_MISO is high, MISO_INTER shall output >2.5V at 1mA load When D2A_SPI_MISO is low, MISO_INTER shall output <0.4V at 1mA load	
	HWR006_MISO_INTER	When WAKE_TONE_DET is high, MISO_INTER shall be off	

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	SPI_RDY_INTER	When D2A_SPI_SPI_RDY is high, SPI_RDY_INTER shall output >2.5V at 1mA load When D2A_SPI_SPI_RDY is low, SPI_RDY_INTER shall output <0.4V at 1mA load	
		When WAKE_TONE_DET is high, SPI_RDY_INTER shall be off	
	CSB_INTER	CSB_INTER shall convert CSB in 3.3V domain into A2D_SPI_CSB in 6V domain When CSB>2.5V, CSB_INTER shall output A2D_SPI_CSB as high When CSB<0.4V, CSB_INTER shall output CSB as low	
		When WAKE_TONE_DET is high, CSB_INTER shall be off	
	SCLK_INTER	SCLK_INTER shall convert SCLK in 3.3V domain into A2D_SPI_SCLK in 6V domain When SCLK>2.5V, SCLK_INTER shall output A2D_SPI_SCLK as high When SCLK<0.4V, SCLK_INTER shall output A2D_SPI_SCLK as low	
		When WAKE_TONE_DET is high, SCLK_INTER shall be off	
TR068 TR069	HWR001_IO_INTER	When GPIO_PUPD_EN or ACTIVE or VAA_OK is low , IO_INTER shall output GPIO pins as high-z When GPIO_PUPD_EN is high, GPIO pins is configured as digital output with 0.4/4V voltage threshold and at least 1mA current ability.	
TR070	HWR002_IO_INTER	When GPIO_AS_IN_EN[11:0] is high, IO_INTER shall compare the GPIO pin's voltage with 1V/2.5V threshold and output corresponding H/L signal to GPIO_HL When GPIO_AS_IN_EN is low, GPIO_HL shall keeps low Leakage on GPIO pins into IO_INTER shall <1uA when configured as digital input	
TR071	HWR003_IO_INTER	IO_INTER should only pull up/down GPIO0 according to SCL when I2C_MAS_EN is H	
TR071	HWR004_IO_INTER	IO_INTER should only pull down GPIO1 according to SDA_OUT with 100ohm resistor when I2C_MAS_EN is H IO_INTER should only pull up GPIO1 to **3.3V** with 10k typical resistor when I2C_MAS_EN is H	
TR071	HWR005_IO_INTER	IO_INTER should output SDA_IN H to I2C_MAS when GPIO1 is H when I2C_MAS_EN is high IO_INTER should output SDA_IN L to I2C_MAS when GPIO1 is L when I2C_MAS_EN is high	
TR071	HWR006_IO_INTER	GPIOn_ANA(n=0-11) shall be buffered from GPIOn(n=0-11) when all GPIO_PUPD_EN, GPIO_AS_IN_EN, SPI_EN, I2C_MAS_EN are 1, otherwise, corresponding GPIOn_ANA(n=0-11) shall be pulled down to AGND	
TR085	IO_INTER	GPIOn_ANA(n=0-11) shall be buffered from GPIOn(n=0-11) when all GPIO_PUPD_EN, GPIO_AS_IN_EN, SPI_EN, I2C_MAS_EN are 1, otherwise, corresponding GPIOn_ANA(n=0-11) shall be pulled down to AGND	
TR090	IO_INTER	When FLT_WAKE and SPI_EN are high, corresponding GPIO2 shall be pulled low	

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TR044	HWR001_CBFET	CBFET **shall** provide a 2.5ohm @85 degree NMOS switch between every two adjacent Bn pins	
TR042 TR045 TR046 TR047 TR048 TR049 TR050	HWR002_CBFET	The switch shall only be closed when the corresponding CB_CH_EN n and REF_OK are both high The switch shall only be open when the corresponding CB_CH_EN n or REF_OK is low	
TR043	HWR003_CBFET	The max operating voltage of the CB switch shall be higher than 16V	
TR078	HWR004_CBFET	When hot plug happens, Bn pins may have a very big voltage slew rate, the shutdown resistor between gate and source of the NMOS CB switch shall be small enough to prevent CB switch turned on by coupling of parasitic capacitors.	
TR081	HWR005_CBFET	The mismatch of balance current for each separately enabled channel **shall** <10mA at 4.25V under same temp	
TR044	HWR001_PACK	Delta Tc of BM02A with 9 channels' 240mA balance current **shall** <20℃ at Ta=85℃	
TR000	HWR000_DRIVE	A pin named LDOIN **shall** output 5.7V	
TR000	HWR001_DRIVE	The accuracy of LDOIN **should** be 5% at full temp	
TR001	HWR002_DRIVE	The current consumption of a block named DRIVE **should** < 4uA at room temp	
TR001	HWR003_DRIVE	The max current-limiting of DRIVE pin **shall** be 2mA(typ), 1mA(min) @beta=200	xx616:img
TR001	HWR004_DRIVE	DRIVE block **shall** always on LDOIN **shall** feedback to DRIVE block	
TR002	HWR005_DRIVE	DRIVE **should** build within 1ms when the BAT is powered on	
TR017	HWR006_DRIVE	The UVLO threshold of BAT in DRIVE block **shall** <9V at room temp	
TR002	HWR007_DRIVE	The UVLO threshold of LDOIN in DRIVE block **should** <5.3V at room temp, and the Threshold hysteresis **should** be 100mV, deglitch time **should** be 600us When LDOIN is set up, DRIVE block **shall** output signal flag LDOIN_OK, and current source I_START The accuracy of current source I_START **shall** <30%	
TR000	HWR008_DRIVE	Thermal sensor TSD block **shall** be present in DRIVE block TSD block **shall** output TSD to short DRIVE pin to GND. TSD threshold **shall** be 150℃ TSD block **shall** be close to both of DRIVE and VAA block on layout	
TR000	HWR000_VAA	A pin named VAA **shall** output 5V	
TR001	HWR001_VAA	The current consumption of a block named VAA **should** < 5uA at full temp Bias current **shall** be I_START	

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TR001	HWR002_VAA	VAA block current-limiting **shall** support 20mA at most over full temp scale VAA block **should** switch current-limiting to 40mA	
TR001	HWR003_VAA	VAA block **shall** work in both sleep mode and active mode	
TR002	HWR004_VAA	VAA **should** build within 0.5ms when the flag signal LDOIN_OK is H	
TR022	HWR005_VAA	The accuracy of power VAA **should** be 3% at full temp	
TR002	HWR006_VAA	When VAA is set up, VAA block should output signal flag VAA_OK	
TR001	HWR007_VAA	The input refer voltage of VAA **shall** from pre-ref, when BG_OK is H, the refer voltage **shall** switch to BG output	
TR000	HWR000_VDD	A pin named VDD **shall** output 1.8V	
TR000 TR032	HWR001_VDD	The accuracy of power VDD **should** be 5% at full temp	
TR001	HWR002_VDD	The current consumption of a block named VDD **should** < 5uA at full temp Bias current **shall** be I_START	
TR001	HWR003_VDD	VDD block current-limiting **shall** support 10mA at most over full temp scale	
TR001	HWR004_VDD	VDD block **shall** work in both sleep mode and active mode	
TR002	HWR005_VDD	VDD **should** build within 0.5ms when the flag signal LDOIN_OK is H	
TR002	HWR006_VDD	When VDD is set up, VDD block should output signal flag VDD_OK	
TR018 TR080	HWR000_CP	Block CP output voltage VCP **shall** be BAT+5V when the output is no-load	
TR080	HWR001_CP	Block CP min output voltage VCP **shall** be BAT+3V when the max output load is 150mA	
TR018	HWR002_CP	The ripple of VCP **shall** <300 mV, when the current load is 150uA	
TR018 TR001	HWR003_CP	Block CP **shall** start work when REF_OK is H Block CP **shall** work during active mode or MON_WAKE is high or CB_EN is high	
TR001	HWR004_CP	The current consumption of a block named CP **should** < 50uA at full temp Bias current **shall** be I_REF	
TR000 TR022	HWR000_REFP	A block named REFP output two voltages **shall** be named REFP and REFN The output voltage of REFP-REFN **shall** be 2.5V (typ)	
TR022	HWR001_REFP	The output of REFP-REFN **shall** be trimmed by TRIM The temp drift of REFP-REFN **shall** <5ppm/℃ The long term drift of REFP-REFN **shall** <20ppm/sqr(khr)	
TR022	HWR002_REFP	The DC accuracy of REFP-REFN **shall** be 0.5‰ at room temp	

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TR001 TR003	HWR003_REFP	REFP block **shall** only work in active mode or MON_WAKE is high REFP block **shall** start work when IREF_OK is H	
TR001	HWR004_REFP	The current consumption of a block named REFP **should** < 90uA at full temp Bias current **shall** be I_REF	
TR001	HWR005_REFP	REFP block **shall** support 10mA current load at most over full temp scal	
TR001 TR022	HWR006_REFP	When REFP is set up, REFP block should output flag signal REFP_OK	
TR016	HWR000_BG	The output of BG **shall** be trimmed by TRIM The temp drift of VBG **shall** <50ppm/℃	
TR016	HWR001_BG	The DC accuracy of VBG **shall** be 0.5%at room temp	
TR001	HWR002_BG	The current consumption of a block named BG **should** < 20uA at full temp Bias current **shall** be I_START	
TR001	HWR003_BG	BG block **shall** work in both sleep mode and active mode BG block **shall** start work when VAA_OK is H	
TR002	HWR004_BG	When BG is set up, BG block **shall** output flag signal BG_OK	
TR000	HWR000_TREF	A pin named TREF **shall** output 2.5V	
TR017	HWR001_TREF	Output voltage TREF **shall** have 10% accuracy at (10/12)kOhm ~200kOhm load at full temp TREF **shall** work stably without resistance load	
TR001	HWR002_TREF	The current consumption of TREF block **should** <20uA Bias current **shall** be I_REF	
TR002 TR055	HWR003_TREF	TREF rise time **shall** within 500us at every load case @2.2uF	
TR55	HWR004_TREF	TREF block **shall** work when ACT is H or MON_WAKE is high	
TR001	HWR005_TREF	TREF block **shall** shutdown when IREF_OK is L	
TR001	HWR006_TREF	When TREF is set up, TREF **shall** output flag signal TREF_OK	
TR001	HWR007_TREF	TREF block current-limiting **shall** support 5mA at most over full temp scale	
TR001	HWR000_IREF	IREF **shall** powered by VAA, and work in both active mode and sleep mode	
TR001 TR018	HWR001_IREF	The input refer voltage of IREF **shall** be VBG signal	
TR013 TR014 TR018	HWR002_IREF	The accuracy of IREF signal **shall** be 10% at full temp The output of IREF signal **shall** be trimmed by TRIM	Res @temp -40~150C -0.17%~0.65% MC of IREF 1sigma=1.3%
TR001	HWR003_IREF	IREF block **shall** start work when BG_OK is H	
TR001	HWR004_IREF	The current consumption of a block named IREF **should** < 3uA at full temp Bias current **shall** be I_START	

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TR001	HWR005_IREF	When IREF is set up, IREF **shall** output flag signal IREF_OK	
TR001 TR022 TR056	HWR000_REF	REF block set up seq **shall** be like the follow pic 	
TR022	HWR000_VPTAT	VPTAT output accuracy shall meet k(T+-4) (T is the absolute temperature of junction, Kelvin), T=233K-400K	
TR047	HWR000_BE	The input current source of BE block **shall** be I_REF	
TR047	HWR001_BE	There **shall** be have 9 BE blocks on layout, each BE is placed near every two groups of CBFETs	
TR047	HWR000_JOT_DAC	Signal CB_TWARN_THRESH[3:0] **shall** select and output JOT_REF based on VBG	
TR047	HWR001_JOT_DAC	The scale of JOT_REF **shall** make the CB_TWARN programable scale is 100℃-150℃, accuracy is 5℃, step is 5℃	
TR013 TR014	HWR000_CLK	LCLK block **shall** output clock signal CLK_256K 256kHz, with 5% accuracy at full temp The duty of CLK_256K **shall** be 50% The output of CLK_256K **shall** be trimmed by TRIM	
TR003 TR013 TR014	HWR001_CLK	LCLK **shall** work during active mode and sleep mode	
TR001	HWR002_CLK	CLK block **shall** work when REF_OK and VDD_OK is H	
TR032	HWR003_CLK	HCLK block **shall** output clock signal CLK_32M 32MHz by PLL based on CLK_256K, with 5% accuracy at full temp	
TR003	HWR004_CLK	When CLK_32M is established, CLK block **shall** output flag signal CLK_32M_OK	
TR013 TR014	HWR005_CLK	When CLK_256K is established, CLK block **shall** output flag signal CLK_256K_OK	
TR003	HWR006_CLK	CLK_256K, CLK_32M and CLK_32M_OK signal **shall** work as following seq 	
TR001 TR003	HWR007_CLK	HCLK **shall** work only during active mode or MON_WAKE is high	
TR001	HWR008_CLK	The current consumption of LCLK block **should** < 10uA at full temp The current consumption of HCLK block **should** <150uA at full temp Bias current **shall** be I_REF	rev0 output 256k ->512k: 9.3uA ->12uA
TR047	HWR009_CLK	LCLK block **shall** output JOT_CLK to JOT_CMP for check periodically	

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TR003 TR007 TR030	HWR000_SEQ	When WAKE_TONE_DET is H (rise edge), The output signal ACT **shall** be H, and DRSTB **shall** reset to L last 8us, then set to H, SLEEP and SD **shall** be L When STA_TONE_DET is H (rise edge), The output signal ACT **shall** be H (only during sleep mode), SLEEP and SD **shall** be L	
TR003 TR008 TR030	HWR001_SEQ	When SD_TONE_DET is H (rise edge), The out signal SD **shall** be H, ACT and SLEEP **shall** be L When D2A_TO_SD is H (rise edge), The out signal SD **shall** be H, ACT and SLEEP **shall** be L	
TR003 TR009 TR030	HWR002_SEQ	When D2A_TO_SLEEP is H (rise edge), The out signal SLEEP **shall** be H, ACT and SD **shall** be L	
TR010 TR030	HWR003_SEQ	DRSTB **shall** be L when CLK_256K_OK is L DRSTB **shall** be L when VAA_OK is L DRSTB **shall** be L when VDD_OK is L When DRSTB from L to H, ACT **shall** be output H, besides, SLEEP and SD **shall** be L	
TR014	HWR004_SEQ	ACT **shall** be H when LCTO_SET input H (rise edge) and LCTO_SEL[1:0]=ACT, besides, SLEEP and SD **shall** be L SLEEP **shall** be H when LCTO_SET input H (rise edge) and LCTO_SEL=SLEEP, besides, SLEEP and SD **shall** be L SD **shall** be H when LCTO_SET input H (rise edge) and LCTO_SEL=SD, besides, SLEEP and ACT **shall** be L	
TR003	HWR005_SEQ	When LDOIN_OK is H, SEQ block **shall** start work When LDOIN_OK is H, the default value of output **shall** be: ACT=0; SLEEP=0; SD=1; DRSTB=0	
TR089, TR091	HWR006_SEQ	When WAKE_PING_DET is H (rise edge), The output signal ACT **shall** be H, and DRSTB **shall** reset to L last 8us, then set to H, SLEEP and SD **shall** be L	
TR093	HWR007_SEQ	When STA_PING_DET is H (rise edge), The output signal ACT **shall** be H (only during sleep mode), SLEEP and SD **shall** be L	
TR092	HWR008_SEQ	When SD_PING_DET is H (rise edge), The out signal SD **shall** be H, ACT and SLEEP **shall** be L	
TR001 TR015	HWR000_RST_REG	RST_REG **shall** be powered by always on LDOIN RST_REG **shall** work when LDOIN_OK is H, during three work modes RST_REG **shall** be reset when LDOIN_OK is L	
TR015	HWR001_RST_REG	When the LCTO_SD is a rise edge, LCTO_SD_LATCH **shall** output H When the CLK_256K_OK is a falling edge, CLK_256K_OKB_LATCH **shall** output H When the VAA_OK is a falling edge, VAA_OKB_LATCH **shall** output H When the VDD_OK is a falling edge, VDD_OKB_LATCH **shall** output H	
TR015	HWR002_RST_REG	RST_REG **shall** be reset by RST_XXX_LATCH, when it is written to 1.	seperate signal XXX confer block diagram

TR ID	HWR ID	Description	Note
TR038	HWR003_RST_REG	COMM_DIG_SETTING **should** include TOP_DEV, DIR_SEL, DEV_ADD, DEV_NUM COMM_DIG_SETTING **should** be latched in RST_REG when ADD_W_EN falling edge RST_REG **shall** output default values included by COMM_DIG_SETTING_LATCH	
TR038	HWR004_RST_REG	The default value of XXX_LATCH and COMM_DIG_SETTING_LATCH shall be same as corresponding register in digital core	
	HWR005_RST_REG	When SDB is low, CLK_256K_OKB, VDD_OKB and VAA_OKB shall be blanked by RST_REG	
TR001	HWR001_CKGEN1	CKGEN1 shall generate CLK_OUT. CLK_OUT shall be from CLK_32M when CLK_32M_OK is high, and from CLK_256K when CLK_32M_OK is low.	
TR001	HWR002_CKGEN1	CKGEN1 shall generate CLK_SLOW. CLK_SLOW shall be from divided CLK_32M_EN when CLK_32M_OK high, and from CLK_256K when CLK_32M_OK low.	
TR001	HWR003_CKGEN1	Higher clock gatings shall be used in CKGEN1. The gate signals in higher clock gatings are CLK_32M_OK (for CLK_REG) , D2A_CELL_ADC_EN(for CLK_ADC), D2A_AUX_ADC_EN(for CLK_AUX_ADC).	
TR001	HWR004_CKGEN1	Higher clock gatings shall be used in CKGEN1. The gate signals in higher clock gatings are MTP_EN(for CLK_MTP), CB_EN(for CLK_CB), I2C_MAS_EN(for CLK_I2C).	
TR001, TR073	HWR005_CKGEN1	CKGEN1 shall output CLK_32M_SC. When SCAN_MODE is high, CLK_32M_SC shall be from SCAN_CLK, when SCAN_MODE is low, CLK_32M_SC shall be from CLK_32M.	
TR001	HWR006_CKGEN1	CLK_REG shall be divided clock from CLK_32M. CLK_REG should be 8MHz.	
TR073	HWR007_CKGEN1	CKGEN1 shall mux all clocks with scanmux. Each scanmux shall output functional clock when SCAN_NODE is low, and output SCAN_CLK when SCAN_MODE is high. The clock outputs of CKGEN1 shall be CLK_REG_SC, CLK_ADC_SC, CLK_MTP_SC, CLK_CB_SC, CLK_I2C_SC, CLK_SLOW_SC, CLK_OUT_SC.	
TR022, TR055	HWR008_CKGEN1	CKGEN1 shall output ADC_CLK, ADC_CLK_H according to ADC_CLK_SET.	refer to BM02A _ ADC_ Design _ Summaries. xlsx
TR001	HWR001_MTP_INTERF	Higher clock gating signal MTP_EN shall be generated in MTP_INTERF. MTP_EN shall be high when MTP write or MTP read starts, and shall be low when MTP write and MTP read ends. MTP_EN shall be initially high for MTP loading.	
TR001, TR022	HWR002_MTP_INTERF	MTP_INTERF shall support writing MTP via MTP_CTRL_BITS in DS_REG. MTP write starts when WR_MTP is high. MTP write ends when all MTP address are covered. Refer to ".pdf"	
TR001, TR022	HWR003_MTP_INTERF	MTP_INTERF shall support reading MTP after reset. MTP read starts after reset(DRSTB posedge or SOFT_RSTB posedge) when CLK_32M_EN is high. MTP read ends when all MTP address are covered. Refer to ".pdf"	

TR ID	HWR ID	Description	Note
TR023	HWR001_MTP_TOP	Data in MTP shall be loaded to DS_REG via DOUT after reset(DRSTB posedge or SOFT_RSTB posedge) done.	
TR022	HWR002_MTP_TOP	Load_done shall be high after MTP load done.	
TR004, TR007, TR030	HWR001_TONE_CTRL	TONE_CTRL shall output WAKEUP TONE(consist of 90 logic-1 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN when WAKE_TONE_DET high.	
TR004, TR007, TR030	HWR002_TONE_CTRL	TONE_TRANS_EN shall include TONE_TRANS_EN_N and TONE_TRANS_EN_S. TONE_TRANS_EN_N or TONE_TRANS_EN_S shall be the opposite direction of WAKE_TONE_DET, STA_TONE_DET.	
TR004 TR007 TR030	HWR003_TONE_CTRL	TONE_CTRL shall output STA TONE(consist of 30 logic-1 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN when received STA_TONE_DET.	
TR030	HWR004_TONE_CTRL	TONE_CTRL shall output SD TONE(consist of 270 logic-0 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN after SD_TONE_GEN high. Direction in TONE_TRANS_EN shall base on SPI_DIR	refer to " how ...ppt"
TR030	HWR005_TONE_CTRL	TONE_CTRL shall output FLT TONE(consist of 90 logic-0 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N every 50ms only when SLEEP high after FLT_WAKE high.	
TR030	HWR006_TONE_CTRL	TONE_CTRL shall output HB TONE(consist of 30 logic-0 couplets) on TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N every 400ms only when SLEEP high.	refer to " how ...ppt"
TR030	HWR007_TONE_CTRL	The period of TONE_CLK for all tones should be 11us.	refer to " how ...ppt"
TR030	HWR008_TONE_CTRL	Clr_SD_TONE_GEN shall be high after SD_TONE_GEN synchronization.	
TR030	HWR009_TONE_CTRL	TONE_CTRL shall not output HB TONE on TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N once FLT_WAKE high. After FLT_WAKE is 0 again, TONE_CTRL shall output HB TONE on TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N every 400ms only when SLEEP high.	
TR030	HWR010_TONE_CTRL	TONE_TRANS_EN shall be reset to 0 when D2A_TX_EN_S or D2A_TX_EN_N(in D2A_TX) is high.	
TR030	HWR011_TONE_CTRL	WAKE TONE and STA TONE shall have higher priority to HB TONE and FLT TONE.	
TR094, TR095	HWR012_TONE_CTRL	TONE_CTRL shall generate wake tone when WAKE_TONE_GEN is high Direction in TONE_TRANS_EN shall base on SPI_DIR	
	HWR013_TONE_CTRL	TONE_CTRL shall output clr_WAKE_TONE_GEN high after WAKE_TONE_GEN is detected as high	
	HWR016_TONE_CTRL	TONE_CTRL shall output a high pulse on D2A_CLR_WAKEUP when WAKE_TONE_DET is high and WAKE TONE is already generated at the opposite direction of WAKE_TONE_DET	
TR099	HWR014_TONE_CTRL	TONE_CTRL shall generate STA tone when STA_TONE_GEN is high Direction in TONE_TRANS_EN shall base on SPI_DIR	
TR099	HWR015_TONE_CTRL	TONE_CTRL shall output clr_STA_TONE_GEN high after STA_TONE_GEN is detected as high	

TR ID	HWR ID	Description	Note
TR008, TR009	HWR001_DS_BASIC	DS_BASIC shall extract rx_data[8:0] (1 new frame bit+ 8 data bits) from A2D_RX.	
TR037, TR040, TR041	HWR002_DS_BASIC	DS_BASIC shall start frame propagation on D2A_TX in the opposite direction of A2D_RX.	
TR032	HWR003_DS_BASIC	DS_BASIC should re-locate the received signal bit by bit.	
TR032	HWR004_DS_BASIC	DS_BASIC should use majority vote (10%) to sample A2D_RX.	
TR030	HWR005_DS_BASIC	D2A_RX_EN shall be default high D2A_TX_EN, D2A_RX_EN，and TONE_TRANS_EN, D2A_RX_EN shall not be high at the same time at same port	
TR089	HWR006_DS_BASIC	the corresponding direction of SPI_DIR in D2A_RX_EN shall be low when SPI_EN is high	
TR030	HWR007_DS_BASIC	After preamable + SYNC[1:0] are received, the opposite A2D_RX data shall be blanked	
TR030	HWR008_DS_BASIC	A new frame is identified by DS_BASIC when SOF bit is recognised	
TR030	HWR011_DS_BASIC	After (0.5us+STACK_RESP_CMD) bus short blank time from the complete reception of last byte, the new preamable shall not be identified by DS_BASIC until a 0.5us bus idle (logic-0) is detected to avoid faulty preamable identification due to ring of communication bus	
TR098	HWR009_DS_BASIC	The output D2A_TX_EN (N) of DS_BASIC shall only be high when COMN_TX_DIS is low The output D2A_TX_EN (S) of DS_BASIC shall only be high when COMN_TX_DIS is low	
TR089	HWR010_DS_BASIC	When SPI_EN high and SPI_DIR is south, DS_BASIC shall propagate frame to north When SPI_EN high and SPI_DIR is north, DS_BASIC shall propagate frame to south	
	HWR012_DS_BASIC	For each byte, the following bits shall start to be extracted only after preamable + SYNC[1:0] are received correctly(timing and data)	
TR097	HWR001_SPI_BASIC	The SOF identification by SPI_BASIC should be based on CSB falling edge	
TR089, TR103	HWR002_SPI_BASIC	Each bit should be captured on low to high clock transitions of A2D_SPI_SCLK and propagated on high to low clock transition of A2D_SPI_SCLK Default SCLK shall be logic-0, MOSI and MISO shall be logic-1 For each byte, MSB shall be transmitted first	
TR089	HWR003_SPI_BASIC	SPI_BASIC shall extract data[7:0] into 8-byte RX FIFO from A2D_SPI_SCLK and A2D_SPI_MOSI. SPI_BASIC shall start propagation of frame in 8-byte TX FIFO on A2D_SPI_SCLK and D2A_SPI_MISO.	
TR097	HWR004_SPI_BASIC	SPI communication clear pattern (0x00 as INIT byte after CSB's falling edge) shall be monitored by SPI_BASIC Once communication clear pattern is detected, output SPI_CLR_DET high pulse, TX FIFO and TX FIFO shall be reset	

TR ID	HWR ID	Description	Note
TR102	HWR005_SPI_BASIC	Once COPY_NXT is detected (every COPY_NXT detection should delay 30ns), SPI_BASIC shall transmit next RX FIFO data and SPI_SOF bit	
TR102	HWR006_SPI_BASIC	When RESP is high, there shall be a 60us timer in SPI_BASIC, which shall start to count by the first reception of tx_data[8:0] and be reset by the reception of tx_data[8:0] SPI_BASIC shall output TX_DONE high once the 60us timer timeout and TX_FIFO is totally empty	
TR101	HWR007_SPI_BASIC	When RESP is low, SPI_BASIC shall output D2A_SPI_MISO logic-1 When RESP is high, RX FIFO in SPI_BASIC shall reject A2D_SPI_MOSI (CLR_DET shall not reject A2D_SPI_MOSI when RESP is high)	
TR101	HWR008_SPI_BASIC	SPI_BASIC shall only output data bytes in TX FIFO to D2A_SPI_MISO when RESP is high	
TR100	HWR009_SPI_BASIC	SPI_BASIC shall output FIFO_OF when RX FIFO is overflow at RESP is low or TX FIFO is overflow at RESP is high SPI_BASIC shall output FIFO_UF when TX FIFO is underflow at RESP is high	
TR100	HWR010_SPI_BASIC	When RESP is low: D2A_SPI_SPI_RDY shall be default high D2A_SPI_SPI_RDY shall be low in 2us when RX FIFO>4 bytes D2A_SPI_SPI_RDY shall be high in 2us when RX FIFO<=2 bytes	
TR100	HWR011_SPI_BASIC	When RD_DET is high: D2A_SPI_SPI_RDY shall be default low D2A_SPI_SPI_RDY shall be high in 2us when PING/PONG is full or TX FIFO 60us timer timeout D2A_SPI_SPI_RDY shall be low in 2us when any PING/PONG is empty (D2A_SPI_SPI_RDY low shall be at least 2us)	
TR097	HWR003_BASIC_CTRL	BASIC_CTRL shall extract rx_data[8:0] (1 SOF bit+8 data bit) from SPI_BASIC	
TR089	HWR001_BASIC_CTRL	When SPI_EN high: When RESP high, BASIC_CTRL shall select SPI_BASIC to receive tx_data, which comes from rx_data of DS_BASIC or R When RESP low, BASIC_CTRL shall select SPI_BASIC into rx_data When RESP low, BASIC_CTRL shall select DS_BASIC to transmit tx_data When SPI_EN low: BASIC_CTRL shall select DS_BASIC into rx_data BASIC_CTRL shall select DS_BASIC to transmit tx_data BASIC_CTRL shall record read command reception port (COMN/COMS), and transmit response to the same port	
TR001	HWR002_BASIC_CTRL	When CLK_32M_OK is low, BASIC_CTRL shall be synchronously-reset to initial state.	
TR037, TR040, TR041	HWR001_COMM_CTRL	COMM_CTRL shall support frame propagation on tx_data from rx_data.	

TR ID	HWR ID	Description	Note
TR001	HWR002_COMM_CTRL	When CLK_32M_OK is low, COMM_CTRL shall be synchronously-reset to initial state.	
TR008, TR009, TR034, TR036	HWR003_COMM_CTRL	COMM_CTRL shall support writing register bit. COMM_CTRL distinguish device_addr, bytes_num, ini_reg_addr and data from rx_data, and then write to DS_REG via W. Reg_addr shall automatically add by 1 when bytes_num > 1 for continuous writing. If device_addr not match with DEV_ADD(in COMM_DIG_SETTING), no register shall be written. If received direction not match with DIR_SEL(in COMM_DIG_SETTING), no register shall be written.	
TR030, TR033, TR035	HWR004_COMM_CTRL	COMM_CTRL shall support reading register bit. COMM_CTRL distinguish device_addr, bytes_num, and ini_reg_addr from rx_data, and then send reg_addr via W to DS_REG(preparing to response register data). If device_addr not match with DEV_ADD(in COMM_DIG_SETTING), no register shall be read. If received direction not match with DIR_SEL(in COMM_DIG_SETTING), no register shall be read.	
TR030, TR033, TR035	HWR005_COMM_CTRL	When responsing, COMM_CTRL shall extract data(corresponding to reg_addr) from COMM_REG via R, then send device_addr, bytes_num, ini_reg_addr and data to BASIC_CTRL via tx_data. Reg_addr shall automatically add by 1 when bytes_num > 1 for continuous reading.	
TR030	HWR006_COMM_CTRL	Data format in D2A_TX and A2D_RX shall be as described : The character shall consist of 0.5-bit preamble bit, 2-bit SYNC bits,1-bit SOF bit, 8-bit DATA bit,1-bit CERR bit,0.5-bit postable bit SOF bit should represent the start of frame The DATA of character shall send LSB then MSB Before each character, there shall be 1.375us idle time. After each character,0.5us short time shall be present. The baud rate of DATA communication shall be 2Mbps. The logic 1 of bit shall consist of 1 differential couplet: positive half-bit first, negative half-bit then The logic 0 of bit shall consist of 1 differential couplet: negative half-bit first, positive half-bit then	waveform for information, 15ohm, 45K
TR030	HWR007_COMM_CTRL	Data format in D2A_TX and A2D_RX shall be as described : INIT byte in D2A_TX and A2D_RX shall: bit 7 define the frame type: 1 is command, 0 is response for command, bit6-bit4: 000 is Single Read, 001 is Single Write, 010 is Stack Read, 011 is Stack Write; bit3-bit0: represent the number of DATA bytes (max 16 bytes) for response, bit6-bit0: represent the number of DATA bytes (max 128 bytes)	
TR030	HWR008_COMM_CTRL	Data format in D2A_TX and A2D_RX shall be as described : DATA byte in D2A_TX and A2D_RX shall: define the data value to be written for write command define the byte number to be read for read command	
TR030	HWR009_COMM_CTRL	Data format in D2A_TX and A2D_RX shall be as described : CRC bytes shall use CRC-16-IBM polynomial (x^16+x^15+x^2+1) with 0xFFFF initialization	

TR ID	HWR ID	Description	Note
TR030	HWR010_COMM_CTRL	Data format in D2A_TX and A2D_RX shall be as described : Single Write command frame shall consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes Stack Write command frame shall consist of 1 INIT byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes Single Read command frame shall consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, 1 DATA byte, 2 CRC bytes Stack Read command frame shall consist of 1 INIT byte, 2 REG_ADD bytes, 1 DATA byte, 2 CRC bytes Response frame of each device shall consist of 1 INIT byte, 1 DEV_ADD byte, 2 REG_ADD bytes, n DATA bytes, 2 CRC bytes	
TR030	HWR011_COMM_CTRL	A new frame is identified by COMM_CTRL when SOF bit is recognised high	
TR030	HWR012_COMM_CTRL	After receiving Stack Read Command: If TOP_DEV is low, COMM_CTRL shall send itselfs' response frame in tx_data only when response frame from +1 device address is propagated. If TOP_DEV is high, COMM_CTRL shall send itselfs' response frame in tx_data to BASIC_CTRL.	
TR030, TR096	HWR013_COMM_CTRL	COMM_CTRL shall program the delay time(from 0.25us-15.75us) between characters by STACK_RESP_CMD. When SPI_EN is low, STACK_RESP_CMD shall program the self-generated response delay only When SPI_EN is high, STACK_RESP_CMD shall program the self-generated(from SPI RX FIFO) command delay only	
TR032	HWR014_COMM_CTRL	COMM_CTRL should sample A2D_RX using CLK_32M COMM_CTRL should transmit D2A_TX using CLK_32M	
TR037, TR040, TR041	HWR015_COMM_CTRL	COMM_CTRL should identify Broadcast Read Command as Addressing Identification Command	Refer to BM02A_IOS
TR037, TR040, TR041	HWR016_COMM_CTRL	If signal frame type is address identification, frame propagation shall be canceled. If signal frame type is not address identification, frame propagation shall start after a byte is completely received from rx_data.	
TR013, TR014	HWR017_COMM_CTRL	FRAME_DONE shall be generated when a frame is received completely. FRAME_DONE shall be a pulse.	
TR037, TR040, TR041, TR089	HWR019_COMM_CTRL	When SPI_EN is high, Addressing Identification Command shall be not be executed (only propagated)	
TR097	HWR020_COMM_CTRL	When CLR_DET is detected at SPI_EN is high, RESP, RD_DET and COPY_NXT of COMM_CTRL shall be reset (then, tx_data shall not propagate the comm clr pattern: 0x00 with SOF=1)	
TR102	HWR021_COMM_CTRL	COMM_CTRL shall output RESP low default When valid (without CRC fault) read command (no matter single read command, stack read command or addressing command(broadcast read command), no matter reading of itself or reading of AFE) is received at SPI_EN is high, output RESP high When TX_DONE is high, RESP comes back to low	

TR ID	HWR ID	Description	Note
TR102	HWR022_COMM_CTRL	COPY_NXT shall output high only when RESP is low at SPI_EN is high COPY_NXT shall be default high when RESP is low COMM_CTRL shall output COPY_NXT high when one byte received rx_data[8:0] is already propagated to tx_data[8:0] (including STACK_CMD) COPY_NXT shall be cleared to low when rx_data[8:0] is received	
TR100	HWR023_COMM_CTRL	COMM_CTRL shall output RD_DET low default When read command (according to INIT byte) is detected at SPI_EN is high, output RD_DET high When TX_DONE is high, RESP comes back to low	
TR013, TR014	HWR001_COMM_TO	COMM_TO shall contain a watchdog counter The counter shall be reset when FRAME_DONE is high, or when ACT is low. The timer **shall** support being programmed from 100ms to 1h with 8 steps, by PROG_SCTO or PROG_LCTO.	
TR013	HWR002_COMM_TO	COMM_TO shall output SET_SCTO when counter reach the the threshold programmed by the PROG_SCTO[2:0].	
TR014	HWR003_COMM_TO	COMM_TO shall output SET_LCTO when counter reach the the threshold programmed by PROG_LCTO[2:0].	
TR008, TR009	HWR001_COMM_REG	There shall be TO_SD bit in DS_REG to output D2A_TO_SD respectively when being written by COMM_CTRL. TO_SD and D2A_TO_SD shall be pulses. Pulse high width shall > 8us.	
TR008, TR009	HWR002_COMM_REG	There shall be TO_SLEEP bit in DS_REG. TO_SLEEP shall be high when written high via COMM_DIG, and shall be low when clr_TO_SLEEP high.(Pulse high width shall > 8us).	
TR013	HWR003_COMM_REG	The SCTO threshold, PROG_SCTO[2:0] shall be defined in DS_REG.	
TR014	HWR004_COMM_REG	The LCTO threshold, PROG_LCTO[2:0] shall be defined in DS_REG.	
TR014	HWR005_COMM_REG	There shall be LCTO_SEL[1:0] bits in DS_REG and output to analog part.	
TR022	HWR008_COMM_REG	TRIM_ADC bits(92 bytes) shall be defined in DS_REG. TRIM_ADC shall only be written or read when TRIM_EN is high.	
TR018, TR022	HWR009_COMM_REG	ADC_DATA_LPF(including ADC_LPF_CH1-18[15:0]) **shall** be readable via DS_REG.	
TR018, TR022	HWR010_COMM_REG	ADC_SETTING_REG shall be defined in DS_REG. ADC_SETTING_REG shall include ADC_MODE_REG[1:0], ADC_CHP_EN_REG, ADC_CLK_SET_REG[1:0], CH_DT_REG[1:0], CH_STL_REG[3:0], CH_TOP_STL_REG[3:0], DLPF_FC_REG[2:0], GPIO_REF_SEL_REG[11:0].	
TR023, TR024, TR029	HWR011_COMM_REG	There shall be register bits in DS_REG to output ADC_GO including one-round-robin(ADC_SGLE_GO) and continuous measurement(ADC_CNTI_GO). ADC_GO shall be cleared when clr_ADC_GO high or CLK_32M_OK low. ADC_GO high pulse width shall >8us.	Follow "BM02A_ ADC_ Sequences. vsd"

TR ID	HWR ID	Description	Note
	HWR012_COMM_REG	MON_WAKE_GO shall be defined in DS_REG. MON_WAKE_GO shall be cleared when clr_MON_WAKE_GO high.	
TR023, TR024	HWR013_COMM_REG	FREEZE bit shall be defined DS_REG.	
TR029	HWR014_COMM_REG	CELL_ADC_DATA(including ADC_CH1-18[15:0]) and OTH_ADC_DATA(including ADC_GPIO0-11[15:0], ADC_VPTAT[15:0], xxx) shall support being read by COMM_CTRL.	
TR029	HWR015_COMM_REG	DLPF_FC[2:0] shall be defined in DS_REG. DLPF_FC range：10Hz-1kHz, 8 steps DLPF_FC[2:0] shall include disable control	
TR027	HWR016_COMM_REG	RR_COUNTER, ADC_DATA_LPF and OTH_ADC_DATA shall all be stored in DS_REG with continuous addresses.	CELL_ADC_DATA are needed in roadtest.
TR028	HWR018_COMM_REG	RR_COUNTER[15:0] shall support being read by COMM_CTRL.	
TR030	HWR019_COMM_REG	STACK_RESP_CMD[5:0] shall be defined in DS_REG and output to COMM_CTRL.	
TR030	HWR020_COMM_REG	SD_TONE_GEN and SD_TONE_DIR shall be defined in DS_REG and output to TONE_CTRL. SD_TONE_GEN shall be high when written 1 via COMM_DIG, and shall be clear when clr_SD_TONE_GEN is high.	
TR037	HWR021_COMM_REG	TOP_DEV, DIR_SEL, DEV_ADD[6:0], DEV_NUM[6:0], ADD_W_EN shall support being read by COMM_CTRL	
TR037	HWR022_COMM_REG	ADD_W_EN shall only be set 1 when address identify starts. ADD_W_EN shall not be cleared when address identify ends. ADD_W_EN shall be 0 when writing via COMM_CTRL.	
TR038	HWR023_COMM_REG	COMM_DIG_SETTING shall be defined in DS_REG (default values from XXX_LATCH) COMM_DIG_SETTING shall include TOP_DEV, DIR_SEL, DEV_ADD[6:0]. TOP_DEV, DIR_SEL, DEV_ADD shall not be changed when ADD_W_EN is low.	
TR023, TR024	HWR024_COMM_REG	DEV_NUM[6:0] shall be defined in DS_REG (default values from DEV_NUM_LATCH) DEV_NUM is changed by COMM_CTRL address identifying or written via COMM_CTRL when ADD_W_EN high. When address identify starts, DEV_NUM is clear to 0. DEV_NUM adds by step 1 when a response is received . DEV_NUM shall not be changed when ADD_W_EN is low.	DEV_NUM means Remaining device number in the system.
TR043, TR045	HWR025_COMM_REG	CB_CTRL_SETTING_REG **shall** be defined in DS_REG and output to CB_CTRL. CB_CTRL_SETTING_REG **shall** include CBFET_EN_REG1-18, CB_GO, CB_MANUAL_REG. CB_GO **shall** be high when written high via COMM_CTRL, and be low when clr_CB_GO.	
TR046	HWR026_COMM_REG	CB_CTRL_SETTING_REG **shall** include CB_TO_THRESH_REG1-18[9:0] (to cover 12h, step 1s-1min) and CB_UNIT_REG[17:0] (0 means second and 1 means minute). Default value of CB_TO_THRESH_REG1-18[9:0] **shall** be 10'h3FF and default CB_UNIT is 1.	
TR047	HWR027_COMM_REG	CB_CTRL_SETTING_REG **shall** include CB_TWARN_THRESH_REG[3:0], covering, 100℃-150℃，step 5℃.	

TR ID	HWR ID	Description	Note
TR047	HWR028_COMM_REG	CB_CTRL_SETTING_REG **shall** include JOT_EN_REG, with default value 1.	
TR062	HWR029_COMM_REG	CB_CTRL_SETTING_REG **shall** include GPIO_CBOT_EN_REG, with default value 1.	
TR048, TR056, TR057, TR062, TR063	HWR030_COMM_REG	CB_OT_PACK_THRESH_REG[4:0] and CB_OT_PCB_THRESH_REG[4:0] shall be defined in DS_REG. GPIO_OTUT_THRESH_SEL_REG[11:0] shall be defined in DS_REG	
TR048, TR056, TR057, TR062, TR063, TR055, TR057, TR060	HWR031_COMM_REG	MON_WAKE_PERIOD_REG[5:0] shall be defined in DS_REG	
TR049	HWR033_COMM_REG	CB_CTRL_SETTING_REG **shall** include CB_MANU_PAUSE, with default value 0.	
TR050	HWR034_COMM_REG	CB_CTRL_SETTING_REG **shall** include ADC_PAUSE_EN_REG, with default value 1.	
TR051	HWR035_COMM_REG	CB_CTRL_SETTING_REG **shall** include FLT_STOP_EN_REG, with default value 1.	
TR018, TR019, TR051	HWR036_COMM_REG	All fault bits shall have corresponding mask bit(except CONF_REG_CRC_FLT) defined in DS_REG.	
TR052	HWR037_COMM_REG	CB_CTRL_SETTING_REG **shall** include CB_PERIOD_REG[2:0].	
TR053	HWR038_COMM_REG	CB_CTRL_SETTING_REG **shall** include CB_DUTY_REG[2:0].	
TR054	HWR039_COMM_REG	CB_ODD_CNT[15:0] and CB_EVEN_CNT[15:0] **shall** be readable via COMM_CTRL.	
TR054	HWR040_COMM_REG	CB_CH_EN_FULL_DUTY[17:0] **shall** be readable via COMM_CTRL.	
TR055, TR057, TR060	HWR041_COMM_REG	CELL_OV_THRESH_REG[6:0], CELL_UV_THRESH_REG[6:0] shall be defined in DS_REG.	
TR022	HWR042_COMM_REG	TRIM_ANA(32 bytes) shall be defined in DS_REG. TRIM_ANA shall only be written when TRIM_EN is high. TRIM_ANA shall be readable regardless of TRIM_EN. In TRIM_ANA: TRIM_L_CLK[x:0] shall be in one byte address. TRIM_H_CLK[x:0] shall be in one byte address. TRIM_BG[x:0] shall be in one byte address. TRIM_IREF[x:0] shall be in one byte address.	x to be detailed.
TR022	HWR043_COMM_REG	MTP_CTRL_BITS(including WR_MTP) shall be defined in DS_REG. MTP_CTRL_BITS in DS_REG shall only be written when TRIM_EN is H.	
TR056, TR063	HWR044_COMM_REG	GPIO_OT_PACK_THRESH_REG[4:0], GPIO_UT_PACK_THRESH_REG[2:0], GPIO_OT_PCB_THRESH_REG[4:0], GPIO_UT_PCB_THRESH_REG[2:0] shall be defined in DS_REG.	
TR068, TR069	HWR045_COMM_REG	GPIO_PUPD[11:0], GPIO_PUPD_EN[11:0], GPIO_AS_IN_EN[11:0] shall be defined in DS_REG to output H/L/HZ to IO.	

TR ID	HWR ID	Description	Note
TR068, TR070	HWR046_COMM_REG	GPIO_HL[11:0] shall be readable via COMM_CTRL.	
TR071	HWR047_COMM_REG	I2C_CTRL, I2C_MAS_EN shall be defined in DS_REG. I2C_CTRL shall include WR_DATA[7:0], WR_GO. RD_DATA[7:0] from i2c_slave shall be readable from COMM_CTRL. ACK_BIT from i2c_slave shall be readable from COMM_CTRL.	
TR072	HWR048_COMM_REG	X-Y and lot information shall be defined in DS_REG as the shadow register of MTP, and shall be read only for customer.	
TR083	HWR049_COMM_REG	SOFT_RSTB_REG shall be defined in DS_REG. SOFT_RSTB_REG shall be default high. When written 0 via COMM_CTRL, SOFT_RSTB_REG shall be low. When clr_SOFT_RSTB, SOFT_RSTB_REG shall be high.	
TR001, TR055, TR056	HWR050_COMM_REG	MON_WAKE_EN_REG shall be defined in DS_REG.	
TR089	HWR051_COMM_REG	SPI_DIR shall be defined in DS_REG, default south.	
TR094, TR095	HWR052_COMM_REG	WAKE_TONE_GEN shall be defined in DS_REG WAKE_TONE_GEN shall be reset when clr_WAKE_TONE_GEN is high	
TR099	HWR053_COMM_REG	STA_TONE_GEN shall be defined in DS_REG STA_TONE_GEN shall be reset when clr_STA_TONE_GEN is high	
TR098	HWR054_COMM_REG	COMN_TX_DIS and COMN_TX_DIS shall be defined in DS_REG, default 0	
TR050	HWR055_COMM_REG	CB_SETTLE[4:0] shall be defined in DS_REG, cover 200us(ensure 200us range is covered, the more the better)	
	HWR056_COMM_REG	OVUV_DEGL_REG[4:0] shall be defined in DS_REG.	
	HWR057_COMM_REG	OVUV_OTUT_EN_REG shall be defined in DS_REG.	
TR083	HWR001_SOFT_RSTB_sync	SOFT_RSTB shall be synchronized in SOFT_RSTB_sync. Output clr_SOFT_RSTB shall be high when synchronized SOFT_RSTB is low, clr_SOFT_RSTB shall be low when synchronized SOFT_RSTB is high.	
TR008, TR009	HWR001_TO_SLP_sync	TO_SLEEP shall be synchronized in TO_SLP_sync. Output clr_TO_SLEEP shall be high when synchronized TO_SLEEP is high, clr_TO_SLEEP shall be low when synchronized TO_SLEEP is low.	
TR013	HWR001_FLT_REG	There shall be SCTO flag bit in FLT_REG, which shall be set by SET_SCTO.	
TR014, TR015	HWR002_FLT_REG	There shall be LCTO flag bit in FLT_REG, which shall be 1.set by SET_LCTO; or 2.set by LCTO_LATCH.	no LCTO_LATCH from input ??
TR015	HWR003_FLT_REG	There shall be register bits(LCTO_SD, VAA_OKB, VDD_OKB, CLK_256K_OKB, VDD_OV, VDD_UV)in FLT_REG to support being only set by XXX_LATCH FLT_REG shall output RST_XXX_LATCH when register bits is written to 1.	XXX in XXX_LATCH is LCTO_SD, VAA_OKB, VDD_OKB, CLK_256K_OKB, VDD_OV, VDD_UV

TR ID	HWR ID	Description	Note
TR030	HWR004_FLT_REG	FLT_TONE_DET_REG shall be recored in FLT_REG. FLT_TONE_DET_REG shall be high when FLT_TONE_DET is high.	
TR058	HWR005_FLT_REG	GPIO_OTUT (including GPIO_OT[11:0], GPIO_UT[11:0]) shall be recored in FLT_REG.	
TR058	HWR006_FLT_REG	CELL_OVUV (including CELL_OV[17:0] and CELL_UV[17:0]) shall be recored in FLT_REG.	
TR015, TR058	HWR009_FLT_REG	All fault bits shall not be set high when corresponding mask bit(from DS_REG) is 1.	
TR079	HWR010_FLT_REG	COW[18:0] shall be defined in FLT_REG.	
TR015, TR079	HWR011_FLT_REG	All fault bits shall not be written to 1 via COMM_CTRL. All fault bits shall be cleared to 0 when written 0 via COMM_CTRL.	
TR042, TR043, TR045	HWR012_FLT_REG	CB_CONF_FLT shall be recored in FLT_REG.	
	HWR013_FLT_REG	There shall be FIFO_OF flag bit in FLT_REG, which shall be set by FIFO_OF	
	HWR014_FLT_REG	There shall be FIFO_UF flag bit in FLT_REG, which shall be set by FIFO_UF	
TR030, TR065	HWR001_FLT_LOGIC	FLT_LOGIC shall combine all fault regs and output FLT_WAKE.	
TR023, TR024	HWR001_LOW_BYTE_BUF	Low bytes of ADC_DATA_LPF, CELL_ADC_DATA, OTH_ADC_DATA, CB_ODD_CNT, CB_EVEN_CNT, RR_COUNTER, AUX_OTH_ADC_DATA, AUX_ADC_DATA_LPF shall be buffered in LOW_BYTE_BUF, and when reading, the buffered bits shall be output to COMM_CTRL.	
TR022	HWR001_TRIM_LOGIC	TRIM shall be AND results of TRIM_ANA and load_done.	
TR010, TR012	HWR001_RSTGEN	RSTGEN shall output hr_b low to asynchrously reset digital core when DRSTB low is detected. Hr_b shall be released synchronously. Hr_b shall include resetb_CLK(CLK_32M domain), resetb_CLK_OUT(mixed: CLK_32M domain when CLK_32M_OK high, CLK_256`K domain when CLK_32M_OK low) and resetb_CLK_SLOW(CLK_SLOW domain).	
TR012	HWR002_RSTGEN	RSTGEN shall output hr_sr_b low to asynchrously reset partial logic of digital core when DRSTB low or SOFT_RSTB is low. Hr_sr_b shall be released synchronously. Hr_sr_b shall include resetb_SR_CLK(CLK_32M domain), resetb_SR_CLK_OUT(mixed: CLK_32M domain when CLK_32M_OK high, CLK_256K domain when CLK_32M_OK low) and resetb_SR_CLK_SLOW(CLK_SLOW domain).	
TR083	HWR003_RSTGEN	When SOFT_RSTB is written to 0 via COMM_CTRL, output of RSTGEN hr_sr_b shall be pulled low, to reset digital core(excepting for identified device address).	

TR ID	HWR ID	Description	Note
TR073	HWR004_RSTGEN	Hr_b and Hr_sr_b shall all be scan-muxed. When SCAN_MODE high, CKGEN shall switch all registers' asynchronous reset to SCAN_RSTB.	
TR023	HWR001_CALIBRATION	CALIBRATION shall calibrate ADC_RESULT into ADC_DATA by TRIM_ADC.	
TR022	HWR002_CALIBRATION	CALIBRATION shall output signed complementary code results, CELL_ADC_DATA and OTH_ADC_DATA.	refer to BM02A _ ADC_ Design _ Summaries. xlsx
TR001	HWR001_ADC_CTRL	Higher clock gating signal D2A_CELL_ADC_EN shall be generated in ADC_CTRL. D2A_CELL_ADC_EN shall be high when ADC measurement starts(ADC_GO high), and shall be low when ADC measurement ends.	
TR001	HWR002_ADC_CTRL	When CLK_32M_OK is low, ADC_CTRL shall be reset to initial state (except CELL_ADC_DATA, OTH_ADC_DATA and ADC_DATA_LPF)	
TR024	HWR003_ADC_CTRL	ADC_CTRL shall only execute one cycle only when ADC_SGLE_GO or MON_ADC_GO is detected. ADC_CTRL shall only execute continously when ADC_CNTI_GO is detected. ADC_CNTI_GO has higher priority to ADC_SGLE_GO(ADC_CTRL only execute ADC_CNTI_GO when both are detected at the same time).	
TR026	HWR004_ADC_CTRL	ADC_CTRL shall only update till new measurement data is available.	
TR023, TR024	HWR005_ADC_CTRL	When FREEZE_DLY high, CELL_ADC_DATA, ADC_DATA_LPF and OTH_ADC_DATA shall all be freezed. When FREEZE_DLY low, CELL_ADC_DATA, ADC_DATA_LPF and OTH_ADC_DATA shall be allowed updating.	
TR023, TR024	HWR001_ADC_LOGIC	ADC_LOGIC shall convert BIT_STREAM to ADC_RESULT. ADC_LOGIC shall output CH_END, ADC_SEQ according to ADC_SETTING.	refer to BM02A _ ADC_ Design _ Summaries. xlsx
TR023, TR024, TR050	HWR001_RECLK_COMP	A delay shall be added between ADC_GO and ADC_GO_DLY. The delay time shall be depended on DEV_NUM. Tdelay = (DEV_NUM+CB_SETTLE+1) * 8.375us A delay shall be added between FREEZE and FREEZE_DLY. The delay time shall be depended on DEV_NUM. Tdelay = DEV_NUM * 8.375us	
	HWR002_RECLK_COMP	RECLK_COMP shall be reset when CLK_32M_OK is 0.	
TR027, TR028	HWR001_CH_SEL_GEN	RR_END shall be defined in CH_SEL_GEN. RR_END generate high pulse(>8us) when round-robin ends.	
TR018, TR028	HWR002_CH_SEL_GEN	CH_COUNTER shall be defined in CH_SEL_GEN. CH_COUNTER shall add by step 1 when CH_END is high. CH_COUNTER shall be cleared to 0 when current round-robin ends.	?? bit width
TR023, TR024, TR029	HWR005_CH_SEL_GEN	Clr_ADC_GO is high when ADC_GO_DLY(including ADC_SGLE_GO_DLY and ADC_CNTI_GO_DLY) or MON_ADC_GO is synchronized by CLK_REG_SC and adc_ctrl module starts to work. High time of clr_ADC_GO shall last 8us at least.	
TR023, TR024	HWR006_CH_SEL_GEN	CH_SEL_GEN shall update ADC_SETTING_REG to ADC_SETTING when ADC_GO_DLY is high.	

TR ID	HWR ID	Description	Note
TR031	HWR001_DLPF	DLPF shall filter CELL_ADC_DATA to ADC_DATA_LFP with stage defined according to DLPF_FC(in ADC_SETTING).	
TR018, TR028	HWR000_RR_CNT	RR_COUNTER[15:0] shall be defined to count round-robin number. RR_COUNTER[15:0] shall add by step 1 when current round-robin ends. RR_COUNTER[15:0] shall clear to 0 when ADC_GO_DLY high.	Follow "BM02A_ ADC_ Sequences. vsd"
TR042, TR043, TR045	HWR001_CB_CTRL	Except for CBFET_EN1-18 and CB_MANU_PAUSE, CB_CTRL_SETTING in CB_CTRL shall update directly with CB_CTRL_SETTING_REG when CB_GO. Specially, CBFET_EN1-18 shall update with CBFET_EN_REG1-18 when CB_GO only if settings are correct. When updating, CBFET_EN1-18 shall support 0, 1 and 2 consecutive channels turning on in CB_CH_EN. CBFET_EN1-18 shall not support >2 consecutive channels turning on in CB_CH_EN, if >2 consecutive channels are enabled in CBFET_EN_REG1-18 when CB_MANUAL_REG high, CBFET_EN1-18 shall not be updated by CB_GO. CB_CTRL shall output CB_CONF_FLT to FLT_REG when CB_GO high when CB_MANUAL is high. CB_CTRL shall output CB_TWARN_THRESH[3:0] to analog part.	
TR001	HWR002_CB_CTRL	Higher clock gating signal CB_EN shall be generated in CB_CTRL. CB_EN shall be high when CB_GO high is detected by CB_CTRL, and shall be low when 1.internal counter reaches each channel's target threshold; or 2.CBFET_EN1-18 are all 0.	
TR044	HWR003_CB_CTRL	CB_CTRL shall outputs CB_CH_EN only when CB_GO is detected.	
TR045	HWR004_CB_CTRL	When CB_MANUAL=0, CB_CH_EN shall support switching between odd/even (logic AND with CBFET_EN1-18) group automatically When CB_MANUAL=1, CB_CH_EN shall support being selected by CBFET_EN1-18	
TR046	HWR005_CB_CTRL	There shall be 2 timers (ODD/EVEN) in CB_CTRL, max 12h The timer shall only count when CB_GO is detected CB_CTRL outputs CB_CH_EN H only if the timer does not touch the CB_TO_THRESH.	
TR047	HWR006_CB_CTRL	CB_CTRL shall outputs CB_CH_EN L if the JOT is high when JOT_EN is high. Timer of balance shall be held if the JOT is H when JOT_EN is high.	
TR062	HWR007_CB_CTRL	CB_CTRL shall outputs CB_CH_EN L if the GPIO_CBOT is H when GPIO_CBOT_EN is high. Timer of balance shall be held if the GPIO_CBOT is H when GPIO_CBOT_EN is high.	
TR049	HWR008_CB_CTRL	CB_CTRL shall outputs CB_CH_EN L if the CB_MANU_PAUSE is H. Timer of balance shall be held if the CB_MANU_PAUSE is H.	
TR050	HWR009_CB_CTRL	CB_CTRL shall outputs CB_CH_EN L only if the D2A_CELL_ADC_EN is H when ADC_PAUSE_EN is high. Timer of balance shall be held if the D2A_CELL_ADC_EN when ADC_PAUSE_EN is high.	
TR051	HWR010_CB_CTRL	CB_CTRL shall outputs CB_CH_EN L if the FLT_WAKE is H when FLT_STOP_EN is high. Timer of balance shall be cleared if the FLT_WAKE is H when FLT_STOP_EN is high.	

TR ID	HWR ID	Description	Note
TR052	HWR011_CB_CTRL	CB_CTRL shall switch the ODD group and the EVEN group among CB_CH_EN every CB_PERIOD. CB_PERIOD shall cover typical 5s-30min, 8steps.	
TR053	HWR012_CB_CTRL	CB_CTRL shall output CB_CH_EN with duty as defined by CB_DUTY every typical 200ms. CB_DUTY shall cover 12.5%-100%, 8steps.	
TR054	HWR013_CB_CTRL	CB_CTRL shall output CB_ODD_CNT[15:0] and CB_EVEN_CNT[15:0].	
TR054	HWR014_CB_CTRL	CB_CTRL shall output CB_CH_EN_FULL_DUTY according to "CB_CH_EN excluding CB_DUTY" to DS_REG.	
TR055, TR056	HWR001_CYC_WAKE	CYC_WAKE shall latch MON_EN_REG, MON_WAKE_PERIOD_REG to MON_EN, MON_WAKE_PERIOD once MON_WAKE_GO is high.	
TR055, TR056	HWR002_CYC_WAKE	CYC_WAKE shall output clr_MON_WAKE_GO high(lasting 1 CLK_SLOW) after reg latch done.	
TR055, TR056	HWR003_CYC_WAKE	CYC_WAKE shall output MON_ADC_GO according to MON_WAKE_PERIOD when D2A_CELL_ADC_EN is high, MON_ADC_GO shall be low MON_ADC_GO shall be cleared by clr_ADC_GO	
TR055, TR056	HWR004_CYC_WAKE	CYC_WAKE shall output MON_WAKE according to MON_WAKE_PERIOD, 200ms-3.2s, step 200ms 3.2s-156.8s, step 3.2s MON_WAKE shall be cleared by RR_END MON_WAKE shall be high earlier xxus than MON_ADC_GO	
	HWR001_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall latch OVUV_OTUT_EN_REG, CELL_OV_THRESH_REG, CELL_UV_THRESH_REG, GPIO_OTUT_THRESH_SEL_REG, GPIO_OT_PACK_THRESH_REG, GPIO_OT_PCB_THRESH_REG, GPIO_UT_PACK_THRESH_REG, GPIO_UT_PCB_THRESH_REG, CB_OT_PACK_THRESH_REG, CB_OT_PCB_THRESH_REG, OVUV_DEGL_REG to OVUV_OTUT_EN, CELL_OV_THRESH, CELL_UV_THRESH, GPIO_OTUT_THRESH_SEL, GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH, OVUV_DEGL once MON_WAKE_GO or ADC_GO_DLY is high.	
	HWR002_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall compare ADC_DATA_LPF with CELL_OV_THRESH and CELL_UV_THRESH when RR_END is high, and output CELL_OVUV according to OVUV_DEGL when OVUV_OTUT_EN is high.	
	HWR003_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall compare OTH_ADC_DATA with GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH according to GPIO_OTUT_THRESH_SEL when RR_END is high, and output GPIO_OTUT, GPIO_CBOT when OVUV_OTUT_EN is high	Not including VBG, VBG2
TR055	HWR004_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall reset when OVUV_OTUT_EN is low.	

TR ID	HWR ID	Description	Note
TR058,TR059	HWR005_OVUV_OTUT_CMP	OVUV_OTUT_CMP shall output CELL_OVUV until counter=OVUV_DEGL The counter shall +1 when fault is detected The max of counter shall be OVUV_DEGL The counter shall -1 when fault is not detected	
TR071	HWR001_I2C_MAS	I2C_MAS shall output SCL and SDA_OUT according to I2C_MAS_EN and I2C_CTRL. I2C_MAS shall support i2c master writing command.	
TR071	HWR002_I2C_MAS	I2C_MAS shall output RD_DATA and ACK_BIT to DS_REG according to SDA_IN	
TR073		All internal power supplies should support output HZ	???
TR073	HWR001_Digital_Core	DFT mode shall be supported in Digital Core to detect stuck-at faults. Scan related signals shall be defined(SCAN_EN, SCAN_CLK, SCAN_RSTB, SCAN_MODE, SCAN_INx are inputs, SCAN_OUTx are outputs, x are integers that >= 1). Maximum value of x(scan chain number) shall be as big as possible.	
TR077	HWR000_TM_KEY_CHECK	TM_KEY_CHECK shall check the TM_KEY using register bits pattern and timing pattern to output TRIM_EN and TMREG_EN TM_KEY_CHECK shall use TMREG_EN to protect TRIM_EN	