Technical Requirement

WP as Prerequisites	Author of TR
AS_v0.0	

ITEM	TR ID	Description

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Operation Mode	TR0_00	The average current consumption of BM06A and its BOM from 12V battery during active mode **shall** <5mA at full temp The average current consumption of BM06A with OVUV & OTUT & CC every 1s and its BOM from battery during sleep mode **shall** <60uA at -40℃-85℃ temp The average current consumption of BM06A and its BOM from battery during shutdown mode **should** <10uA at room temp
Operation Mode	TR0_01	The direct operating mode switching of BM06A **shall** support: shutdown mode<-sleep mode, shutdown mode<->active mode, sleep mode<->active mode
Operation Mode	TR0_02	The time from opearating mode switching signal received to operating mode switching done of BM06A **shall** <3ms at full temp, especially BM06A **shall** support being switched to active mode from sleep mode within 500us with signal pattern received from MCU at full temp
Operation Mode	TR0_03	The active/shutdown mode entrance signal pattern detection of BM06A **shall** reuse SPI communication port
Operation Mode	TR0_04	BM06A **shall** support being switched to sleep mode from active mode by register bit
Operation Mode	TR0_05	The digital core of BM06A **shall** be reset when hard digital reset signal is detected The time from hard digital reset signal received to digital core reset done of BM06A **shall** <500us at full temp
Operation Mode	TR0_06	The hard digital reset signal pattern detection of BM06A **shall** reuse SPI communication port
Operation Mode	TR0_07	BM06A **shall** enter shutdown mode(default) or keep in active mode when a programmable frame communication timer timeout The target operating mode when frame communication timer timeout **shall** support being selected by trim bit The timer **shall** support being programmed from 100ms to 1h (default) with 8 steps, accuracy 5%, by register bit The timer **shall** start to count only during active mode The timer **shall** be reset when a frame is received
Power Supply Capability	TR1_00	The power rail voltage of BM06A for thermal sensors **shall** have accuracy 10% during sleep/active mode at full temp The power rail for thermal sensors **shall** support 0-6 resistor dividers' as load (10k)

ITEM	TR ID	Description
Operation Voltage Range	TR2_00	BM06A **shall** support 5-28V DC input as power input for all functional operation(especially for MOSFETs holding on state)
Measurement	TR3_00	BM06A **shall** support the ADC measurement of 5 channel voltages (consists of 4 battery cell voltages, 1 differential voltage of charging/discharging MOSFETs), 0-6 thermal sensor voltage ratios(consists of battery cells/ PCB/ shunts/charging and discharging MOSFETs), die temperature, BAT voltage, , PACKP voltage, TREF voltage, and charging/discharging current during active and sleep mode The thermal sensor voltage ratios measurement **should** use IO pin The BAT voltage measurement **should** reuse BAT pin The PACKP voltage measurement **should** reuse PACKP pin The TREF voltage measurement **should** reuse TREF pin
Measurement	TR3_01	ADC accuracy for voltage measurement of BM06A **shall** meet the spec under default measurement time (**should** <250us) as below: cell voltage measurement (filter RC=1kohm+4.7nF): □ ±3mV accuracy (1.5V to 4.5V, -40℃ to +125℃) BAT pin voltage measurement(Xohm+XnF): □ ±12mV accuracy (6V to 18V,-40℃ to +125℃) PACKP voltage measurement(Xohm+XnF): □ ±30mV accuracy (0.5V to 40V,-40℃ to +125℃) TREF voltage measurement: □ ±3mV accuracy (1V to 2.5V,-40℃ to +125℃)
Measurement	TR3_02	ADC accuracy for temperature measurement of BM06A **shall** meet the spec under default measurement time (**should** <250us) as below: thermal sensor voltage measurement □ ±3mV accuracy(-20℃ to +65℃) □ ±5mV accuracy(-40℃ to +125℃) die temperature measurement: □ ±5℃ accuracy (-40℃ to +125℃)
Measurement	TR3_03	ADC accuracy for current measurement of BM06A **shall** meet the spec under default measurement time (**should** = 4 cell slots) as below(Xohm+XnF): □ ±0.5% accuracy(1A - 750A, -40℃ to +125℃) □ ±5mA accuracy(5mA - 1A, -40℃ to +125℃) The current shunt **should** be 200uΩ
Measurement	TR3_04	The total time of one round robin' ADC measurement time(including all the voltage, temperature, current measurement) and data readout time **shall** <10ms at full temp (include back-and-forth communication time)

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Measurement	TR3_05	The synchronous time of voltage and current measure **shall** <1ms and **should** be 500us during active mode and sleep mode
Measurement	TR3_06	The measurement accuracy of battery cell voltage **shall** be kept when -2V<VBAT-VC4
Measurement	TR3_07	The address of all ADC measurement data of BM06A **shall** be continuous and **shall** support being read out by one command from MCU
Measurement	TR3_08	The measurement of both cell voltage and temperature **shall** pass 200mA BCI test (error<10mV)
OC Protection	TR4_00	BM06A **shall** support charging and discharging over current(OCC/OCD) protection during active and sleep mode
OC Protection	TR4_01	The OCC and OCD protection threshold **shall** support being programmed separately from 60A to 960A, accuracy 5%, by register bit
OC Protection	TR4_02	The deglitch time of OCC and OCD protection for BM06 from charging or discharging current over OC protection threshold to OC protection action implementation **shall** support being programmed by register bit(typ=20us, accuracy 10%)
OC Protection	TR4_03	The charging and discharging MOSFETs **shall** support being turned off together within 50us(tpy), 100us(max)by BM06 when OCC protection action or OCD protection action implementation during active and sleep mode(STH410N4F7_Ron=1mΩ , 2 series 3 parallel, Qg=141nC)
OC Protection	TR4_04	The OCC and OCD protection functions **shall** support being disabled by register bit
OC Protection	TR4_05	The detected OCC/OCD fault **shall** be recorded in register bit The fault flag register bit **shall** support being written to clear The fault flag **shall** support being masked from being set by register bit
Cell Balance	TR5_00	Passive cell balance for each battery cell of BM06A **shall** be available when MCU requests during both active and sleep mode
Cell Balance	TR5_01	BM06A **shall** support at most 2 battery cell channels' balance at the same time when MCU requests and **shall** forbid adjcent cell channels' balance at the same time.

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Cell Balance	TR5_02	Only enabled channel can be balanced, BM06A **should** support both automatic channel selection and manual channel selection by register bit For automatic mode, the enabled channels **should** be default odd or even channels group, during manual mode, each channel **should** support being selected by register bit
Cell Balance	TR5_03	The odd group and even group of battery cell channels **shall** be switched alternately during automatic mode The switching period **should** be programmable by register bit, range 5s-30min, accuracy 5% at full temp
Cell Balance	TR5_04	BM06A **shall** provide programmable cell balance time threshold by register bit for each battery cell channel, the biggest threshold **shall** support 9h, accuracy 5% at full temp The default value of time threshold for each battery cell channel **shall** be 0 When timer touches any programed time threshold, the balance of this channel **shall** be stopped (timer **shall** go on to count and the balance current **shall** be off)
Cell Balance	TR5_05	Cell balance of BM06A **shall** start (timer **shall** start to count and the balance current **shall** be on) by register bit
Cell Balance	TR5_06	Cell balance of BM06A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) manually by register bit When this register bit is toggled, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR5_07	Cell balance of BM06A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when channel voltage ADC measurement is ongoing and **shall** delay settle time for accurate voltage measurement When channel voltage ADC measurement is not ongoing, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR5_08	Cell balance of BM06A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when junction temperature is over programmable CB_JOT threshold by register bit, 80℃-130℃, 5℃ step, accuracy 5℃ When junction temperature is under the hys 10℃, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)

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Cell Balance	TR5_09	Cell balance of BM06A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when battery pack temperature is over programmable CB_ROT_PACK threshold by register bit, 80℃-130℃, 5℃ step, accuracy 5℃ When junction temperature is under the hys 10℃, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR5_10	Cell balance of BM06A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when PCB temperature is over programmable CB_ROT_PCB threshold by register bit, 80℃-130℃, 5℃ step, accuracy 5℃ When junction temperature is under the hys 10℃, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR5_11	Cell balance of BM06A **shall** support being stopped (timer **shall** clear and the balance current **shall** be off) when any unmasked fault flag is set in register
Cell Balance	TR5_12	During sleep mode, when measured cell voltage touches the programed CB_UV threshold, the balance of this channel **shall** be stopped (timer **shall** clear and the balance current **shall** be off) Battery cell channel CB_UV detection threshold **shall** be programmable by register bit, cover 1.5V-3V, 100mV step
Cell Balance	TR5_13	BM06A **shall** provide balance done (timer touches the time threshold or cell voltage touches the CB_UV threshold) status for each channel by register bit
Cell Balance	TR5_13	Maximum passive cell balance current of BM06A **should** >200mA for each battery cell channel when no adjacent cells balancing, RB=10Ω, Vcell=4.5V, Ta=85℃ Delta Tc between BM06A and ambient temperature **shall** <20℃ at Ta=85℃ when 2 channels balance work with 200mA balance current.
Cell Balance	TR5_14	The mismatch of balance current for each separately enabled channel **shall** <10mA at 4.5V under same temp
Communication	TR6_00	The communication of BM06A **shall** support 2-6MHz half duplex SPI communication during active mode(high level follow VIO=3.3V/5V) (type00 refer to BM04)
Communication	TR6_01	The specified single BM06A device **shall** support being read at least 128 data bytes registers with continuous addresses by one command received from MCU

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Communication	TR6_02	The specified single BM06A device **shall** support being written at least 16 data bytes writable registers with continuous addresses by one command received from MCU
Reversely Wake Up	TR7_00	The OVUV for each battery cell channel **shall** be detected by BM06A periodically during sleep mode The period of OVUV detection **shall** support being programmable by register bit, from 100ms to 2min, 100ms-8s step,accuracy 5% at full temp
Reversely Wake Up	TR7_01	The OTUT for each thermal sensor channel **shall** be detected by BM06A periodically during sleep mode The period of OTUT detection **shall** support being programmable by register bit, from 100ms to 2min, 100ms-8s step,accuracy 5% at full temp
Reversely Wake Up	TR7_02	The OVUV detection period and OTUT detection period **should** share same programmable register bits during sleep mode.
Reversely Wake Up	TR7_03	The battery coulomb counter over threshold fault **shall** be detected by BM06A periodically during sleep mode The period of coulomb counter **shall** support being programmable by register bit, from 100ms to 2s, 100ms step, accuracy 2% at full temp
Reversely Wake Up	TR7_04	The battery coulomb counter number overflow fault **shall** be detected by BM06A periodically during sleep mode The period of coulomb counter **shall** support being programmable by register bit, from 100ms to 2s, 100ms step, accuracy 2% at full temp
Reversely Wake Up	TR7_05	The battery discharging current abnormal change fault(small current change to large one suddenly) **shall** be detected by BM06A periodically during sleep mode The period of current detection **shall** support being programmable by register bit, from 100ms to 2s, 100ms step, accuracy 2% at full temp
Reversely Wake Up	TR7_06	The detection period of coulomb counter over threshold fault, coulomb counter number overflow fault and discharging current abnormal fault **should** share same programmable register bits during sleep mode.
Reversely Wake Up	TR7_07	The coulomb counter value/number detection and discharging current abnormal detection **shall** support asynchronous detection with OVUV/OTUT detection.

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Reversely Wake Up	TR7_08	The detected OVUV&OTUT&discharging current abnormal faults **shall** be recorded in register bit during sleep mode The fault flag register bit **shall** support being written to clear The fault flag **shall** support being masked from being set by register bit
Reversely Wake Up	TR7_09	Battery cell channel OVUV detection of BM06A **shall** meet 5mV accuracy at full temp Battery cell channel OVUV detection threshold **shall** be programmable by register bit, cover OV:2V-5V, 5mV step; UV: 0.7V-3.875V, 5mV step
Reversely Wake Up	TR7_10	Thermal sensor OTUT detection of BM06A **shall** meet 1% accuracy at full temp Thermal sensor OTUT detection threshold **shall** be programmable by register bit, cover OT:5%-36%, 1% step; UT:76%-90%, 2% step
Reversely Wake Up	TR7_11	BM06A **shall** have four groups of programmable OTUT thresholds and different thermal sensing channel **shall** support selecting different threshold by register bit
Reversely Wake Up	TR7_12	Discharging current abnormal detection of BM06A **shall** meet 0.5% accuracy at full temp Abnormal current threshold **shall** be programmable by register bit, cover 1A-60A
Reversely Wake Up	TR7_13	Any OVUV/OTUT/CC over threshold/CC number overflow/discharging current abnormal change/OCC/OCD fault flag set in registers **shall** actively send out wake high signal to SBC within 1ms during sleep mode at full temp
Pre-Driver	TR8-00	The charging/discharging MOSFETs driver voltage **shall**>10V during 5V-28V DC input range and 0-40V PACKP voltage range
Pre-Driver	TR8_01	The charging/discharging MOSFETs **shall** supprt on control separately by MCU during active mode The on time of the charging/discharging MOSFET **shall**<100us(typ), 200us(max) from off state at full temp
Pre-Driver	TR8_02	The charging/discharging MOSFET **shall** supprt off control separately by MCU during active mode The off time of the discharging MOSFET **shall**<50us(typ), 100us(max) from on state at full temp The off time of the charging MOSFET **shall**<50us(typ), 100us(max) from on state at full temp
Pre-Driver	TR8_03	The delay time **shall** within 10us from CMD received from MCU to charging/discharging MOSFETs on/off action implementation

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Pre-Driver	TR8_04	The charging/discharging MOSFETs **shall** support keeping on state during sleep and active mode The charging/discharging MOSFETs **shall** keep default off state after waking up from shutdown mode The charging/discharging MOSFETs **shall** keep on state when digital reset
Pre-Driver	TR8_05	The driver pin **should** support connecting external driver(such as AUIR3242).
CC Protection	TR11_00	The coulomb counter value and number of battery **shall** be detected by BM06A during active and sleep mode Battery coulomb counter value detection of BM06A **shall** meet 0.5%(1A-750A) accuracy at full temp
CC Protection	TR11_01	The coulomb couter value and number **shall** support being recorded by register bit during active and sleep mode The coulomb couter value **shall** be programmable by 32-bit register, cover the full scale range, 1 LSB step The coulomb couter number **shall** be recorded by 16-bit register, cover the full scale range, 1 LSB step
CC Protection	TR11_02	Coulomb counter threshold **shall** be programmable by 32 bits register, cover the full scale range, 1 LSB step
CC Protection	TR11_03	The detected CC value over threshold fault, CC number overflow fault **shall** be recorded in register bit during active and sleep mode The fault flag register bit **shall** support being written to clear during active mode The fault flag **shall** support being masked from being set by register bit during active and sleep mode
CC Protection	TR11_04	The coulomb couter value and number **shall** support be reset by MCU or read operation during active mode The coulomb couter value and number **shall** support be reset by BM06 itself if coulomb couter value or number overflow fault happen during active and sleep mode.
Others	TR12_00	The die X-Y location on wafer and lot information during production for each BM06A chip **shall** be stored in NVM for customer read ONLY The version ID **should** be read ONLY for customer
Others	TR12_01	BM06A **shall** pass AEC-Q100 Grade1 qualification
Others	TR12_02	BM06A **shall** pass ESD HBM: 2kV ESD CDM: 750V for corner pins, 500V for other pins Latch-up: ±200mA
Others	TR12_03	BM06A **shall** survive during 20V(5Vx4) battery pack random hot-plug. especially for current sense pin.

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Others	TR12_04	Current sense pin **should** improve the robustness under the premise of ensuring the accuracy.(ESD HBM: 4kV, ,absolute voltage: -4V-4V)???
Others	TR12_05	Cell balance of BM06A **shall** support working when channel voltage ADC measurement is ongoing (cell balance diagnose requirement)