WP as Prerequisites	Author of TSR
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Technical Safety Requirement

Objective

The objectives of this document are:

- to specify the technical safety requirements. They are derived from the assumed functional safety requirements and the assumed system architectural design;
- to refine the hardware-software interface (HSI) specification initiated in system level;
- to verify that the technical safety requirements and the hardware-software interface (HSI) specification are consistent with the assumed functional safety requirements and the assumed system architectural design.

Safety Mechanism Summery

SM ID	SM Name	Detection interval	Note
SM001	MAIN/AUX measurement path crosscheck	SPFDTI	
SM002	Redundant OVUV&OTUT detection	SPFDTI	
SM003	TWARN detection	SPFDTI	
SM004	CP OV/UV detection	SPFDTI	
SM005	VAA OV/UV detection	SPFDTI	
SM006	VDD OV/UV detection and digital reset	SPFDTI	
SM007	VBG vs REFP and VBG2 vs TREF host check	SPFDTI	
SM008	Regular measurement counter host check	SPFDTI	
SM009	Regular frame counter host check	SPFDTI	
SM010	Response CRC host check	SPFDTI	
SM011	Command CRC detection	SPFDTI	
SM012	Configuration register CRC detection	SPFDTI	
SM013	NVM CRC detection	SPFDTI	
SM014	AGND open detection	SPFDTI	
SM016	Cn path open host check	SPFDTI	
SM017	Multi GPIOn paths host crosscheck	SPFDTI	
SM018	Adjacent BC short host check	SPFDTI	
SM019	Adjacent GPIO short host check	SPFDTI	
SM021	FIT of GAP comparison	MPFDTI	
SM022	BIST of analog comparison path	MPFDTI	
SM024	Register CRC host diagnosis	MPFDTI	
SM025	Redundant fault flag	MPFDTI	
SM026	Command CRC host diagnosis	MPFDTI	
SM028	HB tone injection and detection	SPFDTI	
SM029	Device address host check	SPFDTI	
SM030	Frame byte period detection	SPFDTI	
SM031	FIT of frame byte period detection	MPFDTI	

Safe State Description

Fault Reaction ID	Safe Sate / Degradation for BMS	Safe Sate / Degradation for BM02A	Description
SS1	Battery pack relays are open or other actions are taken.	Fault flag set in communication frame is provided to host.	Fault flag set in communication frame shall be detected by host. Then host is responsible for determining if the battery pack relays shall be open or other actions shall be taken.
SS2	Battery pack relays are open or other actions are taken.	Information (including communication loss) for fault detection/diagnosis is provided to host.	The information (including communication loss) for fault detection/diagnosis shall be provided to host. Then host is responsible for determining if fault exists and if the battery pack relays shall be open or other actions shall be taken.
SS3	Battery pack relays are open or other actions are taken.	FLT tone is generated to transceiver.	FLT tone shall be generated to transceiver, then transceiver shall assert fault pin and enable SBC to power up host. Then host is responsible for determining if fault exists after being powered up and if the battery pack relays shall be open or other actions shall be taken.

Technical Safety Requirement

TSR001

TSR ID	TSR001
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	The MAIN_ADC measurement data (including cell voltage after DLPF and thermal sensor temperature) for host **shall** be crosschecked by AUX_ADC measurement path The AUX_ADC **shall** use separate cell voltage measurement pins from MAIN_ADC The measurement slots of MAIN_ADC and AUX_ADC for same channel **shall** be synchronous. The measurement gap of MAIN_ADC and AUX_ADC at full temp **should** <15mV for cell voltage after DLPF , <1% for thermal sensor temperature The fault threshold for measurement gap of cell voltage after DLPF **should** be programmable from 20mV to 180mV, 5mV step The fault threshold for measurement gap of thermal sensor temperature **should** be programmable from 1% to 8%, 1% step The measurement gap **shall** be compared with fault threshold per measurement round-robin The fault flag for measurement gap of cell voltage after DLPF **should** be filtered by programmable counter from 1 to 32 RR_COUNTER **shall** be frozen when FREEZE is detected
Related SM	SM001: MAIN/AUX measurement path crosscheck
Figures / Diagram	/
Allocated to HW	There shall be a redundant AUX_ADC to automatically compare the gap between MAIN_ADC and AUX_ADC according to programmed fault threshold and filter, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the measurement accuracy of MAIN_ADC is fine
Failure Mode Detected	Battery cell voltage measurement and temperature sensor’s voltage ratio measurement accuracy fails of MAIN_ADC
Corresponding to	ISO 26262-5:2018, Table D.4, “HW redundancy”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR002

TSR ID	TSR002
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	The MAIN_ADC measurement data (including cell voltage after DLPF and thermal sensor temperature) for host **shall** be compared from OVUV&OTUT (besides host's OVUV&OTUT comparison) OVUV threshold **shall** be programmable, OV:2V-5V, 25mV step and UV: 0.7V-3.875V, 25mV step OTUT threshold **shall** be programmable, OT:5%-36%, 1% step and UT:76%-90%, 2% step There **shall** be two groups of OTUT thresholds for each thermal sensor channel, which **shall** support being selected The OVUV&OTUT detection **shall** be executed per measurement round-robin The fault flag for OVUV&OTUT detection **should** be filtered by programmable counter from 1 to 32
Related SM	SM002: Redundant OVUV&OTUT detection
Figures / Diagram	/
Allocated to HW	There shall be OVUV&OTUT detection to automatically compare the MAIN_ADC measurement data per programmed fault threshold and filter, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the measurement accuracy of MAIN_ADC is fine
Failure Mode Detected	MAIN_ADC measurement data (including cell voltage after DLPF and thermal sensor temperature) addressing fails when read by host
Corresponding to	ISO 26262-5:2018, Table D.4, “HW redundancy”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR003

TSR ID	TSR003
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	The junction temperature **shall** be monitored from TWARN threshold
Related SM	SM003: TWARN detection
Figures / Diagram	/
Allocated to HW	There shall be TWARN detection to compare the junction temperature with TWARN threshold, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the junction temperature is fine
Failure Mode Detected	Over-temperature fault of junction
Corresponding to	ISO 26262-11:2018, Table 39, “Thermal monitor”
DC of SM	99.9%
Fault Reaction	Once fault flag detected, go to SS1

TSR004

TSR ID	TSR004
Traced to FSR ID	FSR_01
Highest ASIL	D
Description of TSR	The charge pump output CP **shall** be monitored from OVUV
Related SM	SM004: CP OV/UV detection
Figures / Diagram	/
Allocated to HW	There shall be OVUV detection to compare the CP with VCP_OV and VCP_UV, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the charge pump output CP is fine
Failure Mode Detected	Over voltage of CP. Under voltage of CP.
Corresponding to	ISO 26262-11:2018, Table 37, “Over and under voltage monitoring”
DC of SM	99.9%
Fault Reaction	Once fault flag detected, go to SS1

TSR005

TSR ID	TSR005
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	The analog power VAA **shall** be monitored from OVUV
Related SM	SM005: VAA OV/UV detection
Figures / Diagram	/
Allocated to HW	There shall be OVUV detection to compare the VAA with VVAA_OV and VVAA_UV, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the VAA is fine
Failure Mode Detected	Over voltage of VAA. Under voltage of VAA
Corresponding to	ISO 26262-11:2018, Table 37, “Over and under voltage monitoring”
DC of SM	99.9%
Fault Reaction	Once fault flag detected, go to SS1

TSR006

TSR ID	TSR006
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	The digital power VDD **shall** be monitored from OVUV Once OVUV is detected, the digital core **shall** be reset
Related SM	SM006: VDD OV/UV detection and digital reset
Figures / Diagram	/
Allocated to HW	There shall be OVUV detection to compare the VDD with VVDD_OV and VVDD_UV, and compare the DGND with VDGND_OW, once detected, the digital core shall be reset
Allocated to SW	Host shall read and compare the frame counter with the expected value per SPFDTI to verify the daisy-chain UART communication is fine
Failure Mode Detected	Over voltage of VDD. Under voltage of VDD
Corresponding to	ISO 26262-11:2018, Table 37, “Over and under voltage monitoring”
DC of SM	99.9%
Fault Reaction	Once fault flag detected, go to SS2

TSR007

TSR ID	TSR007
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	REFP and TREF **shall** be monitored from accuracy and oscillation fault by ADC measurement of precise reference The measurement accuracy at full temp **should** <15mV for REFP and TREF
Related SM	SM007: VBG vs REFP and VBG2 vs TREF host check
Figures / Diagram	/
Allocated to HW	VBG&VBG2 shall support being measured by MAIN_ADC with REFP&TREF as the measurement reference respectively
Allocated to SW	Host shall measure VBG&VBG2 and compare VBG&VBG2 with the expected value per SPFDTI to verify the REFP and TREF are fine
Failure Mode Detected	Accuracy and oscillation fault of REFP. Accuracy and oscillation fault of TREF.
Corresponding to	ISO 26262-11:2018, Table 39, “ADC monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR008

TSR ID	TSR008
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	MAIN_ADC measurement **shall** be monitored from timing fault by a measurement counter
Related SM	SM008: Regular measurement counter host check
Figures / Diagram	/
Allocated to HW	There shall be a measurement counter(ADC_DONE/RR_COUNTER) using ADC measurement clock, the counter shall increase by 1 after each measurement round-robin.
Allocated to SW	Host shall read and compare the measurement counter with the expected value per SPFDTI to verify the ADC measurement clock is fine

TSR ID	TSR008
Failure Mode Detected	Timing fault of ADC_EN
Corresponding to	ISO 26262-5:2018, Table D2, “Failure detection by online monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR009

TSR ID	TSR009
Traced to FSR ID	FSR_03
Highest ASIL	D
Description of TSR	Daisy-chain UART communication **shall** be monitored by frame counter Frame counter shall not increase when frame is interrupted by new frame
Related SM	SM009: Regular frame counter host check

TSR ID	TSR009
Figures / Diagram	/
Allocated to HW	There shall be a frame counter to count all the received command and response frames, the counter shall increase by 1 after each command and response frame is received (without CRC fault).
Allocated to SW	Host shall read and compare the frame counter with the expected value per SPFDTI to verify the daisy-chain UART communication is fine
Failure Mode Detected	Repetition/Insertion/Loss/Delay of communication frame.
Corresponding to	ISO 26262-5:2018, Table D.6, “Combination of information redundancy, frame counter and timeout monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR010

TSR ID	TSR010
Traced to FSR ID	FSR_03
Highest ASIL	D
Description of TSR	Daisy-chain UART communication response frame **shall** be monitored by frame CRC Frame CRC **should** be 16-bit
Related SM	SM010: Response CRC host check
Figures / Diagram	/
Allocated to HW	There shall be a frame CRC encoder to generate CRC to each response frame.
Allocated to SW	Host shall calculate and compare the CRC with expected value per SPFDTI to verify the received response frame is fine
Failure Mode Detected	Corruption of communication response frame.
Corresponding to	ISO 26262-5:2018, Table D.6, “Combination of information redundancy, frame counter and timeout monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR011

TSR ID	TSR011
Traced to FSR ID	FSR_03
Highest ASIL	D
Description of TSR	Daisy-chain UART communication command frame **shall** be monitored by frame CRC Frame CRC **should** be 16-bit
Related SM	SM011: Command CRC detection
Figures / Diagram	/
Allocated to HW	There shall be a frame CRC decoder to detect the received command frame per SPDTTI, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the received command frame is fine
Failure Mode Detected	Corruption of communication command frame.
Corresponding to	ISO 26262-5:2018, Table D.6, “Combination of information redundancy, frame counter and timeout monitoring”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR012

TSR ID	TSR012
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	Configuration registers **shall** be monitored by background CRC Background register CRC **should** be 16-bit
Related SM	SM012: Configuration register CRC detection
Figures / Diagram	/
Allocated to HW	There shall be background CRC to monitor both configuration registers and NVM shadow registers continuously, the CRC should be executed per 2ms, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall update corresponding CRC according to expected configuration registers and read NVM shadow registers Host shall detect the fault flag using stack read frame per SPFDTI to verify the configuration registers are fine
Failure Mode Detected	SA1/0 fault of configuration registers Failure of CRC for NVM shadow registers
Corresponding to	ISO 26262-11:2018, Table 33, “Running checksum/CRC”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR013

TSR ID	TSR013
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	Shadow registers of NVM **shall** be monitored by background CRC Background register CRC **should** be 16-bit
Related SM	SM013: NVM CRC detection
Figures / Diagram	/
Allocated to HW	There shall be background CRC to monitor shadow registers of NVM continuously, the CRC should be executed per 2ms, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the shadow registers of NVM are fine
Failure Mode Detected	SA1/0 fault of shadow registers of NVM
Corresponding to	ISO 26262-11:2018, Table 33, “Running checksum/CRC”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR014

TSR ID	TSR014
Traced to FSR ID	FSR_01
Highest ASIL	D
Description of TSR	The AGND path **shall** be monitored from open.
Related SM	SM014: AGND open detection
Figures / Diagram	/
Allocated to HW	There shall be AGND open detection to compare the AGND and B0&B1 with VAGND_OW, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the AGND is fine
Failure Mode Detected	Open from HV battery pack of AGND.
Corresponding to	ISO 26262-5:2018, Table D.2, “Comparator”
DC of SM	99.9%
Fault Reaction	Once fault flag detected, go to SS1

TSR016

TSR ID	TSR016
Traced to FSR ID	FSR_01
Highest ASIL	D
Description of TSR	The Cn path open fault **shall** support being detected by current sink/source at Cn Current sink/source **should** be 500uA Each current sink/source **should** support being enabled separately
Related SM	SM016: Cn path open host check
Figures / Diagram	/
Allocated to HW	There shall be automatic Cn path open detection using current sinks and source at each Cn pin and MAIN_ADC, the open detection shall support being executed by register bit, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall enable the Cn path open detection and detect the fault flag using stack read frame per SPFDTI to verify the path of Cn is not open
Failure Mode Detected	Open from HV battery pack of Cn path.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	99%
Fault Reaction	Once fault flag detected, go to SS1

TSR017

TSR ID	TSR017
Traced to FSR ID	FSR_02
Highest ASIL	D
Description of TSR	The multi GPIOn paths **shall** be monitored by host's expectation about pack's temperature distribution.
Related SM	SM017: Multi GPIOn paths host crosscheck
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall execute all thermal sensors' measurement, read and compare the pack's temperature distribution with the expected value per SPFDTI to verify path of Cn is not open
Failure Mode Detected	Open from HV battery pack of GPIOn path.
Corresponding to	ISO 26262-5:2018, Table D.2, “Comparator”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR018

TSR ID	TSR018
Traced to FSR ID	FSR_01
Highest ASIL	D
Description of TSR	The short circuit between adjacent Cn pin and Bn pin **shall** support being detected by intended enabled CBFET.
Related SM	SM018: Adjacent BC short host check
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall compare the gap of the measured channel voltages by MAIN_ADC and the gap of the measured channel voltages by AUX_ADC, before and after the CBFET is enabled with the expected value per SPFDTI to verify the Cn pin is not short to adjacent Bn pin
Failure Mode Detected	Short circuit between adjacent Cn pin and Bn pin.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR019

TSR ID	TSR019
Traced to FSR ID	FSR_02
Highest ASIL	D
Description of TSR	The short circuit between GPIOn pin and GPIOn-1 pin **shall** support being detected by pull-up/down at GPIO.
Related SM	SM019: Adjacent GPIO short host check
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall compare the gap of the measured thermal sensors temperature by MAIN_ADC before and after the adjacent GPIO's pull-up/down with the expected value per SPFDTI to verify the GPIOn pin is not short to adjacent GPIOn-1 pin
Failure Mode Detected	Short circuit between GPIOn pin and GPIOn-1 pin.
Corresponding to	ISO 26262-5:2018, Table D.10, "Test pattern"
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR021

TSR ID	TSR021
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	The stuck at fault of measurement gap comparison **shall** support being diagnosed by current sink/source injection at Cn and weak pull-up/down injection at GPIOn. Weak pull-up/down injection at GPIOn **should** consist of 10K_20UA_PUPD
Related SM	SM021: FIT of GAP comparison
Figures / Diagram	/
Allocated to HW	There shall be current sink/source (can be enabled separately) at battery cell path into MAIN_ADC There shall be resistor and weak pull-up/down after this resistor at thermal sensor path into AUX_ADC
Allocated to SW	Host shall turn on current sink/source injection at Cn and weak pull-up/down injection at GPIOn, execute all channel voltages and thermal sensors' measurement, and detect the fault flag using stack read frame per MPFDTI to verify the measurement gap comparison is fine
Failure Mode Detected	Battery pack channel voltage absolute value measurement and temperature sensor’s voltage ratio measurement accuracy fails for AUX_ADC. The stuck at fault of GAP_CMP. The accuracy fault and stuck at fault of CS. The stuck at fault of weak PUPD.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR022

TSR ID	TSR022
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	The stuck at fault of analog comparison **shall** support being diagnosed by BIST. The BIST **shall** cover analog comparators The BIST **shall** toggle the analog comparators by both rising and falling input The BIST **should** inject fault by wrong comparison reference
Related SM	SM022: BIST of analog comparison path
Figures / Diagram	/
Allocated to HW	There shall be BIST to inject fault signal into comparators to check if fault signals are set as expected, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall mask corresponding fault flags then execute BIST, and detect the fault flag using stack read frame per MPFDTI to verify the analog comparison path is fine.
Failure Mode Detected	SA0 and SA1 fault of comparators.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	90%
Fault Reaction	Once fault detected, go to SS2

TSR024

TSR ID	TSR024
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	Stuck at fault of configuration register CRC **shall** support being diagnosed by intended wrong CRC injection
Related SM	SM024: Register CRC host diagnosis
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall send wrong CRC and check if the fault flag is set in communication frame per MPFDTI to verify configuration register CRC is fine
Failure Mode Detected	SA0/1 fault of configuration register CRC.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	90%
Fault Reaction	Once fault detected, go to SS2

TSR025

TSR ID	TSR025
Traced to FSR ID	FSR_01, FSR_02, FSR_03
Highest ASIL	D
Description of TSR	Each fault flag **shall** have redundant storage in register considering fault flag in communication frame
Related SM	SM025: Redundant fault flag
Figures / Diagram	/
Allocated to HW	There shall be a redundant fault flag storage for each fault flag, the logic OR of them shall be used to set fault flag in communication frame.
Allocated to SW	Host shall check if the fault flag are set in both initial and redundant storage in register when any fault flag is detected per MPFDTI to verify fault flag storage is fine
Failure Mode Detected	SA0/1 of fault flags.
Corresponding to	ISO 26262-5:2018, Table D.4, “HW redundancy”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR026

TSR ID	TSR026
Traced to FSR ID	FSR_03
Highest ASIL	D
Description of TSR	Stuck at fault of frame CRC decoder **shall** support being diagnosed by frame with intended wrong CRC injection
Related SM	SM026: Command CRC host diagnosis
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall send frame with wrong CRC and check if the fault flag is set in communication frame per MPFDTI to verify frame CRC decoder is fine
Failure Mode Detected	SA0/1 fault of frame CRC decoder.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	90%
Fault Reaction	Once fault detected, go to SS2

TSR028

TSR ID	TSR028
Traced to FSR ID	FSR_06
Highest ASIL	A
Description of TSR	Daisy chain communication integrity **shall** be monitored by heartbeat tone injection and detection during sleep mode
Related SM	SM028: HB tone injection and detection
Figures / Diagram	/
Allocated to HW	There shall be periodical heartbeat tone generation and timing detection during sleep mode
Allocated to SW	Once powered up, host shall check if fault pin of transceiver is asserted
Failure Mode Detected	Daisy chain communication integrity fault
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	90%
Fault Reaction	Once fault detected, go to SS3

TSR029

TSR ID	TSR029
Traced to FSR ID	FSR_03
Highest ASIL	D
Description of TSR	The addressing of daisy-chained devices for Daisy-chain UART communication **shall** be checked by host
Related SM	SM029: Device address host check
Figures / Diagram	/
Allocated to HW	/
Allocated to SW	Host shall send stack read command and compare the device addresses in received responses with the expected value per SPFDTI to verify the addressing of daisy-chain UART communication is fine
Failure Mode	Repetition/Insertion/Loss/Delay of communication frame.

Detected	
TSR ID	**TSR029**
Corresponding to	ISO 26262-5:2018, Table D.6, “Combination of information redundancy, frame counter and timeout monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS2

TSR030

TSR ID	**TSR030**
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	The clock accuracy **shall** be monitored by a communication frame byte period counter in adjacent device
Related SM	SM030: Frame byte period detection
Figures / Diagram	/
Allocated to HW	There shall be a communication frame byte period counter using high frequency clock The counter shall re-count byte by byte. The counter shall compare the byte period with 112.5% expected value and 87.5% expected value, once detected, the fault flag shall be recorded in register and the fault flag shall be set in communication frame
Allocated to SW	Host shall detect the fault flag using stack read frame per SPFDTI to verify the clock accuracy is fine
Failure Mode Detected	Accuracy fault of clock
Corresponding to	ISO 26262-5:2018, Table D2, “Failure detection by online monitoring”
DC of SM	99%
Fault Reaction	Once fault detected, go to SS1

TSR031

TSR ID	TSR031
Traced to FSR ID	FSR_01, FSR_02
Highest ASIL	D
Description of TSR	The stuck at fault of frame byte period detection **shall** support being diagnosed by intended wrong byte period injection. The intended wrong byte period **shall** cover 112.5% expected value and 87.5% expected value
Related SM	SM031: FIT of frame byte period detection
Figures / Diagram	/
Allocated to HW	There shall be STACK_RESP_CMD register to program the expected byte period to cover 112.5% expected value and 87.5% expected value
Allocated to SW	Host shall program the STACK_RESP_CMD register to over 112.5% expected value and lower 87.5% expected value, and detect the fault flag using stack read frame per MPFDTI to verify the frame byte period detection is fine
Failure Mode Detected	The stuck at fault of frame byte period detection.
Corresponding to	ISO 26262-5:2018, Table D.10, “Test pattern”
DC of SM	90%
Fault Reaction	Once fault detected, go to SS2