CB_CTRL

REVISION HISTORY

Revision Number	Date	Description of Change	Author
V0.0	9/23/2022	Draft version	Shaoqiang
V0.1	10/11/2022	Change to Design Spec	Shaoqiang

Table of Content

CB_CTRL

Introduction

Balancing the cells maximizes the capacity of the battery pack and ensures that all energy is available, increasing the life of the battery. CB_CTRL (Cell Balance Control) module provides programmable cell balancing time thresholds for each cell channel, when the timer hits any programmed time threshold, balancing for that channel is stopped (the timer continues to count and the balancing current is turned off).

Main features

The CB_CTRL module has the following features:

- Supports up to 18 cell channels at the same time (HWR001_CB_CTRL)
- Supports both automatic channel selection and manual channel selection (HWR001_CB_CTRL)
- Supports start (timer shall start to count and the balance current shall be on) working by register bit (HWR001_CB_CTRL)
- Supports outputs CB_CH_EN only when CB_GO is detected (HWR003_CB_CTRL)
- Supports separate threshold setting for each cell channel (HWR005_CB_CTRL)
- Timer of balance supports be held if the JOT is H when JOT_EN is high (HWR006_CB_CTRL)
- Supports being paused when any thermal sensor channel is over programmable CB_OT threshold by register bit (HWR007_CB_CTRL)
- Supports being paused manually by register (HWR008_CB_CTRL)
- Supports being paused when channel voltage ADC measurement is ongoing (HWR009_CB_CTRL)
- Supports being stopped when any unmasked fault flag is set in register (HWR010_CB_CTRL)

The odd group and even group of battery cell channels support being switched alternately during automatic mode (HWR011_CB_CTRL)

- Supports programmable average cell balance current by register bit (HWR012_CB_CTRL)
- Provides balance current on/off indication (excluding on/off due to averaging) for each channel by register bit(HWR013_CB_CTRL)
- Supports configuration error detection

Functional Details

Block Diagram

(HWR001_CB_CTRL)

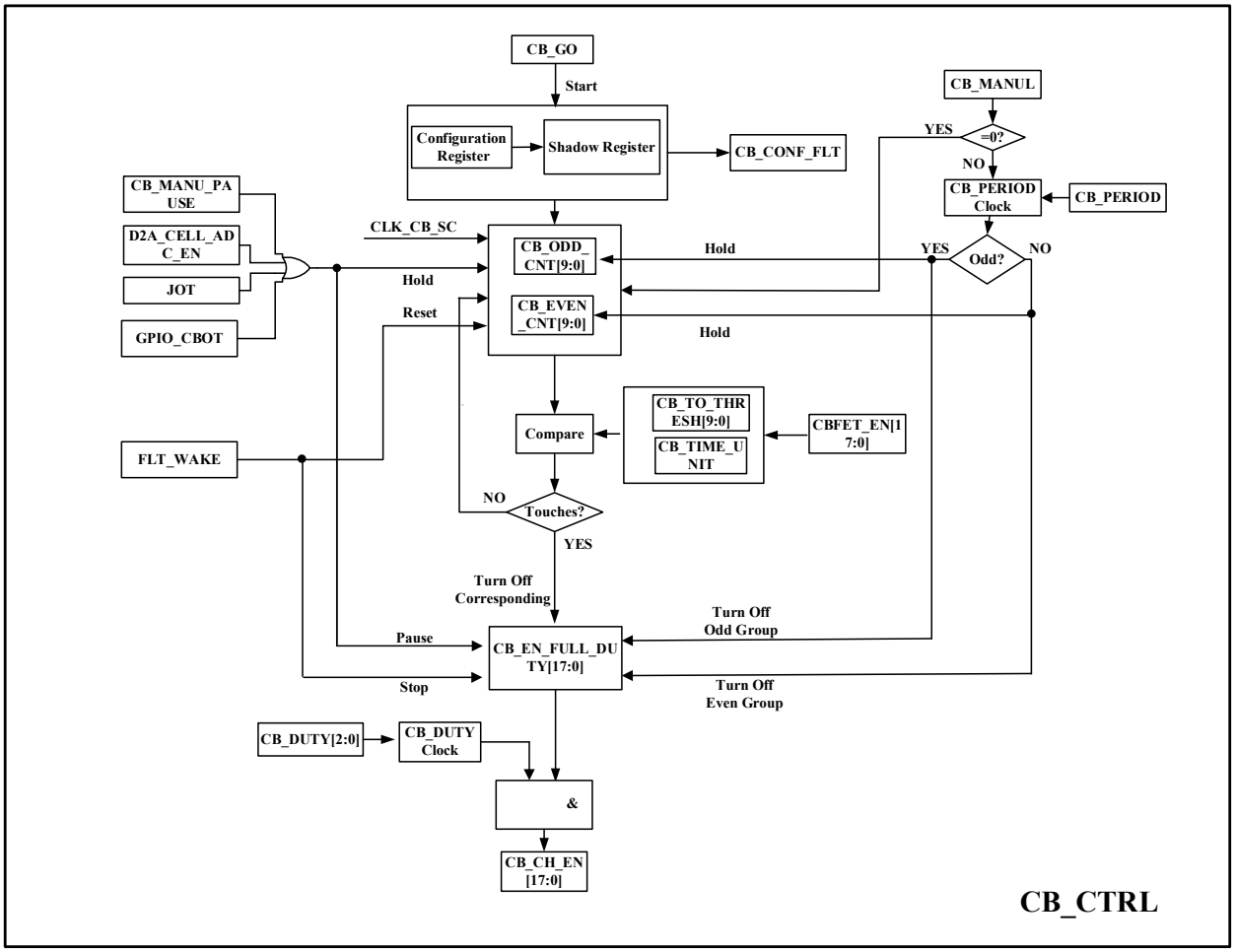

Fig 1CB_CTRL Block Diagram

CB_CTRL supports cell balancing of up to 18 channels. Only enabled channels can be balanced. The schematic diagram of CB_CTRL is shown in Fig 1.CB_CTRL uses shadow register internally. Except for CBFET_ENn(n=1-18) and CB_MANU_PAUSE, CB will update the configuration of the register to the shadow register when CB_GO arrives. For example, CB_MUNAL is updated by CB_MUNAL_REG. Specially, CBFET_ENn shall update with CBFET_EN_REGn when CB_GO only if settings are correct. CB_CTRL supports automatic channel selection and manual channel selection. Channel will stop balancing when reaches the threshold. When all the set channels reach the corresponding threshold, the CB will stop working.

I/O description

Table 1 CB_CTRL I/O description

Pin Name	Direction	Width	Duration	Description
FLT_WAKE	I	1b’	N/A	1: to stop CB_CTRL when FLT_STOP_EN =1'b1
D2A_CELL_ADC_EN	I	1b’	N/A	1: to hold CB_CTRL when ADC_PAUSE_EN =1'b1
JOT	I	1b’	N/A	1: to hold CB_CTRL when JOT_EN =1'b1
GPIO_CBOT	I	1b’	N/A	1: to hold CB_CTRL when GPIO_CBOT_EN =1'b1
CBFET_EN_REG	I	18b’	N/A	CB_EN Input of 18 channels
CB_GO	I	1b’	N/A	To start CB_CTRL and load CB_Setting_REG
CB_MANUAL_REG	I	1b’	N/A	CB mode select, 1: manual , 0:automatic
JOT_EN_REG	I	1b’	N/A	enable JOT to pause CB_CTRL
GPIO_CBOT_EN_REG	I	1b’	N/A	enable GPIO_CBOT to pause CB_CTRL
ADC_PAUSE_EN_REG	I	1b’	N/A	enable ADC_EN to pause CB_CTRL
CB_MANU_PAUSE	I	1b’	N/A	pause CB_CTRL
FLT_STOP_EN_REG	I	1b’	N/A	enable FLT_WAKE to stop CB_CTRL, stop CB_EN, and wait for another CB_GO when FLT_WAKE is "L"
CB_TO_THRESH_REG1-18	I	10b’	N/A	CB threshold time about each channel
CB_UNIT_REG1-18	I	1b’	N/A	unit of CB_TO_THRESH_REG
CB_PERIOD_REG	I	3b’	N/A	in automatic mode, indicate odd/even covert time, 5s-30min, 8steps refer to competitor spec
CB_TWARN_THRESH_REG	I	4b’	N/A	after CB_GO,CB_CTRL output CB_TWARN_THRESH to analog, don’t need other operation
CB_DUTY_REG	I	3b’	N/A	duty of internal PWM, shall cover 12.5%-100%, 8steps

				period is 200ms
CLK_OUT_SC	I	1b’	N/A	system clock
CLK_CB_SC	I	1b’	N/A	function clock, 256K
resetb_SR_CLK_OUT	I	1b’	N/A	reset use for CB_EN
resetb_SR_CLK_SLOW	I	1b’	N/A	reset use for CLK_CB_SC
CB_EN	O	1b’	>1 CLK_CB_SC	"H" when detect CB_GO and "L" when all CH_DONE
CB_CONF_FLT	O	1b’	1 CLK_CB_SC	>2 consecutive channels turn on in CBFET_EN
clr_CB_GO	O	1b’	>1 CLK_CB_SC	output to clear CB_GO
CB_ODD_CNT	O	10b’	>=1 CLK_CB_SC	odd/even is same in manual mode, is different in automatic mode, counter of odd group
CB_EVEN_CNT	O	10b’	>=1 CLK_CB_SC	counter of even group
CB_EN_FULL_DUTY	O	18b’	>=1 CLK_CB_SC	output CB_CH_EN with full duty
CB_TWARN_THRESH[3:0]	O	4b’	>1 CLK_CB_SC	after CB_GO,CB_CTRL output CB_TWARN_THRESH to analog, don’t need other operation
CB_CH_EN	O	18b’	>=1 CLK_CB_SC	output CB_CH_EN after &PWM

State Machine

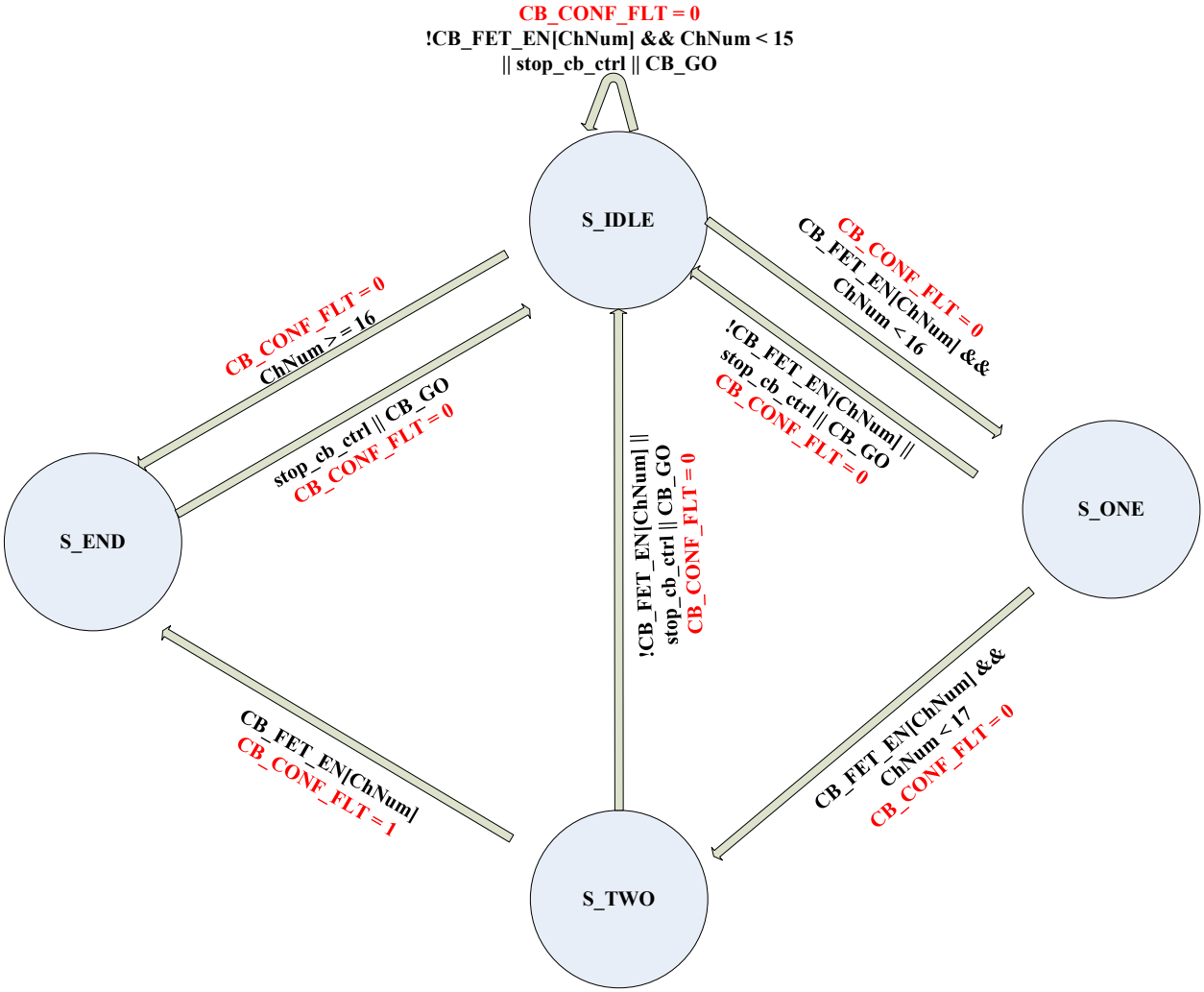

Fig 2 State machine of detect configuration error

This state machine is mainly used to detect whether there is configuration error. That is, in manual mode, three consecutive adjacent channels are enabled. If this error occurs, CB_CTRL will be generated CB_CONF_ FLT. After CB_GO is synchronized, CB_CTRL does not immediately enter the battery balance time, but requires fault detection first. Fault detection needs to detect a maximum of 18 channels, that is, 18 CLK_CB_SC.

Mode Selection

(HWR005_CB_CTRL, HWR009_CB_CTRL)

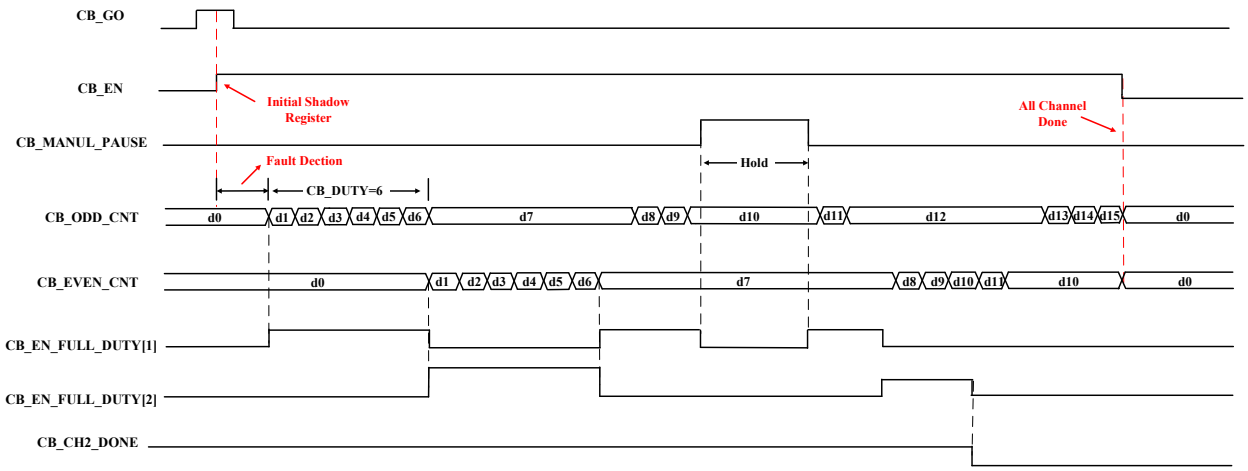

Fig 3Waveform diagram of CB_CTRL in automatic mode

CB_CTRL can select the working mode by configuring CB_MANUL_REG, which is divided into automatic mode (CB_MANUL=0) and manual mode (CB_MANUL=1).For automatic mode, the enabled channels are divided into odd or even channel groups according to the channel number, and each group is cell-balanced in turn according to CB_PERIOD, as show in Fig2.In manual mode, CB will no longer distinguish between odd and even groups, the CB_ODD_CNT and CB_EVEN_CNT counter will count together, and CB_PERIOD will no longer work. When the counter reaches the threshold of the enabled channel, the channel will be closed, and when the counter reaches the threshold time of all channels, the CB stops working.

Table1. Grouping Details

	Even Group	Odd Group
Channel Number	1,3,5,7,9,11,13,15,17	2,4,6,8,10,12,14,16,18
Automatic Mode	Always Start Firstly	Always Start Secondly
Manual Mode	Treated as same group	

Note: In automatic mode, even group always start counting firstly.

Pause and Stop Control

(HWR006_CB_CTRL, HWR007_CB_CTRL, HWR008_CB_CTRL, HWR009_CB_CTRL, HWR010_CB_CTRL)

CB_CTRL supports pausing or stopping during cell balancing. When suspending, turn off the corresponding suspend signal, CB_CTRL can resume work, but can only be restarted by CB_GO after stopping.

Table2. Conditions for pause and stop of CB

	Pause	Stop
1	CB_MUNU_PAUSE_REG	FLT_WAKE &FLT_STOP_EN_REG
2	D2A_CELL_ADC_EN & ADC_PAUSE_EN_REG	
3	JOT & JOT_EN_REG	
4	GPIO_CBOT &GPIO_CBOT_EN_REG	

Internal Pulse Width Modulation

(HWR012_CB_CTRL, HWR013_CB_CTRL)

CB supports pulse width modulation (PWM) of CB_EN_FULL_DUTY. The period after PWM is fixed at 200ms, and there are 8 kinds of adjustable duty cycles, which are controlled by CB_DUTY_REG.

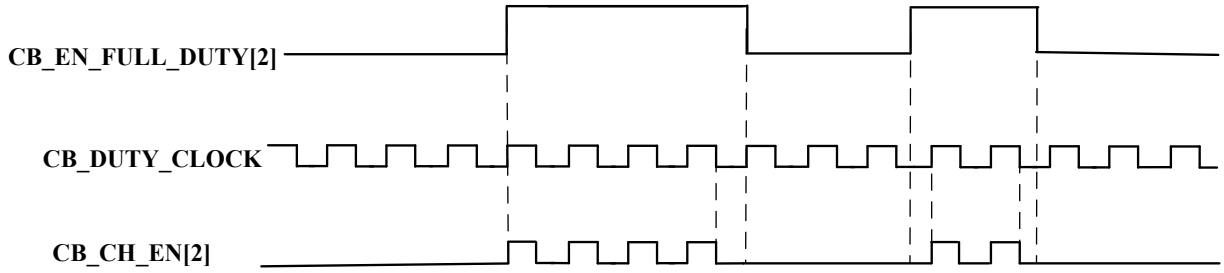

Fig 3 Schematic diagram of a PWM with a duty cycle of 1/2

Fault Detection

When CB_MUAL is configured to 1(manual mode), a configuration error judgment will be carried out. If there is a configuration error, CB_CTRL will immediately end and generate CB_CONF_FLT. When CB_CONF_FLT_MSK is 0, CB_CONF_FLT will be written to the FAULT register.