Technical Requirement

WP as Prerequisites	Author of TR
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ITEM	TR ID	Description
Compatibility	TR0_00	BM21A **should** have pin to pin compatibility with xx718 (BB pin can be NC)

ITEM	TR ID	Description
Operation Mode	TR1_00	BM21A **shall** have 3 operating modes: The average current consumption of BM21A and its BOM from PACK+ during active mode **shall** <10mA at full temp The average current consumption of BM21A with OVUV&OTUT detection every 1s and its BOM from PACK+ during sleep mode **shall** <100uA at full temp The average current consumption of BM21A and its BOM from PACK+ during shutdown mode **should** <10uA at room temp
Operation Mode	TR1_01	The time from opearating mode switching signal received to operating mode switching done of BM21A **shall** <10ms at full temp
Operation Mode	TR1_02	The direct operating mode switching of BM21A **shall** support: shutdown mode<-sleep mode, shutdown mode<->active mode, sleep mode<->active mode
Operation Mode	TR1_03	12 daisy-chained BM21As **shall** support being switched to active mode from sleep or shutdown mode within 40ms with signal pattern received from MCU at full temp
Operation Mode	TR1_04	12 daisy-chained BM21As **shall** support being switched to shutdown mode from sleep or active mode within 100ms with signal pattern received from MCU at full temp
Operation Mode	TR1_05	12 daisy-chained BM21As **shall** support being switched to sleep mode from active mode within 100ms with signal pattern received from MCU at full temp
Operation Mode	TR1_06	The active mode entrance signal pattern detection of BM21A **shall** reuse communication port The active mode entrance detection of BM21A **shall** use noise free signal pattern w.r.t 50% magnitude and 10% occurrence The active mode entrance signal pattern detection of BM21A **shall** support both north and south communication direction
Operation Mode	TR1_07	The shutdown mode entrance signal pattern detection of BM21A **shall** reuse communication port The shutdown mode entrance detection of BM21A **shall** use noise free signal pattern w.r.t 50% magnitude and 10% occurrence The shutdown mode entrance signal pattern detection of BM21A **shall** support both north and south communication direction The shutdown mode entrance signal pattern detection of BM21A **should** be based on the edge detection of register bit

ITEM	TR ID	Description
Operation Mode	TR1_08	The sleep mode entrance signal pattern detection of BM21A **shall** reuse communication port The sleep mode entrance detection of BM21A **shall** use noise free signal pattern w.r.t 50% magnitude and 10% occurrence The sleep mode entrance signal pattern detection of BM21A **shall** support both north and south communication direction The sleep mode entrance signal pattern detection of BM21A **should** be based on the edge detection of register bit
Operation Mode	TR1_09	BM21A **shall** support hard digital reset signal pattern detection without digital core engagement during sleep/active mode The digital core of BM21A **shall** be reset when hard digital reset signal pattern is detected
Operation Mode	TR1_10	The time from hard and soft digital reset signal pattern received to digital core reset done of BM21A **shall** <10ms at full temp
Operation Mode	TR1_11	The hard and soft digital reset signal pattern detection of BM21A **shall** reuse communication port The hard and soft digital reset signal pattern detection of BM21A **shall** use noise free signal pattern w.r.t 50% magnitude and 10% occurrence The hard and soft digital reset signal pattern detection of BM21A **shall** support both north and south communication direction The soft digital reset signal pattern detection of BM21A **should** be based on the edge detection of register bit
Operation Mode	TR1_13	BM21A **shall** enter shutdown mode when a fixed 2s frame communication timer timeout The timer **shall** start to count only during active mode The timer **shall** be reset when a frame is received
Operation Mode	TR1_14	BM21A **shall** enter active mode after digital core reset done The cause of digital reset excluding MCU's intention **shall** be recorded by register bit The register bit **shall** support being written to clear The fault flag **shall** support being masked from being set by register bit
Operation Mode	TR1_15	BM21A **shall** support soft digital reset signal pattern detection during active mode The digital core of BM21A **shall** be soft reset when soft digital reset signal pattern is detected

ITEM	TR ID	Description
Operation Mode	TR1_16	12 daisy-chained BM21As **should** support being hard digital reset from sleep or active mode to active mode within 20ms with signal pattern received from MCU at full temp
Power Supply Capability	TR2_00	The power rail voltage of BM21A for thermal sensors **shall** have +-5mV accuracy during sleep/active mode at full temp The power rail for thermal sensors **shall** support 0-12 resistor dividers' as load (10k-200k) The power rail of thermal sensor OVUV detection threshold **shall** be fixed 2.515V and 2.485V.
Operation Voltage Range	TR3_00	BM21A **shall** support 9-100V DC input as power input for functional operation
Measurement	TR4_00	BM21A **shall** support the ADC measurement of 6-18 channel voltages (consists of 6-18 battery cell voltages plus 0-2 bus bar voltages), 0-12 auxiliary input voltages plus power rail voltage of thermal sensors (can be taken as 0-12 thermal sensor voltage ratios), die temperature and battery pack voltage during active mode The auxiliary input voltages measurement **should** reuse digital IO pin The battery pack voltage measurement **should** reuse BAT pin
Measurement	TR4_01	The connection of busbar **shall** support random location selected by register bit except top/bottom and adjacent 2 busbars for BM21A
Measurement	TR4_02	The spared channel without connection of battery cell **shall** support random location except bottom for BM21A
Measurement	TR4_03	The differential leakage into each measurement pin couplet (battery cells, busbars, thermal sensors) of BM21A during measurement **shall** <1uA at full temp

ITEM	TR ID	Description
Measurement	TR4_04	ADC accuracy of BM21A **shall** meet the spec under default measurement time (**should** <150us) as below: battery cell voltage and bus bar voltage measurement (1kohm+4.7nF): □ ±1mV accuracy (1.5V to 4.5V, 25℃) □ ±2mV accuracy (1.5V to 4.5V, -20℃ to +65℃) □ ±5mV accuracy (-2V to 5V,-40℃ to +125℃) □ ±10mV accuracy (-2V to 5V, -40℃ to +125℃) within 10 years auxiliary input voltages plus power rail voltage of thermal sensors: □ ±2mV accuracy (auxiliary input: 0.5V to 4V, power rail: 2.5V, -20℃ to +65℃) □ ±5mV accuracy (auxiliary input: 0V to 4.5V, power rail: 2.5V, -40℃ to +125℃) □ ±0.16% accuracy (thermal sensor voltage ratio: 10% to 90% VTREF, -20℃ to +65℃) □ ±0.4% accuracy (thermal sensor voltage ratio: 0 to 100% VTREF, -40℃ to +125℃) die temperature measurement: □ ±5℃ accuracy (-40℃ to +125℃) battery pack voltage measurement: □ ±200mV accuracy (-40℃ to +125℃)
Measurement	TR4_05	The skew time of all stack 216(18x12) channel voltages' ADC measurement when one command received from MCU **should** <200us and **shall** <1ms at full temp ADC accuracy of battery cell voltage and bus bar voltage measurement **shall** meet the spec under the <1ms skew time: ±3mV accuracy (1.5V to 4.5V, 25℃)
Measurement	TR4_06	The skew time of all stack 144(12x12) thermal sensor voltage ratios' ADC measurement with one command received from MCU **should** <200us and **shall** <12ms at full temp
Measurement	TR4_07	The duration time from read command is sent out from MCU to all 12 daisy-chained BM21As' 216(18x12) channel voltages ADC measurement data are received by MCU **shall** <10ms at full temp
Measurement	TR4_08	The ADC measurement data of each channel of BM21A **shall** only be updated till new measurement data of this channel is available
Measurement	TR4_09	The all ADC measurement data of BM21A **shall** support being read with one command received from MCU
Measurement	TR4_10	There **shall** be information for MCU to judge if the read ADC measurement data is newly updated

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Measurement	TR4_11	The measurement data stored in registers of BM21A **should** be filtered to <-3dB from battery cell voltage noise those frequencies > fc The fc **should** be programmable from typical 10Hz to 1kHz with 8 steps by register bit
Measurement	TR4_12	The measurement accuracy of battery cell voltage **shall** be kept when -2V<VBAT-VC18
Measurement	TR4_13	The measurement of both cell voltage and auxiliary input voltage **shall** pass 300mA BCI test (error<10mV)
Communication	TR5_00	The communication of BM21A **shall** support xx600 communication protocol
Communication	TR5_01	The communication of BM21A **shall** support daisy-chained BM21As isolated by typical 2.2nF capacitors and min 150uH max 1.4mH transformer
Communication	TR5_02	The error rate of communication **should** <0.001% during communication burn-in test For the communication burn-in test, BM21A devices **shall** be isolated by 2m communication cable plus caps only, transformers only, or cap+choke 6 daisy-chained BM21A devices **shall** burn-in 8h at -40℃, 25℃, 125℃ 12 or 24 daisy-chained BM21A devices **shall** burn-in 24h at 25℃
Communication	TR5_03	The specified single BM21A device **shall** support being read at least 128 bytes registers with continuous addresses by one command received from MCU
Communication	TR5_04	The specified single BM21A device **shall** support being written at least 16 bytes writable registers with continuous addresses by one command received from MCU
Communication	TR5_05	The whole stack BM21A devices **shall** support being read at least 128 bytes registers with continuous addresses by one command received from MCU
Communication	TR5_06	The whole stack BM21A devices **shall** support being written at least 16 bytes writable registers with continuous addresses by one command received from MCU
Communication	TR5_07	The device addresses of 12 daisy-chained BM21As **shall** support being identified by MCU
Communication	TR5_08	The identified device addresses of BM21A **should** be kept during all operating mode unless being identified by MCU again or power off
Communication	TR5_09	The communication between adjacent BM21As **shall** pass BCI 300mA test (no communication fault)

ITEM	TR ID	Description
Communication	TR5_10	When ring architecture is used, if one any communication node is open among 12 daisy-chained BM21As and transceiver, all daisy-chained BM21As **shall** still support being written and read by MCU
Communication	TR5_11	When the isolators configuration are same for each BM21A, the difference of average communication current consumption among all 12 daisy-chained BM21As **should** <1mA
Communication	TR5_12	The command frame propagation of top device defined in the daisy-chained BM21As **shall** support being disabled by register bit.
Cell Balance	TR6_00	Passive cell balance for each battery cell of BM21A **shall** be available when MCU requests during both active and sleep mode, no matter battery cell/busbar use separate balance channels or busbar+battery cell share two adjacent balance channels
Cell Balance	TR6_01	BM21A **shall** support at least 9 battery cell channels' balance at the same time when MCU requests Only enabled channel can be balanced, BM21A **should** support both automatic channel selection and manual channel selection by register bit For automatic mode, the enabled channels **should** be default odd or even channels group, during manual mode, each channel **should** support being selected by register bit
Cell Balance	TR6_02	Maximum passive cell balance current of BM21A **should** >300mA and **shall** >240mA for each battery cell channel when no adjacent cells balancing, RB=10Ω, Vcell=5V, Ta=85℃ Delta Tc of BM21A with 9 channels' 240mA balance current **shall** <20℃ at Ta=85℃
Cell Balance	TR6_03	Cell balance of BM21A **shall** start (timer **shall** start to count and the balance current **shall** be on) by register bit
Cell Balance	TR6_04	BM21A **shall** provide programmable cell balance time threshold by register bit for each battery cell channel, the biggest value of threshold **shall** >12h, step 1s-1min, accuracy 5% at full temp The default value of time threshold for each battery cell channel **shall** be the biggest When timer touches any programed time threshold, the balance of this channel **shall** be stopped (timer **shall** go on to count and the balance current **shall** be off)

ITEM	TR ID	Description
Cell Balance	TR6_05	Cell balance of BM21A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when junction temperature is over programmable CB_JOT threshold by register bit, 90℃-125℃, 5℃ step, accuracy 5℃ When junction temperature is under the hys 10℃, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR6_06	Cell balance of BM21A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when any thermal sensor channel is over programmable CB_ROT threshold by register bit, 125mV-900mV, 25mV step, 25mV accuracy at full temp The detection period of CB_ROT **should** share same configuration with OTUT detection BM21A **shall** have two programmable CB_ROT thresholds sharing same threshold range to be selected by register bit for each thermal sensing channel When all thermal sensor temperatures are under the hys 50mV, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR6_07	Cell balance of BM21A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) manually by register bit When this register bit is toggled, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR6_08	Cell balance of BM21A **shall** support being paused (timer **shall** hold and the balance current **shall** be off) when channel voltage ADC measurement is ongoing When channel voltage ADC measurement is not ongoing, the balance **shall** be resumed (timer **shall** go on to count and the balance current **shall** be on)
Cell Balance	TR6_09	Cell balance of BM21A **shall** support being stopped (timer **shall** clear and the balance current **shall** be off) when any unmasked fault flag is set in register
Cell Balance	TR6_10	The odd group and even group of battery cell channels **shall** be switched alternately during automatic mode The switching period **should** be programmable by register bit, range 5s-30min, 8 steps, accuracy 5% at full temp
Cell Balance	TR6_11	BM21A **shall** support programmable average cell balance current by register bit, range 12.5%-100% maximum cell balance current value, step 12.5%, accuracy 5% at full temp The cell balance current **should** be averaged within every 0.2s duration

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Cell Balance	TR6_12	BM21A **shall** provide balance done (timer touches the time threshold or cell voltage touches the CBUV threshold) status for each channel by register bit BM21A **shall** provide information about remaining balance time for each channel by register bit
Cell Balance	TR6_13	The mismatch of balance current for each separately enabled channel **shall** <10mA at 4.25V under same temp
Cell Balance	TR6_14	During sleep mode, when measured cell voltage touches the programed CBUV threshold, the balance of this channel **shall** be stopped (timer **shall** go on to count and the balance current **shall** be off) Battery cell channel CBUV detection threshold **shall** be programmable by register bit, cover 2.45V-4V, 5mV step When busbar+battery cell share two adjacent balance channels (two adjacent CBFETs are enabled), the busbar channel **shall** ignore CBUV threshold
Reversely Wake Up	TR7_00	The OVUV for each battery cell channel **shall** be detected by BM21A periodically during sleep mode The period of OVUV detection **shall** support being programmable by register bit, from 200ms to 3.2s, 200ms step,from 3.2s to 156.8s, 3.2s step, accuracy 5% at full temp
Reversely Wake Up	TR7_01	The OTUT for each thermal sensor channel **shall** be detected by BM21A periodically during sleep mode The period of OTUT detection **shall** support being programmable by register bit, from 200ms to 3.2s, 200ms step,from 3.2s to 156.8s, 3.2s step, accuracy 5% at full temp
Reversely Wake Up	TR7_02	The OVUV detection period and OTUT detection period **should** share same programmable register bits
Reversely Wake Up	TR7_03	The detected OVUV&OTUT fault for each channel **shall** be recored in register bit The fault flag register bit **shall** support being written to clear The fault flag **shall** support being masked from being set by register bit
Reversely Wake Up	TR7_04	Battery cell channel OVUV detection of BM21A **shall** meet 5mV accuracy at full temp Battery cell channel OVUV detection threshold **shall** be programmable by register bit, cover OV:2V-5V, 25mV step; UV: 0.7V-3.875V, 5mV step.

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Reversely Wake Up	TR7_05	Thermal sensor OTUT detection of BM21A **shall** meet 25mV accuracy at full temp Thermal sensor OTUT detection threshold **shall** be programmable by register bit: cover OT:125mV-900mV, 25mV step; UT:1900mV-2250mV, 50mV step.
Reversely Wake Up	TR7_06	BM21A **shall** have two groups of OTUT programmable thresholds sharing same threshold range for each thermal sensing channel For each thermal sensing channel, the threshold group **shall** support being selected by register bit
Reversely Wake Up	TR7_07	The differentail leakage into each OVUV&OTUT comparison pin couplet (battery cells, thermal sensors) of BM21A during comparison **shall** <1uA at full temp
Reversely Wake Up	TR7_08	Among 12 daisy-chianed BM21As, any BM21A with any OVUV&OTUT fault flag set in registers **shall** actively send out wake signal to SBC only during sleep mode The time from any OVUV&OTUT fault flag is set in registers to wake signal is received by transceiver **shall** <100ms at full temp
Reversely Wake Up	TR7_09	The OVUV and OTUT detection of BM21A for each channel **shall** have typical 150us deglitch time which counts from fault occurs to fault flag set in register
Digital IO	TR8_00	BM21A **shall** have 12 digital IO channels
Digital IO	TR8_01	The each digital IO of BM21A **shall** support being selected as push-pull output by register bit during active mode
Digital IO	TR8_02	When the digital IO of BM21A is configured as push-pull output: Digital IO **shall** be pulled to >4V at 1mA load current within 1ms when logic high enabled and pulled to <0.4V at 1mA sink current within 1ms when logic low enabled by register bit at full temp The output current limit of each digital IO **shall** have typ 8mA at full temp
I2C Master	TR9_00	BM21A **shall** support reading and writing the I2C slave 24C02 (E2PROM) of during active mode The reading and writing of I2C slave 24C02 **should** reuse digital IO pin
Others	TR10_00	The die X-Y location on wafer and lot information during production for each BM21A chip **shall** be stored in NVM for customer read ONLY The version ID **should** be read ONLY for customer
Others	TR10_01	BM21A **shall** pass AEC-Q100 Grade1 qualification

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Others	TR10_02	BM21A **shall** pass ESD HBM: 2kV ESD CDM: 750V for corner pins, 500V for other pins Latch-up: ±200mA BM21A **shall** pass customized EMC test requirement
Others	TR10_03	Maximum die size of BM21A **shall** <22mm^2
Others	TR10_04	Package of BM21A **shall** be LQFP 10x10-64E
Others	TR10_05	FT time @ room temp for BM21A **shall**<6s
Others	TR10_06	BM21A **shall** survive during 90V(5Vx18) battery pack random hot-plug
Maintain	TR11_00	If the number of open wire faults for FPC (including channel harness and thermal sensor harness) <=2, the fault flag in register bit **shall** provide the accurate location information The register bit **shall** support being masked from being set by register bit The register bit **shall** support being written to clear
Maintain	TR11_01	Each CBFET open/short status and each RCB drift status of BM21A **should** support being diagnosed by host
Maintain	TR11_02	The communication cable open fault during sleep mode **should** be alerted to MCU within 1s.
48V	TR12_00	BM21A **should** support 48V (14 battery cells or 16 battery cells) battery system with pack current sensing and SPI interface by re-bonding
48V_FUSE/RELAY	TR13_00	BM21A **shall** support the measurement of fuse voltage and relay voltage fuse voltage measurement (4.7nF): □ ±1mV accuracy (-1V to 1V, 25℃) □ ±2mV accuracy (-1V to 1V, -20℃ to +65℃) □ ±5mV accuracy (-1V to 1V,-40℃ to +125℃) relay voltage measurement (1kohm+4.7nF): □ ±1mV accuracy (-1V to 1V, 25℃) □ ±2mV accuracy (-1V to 1V, -20℃ to +65℃) □ ±5mV accuracy (-1V to 1V,-40℃ to +125℃)
48V_CS	TR14_00	BM21A **shall** support the measurement of shunt voltage(100uOhm or 200uOhm, 10nF) at typical 3ms measurement slot: □ ±1uV offset accuracy (40℃ to +125℃) □ ±0.3% gain accuracy (-150mV to 150mV ,-40℃ to +125℃) □ 3uVrms noise (25℃)
48V_CS	TR14_00	The measurement of shunt voltage shall reuse GPIO pins, which can be disabled by NVM

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48V_CS	TR14_01	The shunt voltage measurement shall be always synchronous with all battery cell voltage measurement within 1 measurement round-robin
48V_CS	TR14_02	The shunt voltage measurement accuracy shall be automatically detected by redundant fuse/relay measurement with 5mV error
48V_CC	TR15_00	The measurement result shall support being sumed by coulmber counter The CC can be clear by read/register trigger? The counter shall alert the full There shall be a number to count the measurement times
48V_CC	TR15_01	The CC shall be available at both active and sleep mode for active mode, the measurement of shunt voltage shall be continuous for sleep mode, the period of measurement of shunt voltage shall be programmable from 1s to 10s
48V_OC	TR16_00	The OCC/OCD comparison shall be available at both active and sleep mode
48V_OC	TR16_01	The OCC comparison threshold shall be programmable from 30mV to 150mV
48V_OC	TR16_02	The OCD comparison threshold shall be programmable from 50mV to 200mV
48V_OC	TR16_03	The OCC and OCD comparison deglitch shall be programmable from 50us to 200us
48V_OC	TR16_04	Once OC, the fault flag shall be set
48V_SPI	TR17_00	The power rail of SPI shall be VIO from SBC, 3.3V or 5V, can reuse GPIO pin
48V_SPI	TR17_01	The SPI shall support 2-6MHz, type 00, half-duplex
48V_SPI	TR17_02	The SPI protocol shall support at least 16 byte continuous writing and at least 128 byte continuous reading
48V_WAKE	TR18_00	Once any fault flag set during sleep mode, the WAKE shall be pulled high to >4V within 1ms, can reuse FLTB pin
48V_GPIO	TR19_00	BM21A shall support at least 8 GPIO for digital input/output and aux input measurement and thermal power rail measurement
48V_FLTB	TR20_00	Once any fault flag set during active mode, the FLTB shall be pulled high to <1V within 1ms, can reuse GPIO pin

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