TONE_CTRL IP SPEC

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Introduction

The TONE_CTRL module is used to generate tones.

Feature

Key features of the TONE_CTRL module are:
•All functions are for both AFE and bridge application
•Generate WAKEUP TONE when received WAKE_TONE_DET or WAKE_TONE_GEN high.
•Generate STA TONE when received STA_TONE_DET or when STA_TONE_GEN high.
•Generate SD TONE on N port after SD_TONE_GEN high. Direction in TONE_TRANS_EN shall base on SPI_DIR.
•Generate FLT TONE on N port every 50ms when SLEEP high and FLT_WAKE high.
•Generate HB TONE on N port every 400ms when SLEEP high and FLT_WAKE low.
•TONE transmitting and daisy chain transmitting are mutually exclusive.
•WAKE TONE and STA TONE shall have higher priority to HB TONE and FLT TONE.

1.所有的功能兼容AFE和bridge
2.当接收到**WAKE_TONE**（**WAKE_TONE_DET**为高），或者**WAKE_TONE_GEN**为高，会产生WAKEUP_TONE
3.当STA_TONE_DET为高，或者STA_TONE_GGEN,会产生STA_TONE
4.当SD_TONE_GEN为高，会产生STA_TONE（N port）。TONE_TRANS_EN的方向由SPI_RDY决定
5.当SLP MODE，FLT_WAKE为低，每400ms在北口产生HB TONE。如果FLT_WAKE为高，则每50ms在北口产生FLT_TONE.
6.TONE的传输和菊花链的传输是互斥的
7.**WAKE TONE**以及**STA TONE**的优先级要高于**HB TONE** 和**FLT TONE**.

Register Definition

Register Map

Table 1 1TONE_CTRL Register Map

Name	Add	D7	D6	D5	D4	D3	D2	D1	D0	Default
CTRL1	0x2002	SOFT_RSTB	DIR_SEL		WAKE_TONE_GEN	STA_TONE_GEN	SD_TONE_GEN	TO_SD	TO_SLEEP	0x80
CTRL2	0x2003						CMP_BIST_GO	ADD_W_EN	SPI_DIR	0x00

Functional Details

Block Diagram

The following diagram shows the TONE_CTRL architecture and internal modules and connections.

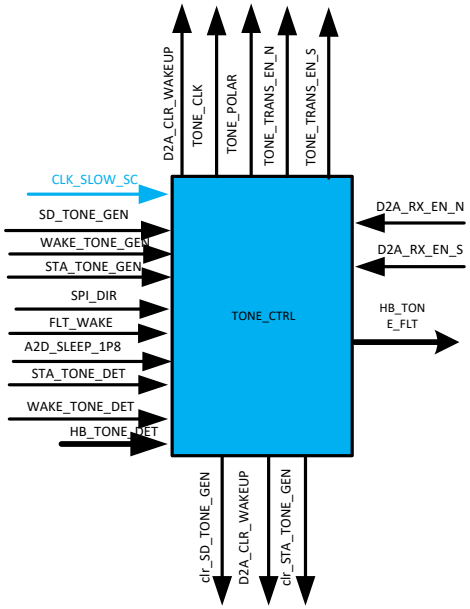

Figure 1 TONE_CTRL diagram

Module input/output list

Name	Dir	Width	Discirption	duration
D2A_CLR_WAKEUP	O	1	Pulse for analog to clear A2D_WAKE_UP_x	1 CLK_256K
clr_WAKE_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear WAKE_TONE_GEN	1 CLK_256K
clr_STA_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear STA_TONE_GEN	1 CLK_256K
pos_HBFSAT	O	1	HB too fast condition is detected	1 CLK_256K
pos_HBTO	O	1	HB too slow(timeout) condition is detected	1 CLK_256K
TONE_TRANS_EN_N	O	1	N port tone transmission enable	Level(CLK_OUT domain)
TONE_TRANS_EN_S	O	1	S port tone transmission enable	Level(CLK_OUT domain)
TONE_CLK	O	1	Tone clock	1 CLK_256K
TONE_POLAR	O	1	Tone polar(1: positive tone; 2: negative tone)	Level(CLK_256K domain)
rx_en_256K	O	1	Synchronoused rx_en_ds_or_spi by CLK_256K	Level(CLK_256K domain)
SLEEP_MODE	O	1	Synchronoused A2D_SLEEP_1P8 by CLK_256K	Level(CLK_256K domain)
SD_TONE_GEN_EN	O	1		
clr_SD_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear SD_TONE_GEN	1 CLK_256K

CLK_256K_SC	I	1	Scan-muxed CLK_256K	50% duty
resetb_CLK_256K	I	1	Asynchronous reset signal(synchronously released by CLK_256K)	Level(CLK_256K domain)
SOFT_RSTB	I	1	Soft reset	Level(CLK_SLOW domain)
CLK_OUT_SC	I	1	CLK_OUT after scan mux	
resetb_SR_CLK_OUT	I	1	Asynchronous reset signal (synchronously released by CLK_OUT) and SOFT_RSTB logic	Level(CLK_OUT domain)
A2D_WAKE_UP_N	I	1	Wake tone detected from N port	async
A2D_WAKE_UP_S	I	1	Wake tone detected from S port	async
A2D_STA_DET_N	I	1	STA tone detected from N port	async
A2D_STA_DET_S	I	1	STA tone detected from S port	async
HB_TONE_DET	I	1	Heart beat tone detected	async
D2A_RX_EN_S	I	1	enable daisy chain receiving on S port	Level(CLK_32M domain)
D2A_RX_EN_N	I	1	enable daisy chain receiving on N port	Level(CLK_32M domain)
WAKE_TONE_GEN	I	1	Register bit from u_COMM_REG to generate wake tone	Level(CLK_REG domain)
STA_TONE_GEN	I	1	Register bit from u_COMM_REG to generate sleep to active tone	Level(CLK_REG domain)
A2D_SLEEP_1P8	I	1	Sleep mode indication	async
SD_TONE_GEN	I	1	Register bit from u_COMM_REG to generate shut down tone	Level(CLK_REG domain)
SPI_EN	I	1	Enable SPI	Async
SPI_DIR	I	1	"1" for north interface, "0" for south interface	Level(CLK_REG domain)
SPI_RX_EN	I	1	Indicate RX_DATA_SPI is update	1 CLK_REG
rx_en	I	1	daisy chain signal is being received	Level(CLK_32M domain)
tx_en_32M	I	1		
state_rx_init	I	1	state is STATE_INIT	1 CLK_REG
state_rx_bps	I	1	state is STATE_BYPASS	1 CLK_REG
FLT_WAKE	I	1	Indicate fault status	Level(CLK_SLOW domain)

Clock Domain

The clock for TONE_CTRL is CLK_256K_SC and CLK_OUT_SC.
For TONE_TRANS_EN_X related logics, CLK_OUT_SC is used.
For others, CLK_256K_SC is used.

TONE_CTRL function description

TONE_CTRL module is a sub module in COMM_DIG. It generates 5 kinds of tones. The 5 tones are described in Table2 and From2.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time between pulses of COMM tones COMM tones: WAKE,	$t_{COMMTONE}$			11	15	us

STA, SHUTDOWN						
HIGH time of each pulse of COMM tone	$t_{COMMTONE\_HI}$		0.92	1	1.08	us
LOW time of each pulse of COMM tone	$t_{COMMTONE\_LO}$		0.92	1	1.08	us
Time between pulses of FAULT tones	$t_{FLTTONE}$			11.5		us
HIGH time of each pulse of FAULT tone	$t_{FLTTONE\_HI}$			1		us
LOW time of each pulse of FAULT tone	$t_{FLTTONE\_LO}$			1		us
Time between pulses of HB tones	t_{HBTONE}			11.5		us
HIGH time of each pulse of HB tone	t_{HBTONE_HI}			1		us
LOW time of each pulse of HB tone	t_{HBTONE_LO}			1		us
Period between HB tone burst	t_{HB_PERIOD}		360	400	440	ms
Timeout to not receive HB	$t_{HB\_TIMEOUT}$		0.9	1	1.1	s
Time to receive HB too fast	t_{HB_FAST}			200		ms
Period between FAULT tone burst	t_{FLT_PERIOD}			50		ms
FAULT tone latency in stack devices	$t_{FLTS\_LATENCY}$	From time a device receives the tone to the time the same device detects and generates its fault tone		48		us
FAULT tone latency in base device	$t_{FLTB\_LATENCY}$	From time a device receives the tone to the time the same device detects and asserts fault pin		24		us

Table2 timing requirement for tones

WAKE tone			STA tone			SHUTDOWN tone			HB tone			FT tone		
n	nDET	Polar	n	nDET	Polar	n	nDET	Polar	n	nDET	Polar	n	nDET	Polar
90	60	+	30	20	+	270	180	-	30	20	-	90	60	-

Table3 Numbers and Polarity of Tones

In CLK_256K domain, 1 clock is 3.9us, so 1us width pulses will be generated in analog part. In digital part, all tones are generated on outputs TONE_CLK, TONE_POLAR, TONE_TRANS_EN_N, TONE_TRANS_EN_S.

TONE_CLK: (HWR001/003/004/005/006_TONE_CTRL)
If a tone is being generated, TONE_CLK is always 1 clock high with 3 clocks period(HWR007_TONE_CTRL). After the corresponding numbers of pulses(in Table3) are sent, TONE_CLK stops toggling.

TONE_POLAR:
According to Table3, when sending WAKE tone or STA tone, TONE_POLAR is high. When sending other tones, TONE_POLAR is low.

TONE_TRANS_EN_N:
When sending tone because of analog detected tones on S port(HWR002_TONE_CTRL) (A2D_WAKE_UP_S(HWR001_TONE_CTRL) or

A2D_STA_DET_S(HWR003_TONE_CTRL)), TONE_TRANS_EN_N is high to deliver the tone.

When sending WAKE(HWR012_TONE_CTRL) tone, STA(HWR014_TONE_CTRL) tone or SHUTDOWN(HWR004_TONE_CTRL) tone because of corresponding register bit X_GEN, if SPI_DIR is low, TONE_TRANS_EN_N is high.

When sending HB(HWR006_TONE_CTRL) tone or FLT(HWR005_TONE_CTRL) tone, TONE_TRANS_EN_N is high. HB tone is sent when SLEEP_MODE high and FLT_WAKE low, FLT tone is sent when SLEEP high and FLT_WAKE high(HWR009_TONE_CTRL). If SLEEP_MODE changes to active mode(A2D_SLEEP_1P8 changes to high), BM20A response to A2D_WAKE_UP_N/A2D_WAKE_UP_S/A2D_STA_DET_N/A2D_STA_DET_S immediately. (HWR011_TONE_CTRL)

As daisy chain transmitting are always start after receiving(copy or response), TONE_TRANS_EN_N changes to 0 when daisy chain starts receiving(HWR010_TONE_CTRL).

TONE_TRANS_EN_S:

When sending tone because of analog detected tones on N(HWR002_TONE_CTRL) port(A2D_WAKE_UP_N(HWR001_TONE_CTRL) or A2D_STA_DET_N(HWR003_TONE_CTRL)), TONE_TRANS_EN_S is high to deliver the tone.

When sending WAKE(HWR012_TONE_CTRL) tone, STA(HWR014_TONE_CTRL) tone or SHUTDOWN(HWR004_TONE_CTRL) tone because of corresponding register bit X_GEN, if SPI_DIR is high, TONE_TRANS_EN_S is high.

As daisy chain transmitting are always start after receiving(copy or response), TONE_TRANS_EN_N changes to 0 when daisy chain starts receiving(HWR010_TONE_CTRL).

Clr_xxx(xxx is SD_TONE_GEN, WAKE_TONE_GEN, STA_TONE_GEN) is generated after synchronizing the tone source to clear the tone starting state.(HWR008/013/015_TONE_CTRL). (Refer to Figure2)

Specially, D2A_CLR_WAKEUP is high after the corresponding numbers of pulses (in Table3) are sent(HWR016_TONE_CTRL). (Refer to Figure3)

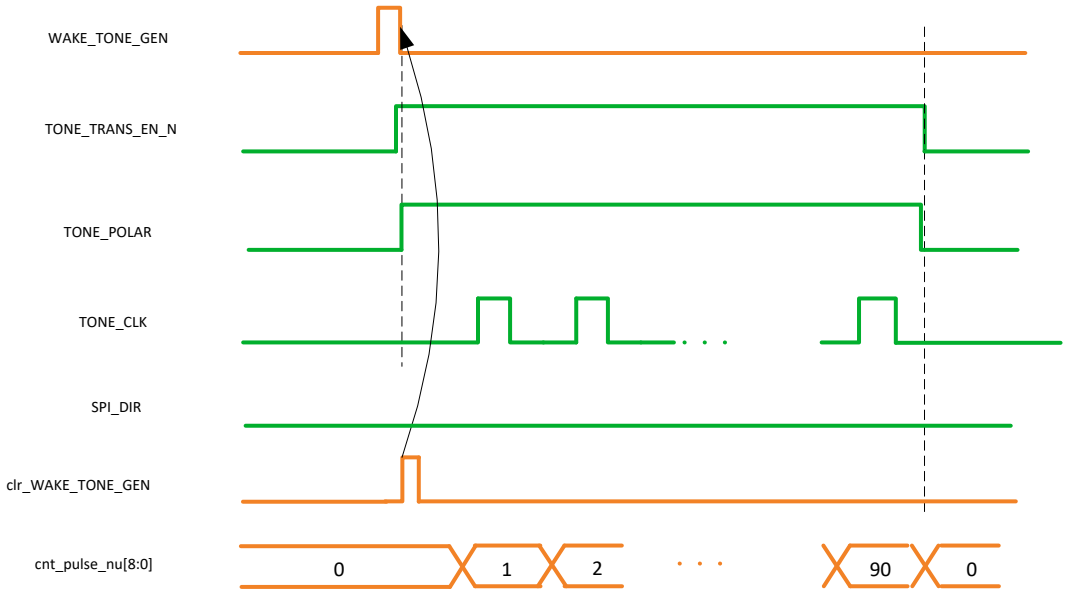

Figure2 WAKE_TONE_GEN is written high

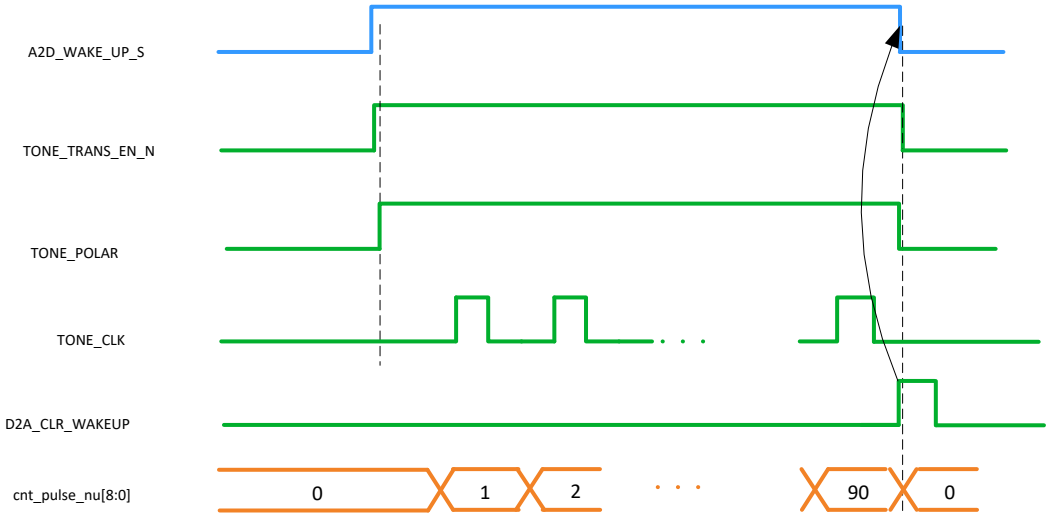

Figure3 receive A2D_WAKE_UP_S