

Version control

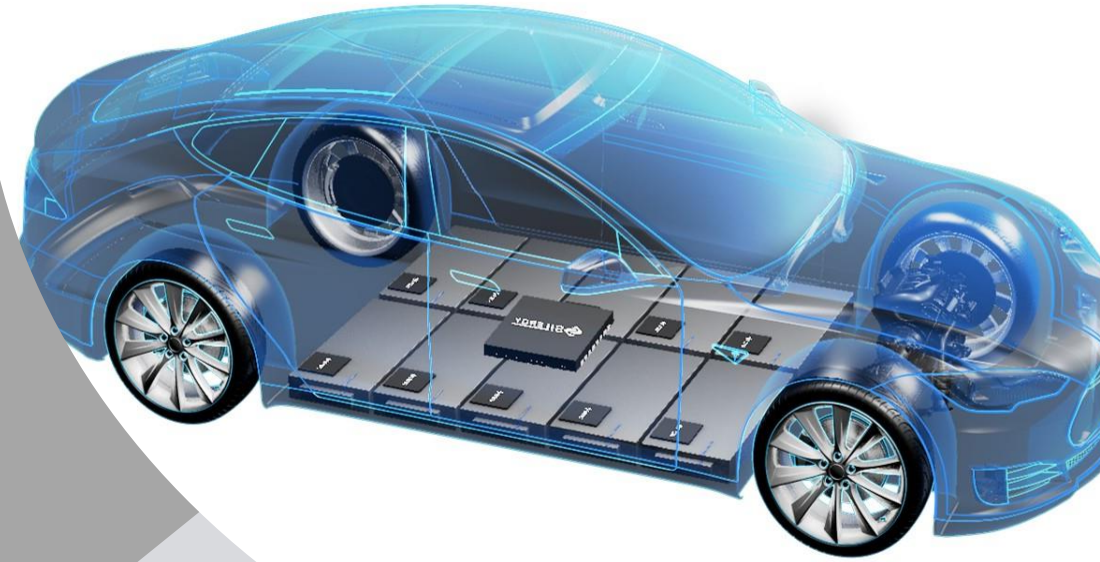
Version	Change note	Who	Date
1.0	Initial release	S.H	6/10/2023



HV Battery Monitoring Solution for ESS/EV

Battery-BMS

June/2023



Overview

- Silergy introduction
- Silergy automotive footprint
- HV BMS AFE for automotive and ESS
 - Silergy BMS overview
 - Roadmap and devices introduction
 - Validation progress
 - Customer design progress
 - Customer A surge test on battery module
 - Customer B surge & comm line AC injection
 - Customer C balancing channel large negative pulse
 - Customer D full EMC test on production grade 400V board

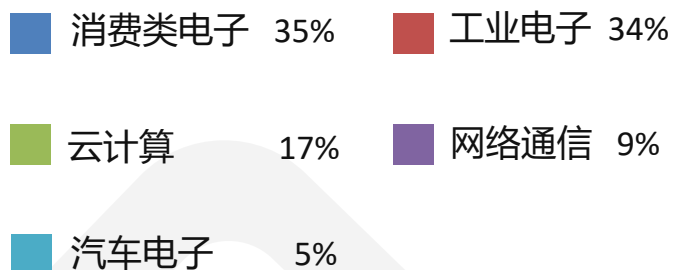
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公司概况



2022 营收:



员工总数: 1,500名, 研发1080名



主营产品:

直流转换, 交直流转换, 多路电源管理, 电池管理系统, LED照明, LED背光, 快充, 无线充电, 保护开关, 静电/浪涌保护, 电机驱动, 电表计量, 电池计量芯片, 放大器, 光传感器, 射频, 时钟和计时等。



全球专利授权总数: 1615项

业绩快速增长

2021年营收: 52亿人民币, 2022年营收: 55亿人民币。



Analog & Embedded Products

模拟电源产品 Analog Power Products
直流转换 DC/DC
交直流转换 AC/DC
保护开关&低压差线性稳压器 Protection Switch&LDO
多通道电源管理芯片 PMIC
电源模块 Power Module
电池管理 Battery
马达驱动 Motor Driver
LED驱动 LED Driver
数字电源 Digital Power
以太网供电 PoE

模拟信号链 Analog Signal Chain
放大器 Amplifiers
数据转换 Data Converters
时钟&计时 Clock & Timing
BMS 模拟前端 BMS AFE
音频 Audio
胎压监测 TPMS
传感器 Sensors
接口 Interface

嵌入式处理芯片 Embedded Processing
电表计量 Metering
微处理器 MCUs
蓝牙组网/射频 BLE Mesh/RF/SAR

广泛的终端应用



战略部署：电信通信能源，汽车电子，AI智能交互，服务器

矽力杰核心竞争力

国际化团队

来自世界各地的多元化技术领导团队，专注于提供创新、勤奋执行和快速响应的最佳组合，为客户提供最优质的模拟芯片解决方案及最佳的技术支持。

IDM模式

领先的技术

立足于创新的IDM平台模式

- ◆ 自主专利的半导体工艺器件技术和封装技术
- ◆ 超过1615项专利授权，414项申请中专利

致力于开发业界领先的产品

- ◆ 小型化
- ◆ 高效率
- ◆ 智能化

12寸晶圆生产制造基地 实现产能自主可控

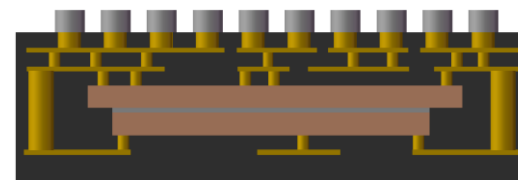
- 公司名称: 杭州富芯半导体
- 总投资额: ~540亿人民币
- 生产工艺: 12寸/90~55nm
- 月产能: 4-5万片 (一期)
- 投产时间: 2022年10月



国家大基金二期投资项目, 定位先进工艺节点, 高端模拟IC

先进封装制程工厂

- 公司名称: 合肥矽迈微电子
- 总投资额: ~8000万美金
- 建筑面积: ~90,000m²
- 主要产品
 - 电源模块
 - 特殊工艺及高功率密度产品
 - 汽车类产品



Global Presence



Overview

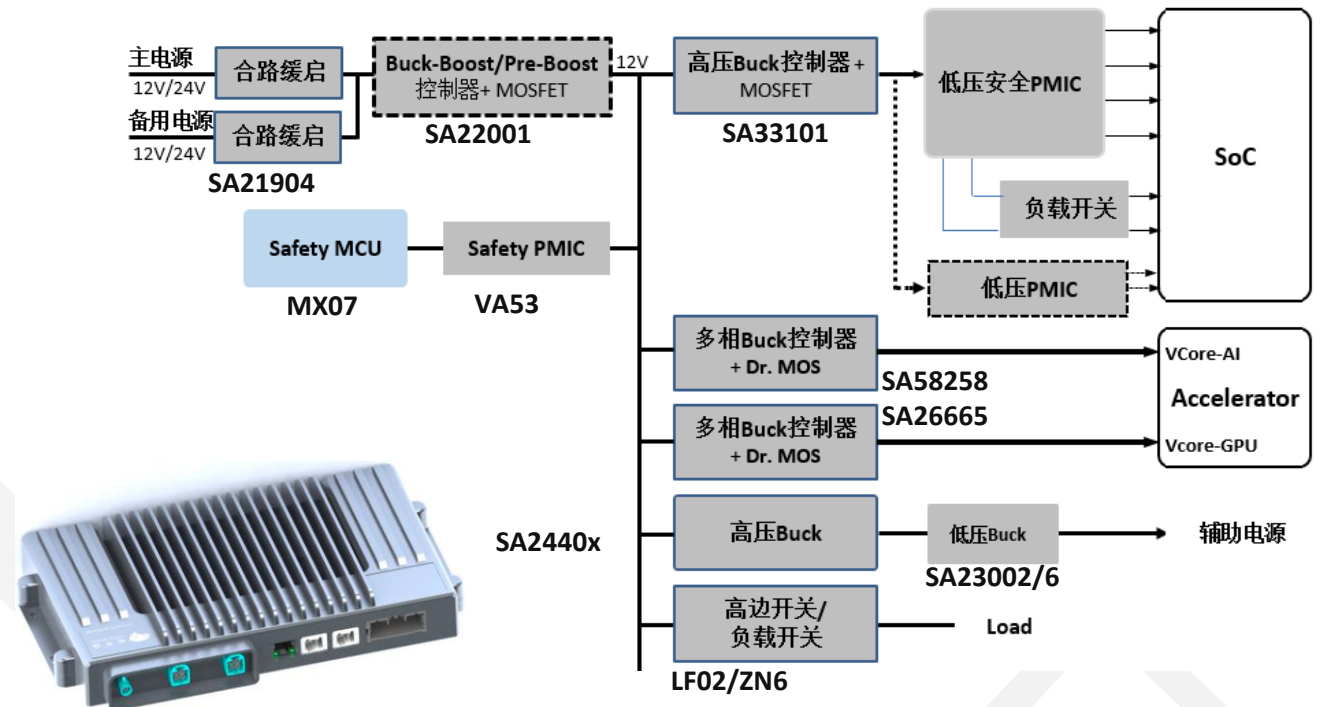
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自动驾驶(辅助)电源系统方案

自动驾驶(辅助)系统接收外部传感器的环境数据，进行处理决策规划，并通过执行机构实现对车辆的自动驾驶或驾驶辅助，是新一代智能网联汽车的核心部件。矽力杰重点布局开发完整电源解决方案。

矽力杰器件：

- SA21904: 合路缓启控制器(在研, MP Q4 2023)
- SA22001: Buck-Boost控制器OL25(在研, MP Q4 2023)
- SA33101: Buck控制器(在研, MP Q2 2023),
- SA58258: 8路多相控制 (在研, MP Q4 2023)
- SA26665: 大电流DR MOS(在研, MP Q3 2023)
- 低压安全PMIC (定义中, MP Q1 2024)
- 低压核供电PMIC (定义中, MP Q1 2024)
- VA53: 安全MCU配套安全PMIC (在研, MP Q4 2023)
- MX07: 安全MCU (定义中)
- 电源、接口保护器件 (量产中)
- 高边驱动LF0x, 负载开关ZN66(在研, MP Q2 2023)

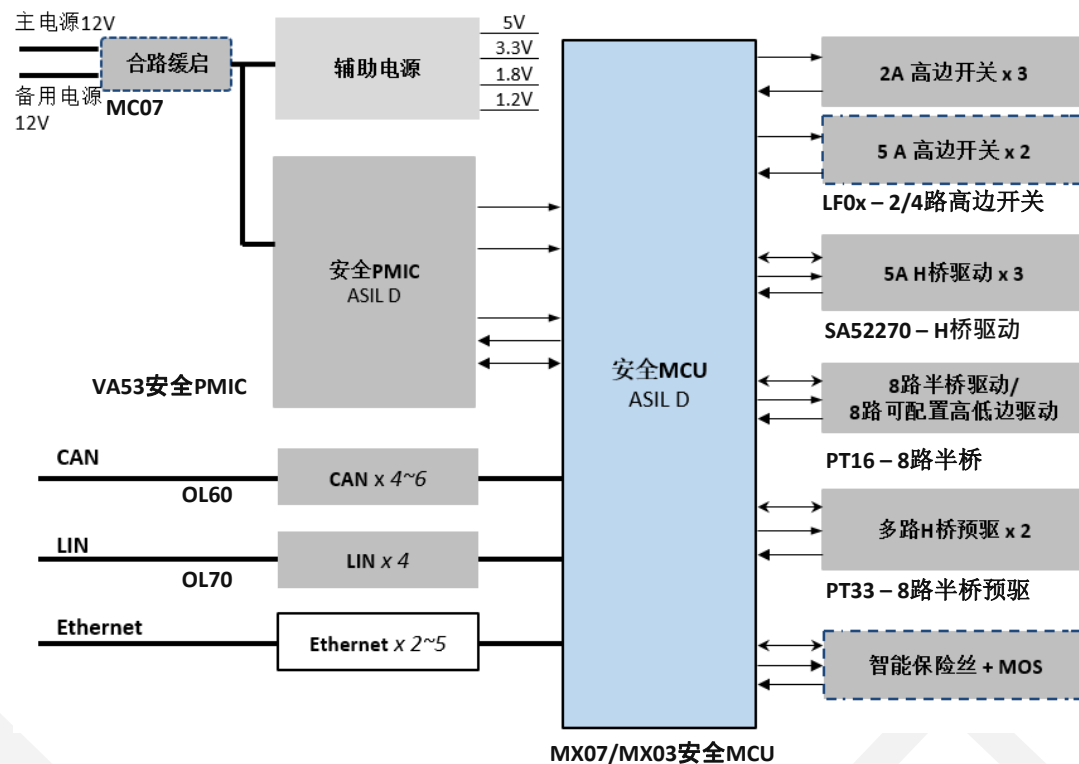
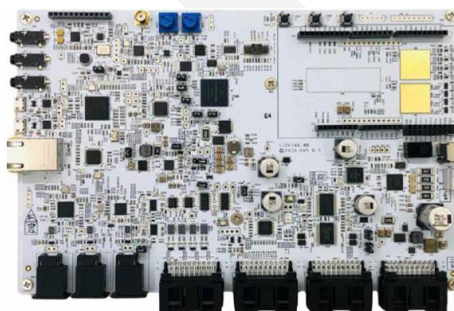


车身/接口区域控制器方案

车身/接口区域控制器用于车身或本区域内通讯连接、数据处理、逻辑控制、设备驱动、电源分配，是新一代智能网联汽车的核心部件。矽力杰重点布局开发完整系统解决方案。

矽力杰器件：

- SA21803: 高边驱动 (在研, MP Q2 2023)
- SA52270: H桥驱动 (在研, MP Q2 2023)
- PT16: 8路半桥驱动 (在研, MP Q2 2023)
- PT33: 8路半桥预驱 (在研, MP Q4 2023)
- 可配置高低边、智能保险丝 (定义中)
- 安全MCU MX03(样品中, MP Q4 2023)
- VA53: 安全PMIC (在研, MP Q4 2023)
- OL60: 通讯接口芯片 (在研, MP Q4 2023)
- 电源、接口保护器件 (量产中)

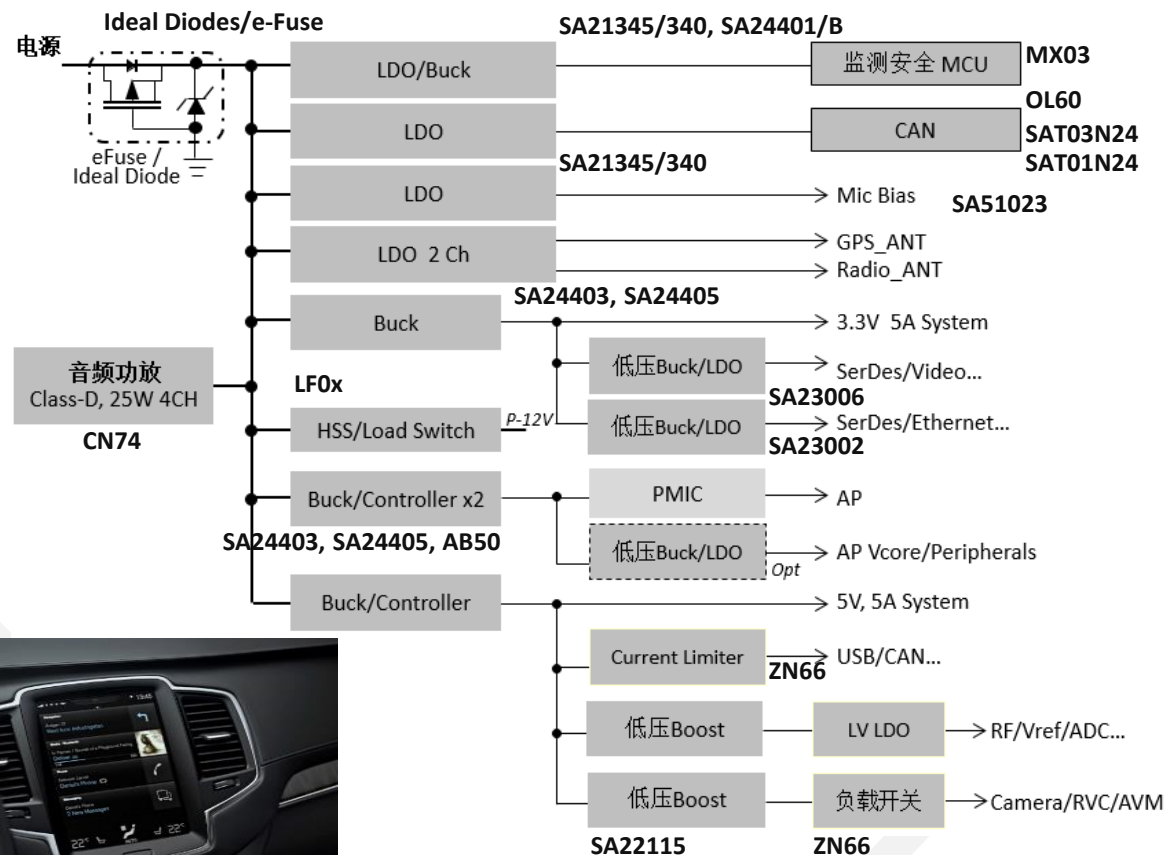


信息娱乐系统/智能座舱系统方案

信息娱乐系统/智能座舱提供信息娱乐、网络连接、智能交互(与人/HMI, 路/V2X, 车/IVN)、感知(环境/AVM, DVR, 乘员/DMS, OMS, IMS)等功能, 是汽车从交通工具向“第三生活空间”演进的重要纽带和关键节点。矽力杰已有完整量产系统解决方案。

矽力杰器件：

- SA21345系列: 高压LDO (量产中)
- SA24401/3: 高压Buck (量产中)
- SA22115: 1.2V~25V, 15A Sync. Boost (量产中)
- SA23002/6: 低压Buck (样品中, MP Q1 2023)
- CN74: 4通道 40W Class-D 音频功放(开发中)
- SA51023: 高共模抑制比音频运放 (量产中)
- SA21803: 高边驱动 (在研, MP Q2 2023)
- 低压安全PMIC (定义中, MP Q2 2024)
- SAT03N24/SAT01N24: LIN/CAN ESD器件 (量产中)
- SA32B16GEF: 安全MCU MX03(样品中 MP Q3 2023)

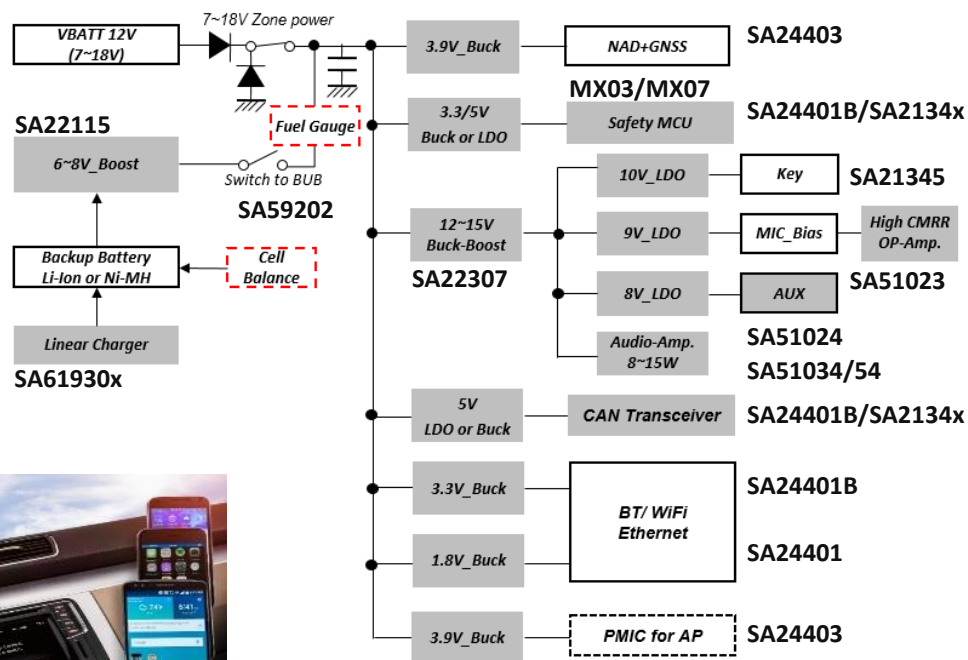


远程通讯单元T-Box系统方案

车身/接口区域控制器是车辆连接外部网络的入口，实现网络接入, 车辆诊断控制, 安全网关以及 OTA, eCall等基本功能，目前正融合5G, V2X, 高精度定位/P-Box, SOA智能网关,向域控制方向发展。矽力杰已有完整量产系统解决方案。

矽力杰器件：

- SA21345系列：高压LDO (量产中)
- SA24401/3: 高压Buck (量产中)
- SA22115: 1.2V~25V, 15A Sync. Boost (量产中)
- SA22307: 24W Buck-Boost Converter (量产中)
- SA61930: 500mA LDO + Linear Charger (量产中)
- SA59202: 电量计Fuel Gauge (量产中)
- SA51023: 高共模抑制比音频运放 (量产中)
- SA51024: 10W Class-D 音频功放(量产中)
- SA51034/54: 8/20W Class-D音频功放(量产中)
- SAT03N24/SAT01N24: LIN/CAN ESD器件 (量产中)



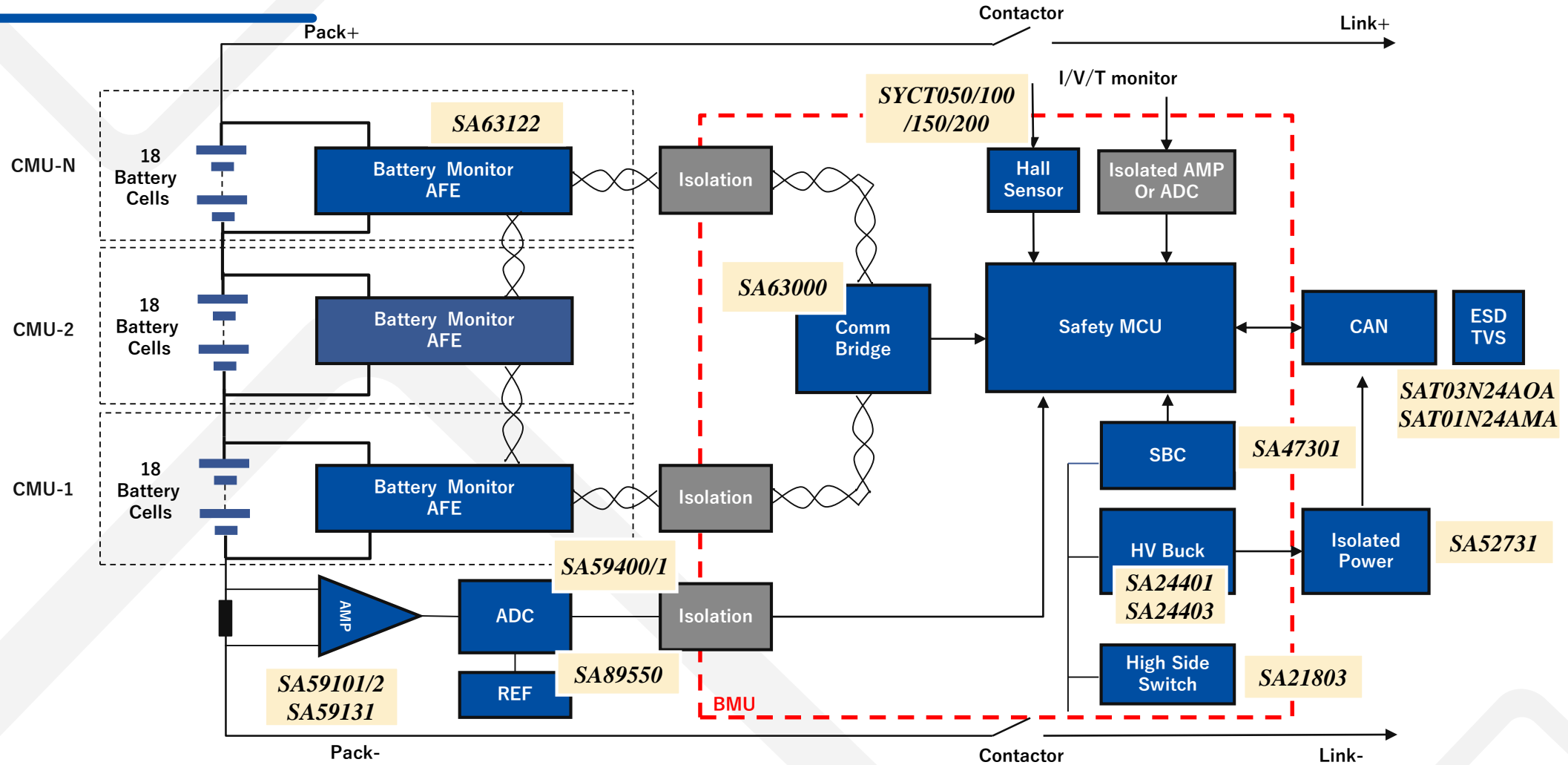
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Team introduction

	AFE团队介绍
IP风险	全球专利授权总数: 1453项(截止2021/10) BMS相关 – 38 项
工艺现状	BCD 0.15um (AFE)
AFE研发团队	40+人
核心研发	SVP高级副总: 17Y in auto BMS, high performance AFE (formerly TI) 20+ 车规产品 BU经理: 16Y in auto BMS, AFE, Gauge, Charger (formerly TI) 4 车规AFE产品/5 工业AFE产品 产品线经理: 10Y in BMS/auto AFE definition, IC design development (formerly TI) 10+ 车规产品 设计总监: 13Y in High performance analog/ADC/BMS/Gauge (Silergy) 10+ 车规产品 功能安全经理: 13Y in auto, BMS, AFE (formerly ADI) 2 车规AFE产品/13+ 车规产品 设计经理: 10Y in ADC, high speed analog, BMS, AFE (formerly TI) 5 车规产品 设计经理: 10Y in High performance analog, auto BMS, AFE, Charger (Silergy) 5 车规产品 系统构架师: 15Y IC develop. 7Y in auto BMS, AFE, (formerly Maxim, TI) 8 车规AFE产品 系统应用经理: 10Y IC develop, 4Y in auto BMS, AFE, 4 车规 AFE
核心工艺	公司CEO: 23Y in Power Device, BCD various platforms (formerly Volterra) 器件总监: 25Y in BCD various platforms (formerly TI) 器件资深经理/设计总监: 30Y in BCD various platforms (formerly LTC) 器件经理: 15Y in BCD various platforms (Silergy)
晶圆	Vanguard, 中芯, UMC, 和舰, TSMC, GTA(积塔)
封测	JCET, HTKJ, TFME(Fujitsu), SCCJ
质量管控	QMS –IATF16949 Certificate; Samsung Eco-partner certificate, Sony-GP certificate 累计Auto IC出货量: 55Mpcs; FIT < 1PPM
量产产品	量产类型有: DCDC/ACDC/PIMC/Power/Charger/Platform/Energy Measurement/Electricity Metering/Power Module
车规产品	已量产汽车级产品多达30+pcs, 并已上车或验证中 具有车规经验和资质
AFE研发现状	工业级AFE 2022年Q2量产, 对标TI-BQ769X0 汽车级AFE 2020年底开始, 目前样片 ready; 对标 TI79718/ADBMS6830/MAX17853

High voltage BMS system solution



Silergy offers one-stop solution for 12-1500V BMS for EV/ESS

Battery monitor roadmap

Developing Definition Concept **Fusa**

Bridge	SA63000 Fusa SPI, 12V Supply Reverse Wakeup TSSOP-16	BMCANFD Fusa 12V Supply, SPI, CAN FD Reverse Wakeup
LV Cell Monitor	SA63564 4S, current sense, HS Driver, SPI QFP7x7-48 SQ68766 16S, +/-3mV accuracy, w/CS, SPI QFP10x10-64	BM48V Fusa 16S, +/-3mV, HS/Pre Driver, CS 48pin
Pack Monitor	BMBJB 8CH Voltage, 2CH NTC, 2CH CS QFP7x7-48	
HV Monitor (stackable)	SA63122 Fusa 18S, +/-3mV accuracy, 12 GPIOs QFP10x10-64 SQ68118 18S, +/-3mV accuracy, 12 GPIOs QFP10x10-64	SA63224 Auto Fusa 24S, +/- 2mV accuracy 100 pin QFP SQ68218 18S, +/-3mV accuracy, 18 GPIOs QFP10x10-64
	BMSPEC Fusa Measure battery impedance	

Sample/ SOP timeline

	SA63122/ SQ68118	SA63000/ SQ63000
Engineering sample	Now	Now
Final sample	Aug/2023	Aug/2023
SOP	4Q2023	4Q2023

Note:

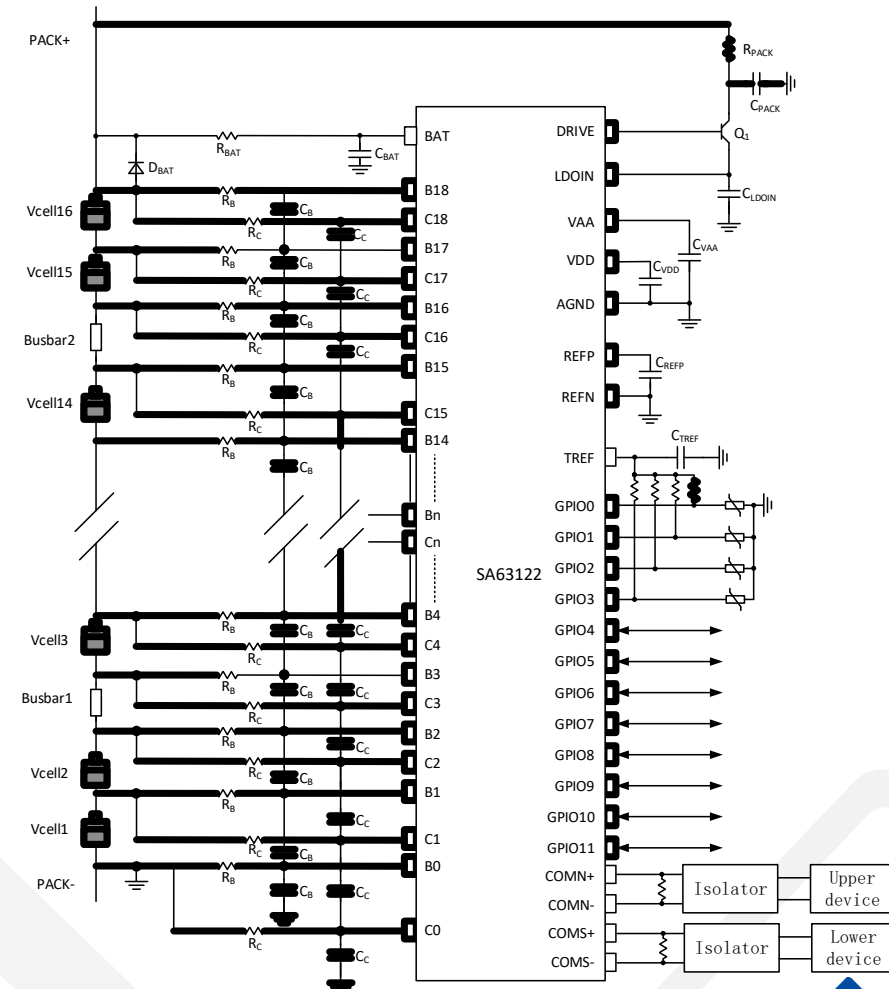
- SA is for automotive
- SQ is for ESS

SA63122 / SQ68118

Features

- Operating voltage range: 9V to 100V
- 18 channels for battery cell voltage measurements
 - Typical $\pm 1\text{mV}$ accuracy (1.5V to 4.5V, $+25^\circ\text{C}$)
 - **$\pm 3\text{mV}$ accuracy (1.5V to 4.5V, -20°C to $+65^\circ\text{C}$)**
 - $\pm 5\text{mV}$ accuracy (-2V to 5V, -40°C to $+125^\circ\text{C}$)
- 12 digital GPIO channels for analog input measurements :
 - $\pm 5\text{mV}$ (0.5V to 4.5V, -40°C to $+125^\circ\text{C}$) for absolute meas.
 - $\pm 0.2\%$ (10% to 90% V_{TREF} , -20°C to $+65^\circ\text{C}$) for ratio meas.
 - $\pm 0.48\%$ (0% to 100% V_{TREF} , -40°C to $+125^\circ\text{C}$) for ratio meas.
- Digital GPIOs supports I²C protocol
- Die temperature senses, accuracy: $\pm 2^\circ\text{C}$ typical, $\pm 5^\circ\text{C}$ max
- Integrated balancing FET, up to 300mA per channel
 - PWM control mode available for cell balancing during SLEEP mode to adjust balancing current online
 - Offline balancing when MCU in sleep
- Reverse wake up on OVUV/OTUT fault when MCU in sleep
 - 18 OV/UV alerts and 12 OT/UT alerts
- 2Mbps Ring Daisy-chain communication
- AEC-Q100 Grade 1
- Support ISO 26262 system design up to ASIL-D
- Package QFP10x10-64pin

Typical Application Diagram

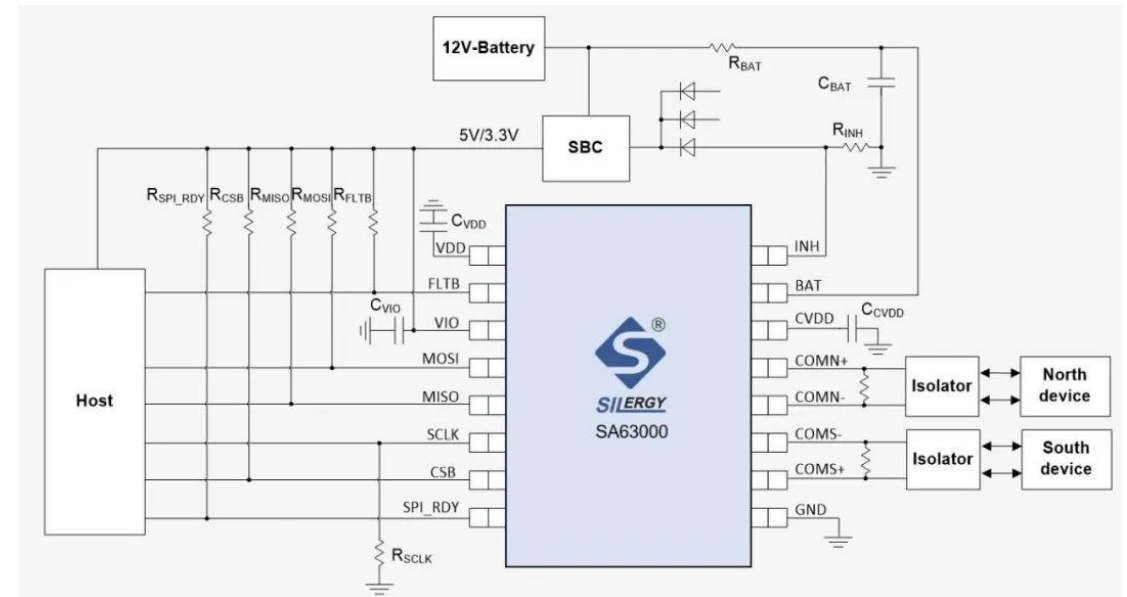


SA63000

Features

- Operating voltage ranges from 4.75V to 24V
 - 2 operation mode: Sleep/Active
 - Reversely waking up host in sleep mode
 - 5uA Current consumption in sleep mode
 - SPI host interface
 - Compatible with 3.3V or 5V logic
 - 2Mbps Ring Daisy-chain communication
 - Safety ISO 26262 ASIL-D capability in Active mode and ASIL-B capability in Sleep mode
 - AEC-Q100 qualified
 - TSSOP-16
-
- Support 12V battery input
 - Withstand 12V load dump
 - Wake up PMIC and Host in Sleep mode
 - One bridge device and one SPI IF to form RING architecture

Typical Application Diagram



Competitor Summary

Features	79616	17853	33771	BM20
Channel	16Cells, 8 GPIOs	14Cells, 6GPIOs	18Cells, 12 GPIOs	18Cells, 12 GPIOs
Busbar Channel	1 BB channel and 2 cell channels	Any channel except bottom	Flexible Bus-bar strategy	Any channel except bottom
Daisy Chain	Diff. UART and Standalone UART Ring(one Bridge IC), 16Bits CRC ±20V common mode range	Diff. UART and Multiplexed SPI No Ring, 8Bits CRC ±25V common mode range	Diff. SPI and Multiplexed SPI Ring(two Bridge ICs), 8Bits CRC -6V to 9V common mode range	Diff. UART and Standalone SPI Ring(one Bridge ICs), 16Bits CRC ±20V common mode range
ADC	Bipolar Continuous&Single Conversion	Bipolar Single Conversion	Unipolar Single Conversion	Bipolar Continuous & Single Conversion
Post Digital LPF	6.5 to 600Hz	Programmable IIR(50 to 120Hz)	Accuracy level up! Partial advantage	Configurable for Cells
Cell Accuracy	±2mV@2V to 4.5V,-20C to 65C ±3mV@-1V to 5V,-40C to 105C ±5mV@-2V to 5V,-40C to 105C	±0.45mV@3.6V,25C ±4.5mV@-2.3V to 2.3V,-40C to 125C ±4.5mV@0.2V to 4.8V,-40C to 125C	±4.5mV@1.5 to 4.5V,-40 to 105C	±1mV @1.5V to 4.5V, +25C ±3mV@1.5V to 4.5V, -20C to +65C ±5mV@-0.3V to 5V, -40C to +125C
GPIO Accuracy	Ratio- ±0.24%@-40C to 125C Absolute- ±3mV@-40C to 125C	Ratio- ±2.5mV@-40C to 125C Absolute- ±3.5mV@-40C to 125C	Ratio-max 16mV@-40C to 125C Absolute- ±11mV@0 to 4.85V,-40C to 125C	Ratio- ±0.2%@-20C to 65C Absolute- ±5mV@-20C to 65C
Time Skew on Cn vs. Bn	Zero	4479us	Not Supported	FuSa Advantage → Zero
Cn to Cn-1 Rating	-80V to +80V	-72V to +72V	-0.3V to 6V	n=1, -6V to +40V;n=2 to 6, -40V to +40V; n=7,-40V to +80V; n=8 to 12, -80V to +80V; n=13, -80V to +100V; n=14 to 18, -100V to +100V
Bn to Bn-1 Rating	-0.3V to 16V	-0.3V to 16V	-0.3V to 10V	-0.3V to 24V
Balancing	240mA, Even/Odd, max 4ohm	300mA, Even/Odd, max 2.5ohm	300mA, All On, typical 0.5ohm, PWM	300mA, Even/Odd, max 4.5ohm, PWM
Balancing Termination	VCB, Manual, Timer, Fault, Thermal	Manual, Timer	Manual, Timer, UV	Manual, Timer, Fault, Thermal
Secondary Protector	OV/UV/OT/UT HW Integrated	Not available at Sleep mode	Periodical wakeup to do measurement	OV/UV/OT/UT HW Integrated, Cyclic
Reverse Wakeup	Supported	Not Supported	Not Supported	Supported
FDTI performance	Sampling and Diagnosis in Parallel Transaction-8 regs write/128 regs read One Broadcast READ to get all data	Sampling and Diagnosis in Series Transaction-1 reg write/1 reg read Multiple Broadcast READ to get all data	Sampling and Diagnosis in Series Transaction-1 regs write/128 regs read No Broadcast READ	Sampling and Diagnosis in Parallel Transaction-8 regs write/128 regs read One Broadcast READ to get all data
Package	HTQFP-64, 10mmx10mm	LQFP-64, 10mmx10mm	QFP-64, 10mmx10mm	TQFP-64, 10mmx10mm

More channels

FuSa Advantage

Robust hotplug/ESD

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Silicon Validation Summary

Test Item	Status	Note
BV	Done	PASS
Mode/Tone	Done	PASS
Power Supply and REF	Done	PASS
Communication	Done	PASS
ADC	Done	PASS
Cell Balance	Done	PASS
Reversely Wake Up	Done	PASS
GPIO	Done	PASS
SM	Done	PASS
Hot-Plug	Done	PASS
PIN FIT	Ongoing	85%
EMC/ESD	Done	PASS
Other (Reliability, FT Optimization)	Done	PASS

1st revision silicon is fully validated, final silicon is expected in early Aug.

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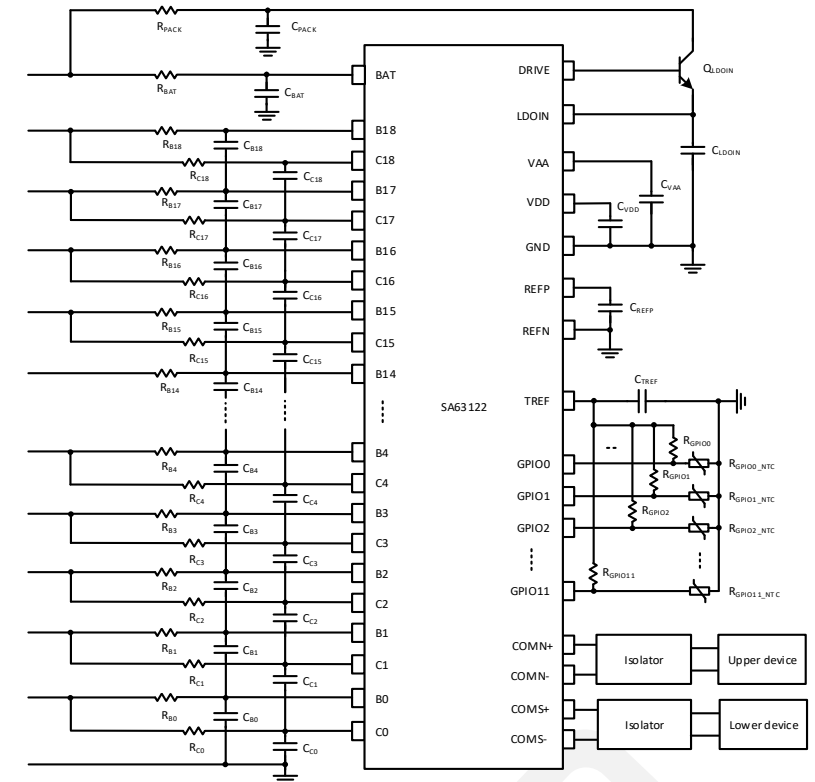
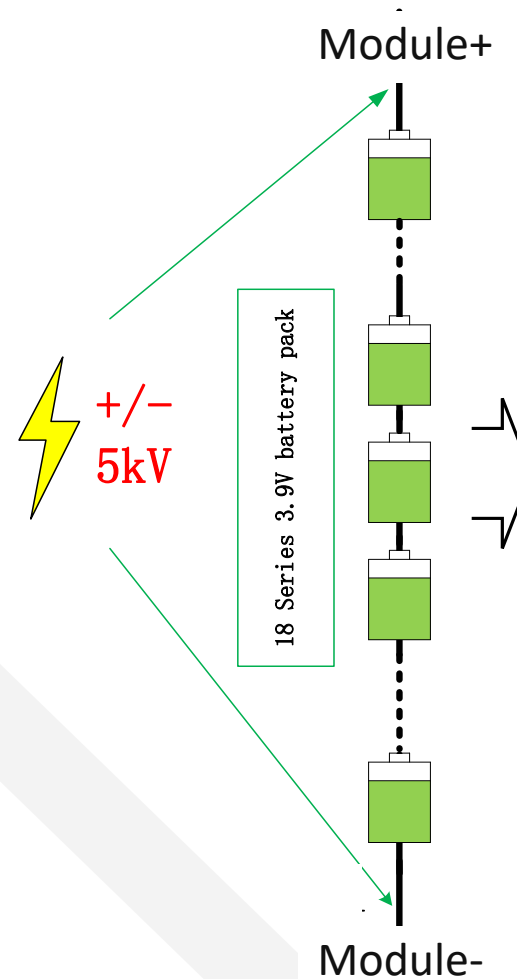
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Customer A | Surge Test setup

Set Up:

- CSU board is connected to a battery module with 18cells, 3.9V/Cell
- Surge test equipment is connected to the module +/- terminal

Positive surge	Negative surge
+1kV	-1kV
+2kV	-2kV
+3kV	-3kV
+4kV	-4kV
+5kV, 5 times	-5kV, 5 times



Customer A | Surge Test result

Before

	CELL	MAIN	AUX
▶	CH1	3.8664	3.8666
	CH2	3.8666	3.8666
	CH3	3.8698	3.8700
	CH4	3.8664	3.8666
	CH5	3.8690	3.8690
	CH6	3.8684	3.8686
	CH7	3.8682	3.8684
	CH8	3.8688	3.8690
	CH9	3.8696	3.8698
	CH10	3.8726	3.8728
	CH11	3.8730	3.8732
	CH12	3.8710	3.8714
	CH13	3.8730	3.8732
	CH14	3.8730	3.8730
	CH15	3.8730	3.8736
	CH16	3.8748	3.8752
	CH17	3.8772	3.8778
	CH18	3.8782	3.8788

After +5kV, 5times

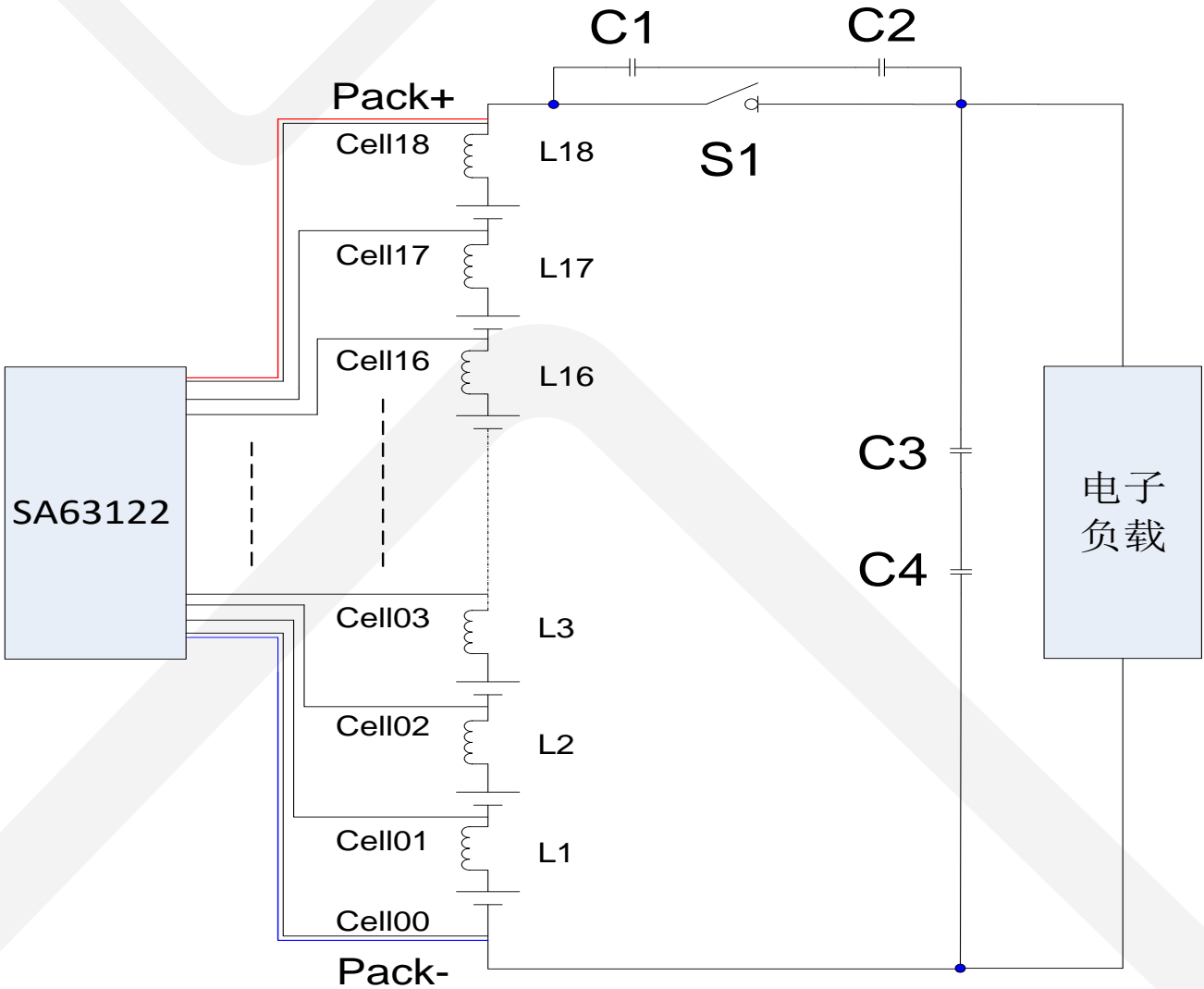
	CELL	MAIN	AUX
▶	CH1	3.8664	3.8668
	CH2	3.8668	3.8666
	CH3	3.8694	3.8696
	CH4	3.8666	3.8670
	CH5	3.8688	3.8690
	CH6	3.8686	3.8686
	CH7	3.8682	3.8686
	CH8	3.8688	3.8690
	CH9	3.8694	3.8696
	CH10	3.8728	3.8728
	CH11	3.8734	3.8736
	CH12	3.8710	3.8714
	CH13	3.8732	3.8734
	CH14	3.8728	3.8730
	CH15	3.8730	3.8734
	CH16	3.8750	3.8752
	CH17	3.8772	3.8776
	CH18	3.8786	3.8790

After +5kV, 5times

	CELL	MAIN	AUX
▶	CH1	3.8666	3.8670
	CH2	3.8668	3.8666
	CH3	3.8694	3.8696
	CH4	3.8666	3.8668
	CH5	3.8688	3.8690
	CH6	3.8686	3.8686
	CH7	3.8680	3.8686
	CH8	3.8688	3.8690
	CH9	3.8694	3.8698
	CH10	3.8726	3.8726
	CH11	3.8732	3.8734
	CH12	3.8712	3.8714
	CH13	3.8730	3.8732
	CH14	3.8728	3.8730
	CH15	3.8732	3.8736
	CH16	3.8748	3.8750
	CH17	3.8772	3.8778
	CH18	3.8788	3.8790

ADC reading sees no obvious difference before / after surge test. **PASS!**

Customer B | Surge Test - Schematic diagram



参数表

C1,C2,C3,C4	3.5uF/500V
L1,L2,L3...L16, L17,L18	470uH
S1	100A
电子负载	IT8514C (1200W)

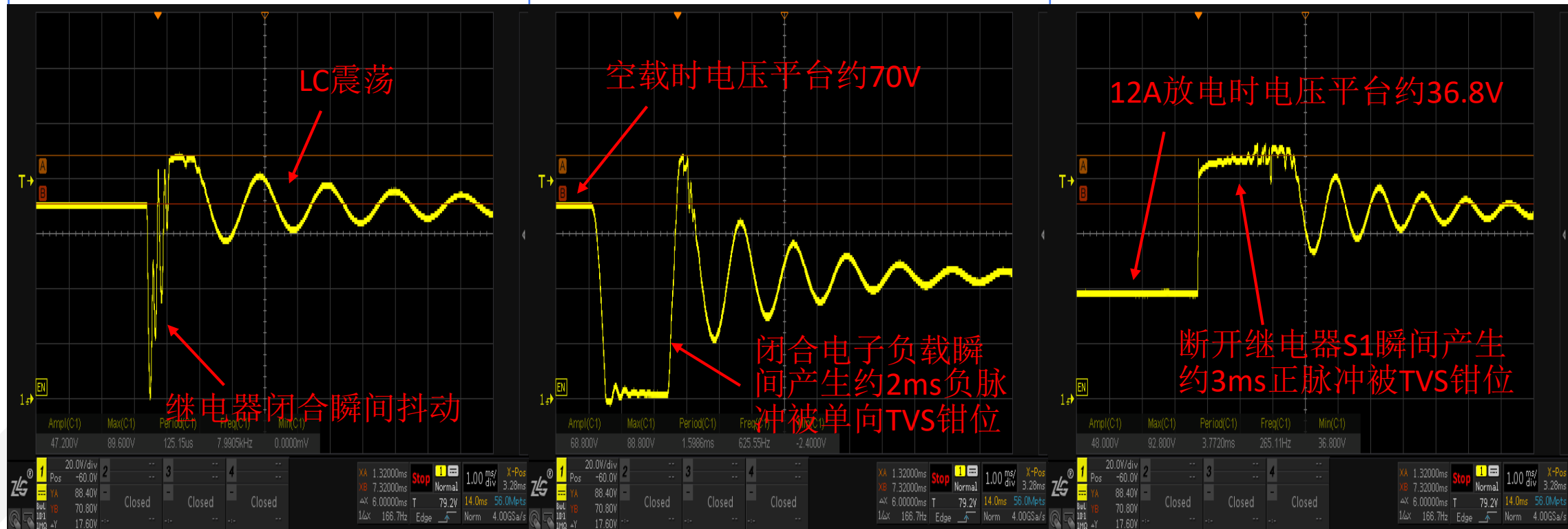
Step 1: 闭合继电器S1;
Step 2: 闭合电子负载;
Step 3: 断开继电器S1;

Customer B | Surge Test - 负载电流12A (Pack+引脚波形)

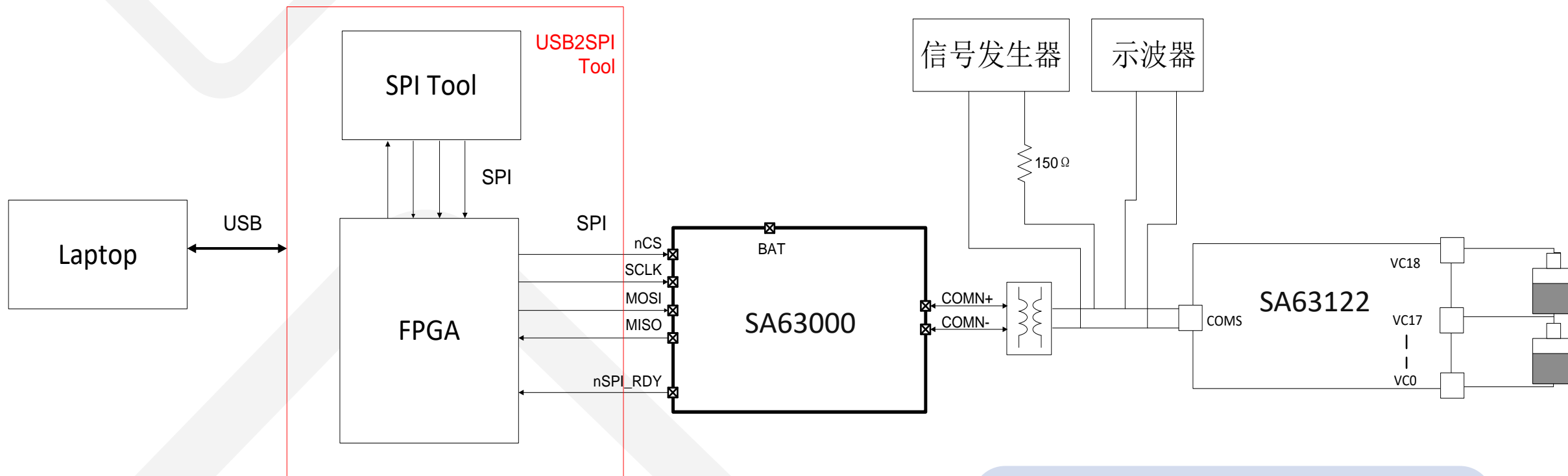
闭合继电器S1

闭合电子负载 (12A)

断开继电器S1



Customer B | AC injection - Schematic diagram



示波器	ZLGZDS1104
信号发生器	AFG31000

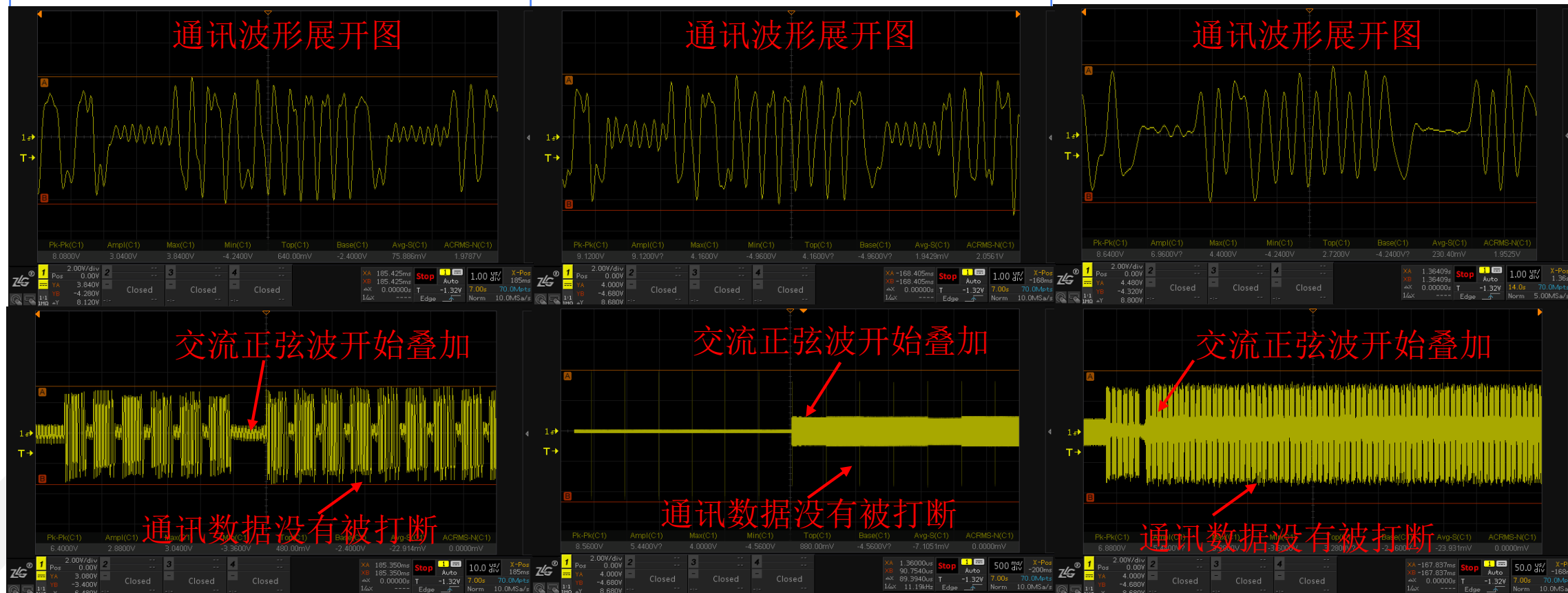
信号发生器输出阻抗 150Ω ，对通讯线进行正弦波形注入，观察波形畸变后通讯是否正常；

Customer B | AC injection – scope waforms

6M 2V 正弦波

5M 2V 正弦波

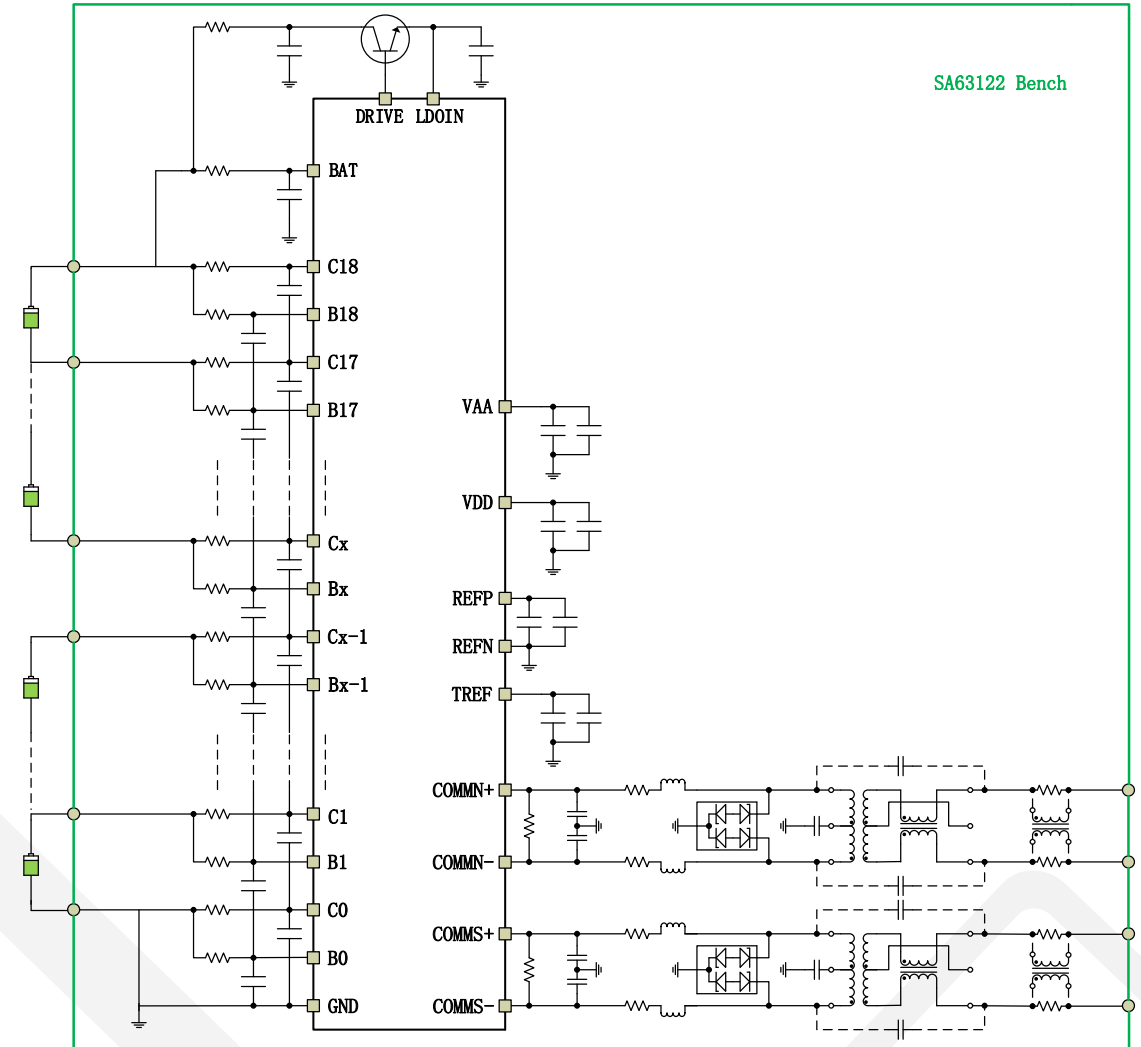
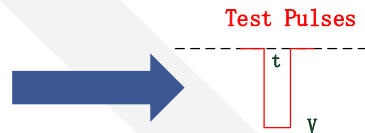
3.5M 2V 正弦波



Customer C | Negative voltage spike on Bn channels

- 3pcs
- Other channels connect voltage source.

V	t
-10V	10us
-10V	100us
-10V	1ms
-20V	10us
-20V	100us
-20V	1ms
-30V	10us
-30V	100us
-30V	1ms



Customer C | Negative voltage spike result (1)

Test Channel: CH2							
Chip ID		VF/V (B1-B2)	VF/V (B2-GND)	VF/V (B1-GND)	Cn ADC error@3.3V/mV	Bn ADC error@3.3V/mV	Conclusion
1#	Pre-test	0.658	0.608	0.622	0.7	0.8	Pass
	Post-test	0.659	0.616	0.62	0.6	0.7	
2#	Pre-test	0.646	0.596	0.611	0.6	0.7	Pass
	Post-test	0.653	0.604	0.617	0.9	0.8	
3#	Pre-test	0.639	0.591	0.603	0.9	1	Pass
	Post-test	0.656	0.607	0.62	0.7	0.9	

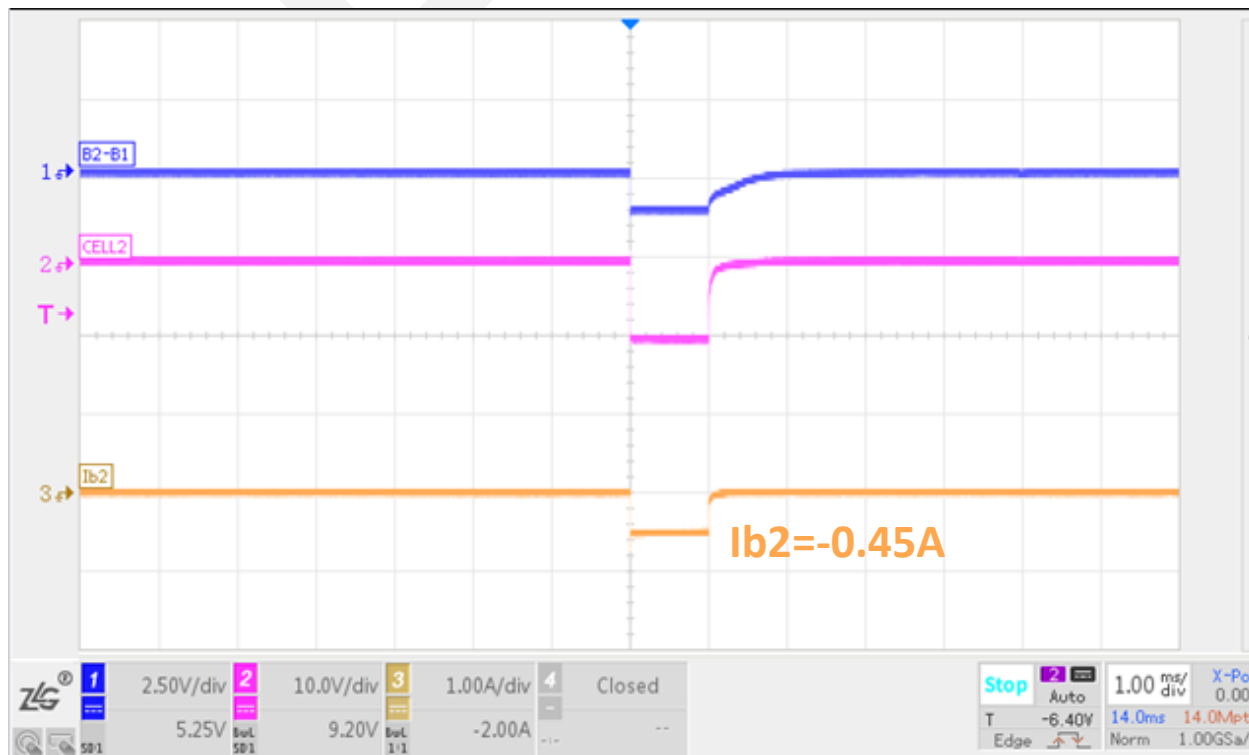
Test Channel: CH9							
Chip ID		VF/V (B8-B9)	VF/V (B9-GND)	VF/V (B8-GND)	Cn ADC error@3.3V/mV	Bn ADC error@3.3V/mV	Conclusion
1#	Pre-test	0.661	0.633	0.608	0.5	0.6	Pass
	Post-test	0.662	0.635	0.606	0.4	0.7	
2#	Pre-test	0.651	0.615	0.597	0.6	0.8	Pass
	Post-test	0.656	0.62	0.603	0.7	0.8	
3#	Pre-test	0.646	0.609	0.592	0.7	0.4	Pass
	Post-test	0.659	0.622	0.605	0.6	0.6	

Select two channels to force negative voltage pulses. Record the ESD forward voltage and ADC error pre/post the test.

No obvious difference on ESD and cell voltage accuracy.

Customer C | Negative voltage spike result (2)

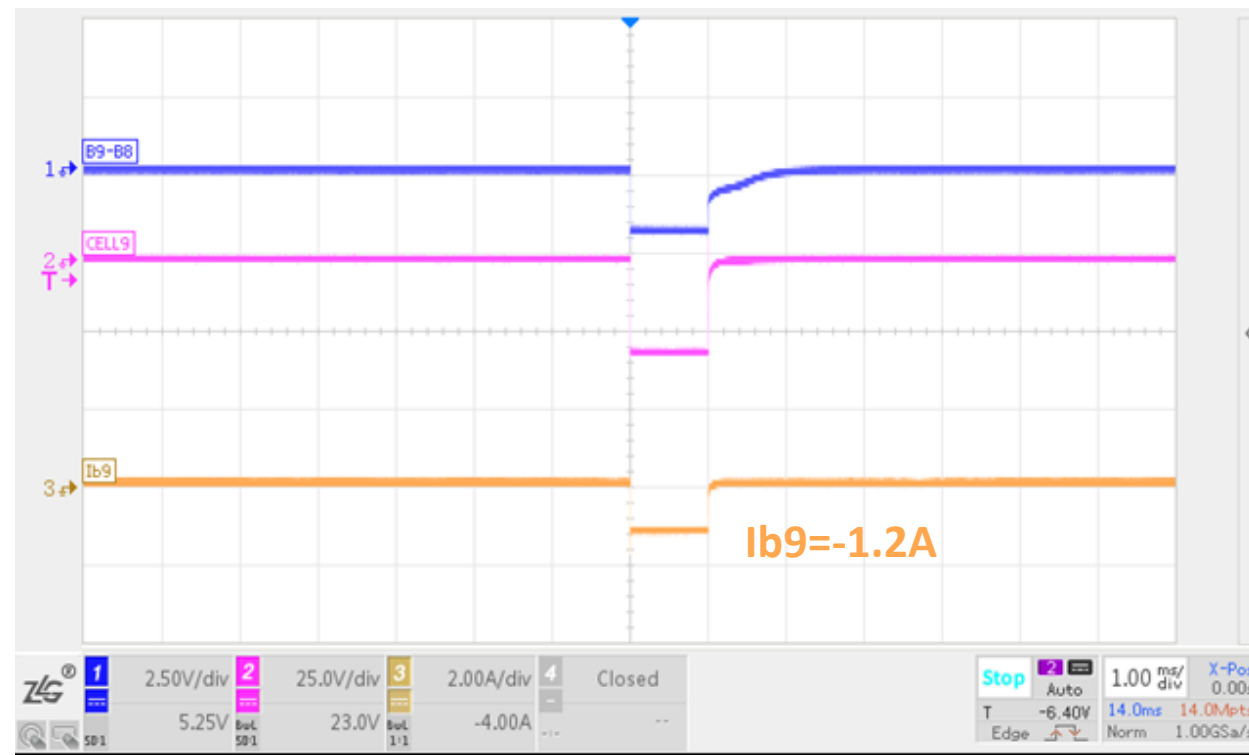
Waveform 1 : -10V, 1ms pulse on CH2



CH1:V(B2-B1) CH2: V(CELL2-CELL1) CH3:Ib2

Note: The resistance of Rb on the bench is 10ohm.

Waveform 2 : -30V, 1ms pulse on CH9



CH1:V(B9-B8) CH2: V(CELL9-CELL8) CH3:Ib9

Customer C | Negative voltage spike result (3)

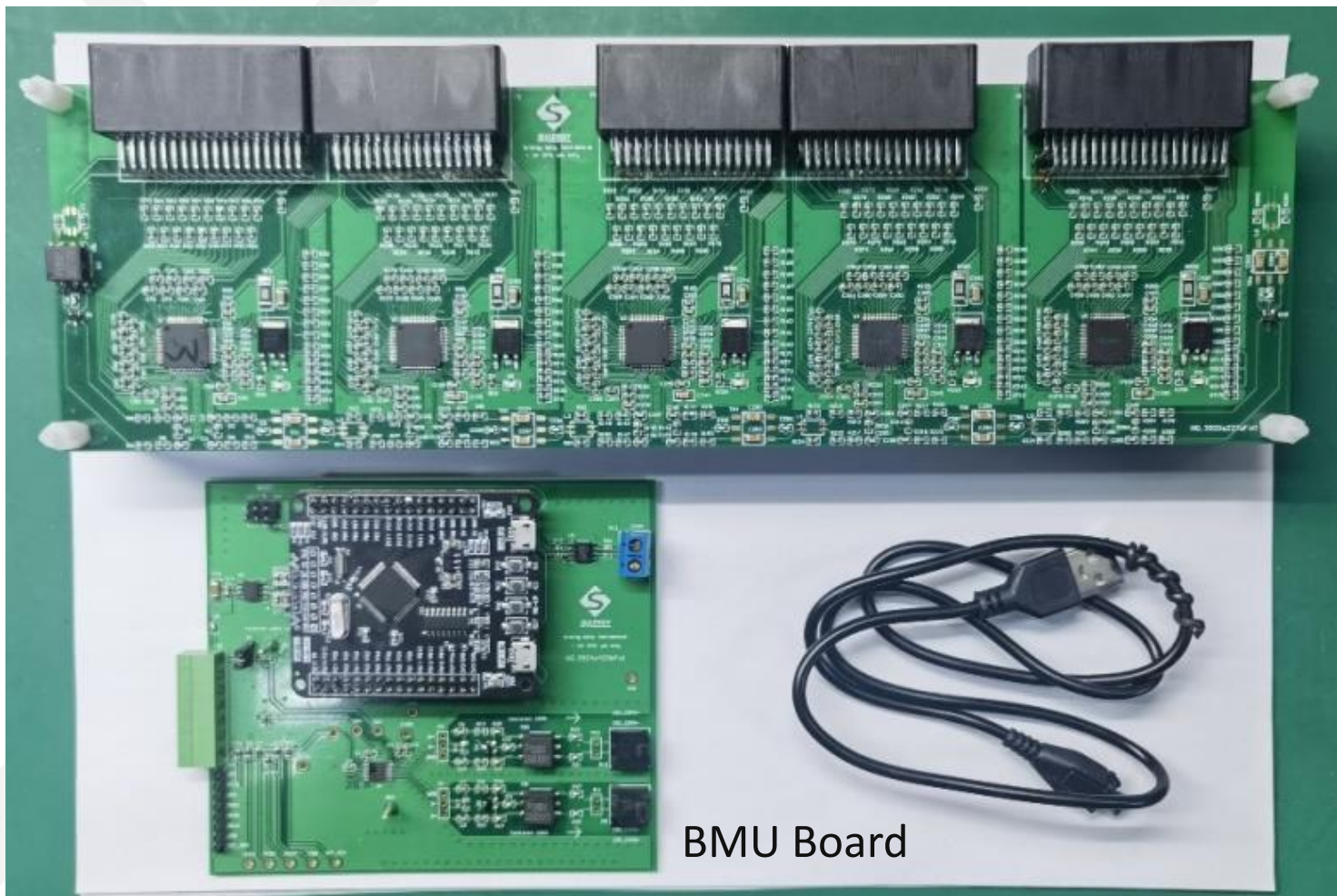
Test condition: Every single channel forces 4.5V.

CHIP ID		leakage_vc2	leakage_vc3	leakage_vc9	leakage_vc10	leakage_vb2	leakage_vb3	leakage_vb9	leakage_vb10	Conclusion
		uA	uA	uA	uA	uA	uA	uA	uA	
		-1	-1	-1	-1	-1	-1	-1	-1	
		1	1	1	1	1	1	1	1	
1#	Pre	-0.0107	-0.0063	-0.0534	-0.0073	0.018	0.019	-0.0294	-0.0091	PASS
	Post	0.0075	-0.012	-0.0275	-0.0226	0.0343	0.0557	-0.0106	-0.0288	
	Post-125C/48h bake	0.005	0.0072	-0.0266	-0.0157	-0.0065	-0.0018	0.0132	0.0109	
2#	Pre	0.0122	-0.0188	0.0011	0.0058	0.0232	0.0368	-0.038	-0.0274	PASS
	Post	-0.0199	-0.018	-0.0559	-0.0391	0.0169	0.0233	-0.0236	-0.013	
	Post-125C/48h bake	-0.0086	-0.0125	-0.0516	-0.0493	0.0214	0.0399	0.005	-0.0061	
3#	Pre	-0.0107	-0.0118	-0.035	-0.0279	0.0254	0.0414	-0.02	-0.0151	PASS
	Post	-0.0032	-0.0012	-0.033	-0.0341	0.0029	-0.0057	-0.0169	-0.0007	
	Post-125C/48h bake	-0.0012	-0.0202	-0.0323	-0.0304	0.0232	0.0357	0.0049	-0.0174	

No obvious change in leakage current, all devices pass -30V spike.

Customer D | production grade 400V board

5 in1 CMU Board for real car application



BMU Board

Form1

SPI_storage

COM: COM7 ☒ COM_OPEN

Write_Data: Send

Stack Number: 5

WAKE: SD: ADDRESS: ADC CONTI: ADC SINGL: COMM CLEAR:

DLFF: ☐ 0 ☐ 1 ☒ 2 ☐ 3 ☐ 4 ☐ 5

Excel Action Path: D:\data.xlsx

NEW: CLOSE:

Read_Data: 47 05 40 00 42 AB 42 A6 42 8E 42 8E 42 99 42 92 42 A6 42 95 42 98 42 A6 42 8C 42 92 42 A3 42 8F 42 90 42 9B 42 97 42 6A 42 AB 42 A4 42 90 42 8D 42 99 42 92 42 A7 42 96 42 99 42 A7 42 8C 42 93 42 A4 42 91 42 92 42 9B 42 98 42 8D 3E 7B 47 04 40 00 42 A3 42 9D 42 93 42 9B 42 A2 42 96 42 95 42 9E 42 9A 42 95 42 A3 42 9C 42 9D 42 AB 42 9E 42 9E 42 92 42 9F 42 A4 42 9C 42 9A 42 9C 42 9B 42 9D 42 9B 42 9D 42 9B

CRC: 第1行CRC正确 第2行CRC正确 第3行CRC正确 第4行CRC正确 第5行CRC正确

Reset:

Excel Chosen: ☐ 1st ☐ 2nd ☐ 3rd ☐ 4th ☒ 5th ☐ All

Time Set: ms

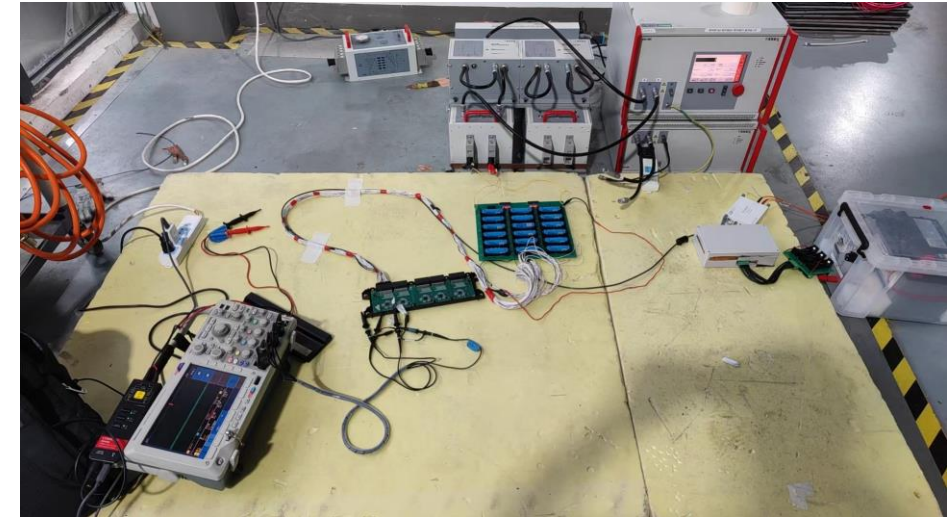
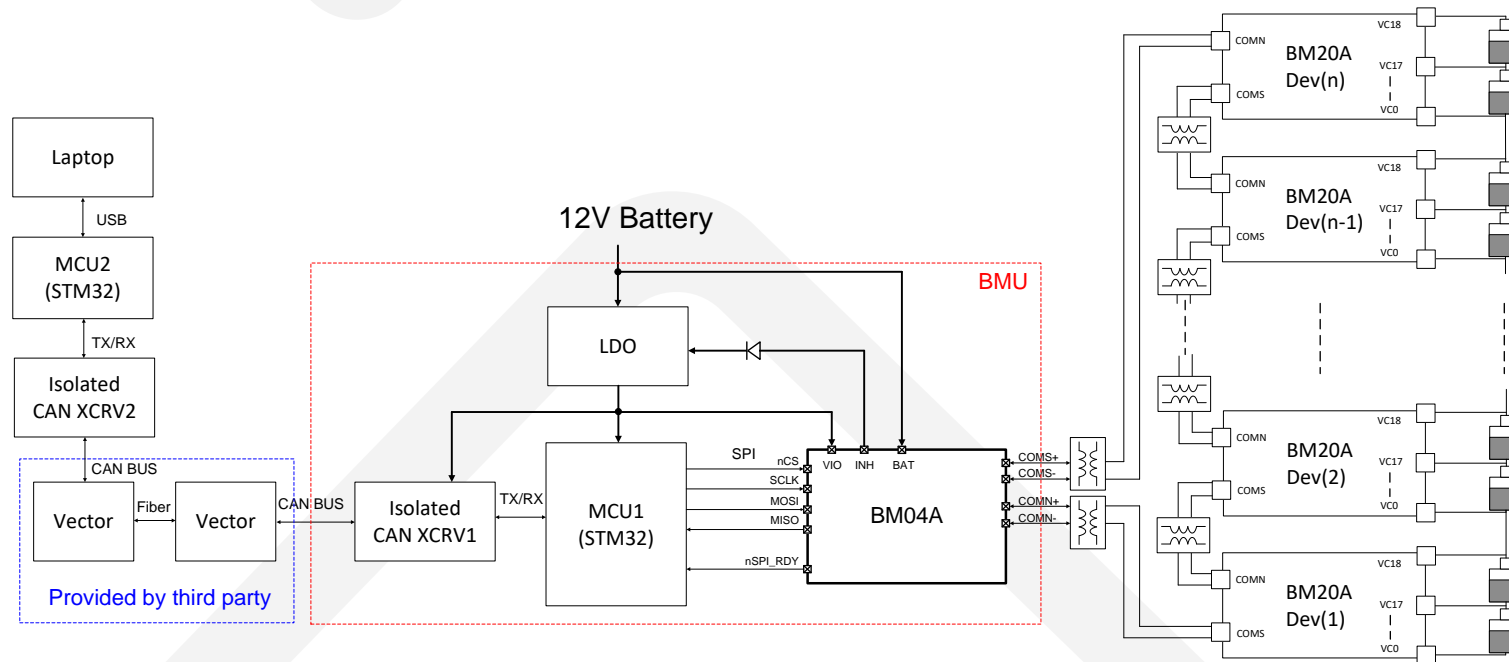
Start: Stop:

电池节数	Main电压	AUX电压
电池1	3.4120	3.4122
电池2	3.4136	3.4136
电池3	3.4116	3.4118
电池4	3.4102	3.4102
电池5	3.4132	3.4132
电池6	3.4092	3.4092
电池7	3.4128	3.4140
电池8	3.4098	3.4112
电池9	3.4096	3.4100
电池10	3.4142	3.4144
电池11	3.4104	3.4108
电池12	3.4108	3.4108
电池13	3.4116	3.4116
电池14	3.4124	3.4128
电池15	3.4122	3.4122
电池16	3.4132	3.4132
电池17	3.4142	3.4146
电池18	3.4102	3.4110

EMC Testing GUI

Test setup HW and SW

Customer D | EMC test setup



Customer D | EMC test result

测试项	测试结果	Note
传导发射电压法CE-AN，测试方法参考CISPR 25：2016标准，要求FM频段满足至少Class 4等级，其他频段至少满足Class 3等级	PASS	通过
传导发射电流法CE-CP，测试方法参考CISPR 25：2016标准，要求FM频段满足至少Class 4等级，其他频段至少满足Class 3等级	PASS	通过
辐射发射ALSE法，测试方法参考CISPR 25：2016标准，要求FM频段满足至少Class 4等级，其他频段至少满足Class 3等级	PASS	通过
大电流注入抗扰BCI，测试方法参考ISO 11452-4：2011标准(200mA)，要求功能等级A	PASS	ADC结果跳动小于10mV
辐射抗扰RI，测试方法参考ISO 11452-2：2004标准，要求至少Level 2达到功能等级A	PASS	ADC结果跳动小于10mV
低频磁场抗扰MFI，测试方法参考ISO 11452-8：2015标准，要求至少Level IV达到功能等级A	PASS	ADC结果跳动小于10mV
浪涌(冲击)抗扰，测试方法参考GBT17626.5：2008标准，要求功能等级C	PASS	无损坏
手持发射机，测试方法参考ISO 11452-9：2012标准，要求Level 2功能等级B，Level 1功能等级A	PASS	ADC结果跳动小于10mV

Customer D | 3rd party test house info



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