# CMP\_BIST\_CTRL

## **REVISION HISTORY**

Revision Number	Date	Description of Change	Author
V0.0	11/2/2022	Draft version	Shaoqiang

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## CMP\_BIST\_CTRL

#### Introduction

CMP\_BIST\_CTRL is mainly used for functional safety to check whether VAA\_OVUV, VDD\_OVUV\_BIST, CP\_OVUV, AGND\_OW fault can be generated correctly.

#### **Main features**

The CMP\_BIST\_CTRL module has the following features:

- •Supports output 400us BIST\_REF\_EN high pulse and 200us BIST\_REF\_EN\_EARLY high pulse when BIST\_GO is detected (HWSR2\_CMP\_BIST\_CTRL)
- •CMP\_BIST\_CTRL shall be reset when CLK\_32M\_OK is low (HWSR1\_CMP\_BIST\_CTRL)
  Supports output clr\_BIST\_GO after BIST\_GO is detected (HWSR3\_CMP\_BIST\_CTRL)
- Before BIST\_REF\_EN\_EARLY turns low, CMP\_BIST\_CTRL shall check if VAA\_OVUV, VDD\_OVUV\_BIST, CP\_OVUV, AGND\_OW are all 1 within 50us, if any is 0, output CMP\_FLT (HWSR4\_CMP\_BIST\_CTRL)

## **Functional Details**

### **Block Diagram**

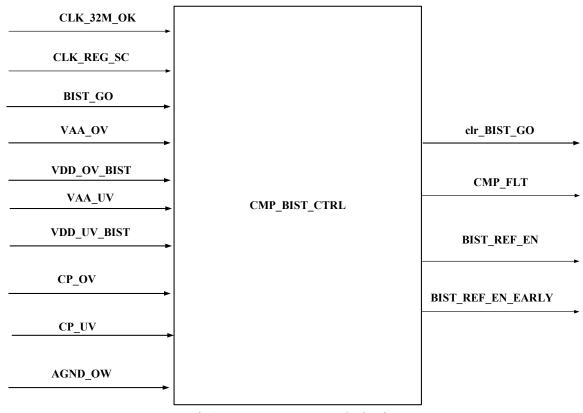


Fig 1 CMP\_BIST\_CTRL Block Diagram

#### I/O description

Table 1 CMP\_BIST\_CTRL I/O description

Pin Name	Direction	Duration	Width	Description
BIST_GO	I	N/A	1b'	To start CMP_BIST_CTRL
VAA_OV	I	N/A	1b'	VAA_OV fault
VAA_UV	I	N/A	1b'	VAA_UV fault
CP_OV	I	N/A	1b'	CP_OV fault
CP_UV	I	N/A	1b'	CP_UV fault
AGND_OW	I	N/A	1b'	AGND_OW fault
VDD_OV_BIST	I	N/A	1b'	VDD_OV_BIST fault
VDD_UV_BIST	I	N/A	1b'	VDD_UV_BIST fault
CLK_32M_OK	I	N/A	1b'	CMP_BIST_CTRL shall be reset when CLK_32M_OK is low
CLK_REG_SC	I	N/A	1b'	Clock for CMP_BIST_CTRL
resetb_SR_CLK_REG	I	N/A	1b'	Reset signal
clr_BIST_GO	O	1	1b'	To clear BIST_GO

		CLK_REG_SC		
CMP_FLT	О	1 CLK_REG_SC	1b'	Detect CMP_BIST fault
BIST_REF_EN	О	400 us	1b'	Output 400us BIST_REF_EN high pulse
BIST_REF_EN_EARLY	О	200us	1b'	Output 200us BIST_REF_EN_EARLY high pulse

**Fault detect** 

(HWSR1\_CMP\_BIST\_CTRL, HWSR2\_CMP\_BIST\_CTRL, HWSR3\_CMP\_BIST\_CTRL, HWSR4\_CMP\_BIST\_CTRL)

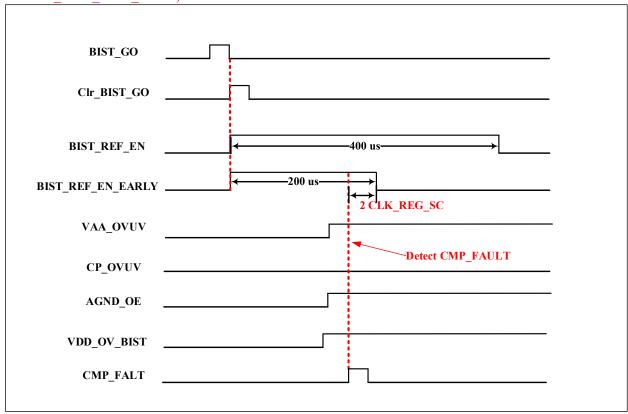


Fig 2 Waveform diagram of CMP\_BIST\_CTRL

When CB\_GO arrives, CMP\_BIST\_CTRL outputs 400ns BIST\_REF\_EN and 200ns BIST\_REF\_EN\_EARLY. At the two CLK\_REG\_SC cycles before BIST\_REF\_EN\_EARLY disappears, CMP\_BIST\_CTRL will detect all faults. If any FAULT is 0, CMP\_FALUT will be generated, indicating that FALULT cannot be generated correctly for the module.