Test Case of Technical Requirement

WP as Prerequisites	Author of TC of TR
TR_v0.47	Shuo Xu

ITEM	TR ID	TC ID	TC Description	Method	Configuration	Pass/Fail Criteria	Priority	Owner
Operation Mode	TR002, TR003, TR004, TR007	TC1_000	From SD to ACT with WAKE tone at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone	Check S1 after B0 generate WAKE tone: WAKE_TONE_DET shall generate H pulse SEQ shall output ACT H, DRSTB H VDD shall build CLK shall build TONE_CTRL shall generate WAKE tone COMN port shall output WAKE tone Other communication related signals act correctly	1	CJ
			From SD to ACT with WAKE tone at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to WAKE tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	Deng block
			From SD to ACT with WAKE tone at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to WAKE tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	Deng block
			From SD to ACT with WAKE tone from north port at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone from north port	Check S1 after B0 generate WAKE tone: WAKE_TONE_DET shall generate H pulse SEQ shall output ACT H, DRSTB H VDD shall build CLK shall build TONE_CTRL shall generate WAKE tone COMN port shall output WAKE tone Other communication related signals act correctly	1	CJ
			From SLEEP to ACT with STA tone at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate TO_SLEEP CMD B0 generate STA tone	Check S1 after B0 generate STA tone: STA_TONE_DET shall generate H pulse SEQ shall output ACT H CLK_32M shall build TONE_CTRL shall generate STA tone COMN port shall output STA tone Other communication related signals act correctly	1	CJ
			From SLEEP to ACT with STA tone at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to STA tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	Deng block

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			From SLEEP to ACT with STA tone at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to STA tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	Deng block
			From SLEEP to ACT with STA tone from north port at 25℃	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	CJ
	TR002, TR003, TR005, TR008	TC1_001	From ACT to SD with SD tone at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate SD tone	Check S1 after B0 generate SD tone: SD_TONE_DET shall generate H pulse SEQ shall output SDB L, DRSTB L VDD shall fall CLK shall fall Other communication related signals act correctly	1	CJ
			From ACT to SD with SD tone at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to SD tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	Deng block
			From ACT to SD with SD tone at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to SD tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	Deng block
			From ACT to SD with TO_SD CMD at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate TO_SD CMD	Check S1 after B0 generate TO_SD CMD: Digital Core shall generate TO_SD CMD to COMN COMN port shall output TO_SD CMD Digital Core shall generate D2A_TO_SD H SEQ shall output SDB L, DRSTB L VDD shall fall CLK shall fall	1	CL
			From ACT to SD with SD tone from north port at 25℃	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	CJ
			From SLEEP to SD with SD tone at 25℃	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	2	CJ
			From SLEEP to SD with SD tone at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to SD tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	Deng block

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			From SLEEP to SD with SD tone at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to SD tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	Deng block
			From SLEEP to SD with SD tone from north port at 25℃	SIM&RT		Check if TONE_DET,SEQ, PS, CLK output correctly including timing	3	CJ
	TR002, TR003, TR006, TR009	TC1_002	From ACT to SLEEP with TO_SLEEP CMD at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate TO_SLEEP CMD	Check S1 after B0 generate TO_SLEEP CMD: Digital Core shall generate TO_SLEEP CMD to COMN COMN port shall output TO_SLEEP CMD SEQ shall output SLEEP H CLK_32M shall fall Other communication related signals act correctly	1	CL
	TR010, TR011, TR012	TC1_003	From ACT to DRST with WAKE tone at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate 2nd WAKE tone	Check S1 after B0 generate 2nd WAKE tone: WAKE_TONE_DET shall generate H pulse SEQ shall output DRSTB L pulse Digital Core shall be hard-reset Other communication related signals act correctly	1	CL
			From ACT to DRST with WAKE tone at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to WAKE tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	CL
			From ACT to DRST with WAKE tone at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to WAKE tone	SIM&RT		Check if TONE_DET,SEQ, PS, CLK, TONE_CTRL, COMM output correctly including timing	3	CL
			From ACT to DRST with SRST CMD at 25℃	SIM&RT	B0 is chained to S1 with C Both B0 and S1 are initially in SD mode BAT=60V for S1 B0 generate WAKE tone B0 generate SRST CMD	Check S1 after B0 generate SRST CMD: Digital Core shall be self-soft-reset Other communication related signals act correctly	1	Qing

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Communication	TR037, TR038, TR040, TR041	TC2_002	Addressing of S1, S2 and S3 from north port at 25℃	SIM&RT	B0 is chained to S1, S2, S3 with C All B0, S1, S2, S3 are initially in SD mode BAT=60V for S1, S2, S3 B0 generate WAKE tone from north port B0 generate ADDR CMD with 0x01 as ADDR	Check after B0 generate ADDR CMD: TOP_DEV, DIR_SEL, DEV_ADD, ADD_W_EN, DEV_NUM of S1, S2, S3 shall change with ADDR CMD RESPs received by B0 from S1, S2, S3 shall be RESP with 0x01, 0x02, 0x03 respectively Other communication related signals act correctly	1	CJ
	TR030, TR033, TR034, TR035, TR036	TC2_000	Single Read DEV_ADD of S1 among B0, S1 and S2 at 25℃	SIM&RT		Check if COMM output correctly	2	Qing
			Stack Read 18*VCELL of B0, S1 and S2 at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	1	CJ
			Single Write CB_GO of S2 among B0, S1 and S2 at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	2	Qing
	TR031, TR032	TC2_001	Stack Write ADC_GO of B0, S1 and S2 with typical 2.2nF capacitors at 25℃	SIM&RT		Check if COMM output correctly	1	CJ
			Stack Write ADC_GO of B0, S1 and S2 with typical 2.2nF capacitors at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	3	CJ
			Stack Write ADC_GO of B0, S1 and S2 with typical 2.2nF capacitors at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	3	CJ
			Stack Write ADC_GO of B0, S1 and S2 with min 150uH max 1.4mH and isolated by 2m communication cable transformer at 25℃	SIM&RT		Check if COMM output correctly	1	CJ
			Stack Write ADC_GO of B0, S1 and S2 with min 150uH max 1.4mH transformer and isolated by 2m communication cable at -40℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	3	CJ

ITEM	TR ID	TC ID	TC Description	Method	Configuration	Pass/Fail Criteria	Priority	Owner
			Stack Write ADC_GO of B0, S1 and S2 with min 150uH max 1.4mH transformer and isolated by 2m communication cable at 125℃ Add noise w.r.t 50% magnitude and 10% occurrence to CMD	SIM&RT		Check if COMM output correctly	3	CJ
	TR039	TC2_003	Single Write MON_WAKE_GO of S2 among B0, S1 and S2 at 25℃ Add 100K-400M BCI noise to CMD	SIM&RT		Check if COMM output correctly	1	CJ
Reversely Wake Up	TR055, TR056, TR057, TR058, TR059, TR060, TR062, TR063, TR064, TR065	TC3_000	GPIO OT in sleep mode at 25℃	SIM&RT	B0 is chained to S1, S2 with C All B0, S1, S2 are initially in SD mode BAT=60V for B0, S1, S2 B0 generate WAKE tone from north port B0 generate ADDR CMD with 0x01 as ADDR B0 generate FLT_MSK CMD to mask other faults B0 generate MON_WAEK_GO CMD B0 generate TO_SLEEP CMD Force GPIO OT at S1	Check S1 after force GPIO OT at S1: MON_ADC_GO shall be high periodically GPIO_OTUT shall be high FLT_WAKE shall be high FLT_TONE is generated at COMN of S1 Check S2 after force GPIO OT at S1: FLT_TONE_DET shall be high FLT_WAKE shall be high FLT_TONE is generated at COMN of S2	1	Lei Nie
Bridge Interface	TR085, TR086, TR087, TR088, TR089, TR090, TR091, TR092, TR093, TR094, TR095, TR096, TR097, TR099, TR100, TR101, TR102, TR103	TC4_000	Other CELL UV when as bridge in sleep mode at 25℃	SIM&RT	Host connect to B0 with SPI B0 is chained to S1, S2 with C in ring architecture All B0, S1, S2 are initially in SD mode BAT=60V for B0, S1, S2 Host generate WAKE ping Host generate WAKE_TONE_GEN CMD Host generate ADDR CMD with 0x01 as ADDR Host generate FLT_MSK CMD to mask other faults Host generate MON_WAEK_GO CMD Host generate TO_SLEEP CMD Force CELL UV at S1	Check S1 after force CELL UV at S1: MON_ADC_GO shall be high periodically CELL_OVUV shall be high FLT_WAKE shall be high FLT_TONE is generated at COMN of S1 Check B0 after force CELL UV at S1: FLT_TONE_DET shall be high FLT_WAKE shall be high FLTB is asserted of B0	1	Wells Cheng

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		TC4_001	Bridge in active mode at 25℃	SIM&RT	Host connect to B0 with SPI B0 is chained to S1, S2 with C in ring architecture All B0, S1, S2 are initially in SD mode BAT=60V for B0, S1, S2 Host generate WAKE ping Host generate WAKE_TONE_GEN CMD Host generate ADDR CMD with 0x01 as ADDR Host generate STACK READ CMD with 0x00 as ADDR	Check B0 after host generate STACK READ CMD with 0x00 as ADDR: 3 RESPs shall be read by host	1	Wells Cheng
Measurement	TR018, TR019, TR020, TR021, TR022, TR023, TR024, TR025, TR026, TR027, TR028, TR029	TC5_000	Measurement accuracy at 25℃	SIM&RT	B0 is chained to S1 with C All B0, S1 are initially in SD mode BAT=60V for B0, S1 B0 generate WAKE tone Host generate ADC_CONTI_GO CMD	Check S1 after host generate ADC_CONTI_GO CMD: Cell measurement accuracy shall be 1mV for -2V, 3.3V, 5V GPIO measurement accuracy shall be 0.2%	1	Lei Nie
		TC5_001	Measurement accuracy at -40℃	SIM&RT	B0 is chained to S1 with C All B0, S1 are initially in SD mode BAT=60V for B0, S1 B0 generate WAKE tone Host generate ADC_SGLE_GO CMD	Check S1 after host generate ADC_SGLE_GO CMD: Cell measurement accuracy shall be 5mV for -2V, 3.3V, 5V GPIO measurement accuracy shall be 0.48%	1	Lei Nie
		TC5_002	Measurement accuracy at 125℃	SIM&RT	B0 is chained to S1 with C All B0, S1 are initially in SD mode BAT=60V for B0, S1 B0 generate WAKE tone Host generate ADC_CONTI_GO CMD Host generate FREEZE CMD	Check S1 after host generate FREEZE CMD: Cell measurement accuracy shall be 5mV for -2V, 3.3V, 5V GPIO measurement accuracy shall be 0.48% RR_COUNTER and ADC measurement result after DLPF shall be freezed	1	Lei Nie
Cell Balance								
Digital IO								
I2C Master								

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