

# TONE\_CTRL IP SPEC

## Table of Contents

Introduction .....	1
Feature .....	1
Register Definition .....	2
Register Map.....	2
Functional Details .....	错误!未定义书签。
Block Diagram .....	错误!未定义书签。

## Introduction

The TONE\_CTRL module is used to generate tones.

## Feature

Key features of the TONE\_CTRL module are:

- All functions are for both AFE and bridge application
- Generate WAKEUP TONE when received WAKE\_TONE\_DET or WAKE\_TONE\_GEN high.
- Generate STA TONE when received STA\_TONE\_DET or when STA\_TONE\_GEN high.
- Generate SD TONE on N port after SD\_TONE\_GEN high. Direction in TONE\_TRANS\_EN shall base on SPI\_DIR.
- Generate FLT TONE on N port every 50ms when SLEEP high and FLT\_WAKE high.
- Generate HB TONE on N port every 400ms when SLEEP high and FLT\_WAKE low.
- TONE transmitting and daisy chain transmitting are mutually exclusive.
- WAKE TONE and STA TONE shall have higher priority to HB TONE and FLT TONE.

## Register Definition

### Register Map

Table 1 1TONE\_CTRL Register Map

Name	Add	D7	D6	D5	D4	D3	D2	D1	D0	Default
CTRL1	0x2002	SOFT_RSTB	DIR_SEL		WAKE_TONE_GEN	STA_TONE_GEN	SD_TONE_GEN	TO_SD	TO_SLEEP	0x80
CTRL2	0x2003						CMP_BIST_GO	ADD_W_EN	SPI_DIR	0x00

## Functional Details

### Block Diagram

The following diagram shows the TONE\_CTRL architecture and internal modules and connections.

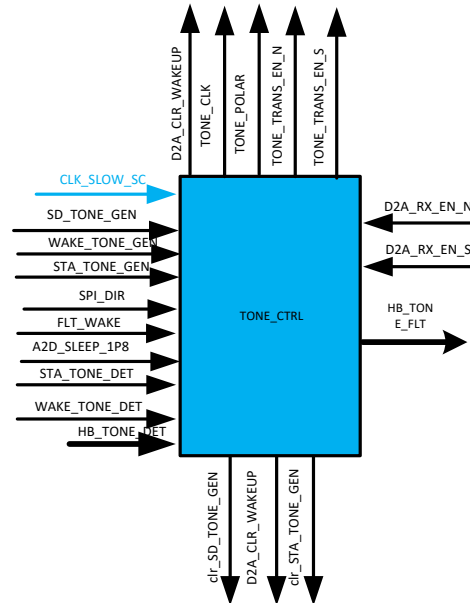


Figure 1 TONE\_CTRL diagram

### Module input/output list

Name	Dir	Width	Discription	duration
D2A_CLR_WAKEUP	O	1	Pulse for analog to clear A2D WAKE UP x	1 CLK_256K
clr_WAKE_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear WAKE TONE_GEN	1 CLK_256K
clr_STA_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear STA TONE_GEN	1 CLK_256K
pos_HBFSAT	O	1	HB too fast condition is detected	1 CLK_256K
pos_HBTO	O	1	HB too slow(timeout) condition is detected	1 CLK_256K
TONE_TRANS_EN_N	O	1	N port tone transmission enable	Level(CLK_OUT domain)
TONE_TRANS_EN_S	O	1	S port tone transmission enable	Level(CLK_OUT domain)
TONE_CLK	O	1	Tone clock	1 CLK_256K
TONE_POLAR	O	1	Tone polar(1: positive tone; 2: negative tone)	Level(CLK_256K domain)
rx_en_256K	O	1	Synchronoused rx_en_ds_or_spi by CLK_256K	Level(CLK_256K domain)
SLEEP_MODE	O	1	Synchronoused A2D_SLEEP_1P8 by CLK_256K	Level(CLK_256K domain)
SD_TONE_GEN_EN	O	1		
clr_SD_TONE_GEN	O	1	Pulse for module u_COMM_REG to clear SD TONE_GEN	1 CLK_256K

CLK_256K_SC	I	1	Scan-muxed CLK_256K	50% duty
resetb_CLK_256K	I	1	Asynchronous reset signal(synchronously released by CLK_256K)	Level(CLK_256K domain)
SOFT_RSTB	I	1	Soft reset	Level(CLK_SLOW domain)
CLK_OUT_SC	I	1	CLK_OUT after scan mux	
resetb_SR_CLK_OUT	I	1	Asynchronous reset signal (synchronously released by CLK_OUT) and SOFT_RSTB logic	Level(CLK_OUT domain)
A2D_WAKE_UP_N	I	1	Wake tone detected from N port	async
A2D_WAKE_UP_S	I	1	Wake tone detected from S port	async
A2D_STA_DET_N	I	1	STA tone detected from N port	async
A2D_STA_DET_S	I	1	STA tone detected from S port	async
HB_TONE_DET	I	1	Heart beat tone detected	async
D2A_RX_EN_S	I	1	enable daisy chain receiving on S port	Level(CLK_32M domain)
D2A_RX_EN_N	I	1	enable daisy chain receiving on N port	Level(CLK_32M domain)
WAKE_TONE_GEN	I	1	Register bit from u_COMM_REG to generate wake tone	Level(CLK_REG domain)
STA_TONE_GEN	I	1	Register bit from u_COMM_REG to generate sleep to active tone	Level(CLK_REG domain)
A2D_SLEEP_1P8	I	1	Sleep mode indication	async
SD_TONE_GEN	I	1	Register bit from u_COMM_REG to generate shut down tone	Level(CLK_REG domain)
SPI_EN	I	1	Enable SPI	Async
SPI_DIR	I	1	"1" for north interface, "0" for south interface	Level(CLK_REG domain)
SPI_RX_EN	I	1	Indicate RX_DATA_SPI is update	1 CLK_REG
rx_en	I	1	daisy chain signal is being received	Level(CLK_32M domain)
tx_en_32M	I	1		
state_rx_init	I	1	state is STATE_INIT	1 CLK_REG
state_rx_bps	I	1	state is STATE_BYPASS	1 CLK_REG
FLT_WAKE	I	1	Indicate fault status	Level(CLK_SLOW domain)

## Clock Domain

The clock for TONE\_CTRL is CLK\_256K\_SC and CLK\_OUT\_SC.  
For TONE\_TRANS\_EN\_X related logics, CLK\_OUT\_SC is used.  
For others, CLK\_256K\_SC is used.

## TONE\_CTRL function description

TONE\_CTRL module is a sub module in COMM\_DIG. It generates 5 kinds of tones. The 5 tones are described in Table2 and From2.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time between pulses of COMM tones COMM tones: WAKE,	t <sub>COMM TONE</sub>			11	15	us

STA, SHUTDOWN						
HIGH time of each pulse of COMM tone	t <sub>COMMTONE_HI</sub>		0.92	1	1.08	us
LOW time of each pulse of COMM tone	t <sub>COMMTONE_LO</sub>		0.92	1	1.08	us
Time between pulses of FAULT tones	t <sub>FLTTONE</sub>			11.5		us
HIGH time of each pulse of FAULT tone	t <sub>FLTTONE_HI</sub>			1		us
LOW time of each pulse of FAULT tone	t <sub>FLTTONE_LO</sub>			1		us
Time between pulses of HB tones	t <sub>HBTONE</sub>			11.5		us
HIGH time of each pulse of HB tone	t <sub>HBTONE_HI</sub>			1		us
LOW time of each pulse of HB tone	t <sub>HBTONE_LO</sub>			1		us
Period between HB tone burst	t <sub>HB_PERIOD</sub>		360	400	440	ms
Timeout to not receive HB	t <sub>HB_TIMEOUT</sub>		0.9	1	1.1	s
Time to receive HB too fast	t <sub>HB_FAST</sub>			200		ms
Period between FAULT tone burst	t <sub>FLT_PERIOD</sub>			50		ms
FAULT tone latency in stack devices	t <sub>FLTS_LATENCY</sub>	From time a device receives the tone to the time the same device detects and generates its fault tone		48		us
FAULT tone latency in base device	t <sub>FLTB_LATENCY</sub>	From time a device receives the tone to the time the same device detects and asserts fault pin		24		us

Table2 timing requirement for tones

WAKE tone			STA tone			SHUTDOWN tone			HB tone			FT tone		
n	nDET	Polar	n	nDET	Polar	n	nDET	Polar	n	nDET	Polar	n	nDET	Polar
90	60	+	30	20	+	270	180	-	30	20	-	90	60	-

Table3 Numbers and Polarity of Tones

In CLK\_256K domain, 1 clock is 3.9us, so 1us width pulses will be generated in analog part. In digital part, all tones are generated on outputs TONE\_CLK, TONE\_POLAR, TONE\_TRANS\_EN\_N, TONE\_TRANS\_EN\_S.

TONE\_CLK: ([HWR001/003/004/005/006\\_TONE\\_CTRL](#))

If a tone is being generated, TONE\_CLK is always 1 clock high with 3 clocks period([HWR007\\_TONE\\_CTRL](#)). After the corresponding numbers of pulses(in Table3) are sent, TONE\_CLK stops toggling.

TONE\_POLAR:

According to Table3, when sending WAKE tone or STA tone, TONE\_POLAR is high. When sending other tones, TONE\_POLAR is low.

TONE\_TRANS\_EN\_N:

When sending tone because of analog detected tones on S port([HWR002\\_TONE\\_CTRL](#)) (A2D\_WAKE\_UP\_S([HWR001\\_TONE\\_CTRL](#))) or

A2D\_STA\_DET\_S([HWR003\\_TONE\\_CTRL](#))), TONE\_TRANS\_EN\_N is high to deliver the tone.

When sending WAKE([HWR012\\_TONE\\_CTRL](#)) tone, STA([HWR014\\_TONE\\_CTRL](#)) tone or SHUTDOWN([HWR004\\_TONE\\_CTRL](#)) tone because of corresponding register bit X\_GEN, if SPI\_DIR is low, TONE\_TRANS\_EN\_N is high.

When sending HB([HWR006\\_TONE\\_CTRL](#)) tone or FLT([HWR005\\_TONE\\_CTRL](#)) tone, TONE\_TRANS\_EN\_N is high. HB tone is sent when SLEEP\_MODE high and FLT\_WAKE low, FLT tone is sent when SLEEP high and FLT\_WAKE high([HWR009\\_TONE\\_CTRL](#)). If SLEEP\_MODE changes to active mode(A2D\_SLEEP\_1P8 changes to high), BM20A response to A2D\_WAKE\_UP\_N/A2D\_WAKE\_UP\_S/A2D\_STA\_DET\_N/A2D\_STA\_DET\_S immediately. ([HWR011\\_TONE\\_CTRL](#))

As daisy chain transmitting are always start after receiving(copy or response), TONE\_TRANS\_EN\_N changes to 0 when daisy chain starts receiving([HWR010\\_TONE\\_CTRL](#)).

TONE\_TRANS\_EN\_S:

When sending tone because of analog detected tones on N([HWR002\\_TONE\\_CTRL](#)) port(A2D\_WAKE\_UP\_N([HWR001\\_TONE\\_CTRL](#)) or A2D\_STA\_DET\_N([HWR003\\_TONE\\_CTRL](#))), TONE\_TRANS\_EN\_S is high to deliver the tone.

When sending WAKE([HWR012\\_TONE\\_CTRL](#)) tone, STA([HWR014\\_TONE\\_CTRL](#)) tone or SHUTDOWN([HWR004\\_TONE\\_CTRL](#)) tone because of corresponding register bit X\_GEN, if SPI\_DIR is high, TONE\_TRANS\_EN\_S is high.

As daisy chain transmitting are always start after receiving(copy or response), TONE\_TRANS\_EN\_N changes to 0 when daisy chain starts receiving([HWR010\\_TONE\\_CTRL](#)).

Clr\_xxx(xxx is SD\_TONE\_GEN, WAKE\_TONE\_GEN, STA\_TONE\_GEN) is generated after synchronizing the tone source to clear the tone starting state.([HWR008/013/015\\_TONE\\_CTRL](#)). (Refer to Figure2)

Specially, D2A\_CLR\_WAKEUP is high after the corresponding numbers of pulses (in Table3) are sent([HWR016\\_TONE\\_CTRL](#)). (Refer to Figure3)

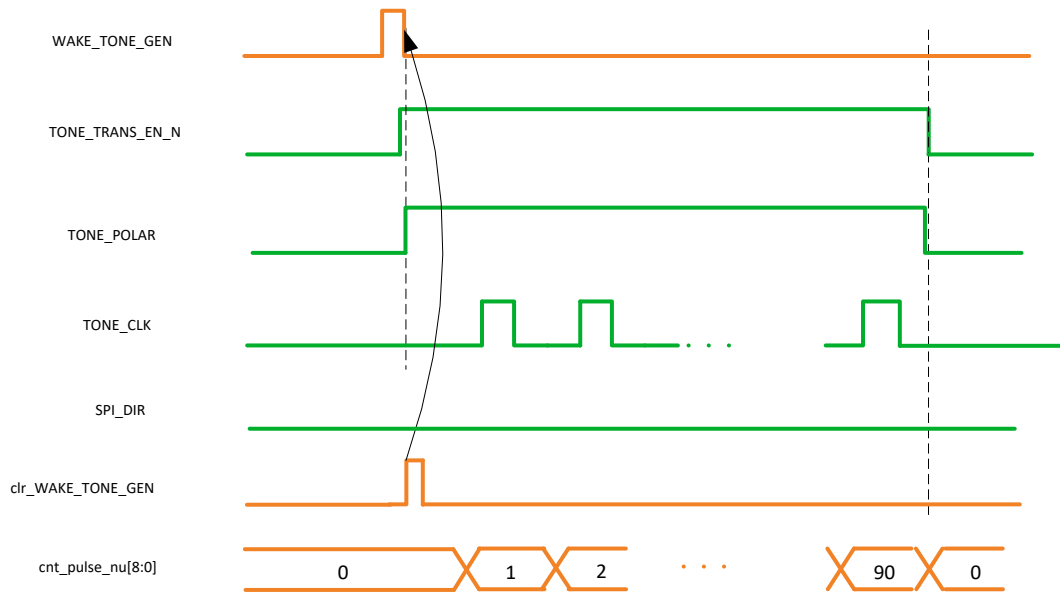


Figure2 WAKE\_TONE\_GEN is written high

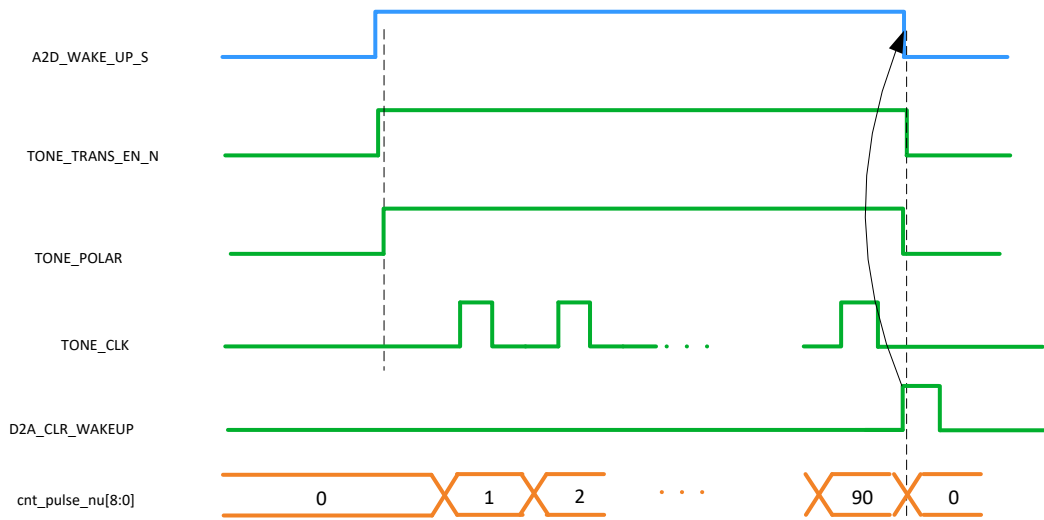


Figure3 receive A2D\_WAKE\_UP\_S