ADS4128 12 位 200MSPS 超低功耗 ADC

1 特性

- 最大采样率：200MSPS
- 使用 1.8V 单一电源的超低功耗：
  - 200MSPS 下 230mW 总体功耗
- 高动态性能：
  - 信噪比 (SNR)：170MHz 时为 69dBFS
  - 无杂散动态范围 (SFDR)：170MHz 时为 85dBc
- 随采样速率动态地进行功率调节
- 输出接口:
  - 支持可编程摆幅和强度的双倍数据速率 (DDR) 低压差分信号 (LVDS)
    - 标准摆幅：350mV
    - 低摆幅：200mV
    - 默认信号强度：100Ω 端接
    - 2x 强度：50Ω 端接
  - 还支持 1.8V 平行 CMOS 接口
- 针对 SNR / SFDR 折衷的高达 6dB 的可编程增益
- DC 偏移校正
- 支持低至 200mV_{PP} 的输入时钟幅值
- 封装：7.00mm × 7.00mm VQFN-48

2 应用

- 无线通信基础设施
- 软件定义无线电
- 功率放大器线性化

3 说明

ADS4128 是一款 12 位模数转换器 (ADC)，其采样速率高达 200MSPS。在由 1.8V 电源供电时，这个器件运用创新的设计技术在实现高动态性能的同时保持极低功耗。此器件非常适合于多载波、高带宽通信 应用。

ADS4128 具有精细增益选项，此选项可被用于在较低的全标度输入范围 （特别是高输入频率条件下） 改善 SFDR 性能。它包括一个 DC 偏移校正环路，此环路可被用于消除 ADC 偏移。在较低的采样速率条件下，ADC 的操作功耗将自动减低，而没有性能损失。

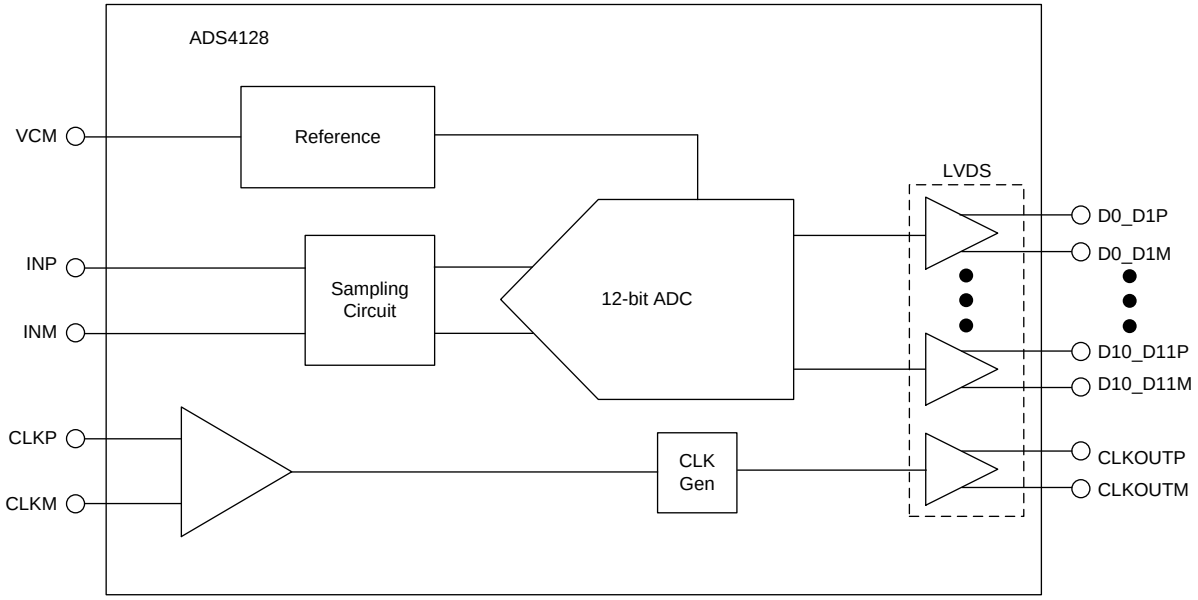
ADS4128 采用紧凑型超薄四方扁平无引线 (VQFN)-48 封装，额定工业温度范围为 –40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS4128	VQFN(48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

ADS4128 框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2012) to Revision A **Page**

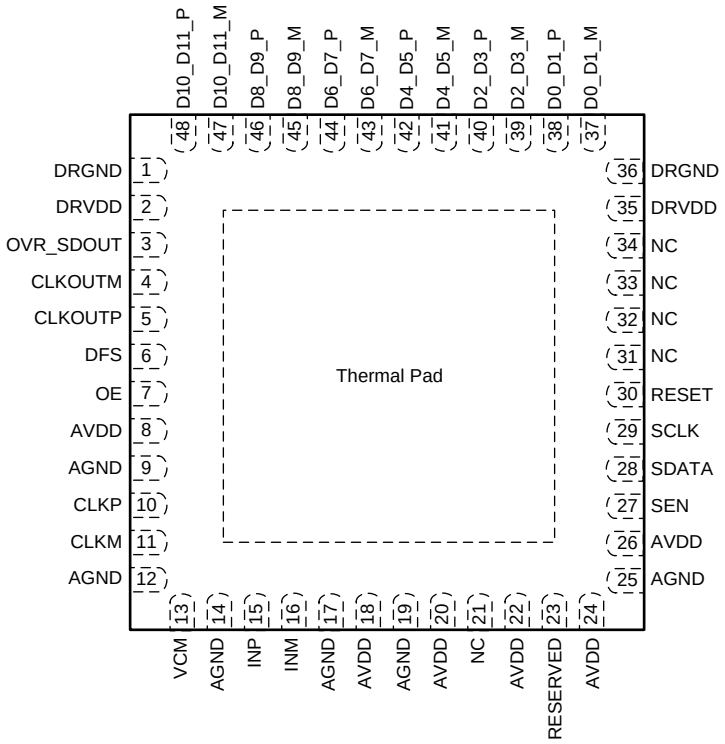
- 已添加 *ESD 额定值表，特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

5 Device Comparison Table

FAMILY	SAMPLING RATE					WITH ANALOG INPUT BUFFERS	
	65 MSPS	125 MSPS	160 MSPS	200 MSPS	250 MSPS	200 MSPS	250 MSPS
ADS412x 12-bit family	ADS4122	ADS4125	ADS4126	ADS4128	ADS4129	—	ADS41B29
ADS414x 14-bit family	ADS4142	ADS4145	ADS4146	—	ADS4149	—	ADS41B49
9-bit	—	—	—	—	—	—	ADS58B19
11-bit	—	—	—	—	—	ADS58B18	—

6 Pin Configuration and Functions

RGZ Package(1)
48-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



The thermal pad is connected to DRGND.

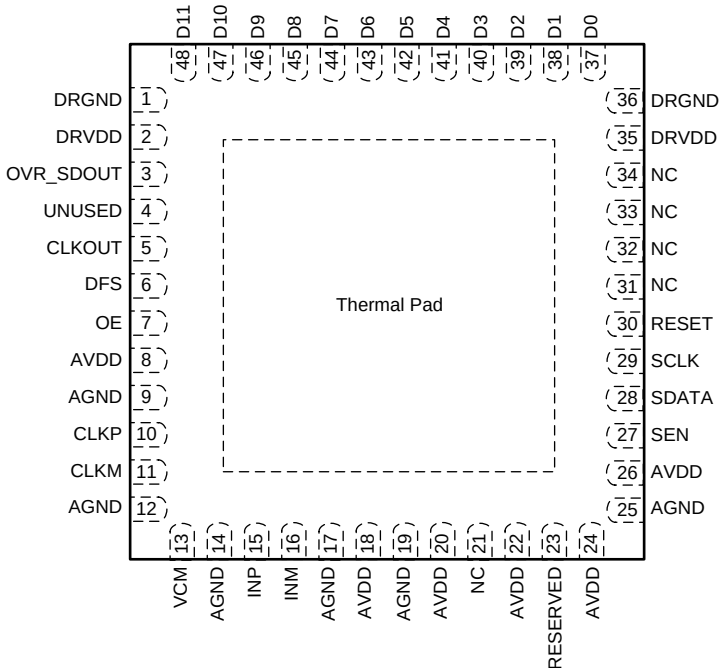
Pin Functions - LVDS Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9, 12, 14, 17, 19, 25	I	Analog ground
AVDD	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
CLKM	11	I	Differential clock input, negative
CLKP	10	I	Differential clock input, positive
CLKOUTM	4	O	Differential output clock, negative
CLKOUTP	5	O	Differential output clock, positive
D0_D1_P	38	O	Differential output data D0 and D1 multiplexed, true
D0_D1_M	37	O	Differential output data D0 and D1 multiplexed, complement
D2_D3_P	40	O	Differential output data D2 and D3 multiplexed, true
D2_D3_M	39	O	Differential output data D2 and D3 multiplexed, complement
D4_D5_P	42	O	Differential output data D4 and D5 multiplexed, true
D4_D5_M	41	O	Differential output data D4 and D5 multiplexed, complement
D6_D7_P	44	O	Differential output data D6 and D7 multiplexed, true
D6_D7_M	43	O	Differential output data D6 and D7 multiplexed, complement
D8_D9_P	46	O	Differential output data D8 and D9 multiplexed, true
D8_D9_M	45	O	Differential output data D8 and D9 multiplexed, complement
D10_D11_P	48	O	Differential output data D10 and D11 multiplexed, true
D10_D11_M	47	O	Differential output data D10 and D11 multiplexed, complement
DFS	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS and CMOS output interface type. See Table 9 for detailed information.
DRGND	1, 36, PAD	I	Digital and output buffer ground

Pin Functions - LVDS Mode (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DRVDD	2, 35	I	1.8-V digital and output buffer supply
INM	16	I	Differential analog input, negative
INP	15	I	Differential analog input, positive
NC	21, 31, 32, 33, 34	—	Do not connect
OE	7	I	Output buffer enable input, active high; this pin has an internal 180-kΩ pull-up resistor to DRVDD.
OVR_SDOUT	3	O	This pin functions as an out-of-range indicator after reset when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESERVED	23	I	Digital control pin, reserved for future use
RESET	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
SCLK	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 11). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
VCM	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

RGZ Package(2)
48-Pin VQFN With Exposed Thermal Pad
CMOS - Top View



The thermal pad is connected to DRGND.

Pin Functions - CMOS Mode

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9, 12, 14, 17, 19, 25	I	Analog ground
AVDD	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
CLKM	11	I	Differential clock input, negative
CLKP	10	I	Differential clock input, positive
CLKOUT	5	O	CMOS output clock
D0	37	O	12-bit CMOS output data
D1	38	O	12-bit CMOS output data
D2	39	O	12-bit CMOS output data
D3	40	O	12-bit CMOS output data
D4	41	O	12-bit CMOS output data
D5	42	O	12-bit CMOS output data
D6	43	O	12-bit CMOS output data
D7	44	O	12-bit CMOS output data
D8	45	O	12-bit CMOS output data
D9	46	O	12-bit CMOS output data
D10	47	O	12-bit CMOS output data
D11	48	O	12-bit CMOS output data
DFS	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS and CMOS output interface type. See Table 9 for detailed information.
DRGND	1, 36, PAD	I	Digital and output buffer ground
DRVDD	2, 35	I	1.8-V digital and output buffer supply
INP	15	I	Differential analog input, positive
INM	16	I	Differential analog input, negative
NC	21, 31, 32, 33, 34	—	Do not connect
OE	7	I	Output buffer enable input, active high; this pin has an internal 180-kΩ pull-up resistor to DRVDD.
OVR_SDOUT	3	O	This pin functions as an out-of-range indicator after reset when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESET	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
RESERVED	23	I	Digital control pin, reserved for future use
SCLK	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 11). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
UNUSED	4	—	Unused pin in CMOS mode
VCM	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD	–0.3	2.1	V
	DRVDD	–0.3	2.1	
Voltage	Between AGND and DRGND	–0.3	0.3	V
	Between AVDD to DRVDD (when AVDD leads DRVDD)	0	2.1	
	Between DRVDD to AVDD (when DRVDD leads AVDD)	0	2.1	
Voltage applied to input pins	INP, INM	–0.3	(1.9) AVDD + 0.3	V
	CLKP, CLKM(2), DFS, OE	–0.3	AVDD + 0.3	
	RESET, SCLK, SDATA, SEN	–0.3	3.9	
Temperature	Operating free-air, T_A	–40	85	°C
	Operating junction, T_J		125	
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP and CLKM is less than |0.3 V|. This setting prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	TYP	MAX	UNIT
SUPPLIES					
AVDD	Analog supply voltage	1.7	1.8	1.9	V
DRVDD	Digital supply voltage	1.7	1.8	1.9	
ANALOG INPUTS					
Differential input voltage range(1)			2		V_{PP}
Input common-mode voltage			V_{CM} ± 0.05		V
Maximum analog input frequency	With 2-V_{PP} input amplitude(2)		400		MHz
	With 1-V_{PP} input amplitude(2)		800		
CLOCK INPUT					
Input clock sample rate, low-speed mode	Enabled(3)	20		80	MSPS
	Disabled(3)	> 80		200	
Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
	LVPECL, ac-coupled		1.6		
	LVDS, ac-coupled		0.7		
	LVCMOS, single-ended, ac-coupled		1.8		V

(1) With 0-dB gain. See the *Fine Gain* section in the *Detailed Description* for relation between input voltage range and gain.
(2) See the *Overview* section in the *Detailed Description*.
(3) See the *Serial Interface* section for details on low-speed mode.

Recommended Operating Conditions (continued)

Over operating free-air temperature range, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Input clock duty cycle	Low-speed mode enabled	40%	50%	60%	
	Low-speed mode disabled	35%	50%	65%	
DIGITAL OUTPUTS					
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND		5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)		100		Ω
T_A	Operating free-air temperature	–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		ADS4128 RGZ (VQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 1-dB gain, and DDR LVDS interface, unless otherwise noted.
Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V. Note that after reset, the device is in 0-dB gain mode.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				12	Bits
SNR	Signal-to-noise ratio, LVDS	f_{IN} = 10 MHz		70		dBFS
		f_{IN} = 70 MHz		70		
		f_{IN} = 100 MHz		69.7		
		f_{IN} = 170 MHz	65.8	69		
		f_{IN} = 300 MHz		68.2		
SINAD	Signal-to-noise and distortion ratio, LVDS	f_{IN} = 10 MHz		69.8		dBFS
		f_{IN} = 70 MHz		69.2		
		f_{IN} = 100 MHz		69.1		
		f_{IN} = 170 MHz	65.5	68.8		
		f_{IN} = 300 MHz		67		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		87		dBc
		f_{IN} = 70 MHz		80		
		f_{IN} = 100 MHz		82		
		f_{IN} = 170 MHz	70	85		
		f_{IN} = 300 MHz		74		
THD	Total harmonic distortion	f_{IN} = 10 MHz		84		dBc
		f_{IN} = 70 MHz		78		
		f_{IN} = 100 MHz		79		
		f_{IN} = 170 MHz	69	83		
		f_{IN} = 300 MHz		73		
HD2	Second-harmonic distortion	f_{IN} = 10 MHz		90		dBc
		f_{IN} = 70 MHz		84		
		f_{IN} = 100 MHz		83		
		f_{IN} = 170 MHz	70	85		
		f_{IN} = 300 MHz		74		
HD3	Third-harmonic distortion	f_{IN} = 10 MHz		87		dBc
		f_{IN} = 70 MHz		80		
		f_{IN} = 100 MHz		82		
		f_{IN} = 170 MHz	70	86		
		f_{IN} = 300 MHz		79		
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		93		dBc
		f_{IN} = 70 MHz		93		
		f_{IN} = 100 MHz		91		
		f_{IN} = 170 MHz	75	90		
		f_{IN} = 300 MHz		88		
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		–85		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		–90		
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input		1		Clock cycles
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.2		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz	–0.95	±0.2	1.6	LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.5	±5	LSBs

7.6 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input voltage range			2		V_{PP}
	Differential input resistance (at dc); see Figure 47			> 1		MΩ
	Differential input capacitance; see Figure 48			4		pF
	Analog input bandwidth			550		MHz
	Analog input common-mode current (per input pin)			0.6		µA/MSPS
VCM	Common-mode output voltage			0.95		V
	VCM output current capability			4		mA
DC ACCURACY						
	Offset error		–15	2.5	15	mV
	Temperature coefficient of offset error			0.003		mV/°C
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			–0.2	±1	%FS
	Temperature coefficient of E_{GCHAN}			0.001		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			85	113	mA
IDRVDD(1)	Output buffer supply current, LVDS interface with 100-Ω external termination	Low LVDS swing (200 mV)		43		mA
		Standard LVDS swing (350 mV)		55	72	
	Output buffer supply current(1)(2) CMOS interface	8-pF external load capacitance f_{IN} = 2.5 MHz		33		
	Analog power			153		mW
	Digital power, LVDS interface	Low LVDS swing (200 mV)		77		mW
	Digital power, CMOS interface(2)	8-pF external load capacitance f_{IN} = 2.5 MHz		59		mW
	Global power-down			10	25	mW
	Standby			185		mW

(1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on the output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Device Functional Modes*).

7.7 Digital Characteristics

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, and 50% clock duty cycle, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE)						
V_{IH}	High-level input voltage	RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels	1.3			V
		OE only supports 1.8-V CMOS logic levels	1.3			
V_{IL}	Low-level input voltage	RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels			0.4	V
		OE only supports 1.8-V CMOS logic levels			0.4	
I_{IH}	High-level input current, SDATA and SCLK(1)	V_{HIGH} = 1.8 V		10		µA
	High-level input current, SEN	V_{HIGH} = 1.8 V		0		
I_{IL}	Low-level input, SDATA and SCLK	V_{LOW} = 0 V		0		µA
	Low-level input, SEN	V_{LOW} = 0 V		10		
DIGITAL OUTPUTS (CMOS INTERFACE: D0 to D11, OVR_SDOUT)						
V_{OH}	High-level output voltage		DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage			0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: DA0P and DA0M to DA11P and DA11M, DB0P and DB0M to DB11P and DB11M, CLKOUTP and CLKOUTM)						
V_{ODH}	High-level output voltage(2)	Standard-swing LVDS	270	350	430	mV
		Low-swing LVDS		200		
V_{ODL}	Low-level output voltage(2)	Standard-swing LVDS	–430	–350	–270	mV
		Low-swing LVDS		–200		
V_{OCM}	Output common-mode voltage		0.85	1.05	1.25	V

(1) SDATA and SCLK have an internal 180-kΩ pull-down resistor.
(2) With an external 100-Ω termination.

7.8 Timing Requirements: LVDS and CMOS Modes(1)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 200 MSPS, sine wave input clock, C_{LOAD} = 5 pF(2), and R_{LOAD} = 100 Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

			MIN	NOM	MAX	UNIT
t_A	Aperture delay		0.6	0.8	1.2	ns
	Aperture delay variation	Between two devices at the same temperature and DRVDD supply		±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	
	ADC latency(4)	Low-latency mode (default after reset)		10		Clock cycles
		Low-latency mode disabled (gain enabled, offset correction disabled)		16		
		Low-latency mode disabled (gain and offset correction enabled)		17		
DDR LVDS MODE(5)(6)						
t_{SU}	Data setup time(3)	Data valid(7) to zero-crossing of CLKOUTP	1.05	1.55		ns
t_H	Data hold time(3)	Zero-crossing of CLKOUTP to data becoming invalid(7)	0.35	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge crossover to output clock rising edge crossover *1 MSPS ≤ sampling frequency ≤ 200 MSPS*	3	4.2	5.4	ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		±0.6		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP – CLKOUTM) *1 MSPS ≤ sampling frequency ≤ 200 MSPS*	42%	48%	54%	
t_{RISE}, t_{FALL}	Data rising time, Data falling time	Rising time measured from –100 mV to 100 mV Falling time measured from 100 mV to –100 mV *1 MSPS ≤ sampling frequency ≤ 200 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rising time, Output clock falling time	Rising time measured from –100 mV to 100 mV Falling time measured from 100 mV to –100 mV *1 MSPS ≤ sampling frequency ≤ 200 MSPS*		0.14		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		50	100	ns
PARALLEL CMOS MODE(8)						
t_{START}	Input clock to data delay	Input clock rising edge crossover to start of data valid(7)			–0.3	ns
t_{DV}	Data valid time	Time interval of valid data(7)	3.5	4.2		ns
t_{PDI}	Clock propagation delay	Input clock rising edge crossover to output clock rising edge crossover *1 MSPS ≤ sampling frequency ≤ 200 MSPS*	4	5.5	7	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1 MSPS ≤ sampling frequency ≤ 200 MSPS*		47%		
t_{RISE}, t_{FALL}	Data rising time, Data falling time	Rising time measured from 20% to 80% of DRVDD Falling time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 200 MSPS*		0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rising time, Output clock falling time	Rising time measured from 20% to 80% of DRVDD Falling time measured from 80% to 20% of DRVDD *1 ≤ sampling frequency ≤ 200 MSPS*		0.35		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20	40	ns

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) The LVDS timings are unchanged for low latency disabled and enabled.
(7) Data valid refers to a logic high of 1.26 V and a logic low of 0.54 V.
(8) Low-latency mode enabled.

7.9 Reset Timing Requirements

Typical values are at 25°C and minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

			MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of active RESET signal that resets the serial registers	10			ns
					1 (1)	µs
t_3		Delay from RESET disable to SEN active	100			ns

(1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1 µs, the device can enter the parallel configuration mode briefly and then return back to serial interface mode.

Table 1. LVDS Timing Across Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
200	1.05	1.55	—	0.35	0.6	—
185	1.1	1.7	—	0.35	0.6	—
160	1.6	2.1	—	0.35	0.6	—
125	2.3	3	—	0.35	0.6	—
80	4.5	5.2	—	0.35	0.6	—

Table 2. CMOS Timing Across Sampling Frequencies (Low Latency Enabled)

SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO OUTPUT CLOCK								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1.6	2.2	—	1.8	2.5	—	4	5.5	7
185	1.8	2.4	—	1.9	2.7	—	4	5.5	7
160	2.3	2.9	—	2.2	3	—	4	5.5	7
125	3.1	3.7	—	3.2	4	—	4	5.5	7
80	5.4	6	—	5.4	6	—	4	5.5	7

Table 3. CMOS Timing Across Sampling Frequencies (Low Latency Disabled)

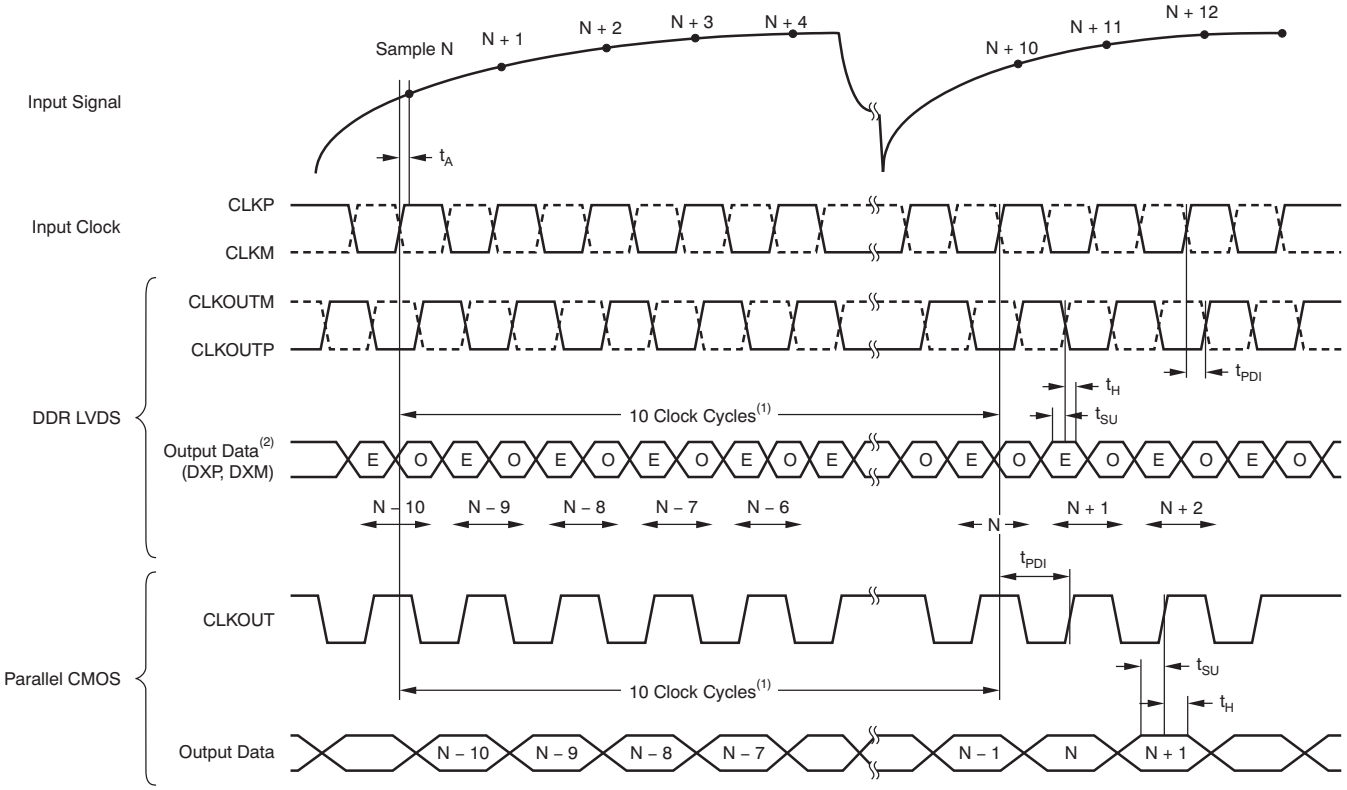
SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO OUTPUT CLOCK								
	t_{SETUP} (ns)			t_{HOLD} (ns)			t_{PDI} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
200	1	1.6	—	2	2.8	—	4	5.5	7
185	1.3	2	—	2.2	3	—	4	5.5	7
160	1.8	2.5	—	2.5	3.3	—	4	5.5	7
125	2.5	3.2	—	3.5	4.3	—	4	5.5	7
80	4.8	5.5	—	5.7	6.5	—	4	5.5	7

Table 4. CMOS Timing Across Sampling Frequencies (Low Latency Enabled)

SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
200	—	—	–0.3	3.5	4.2	—
185	—	—	–1	3.9	4.5	—
170	—	—	–1.5	4.3	5	—

Table 5. CMOS Timing Across Sampling Frequencies (Low Latency Disabled)

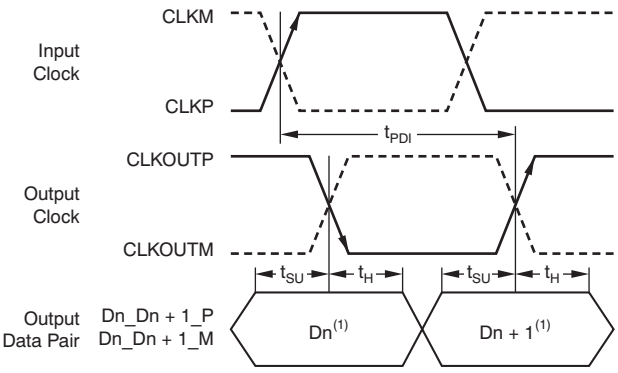
SAMPLING FREQUENCY (MSPS)	TIMING SPECIFIED WITH RESPECT TO INPUT CLOCK					
	t_{START} (ns)			t_{DV} (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX
200	—	—	0.3	3.5	4.2	—
185	—	—	0	3.9	4.5	—
170	—	—	–1.3	4.3	5	—



ADC latency in low-latency mode. At higher sampling frequencies, t_{DPI} is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

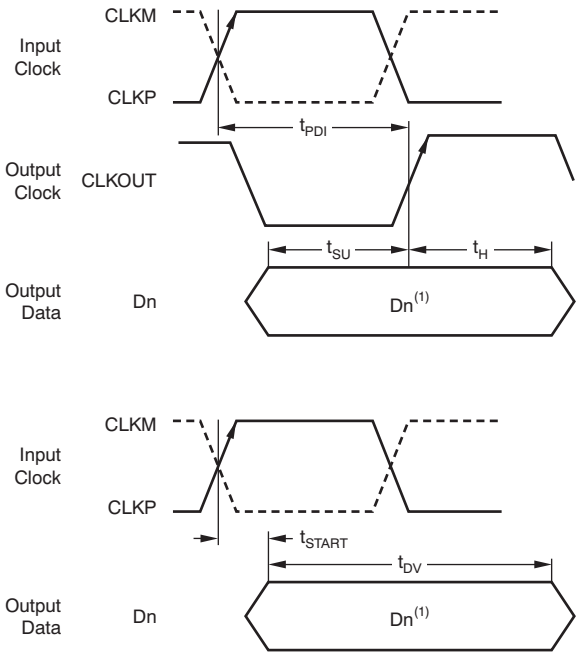
E = Even bits (D0, D2, D4, and so on). O = Odd bits (D1, D3, D5, and so on).

Figure 1. Latency Diagram



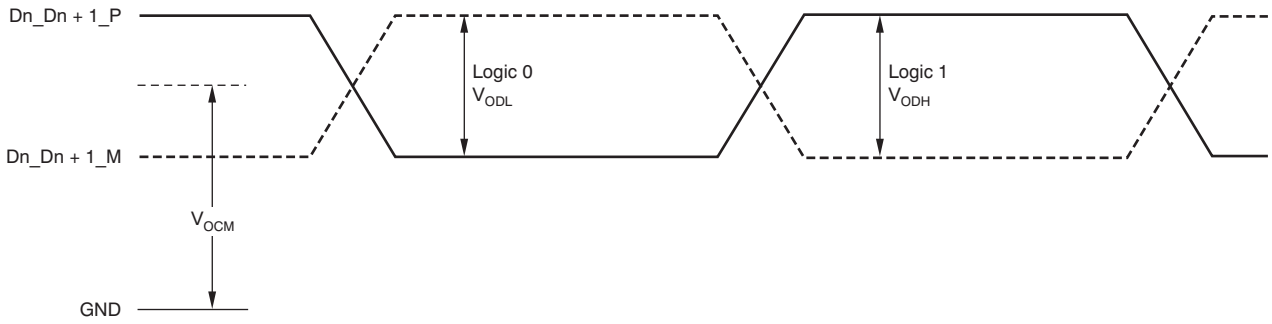
Dn = bits D0, D2, D4, and so on. Dn + 1 = bits D1, D3, D5, and so on.

Figure 2. LVDS Mode Timing



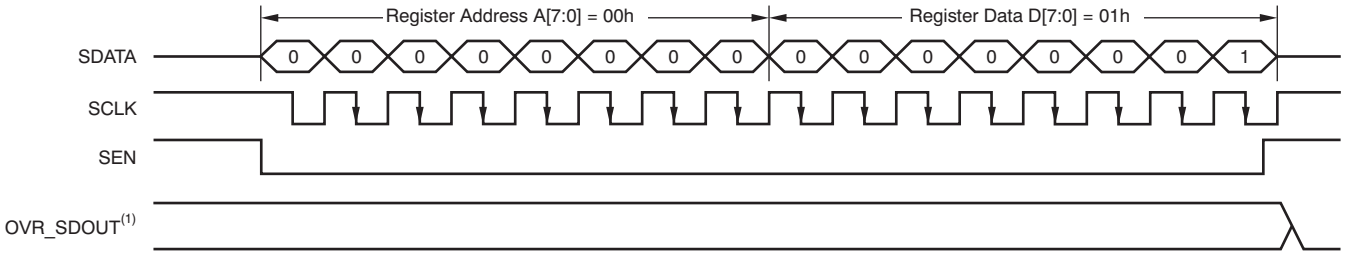
Dn = bits D0, D1, D2, and so forth.

Figure 3. CMOS Mode Timing

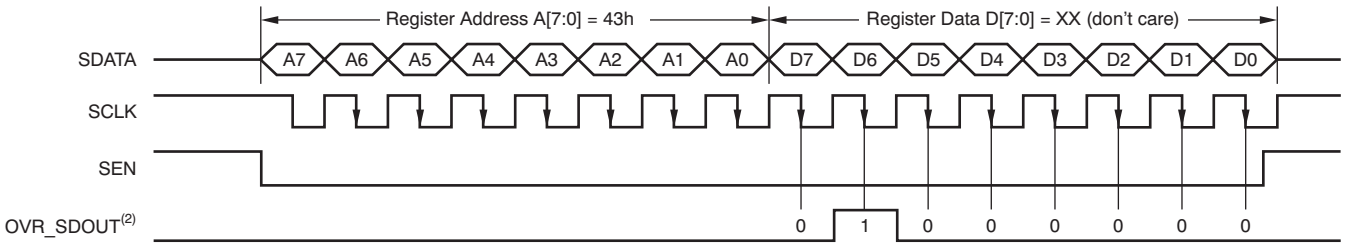


With external 100-Ω termination.

Figure 4. LVDS Output Voltage Levels



a) Enable Serial Readout (READOUT = 1)

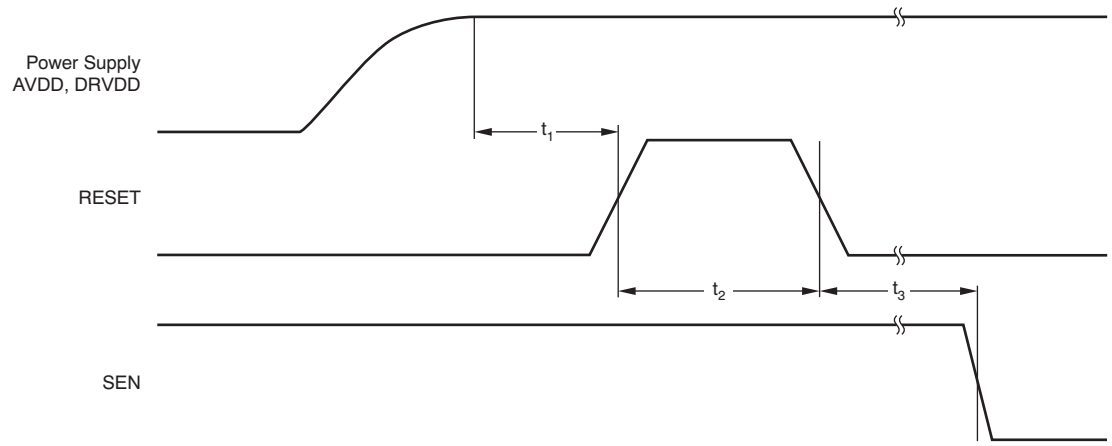


b) Read Contents of Register 43h. This Register Has Been Initialized with 40h (device is put in global power-down mode).

The OVR_SDOUT pin functions as OVR (READOUT = 0).

The OVR_SDOUT pin functions as a serial readout (READOUT = 1).

Figure 5. Serial Readout Timing Diagram



A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 6. Reset Timing Diagram

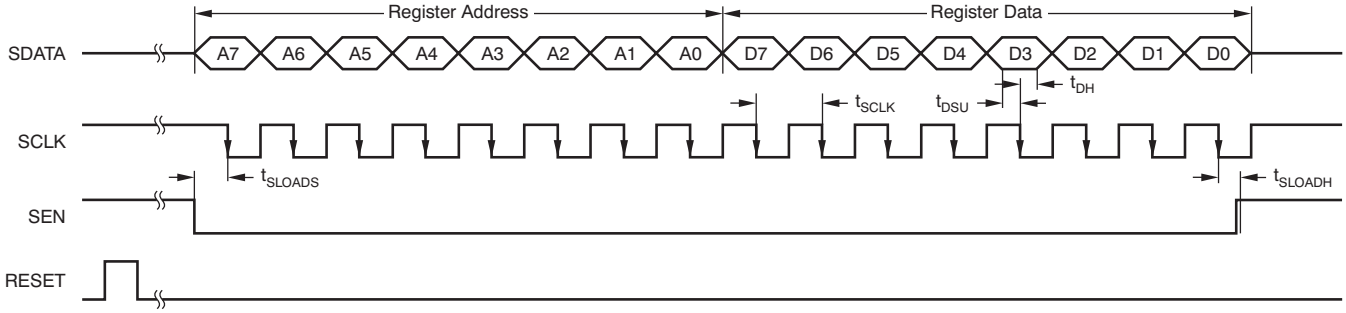


Figure 7. Serial Interface Timing

7.10 Typical Characteristics

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

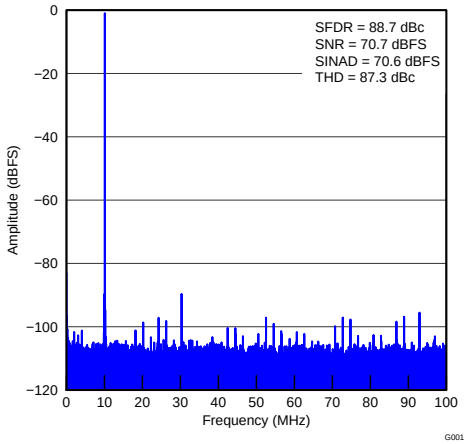


Figure 8. FFT for 10-MHz Input Signal

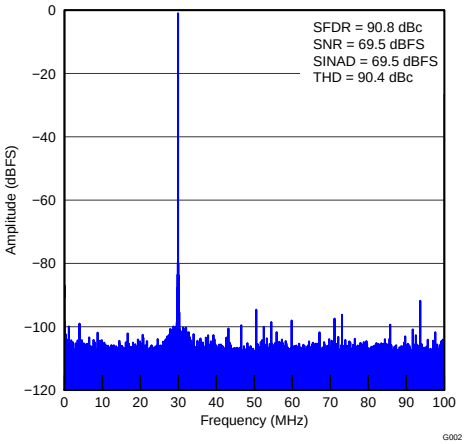


Figure 9. FFT for 170-MHz Input Signal

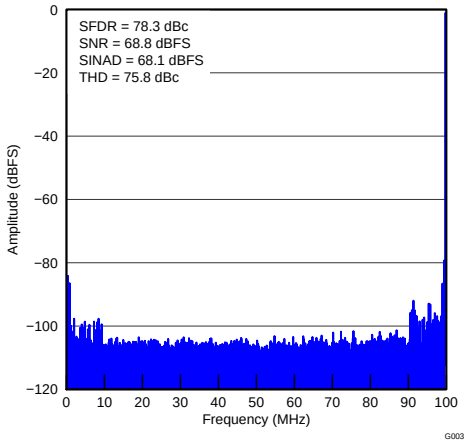


Figure 10. FFT for 300-MHz Input Signal

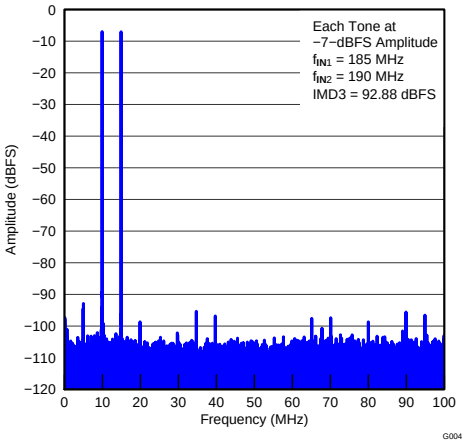


Figure 11. FFT for Two-Tone Input Signal

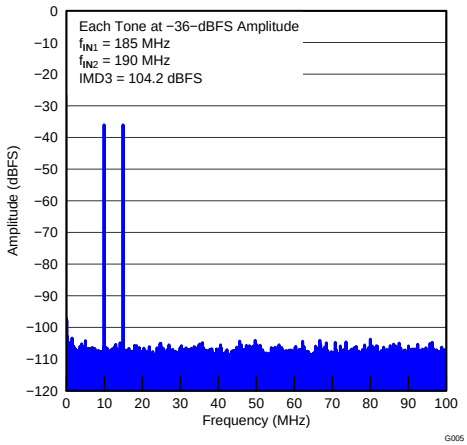


Figure 12. FFT for Two-Tone Input Signal

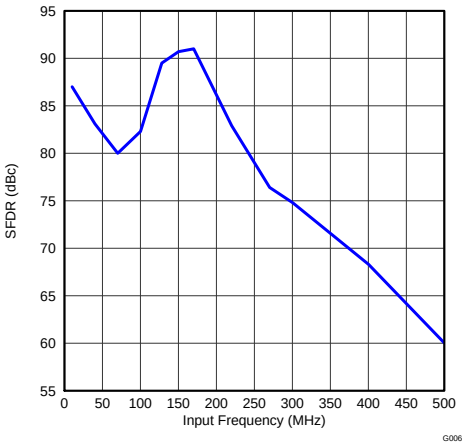


Figure 13. SFDR vs Input Frequency

Typical Characteristics (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

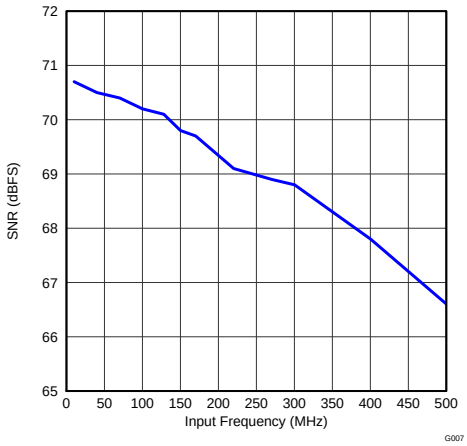


Figure 14. SNR vs Input Frequency

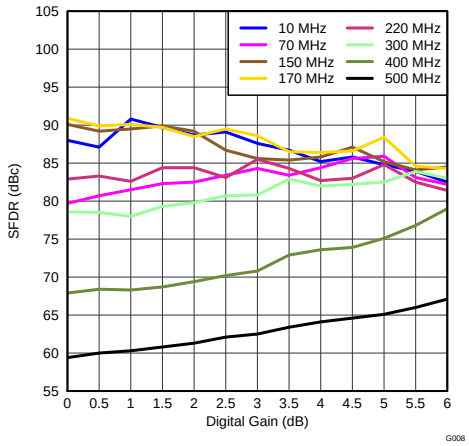


Figure 15. SFDR vs Digital Gain

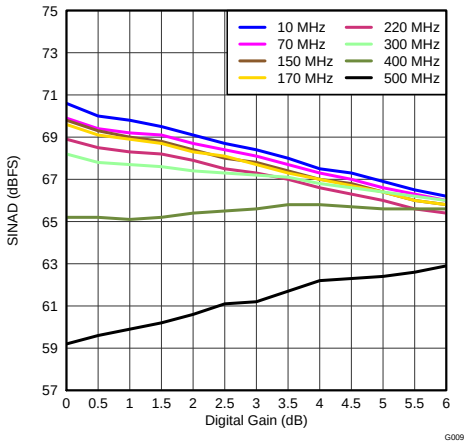


Figure 16. SINAD vs Digital Gain

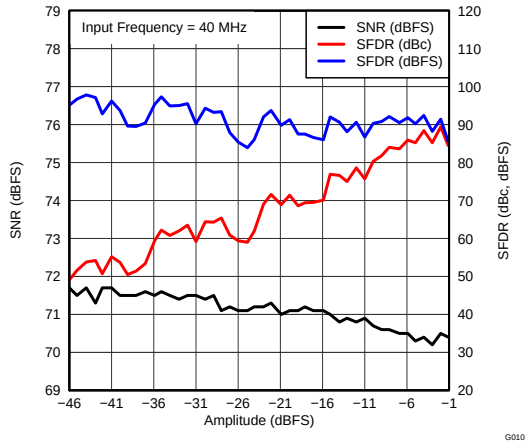


Figure 17. Performance Across Input Amplitude

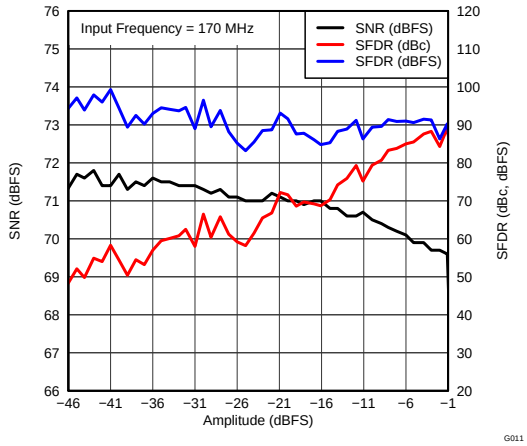


Figure 18. Performance Across Input Amplitude

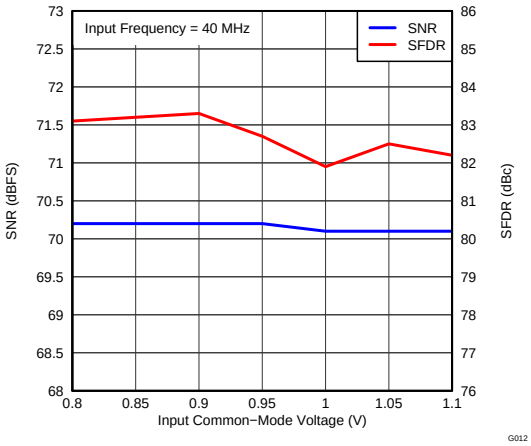


Figure 19. Performance vs Input Common-Mode Voltage

Typical Characteristics (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

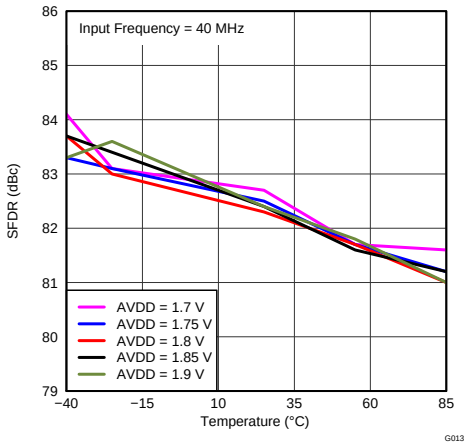


Figure 20. SFDR vs AVDD Supply and Temperature

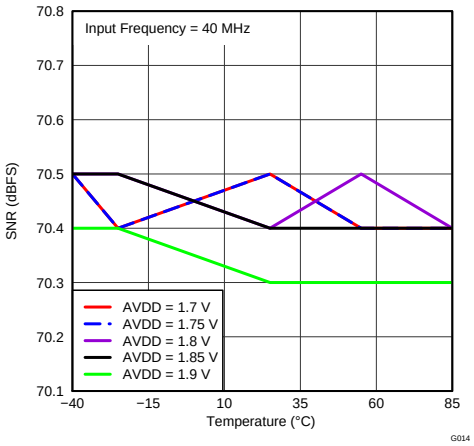


Figure 21. SNR vs AVDD Supply and Temperature

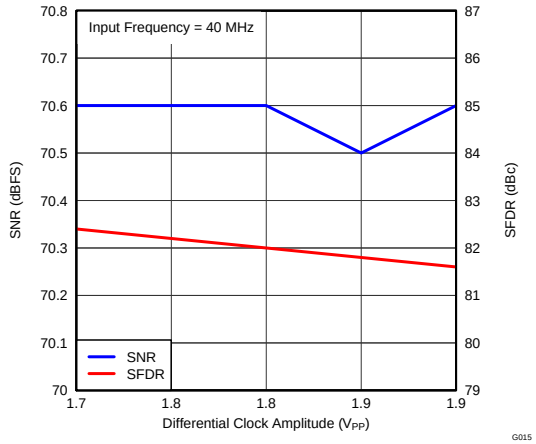


Figure 22. Performance vs DRVDD Supply

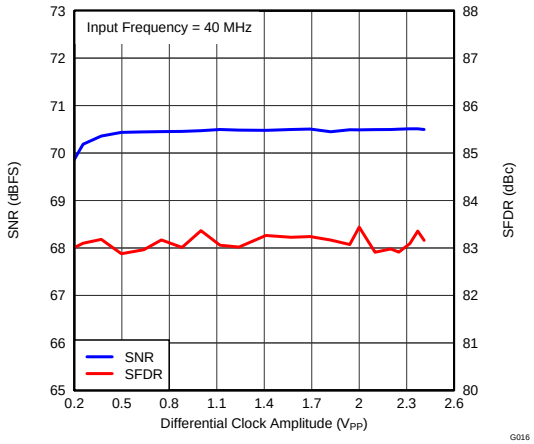


Figure 23. Performance vs Clock Amplitude

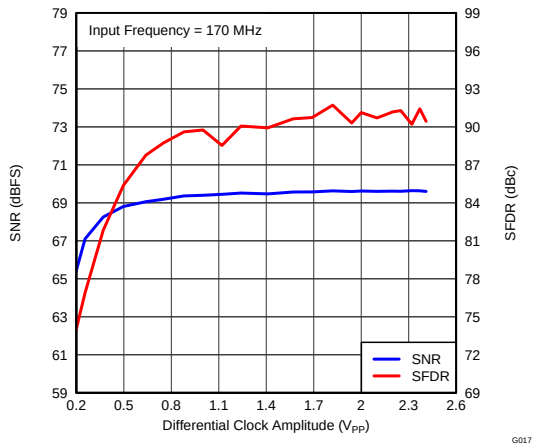


Figure 24. Performance vs Clock Amplitude

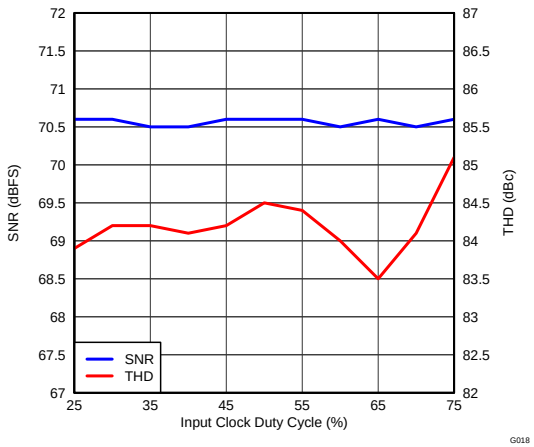


Figure 25. Performance vs Clock Duty Cycle

Typical Characteristics (continued)

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

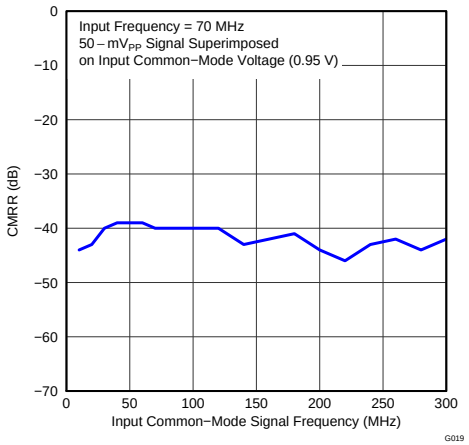


Figure 26. CMRR vs Frequency

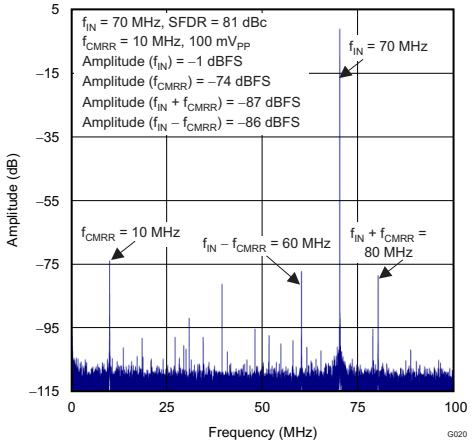


Figure 27. CMRR Spectrum

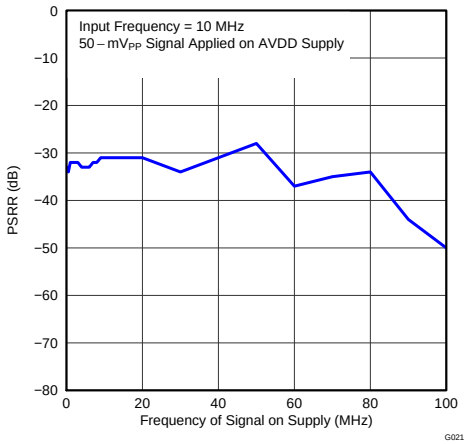


Figure 28. PSRR vs Frequency

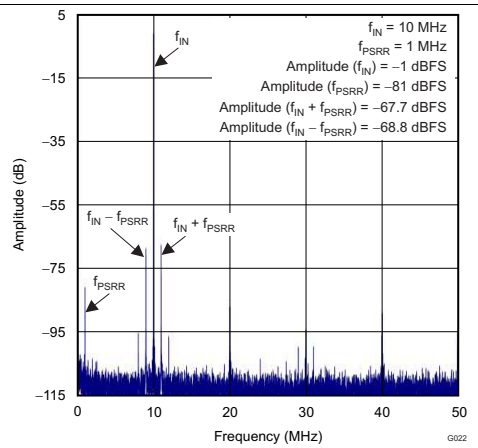


Figure 29. Zoomed View of Spectrum With PSRR Signal

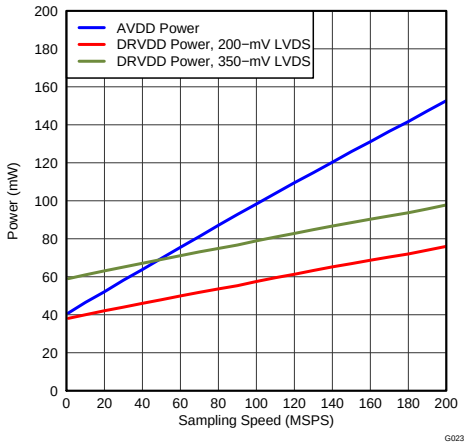


Figure 30. Power vs Sampling Frequency

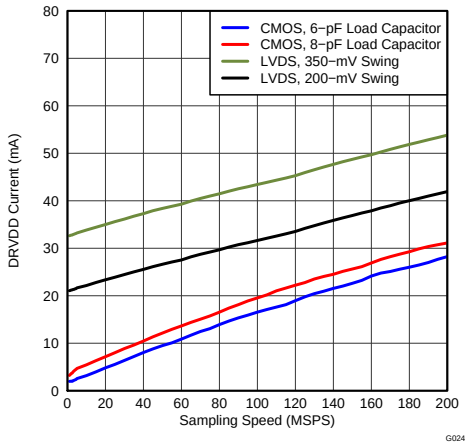


Figure 31. DRVDD Current vs Sampling Frequency

7.11 Typical Characteristics: Contour

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

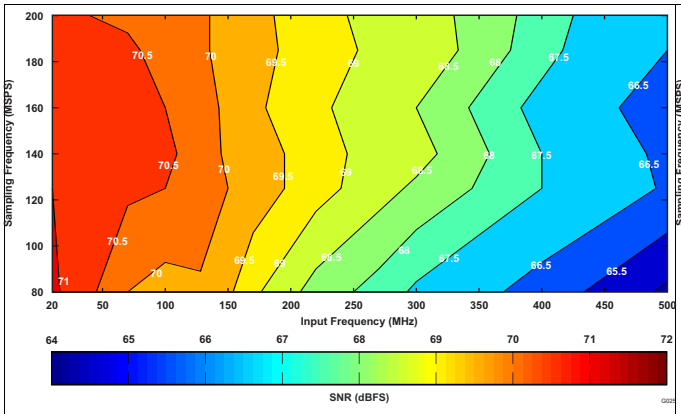


Figure 32. Signal-to-Noise Ratio (0-dB Gain)

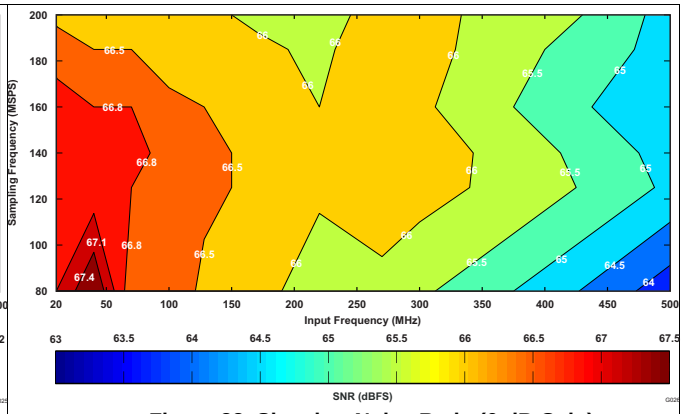


Figure 33. Signal-to-Noise Ratio (6-dB Gain)

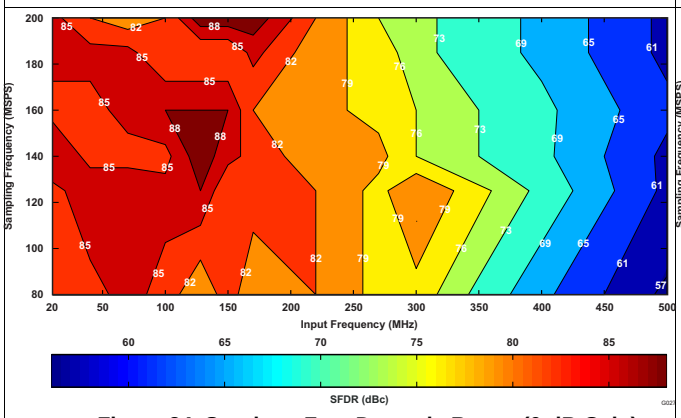


Figure 34. Spurious-Free Dynamic Range (0-dB Gain)

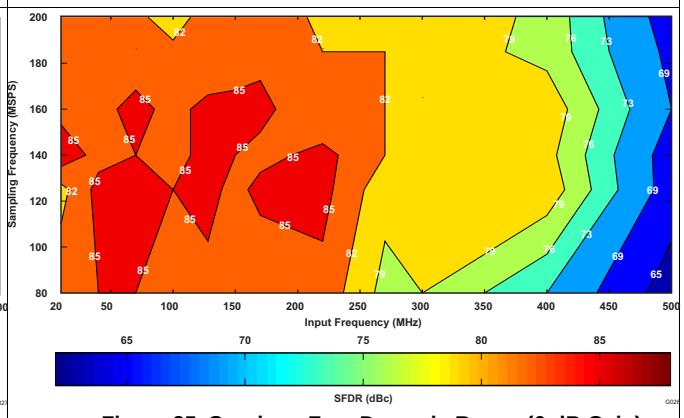


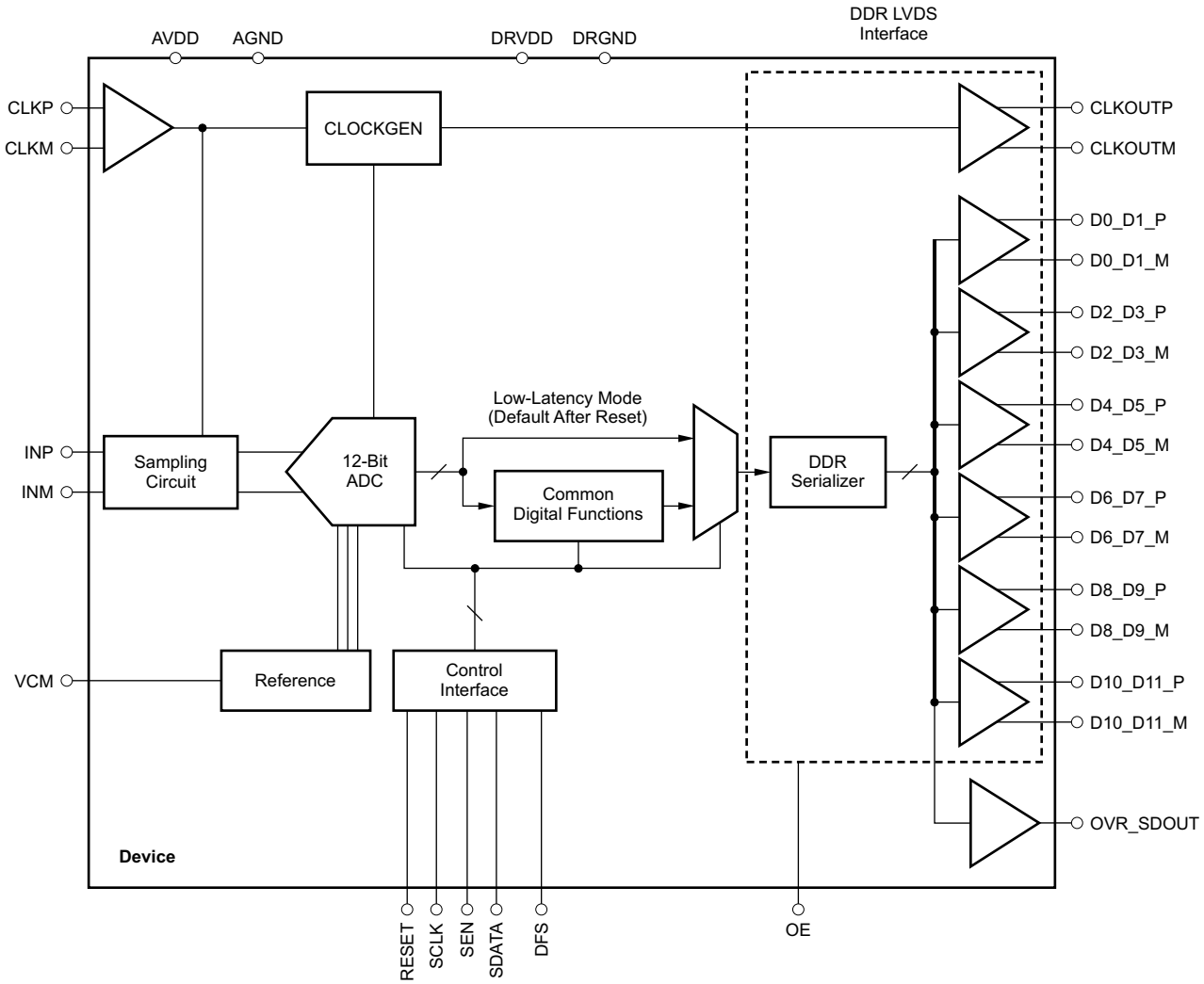
Figure 35. Spurious-Free Dynamic Range (6-dB Gain)

8 Detailed Description

8.1 Overview

The ADS4128 is a high-performance, low-power, 12-bit analog-to-digital converter (ADC) with maximum sampling rates up to 200 MSPS. The conversion process is initiated by a rising edge of the external input clock when the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Migrating From the ADS6149 Family

The ADS4128 is pin-compatible with the previous generation ADS6149 family; this architecture enables easy migration. However, there are some important differences between the generations, as summarized in Table 6.

Table 6. Migrating From the ADS6149 Family

ADS6149 FAMILY	ADS4149 FAMILY (Includes ADS4128)
PINS	
Pin 21 is NC (not connected)	Pin 21 is NC (not connected)
Pin 23 is MODE	Pin 23 is RESERVED in the ADS4128. It is reserved as a digital control pin for an (as yet) undefined function in the next-generation ADC series.
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 0.95 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol
	New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported
ADS61B49 FAMILY	**ADS41B49 AND ADS58B18 FAMILY**
PINS	
Pin 21 is NC (not connected)	Pin 21 is 3.3-V AVDD_BUF (supply for the analog input buffers)
Pin 23 is MODE	Pin 23 is a digital control pin for the RESERVED function. Pin 23 functions as SNR Boost enable (B18 only).
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V, AVDD_BUF is 3.3 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 1.7 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported

8.3.2 Digital Functions and Low-Latency Mode

The device has several useful digital functions such as test patterns, gain, and offset correction. All of these functions require extra clock cycles for operation and increase the overall latency and power of the device. Alternately, the device has a low-latency mode in which the raw ADC output is routed to the output data pins with a latency of 10 clock cycles. In this mode, the digital functions are bypassed. Figure 36 shows more details of the processing after the ADC.

The device is in low-latency mode after reset. In order to use any digital functions, low-latency mode must first be disabled by setting the DIS LOW LATENCY register bit to 1. Afterwards, the respective register bits must be programmed as described in the following sections and in the *Register Maps* section.

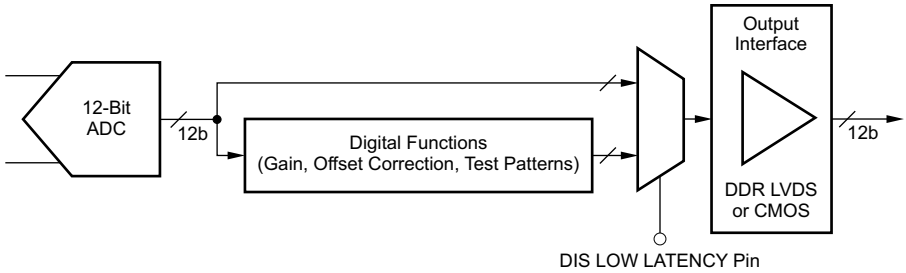


Figure 36. Digital Processing Block Diagram

8.3.3 Gain for SFDR and SNR Trade-Off

The ADS4128 includes gain settings that can be used to get improved SFDR performance. Gain is programmable from 0 dB to 6 dB (in 0.5-dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 7.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades approximately between 0.5 dB and 1 dB. SNR degradation is reduced at high input frequencies. As a result, gain is very useful at high input frequencies because SFDR improvement is significant with marginal SNR degradation. Therefore, gain can be used to trade-off between SFDR and SNR.

After a reset, the device is in low-latency mode and the gain function is disabled. To use gain:

- First, disable low-latency mode (DIS LOW LATENCY = 1).
- This setting enables the gain and puts the device in a 0-dB gain mode.
- For other gain settings, program the GAIN bits.

Table 7. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	2
1	Programmable gain	1.78
2	Programmable gain	1.59
3	Programmable gain	1.42
4	Programmable gain	1.26
5	Programmable gain	1.12
6	Programmable gain	1.00

8.3.4 Offset Correction

The ADS4128 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the EN OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The correction loop time constant is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 8.

Table 8. Offset Correction Loop Time Constant

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0000	1 M	4 ms
0001	2 M	8 ms
0010	4 M	16.7 ms
0011	8 M	33.5 ms
0100	16 M	67 ms
0101	32 M	134 ms

(1) Sampling frequency, f_S = 200 MSPS.

Table 8. Offset Correction Loop Time Constant (continued)

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0110	64 M	268 ms
0111	128 M	537 ms
1000	256 M	1.1 s
1001	512 M	2.15 s
1010	1 G	4.3 s
1011	2 G	8.6 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for every clock cycle offset correction. Note that offset correction is disabled by default after reset.

After a reset, the device is in low-latency mode and offset correction is disabled. To use offset correction:

- First, disable low-latency mode (DIS LOW LATENCY = 1).
- Then set EN OFFSET CORR to 1 and program the required time constant.

8.3.5 Power Down

The ADS4128 has three power-down modes: power-down global, standby, and output buffer disable.

8.3.5.1 Global Power-Down

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) are powered down, resulting in reduced total power dissipation of approximately 10 mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100 µs. To enter the global power-down mode, set the PDN GLOBAL register bit.

8.3.5.2 Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5 µs. The total power dissipation in standby mode is approximately 185 mW. To enter standby mode, set the STBY register bit.

8.3.5.3 Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wakeup time from this mode is fast, approximately 100 ns. This mode can be controlled by using the PDN OBUF register bit or the OE pin.

8.3.5.4 Input Clock Stop

In addition, the converter enters low-power mode when the input clock frequency falls below 1 MSPS. Power dissipation is approximately 80 mW.

8.3.6 Power-Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

8.3.7 Output Data Format

Two output data formats are supported: binary twos complement and offset binary. These formats can be selected by using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

8.4 Device Functional Modes

The ADS4128 has several modes that can be configured using a serial programming interface, as described in Table 9, Table 10, and Table 11. In addition, the device has two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 9. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (DATA FORMAT AND OUTPUT INTERFACE)
0, 100 mV/–0 mV	Twos complement and DDR LVDS
(3/8) AVDD ± 100 mV	Twos complement and parallel CMOS
(5/8) AVDD ± 100 mV	Offset binary and parallel CMOS
AVDD, 0 mV/–100 mV	Offset binary and DDR LVDS

Table 10. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 11. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

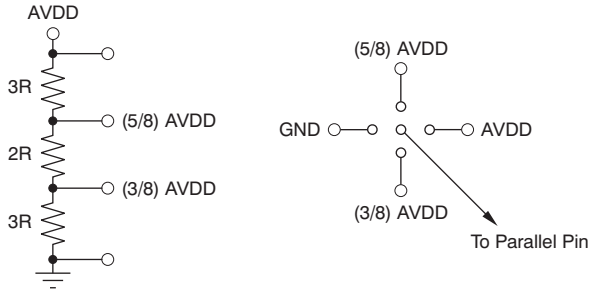


Figure 37. Simplified Diagram to Configure DFS Pin

Table 12. High Performance Modes (1)(2)(3)

MODE	DESCRIPTION
Mode 1	Set the MODE 1 register bits to get best performance across sample clock and input signal frequencies. Register address = 03h, register data = 03h
Mode 2	Set the MODE 2 register bit to get best performance at high input signal frequencies. Register address = 4Ah, register data = 01h

(1) It is recommended to use these modes to get best performance. These modes can be set using the serial interface only.
(2) See the *Serial Interface* section for details on register programming.
(3) Note that these modes cannot be set when the serial interface is not used (when the RESET pin is tied high); see the *Programming* section.

8.4.1 Output Interface Modes

The ADS4128 provides 12-bit data and an output clock synchronized with the data.

8.4.1.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. These modes can be selected by using the LVDS CMOS serial interface register bit or the DFS pin.

8.4.1.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 38.

Even data bits (D0, D2, D4, and so on) are output at the CLKOUTP falling edge and the odd data bits (D1, D3, D5, and so on) are output at the CLKOUTP rising edge. Both the CLKOUTP rising and falling edges must be used to capture all 12 data bits, as shown in Figure 39.

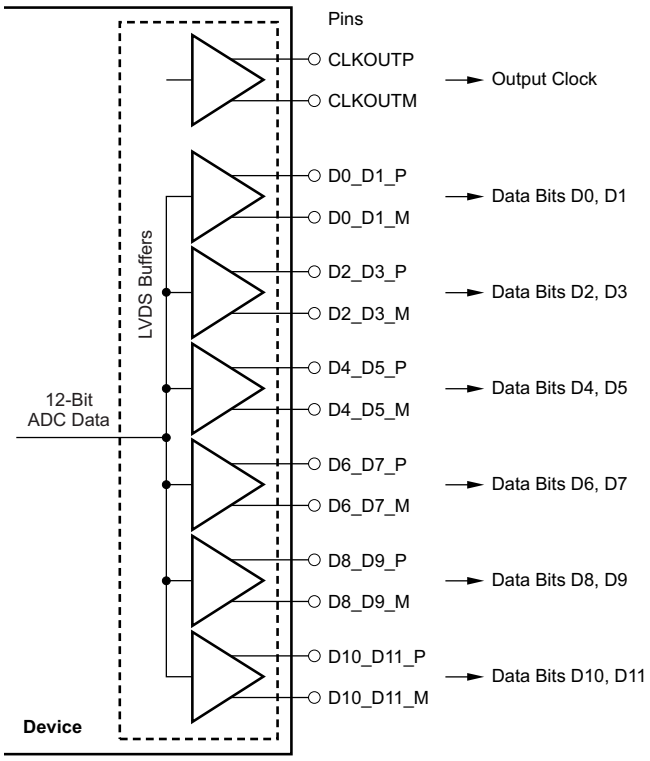


Figure 38. LVDS Data Outputs

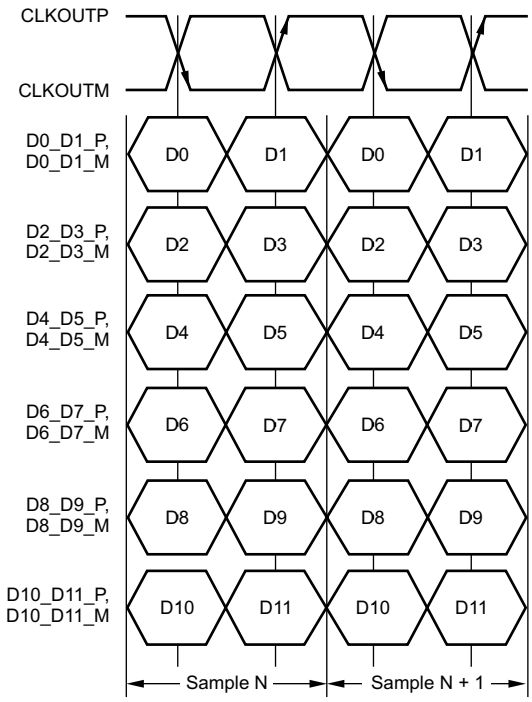


Figure 39. DDR LVDS Interface

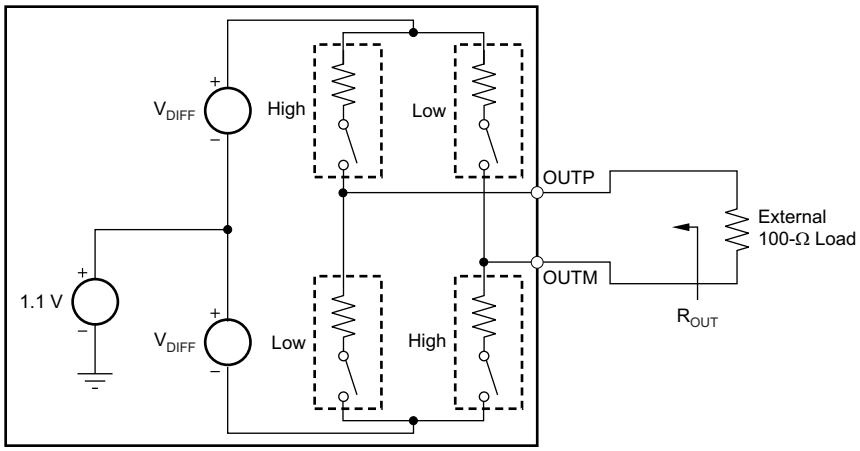
8.4.1.3 LVDS Output Data and Clock Buffers

The equivalent circuit of each LVDS output buffer is shown in Figure 40. After reset, the buffer presents a 100-Ω output impedance to match the external 100-Ω termination.

V_{DIFF} voltage is nominally 350 mV, resulting in a ±350-mV output swing with a 100-Ω external termination. V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the LVDS buffer strength to support 50-Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. This mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.



NOTE: Use the default buffer strength to match the 100-Ω external termination (R_{OUT} = 100 Ω). To match with a 50-Ω external termination, set the LVDS STRENGTH bit (R_{OUT} = 50 Ω).

Figure 40. LVDS Buffer Equivalent Circuit

8.4.1.4 Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The output clock CLKOUT rising edge can be used to latch data in the receiver. Figure 41 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window (even at 200 MSPS) is provided so the data outputs have minimal load capacitance. It is recommended to use short traces (one to two inches or 2,54 cm to 5,08 cm) terminated with less than 5-pF load capacitance; see Figure 42.

In some high-speed applications using CMOS interface, it may be required to use an external clock to capture data. For such cases, delay from the input clock to output data and the data valid times are specified for higher sampling frequencies. These timings can be used to delay the input clock appropriately and use it to capture data.

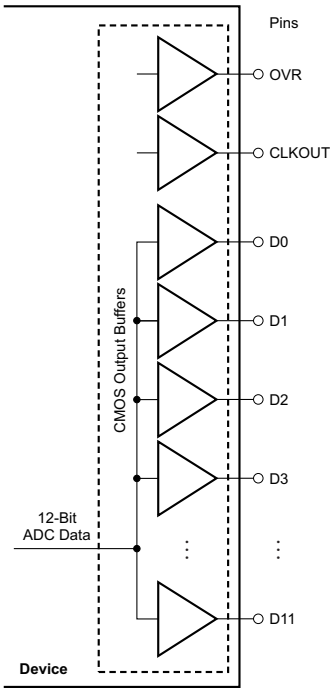


Figure 41. CMOS Output Interface

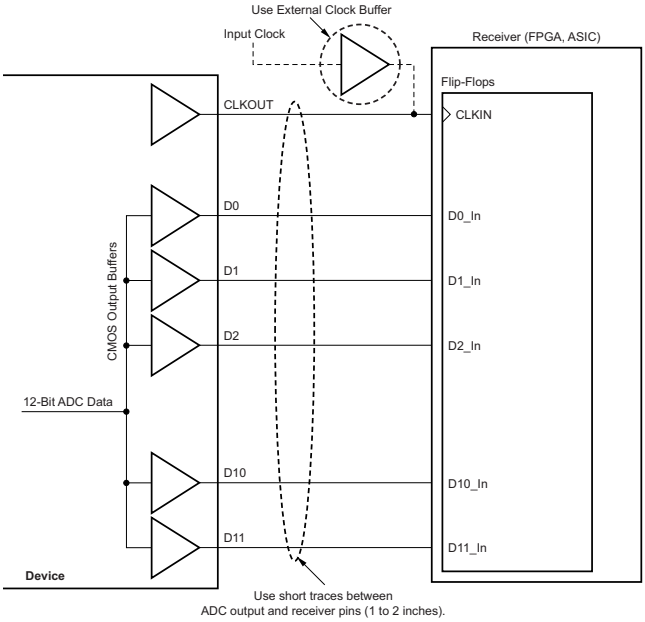


Figure 42. Using the CMOS Data Outputs

8.4.1.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current is determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital Current as a Result of CMOS Output Switching = $C_L \times DRVDD \times (N \times f_{AVG})$

where:

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching. (1)

shows the current across sampling frequencies at a 2-MHz analog input frequency.

8.4.1.6 Input Over-Voltage Indication (OVR Pin)

The device has an OVR pin that provides information about analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off of a DRVDD supply), independent of the output data interface (DDR LVDS or CMOS).

For a positive overload, the D[11:0] output data bits are FFFh in offset binary output format and 7FFh in twos complement output format. For a negative input overload, the output code is 000h in offset binary output format and 800h in twos complement output format.

8.5 Programming

8.5.1 Serial Register Readout

The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to 1. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.

8.5.2 Serial Interface

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can function with an SCLK frequency from 20 MHz down to very low speeds (of a few Hertz) and also with a non-50% SCLK duty cycle.

8.5.2.1 Register Initialization

After power-up, the internal registers must be initialized to default values. This initialization can be accomplished in one of two ways:

1. Either through hardware reset by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 7; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

8.6 Register Maps

Serial Interface Register Map(1) summarizes the functions supported by the serial interface.

8.6.1 Serial Interface Register Map(1)

REGISTER ADDRESS	DEFAULT VALUE AFTER RESET	REGISTER DATA							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
03	00	0	0	0	0	0	0	HIGH PERF MODE 1	
25	00	GAIN				DISABLE GAIN	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		EN OFFSET CORR	0	0	0	0	0
3F	00	CUSTOM PATTERN HIGH D[11:4]							
40	00	CUSTOM PATTERN D[3:0]				0	0	0	0
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL
42	00	CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	0
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
4A	00	0	0	0	0	0	0	0	HIGH PERF MODE 2
BF	00	OFFSET PEDESTAL						0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DF	00	0	0	LOW SPEED		0	0	0	0

(1) Multiple register functions can be programmed in a single write operation.

8.6.2 Register Description

For best performance, two special mode register bits must be enabled:

HI PERF MODE 1 and HI PERF MODE 2.

Table 13. Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] Always write 0

Bit 1 RESET: Software reset applied

This bit resets all internal registers to default values and self-clears to 0 (default = 1).

Bit 0 READOUT: Serial readout

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.
1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout.

Table 14. Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] LVDS SWING: LVDS swing programmability(1)

000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing *increases* to ±410 mV
110010 = LVDS swing *increases* to ±465 mV
010100 = LVDS swing *increases* to ±570 mV
111110 = LVDS swing *decreases* to ±200 mV
001111 = LVDS swing *decreases* to ±125 mV

Bits[1:0] Always write 0

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Table 15. Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits[7:2] Always write 0

Bits[1:0] HI PERF MODE 1: High-performance mode 1

00 = Default performance after reset
01 = Do not use
10 = Do not use
11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

Table 16. Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				DISABLE GAIN	TEST PATTERNS		

Bits[7:4] GAIN: Gain programmability

These bits set the gain programmability in 0.5-dB steps.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1.0-dB gain
0011 = 1.5-dB gain
0100 = 2.0-dB gain
0101 = 2.5-dB gain
0110 = 3.0-dB gain
0111 = 3.5-dB gain
1000 = 4.0-dB gain
1001 = 4.5-dB gain
1010 = 5.0-dB gain
1011 = 5.5-dB gain
1100 = 6.0-dB gain

Bit 3 DISABLE GAIN: Gain setting

This bit sets the gain.
0 = Gain enabled; gain is set by the GAIN bits only if low-latency mode is disabled
1 = Gain disabled

Bits[2:0] TEST PATTERNS: Data capture

These bits verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern

Output data D[11:0] is an alternating sequence of *010101010101* and *101010101010*.

100 = Outputs digital ramp

Output data increments by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095

101 = Output custom pattern (use registers 3Fh and 40h for setting the custom pattern)
110 = Unused
111 = Unused

Table 17. Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] Always write 0

Bit 1 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength

This bit determines the external termination to be used with the LVDS output clock buffer.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2×strength)

Bit 0 LVDS DATA STRENGTH: LVDS data buffer strength

This bit determines the external termination to be used with all of the LVDS data buffers.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2×strength)

Table 18. Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits[7:6] DATA FORMAT: Data format selection

These bits selects the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] Always write 0

Table 19. Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4

Bits[7:0] CUSTOM PATTERN

These bits set the custom pattern.

Table 20. Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0	0	0

Bits[7:2] CUSTOM PATTERN

These bits set the custom pattern.

Bits[3:0] Always write 0

Table 21. Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.
00 = The DFS pin controls the selection of either LVDS or CMOS interface
10 = The DFS pin controls the selection of either LVDS or CMOS interface
01 = DDR LVDS interface
11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

Controls strength of CMOS output clock only.
00 = Maximum strength (recommended and used for specified timings)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bit 3 ENABLE CLKOUT RISE

0 = Disables control of output clock rising edge
1 = Enables control of output clock rising edge

Bits[2:1] CLKOUT RISE POSN: CLKOUT rise control

Controls position of output clock rising edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 500 ps, hold increases by 500 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 100 ps, hold increases by 100 ps
10 = Setup reduces by 200 ps, hold increases by 200 ps
11 = Setup reduces by 1.5 ns, hold increases by 1.5 ns

Bit 0 ENABLE CLKOUT FALL

0 = Disables control of output clock falling edge
1 = Enables control of output clock falling edge

Table 22. Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL CTRL		0	0	DIS LOW LATENCY	STBY	0	0

Bits[7:6] CLKOUT FALL CTRL

Controls position of output clock falling edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 400 ps, hold increases by 400 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Falling edge is advanced by 100 ps
10 = Falling edge is advanced by 200 ps
11 = Falling edge is advanced by 1.5 ns

Bits[5:4] Always write 0

Bit 3 DIS LOW LATENCY: Disable low latency

This bit disables low-latency mode.
0 = Low-latency mode is enabled. Digital functions such as gain, test patterns, and offset correction are disabled.
1 = Low-latency mode is disabled. This setting enables the digital functions. See the *Digital Functions and Low-Latency Mode* section.

Bit 2 STBY: Standby mode

This bit sets the standby mode.
0 = Normal operation
1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits[1:0] Always write 0

Table 23. Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 0 Always write 0

Bit 6 PDN GLOBAL: Power-down

This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 Always write 0

Bit 4 PDN OBUF: Power-down output buffer

This bit set the output data and clock pins.
0 = Output data and clock pins enabled
1 = Output data and clock pins powered down and put in high-impedance state

Bits[3:2] Always write 0

Bits[1:0] EN LVDS SWING: LVDS swing control

00 = LVDS swing control using LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

Table 24. Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HI PERF MODE 2

Bits[7:1] Always write 0

Bit[0] HI PERF MODE 2: High-performance mode 2

This bit is recommended for high input signal frequencies greater than 230 MHz.
0 = Default performance after reset
1 = For best performance with high-frequency input signals, set the HIGH PERF MODE 2 bit

Table 25. Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL				0	0	0	0

Bits[7:4] OFFSET PEDESTAL

These bits set the offset pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

OFFSET PEDESTAL VALUE	PEDESTAL
0111	7 LSB
0110	6 LSB
0101	5 LSB
—	—
000000	0 LSB
—	—
1111	–1 LSB
1110	–2 LSB
—	—
1000	–8 LSB

Bits[3:0] Always write 0

Table 26. Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	BYPASS OFFSET CORR	OFFSET CORR TIME CONSTANT				0	0

Bit 7 FREEZE OFFSET CORR

This bit sets the freeze offset correction.
0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)
1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle. See *Offset Correction*.

Bit 6 Always write 0

Bits[5:2] OFFSET CORR TIME CONSTANT

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE	TIME CONSTANT (Number of Clock Cycles)

0000	1 M
0001	2 M
0010	4 M
0011	8 M
0100	16 M
0101	32 M
0110	64 M
0111	128 M
1000	256 M
1001	512 M
1010	1 G
1011	2 G

Bits[1:0] Always write 0

Table 27. Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits[7:1] Always write 0

Bit 0 LOW SPEED: Low-speed mode

00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80 MSPS.
11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80 MSPS.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Analog Input

The analog input consists of a switched-capacitor-based, differential, sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input INP and INM pin must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Figure 43 shows an equivalent circuit for the analog input.

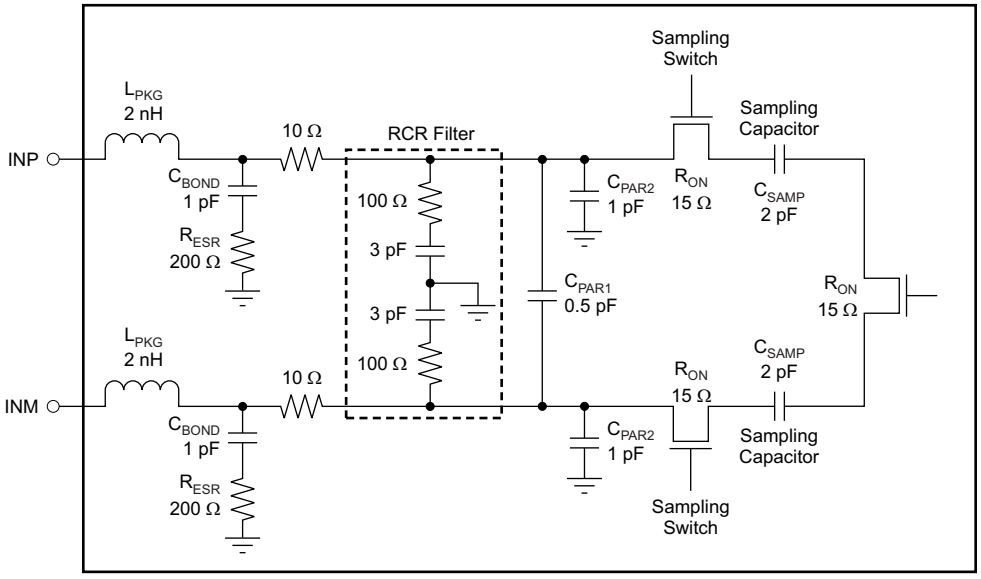


Figure 43. Analog Input Equivalent Circuit

Application Information (continued)

9.1.2 Driving Circuit

Two example driving circuit configurations are shown in Figure 44 and Figure 45—one is optimized for low bandwidth and the other is optimized for high bandwidth to support higher input frequencies. In Figure 44, an external R-C-R filter with 3.3 pF is used to help absorb sampling glitches. The R-C-R filter limits the drive circuit bandwidth, making it suitable for low input frequencies (up to 250 MHz). Transformers such as ADT1-1WT or WBC1-1 can be used up to 250 MHz.

For higher input frequencies, the R-C-R filter can be dropped. Together with the lower series resistors (5 Ω to 10 Ω), this drive circuit provides higher bandwidth to support frequencies up to 500 MHz (as shown in Figure 45). A transmission line transformer (such as ADTL2-18) can be used.

Note that both drive circuits are terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 0.95-V common-mode (VCM) from the device. This termination allows the analog inputs to be biased around the required common-mode voltage.

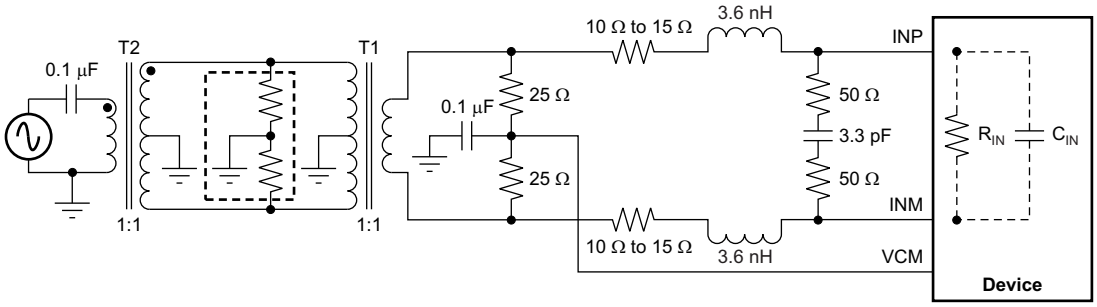


Figure 44. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

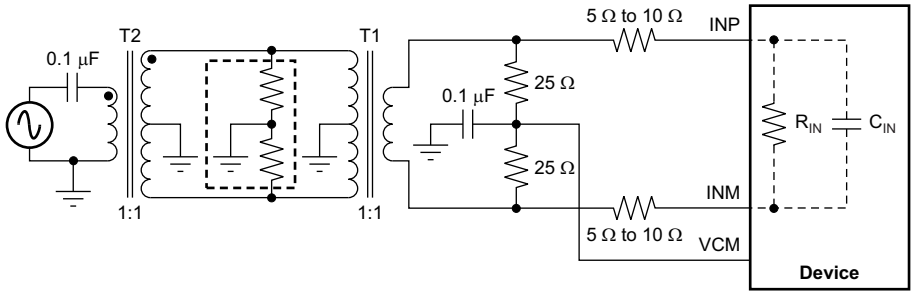


Figure 45. Drive Circuit with High Bandwidth (for High Input Frequencies)

The transformer parasitic capacitance mismatch (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers; refer to Figure 44 and Figure 45. The termination center point is connected to ground to improve the balance between the P (positive) and M (negative) sides. The termination values between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance).

Figure 44 and Figure 45 use 1:1 transformers with a 50-Ω source. As explained in the *Drive Circuit Requirements* section, this architecture helps to present a low source impedance to absorb sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a band-pass or low-pass filter is needed to get the desired dynamic performance, as shown in Figure 46. Such a filter presents low source impedance at the high frequencies corresponding to the sampling glitch and helps avoid performance loss with the high source impedance.

Application Information (continued)

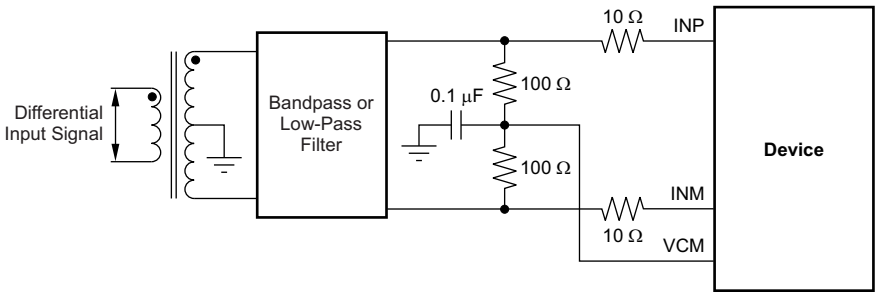


Figure 46. Drive Circuit with 1:4 Transformer

9.1.2.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (less than 50 Ω) for the common-mode switching currents. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches created when the sampling capacitors open and close. The R-C filter cutoff frequency involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the external driving circuit to support the sampling glitches.

In the ADS4128, the R-C component values have been optimized while supporting high input bandwidth (550 MHz). However, in applications where very high input frequency support is not required, glitch filtering can be further improved with an external R-C-R filter; see Figure 44 and Figure 45).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched source impedance. While designing the drive circuit, the ADC impedance must be considered. Figure 47 and Figure 48 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

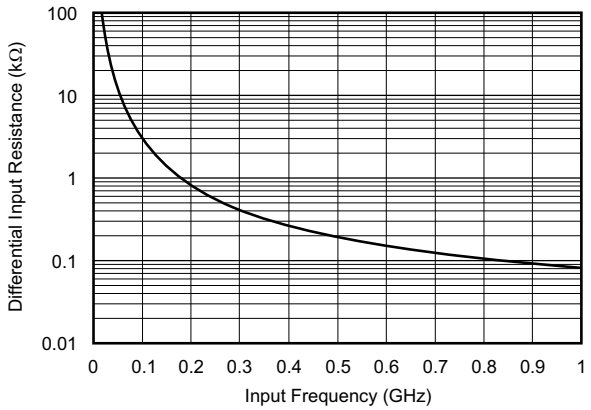


Figure 47. ADC Analog Input Resistance (R_{IN}) Across Frequency

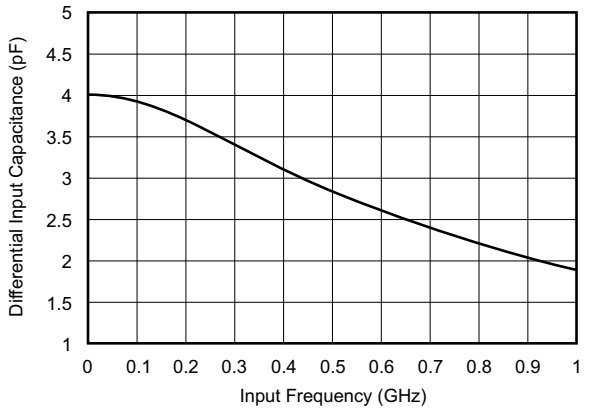


Figure 48. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Application Information (continued)

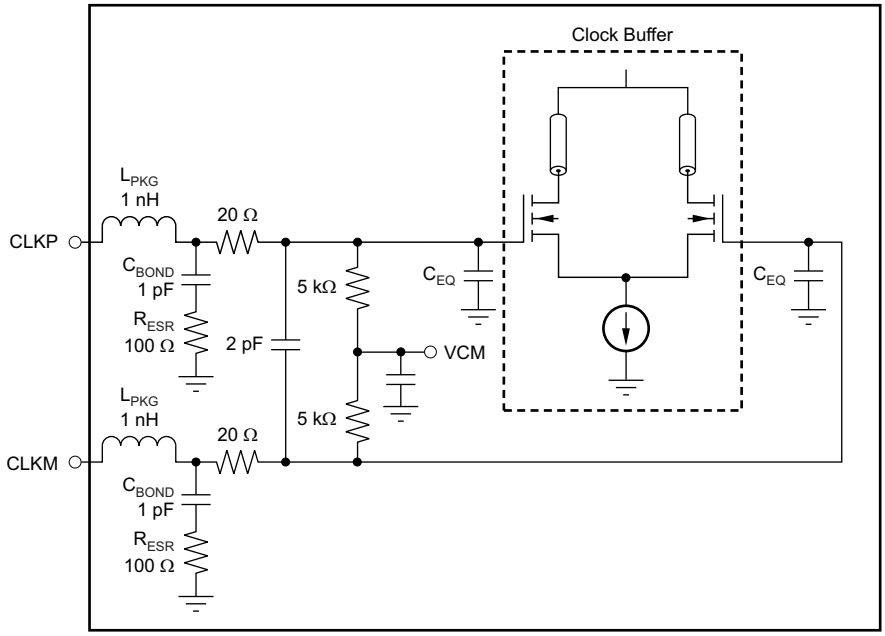
9.1.3 Analog Input

9.1.3.1 Input Common-Mode

To ensure a low-noise, common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each ADC input pin sinks a common-mode current of approximately 0.6 µA per MSPS of clock frequency.

9.1.4 Clock Input

The ADS4128 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 49 shows an equivalent circuit for the input clock.



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 49. Input Clock Equivalent Circuit

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 50. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 51 shows a differential circuit.

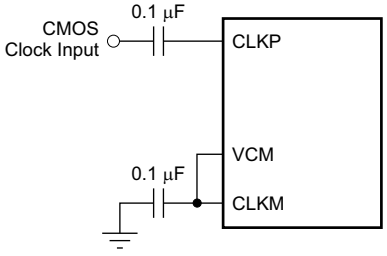


Figure 50. Single-Ended Clock Driving Circuit

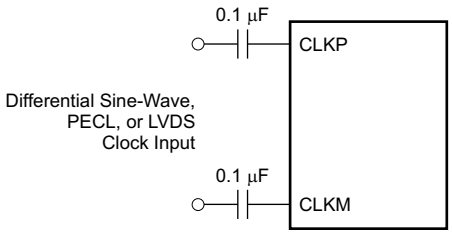
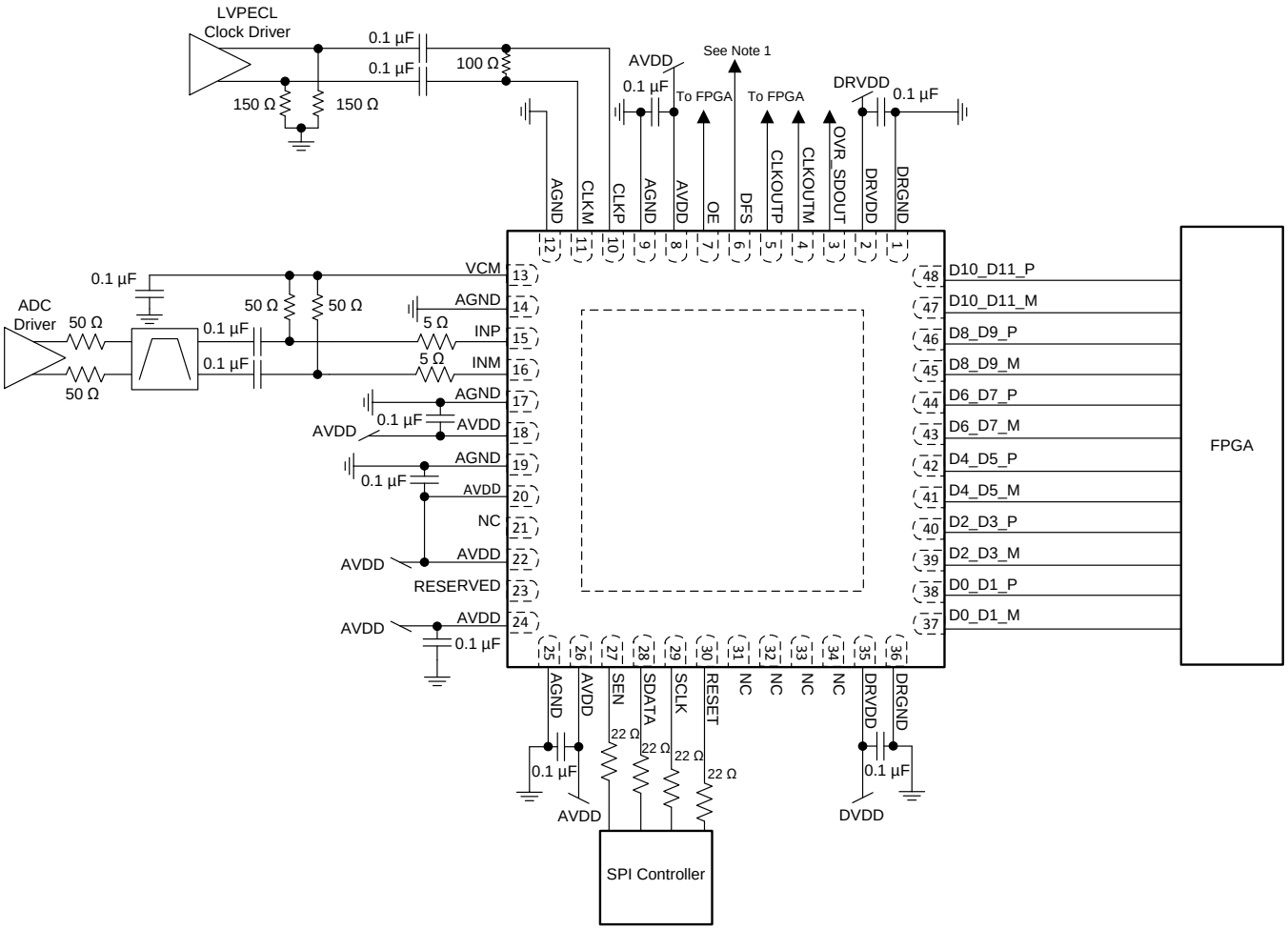


Figure 51. Differential Clock Driving Circuit

9.2 Typical Application

An example schematic for a typical application of the ADS4128 is shown in Figure 52.



(1) Set per mode of operation.

Figure 52. Example Schematic for ADS4128

9.2.1 Design Requirements

Example design requirements are listed in Table 28 for the ADC portion of the signal chain. These do not necessary reflect the requirements of an actual system, but rather demonstrate why the ADS4128 may be chosen for a system based on a set of requirements.

Table 28. Example Design Requirements for ADS4128

DESIGN PARAMETER	EXAMPLE DESIGN REQUIREMENT	ADS4128 CAPABILITY
Sampling rate	≥184.32 Msps	Max sampling rate: 200 Msps
Input frequency	>190 MHz to accommodate full 2nd nyquist zone	Large signal –3 dB bandwith: 400 MHz operation
SNR	>65dBFS at –1 dFBS 170 MHz	69 dBFS at –1 dBFS, 170 MHz
SFDR	>80 dBc at –1 dFBS 170 MHz	85 dBc at –1 dBFS, 170 MHz
Input full scale voltage	2 Vpp	2 Vpp
Overload recovery time	< 3 clock cycles	1 clock cycle
Input full scale voltage	Parallel LVDS	Parallel LVDS
Overload recovery time	< 250 mW per channel	230 mW per channel

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input

The analog input of the ADS4128 is typically driven by a fully differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier affects the combined performance of the ADC and amplifier. The amplifier is often AC coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common-mode voltages. The user can DC couple the amplifier to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

9.2.2.2 Clock Driver

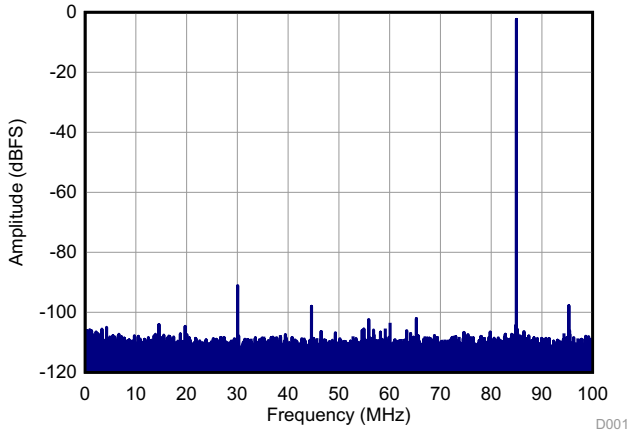
The ADS4128 should be driven by a high performance clock driver such as a clock jitter cleaner. The clock must have low noise to maintain optimal performance. LVPECL is the most common clocking interface, but LVDS and LVCMOS can also be used. Do not drive the clock input from an FPGA unless the noise degradation can be tolerated, such as for input signals near DC where the clock noise impact is minimal.

9.2.2.3 Digital Interface

The ADS4128 supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs, resistors must be placed in series with the outputs to reduce the output current spikes and limit the performance degradation. The resistors must be large enough to limit current spikes, but not so large as to significantly distort the digital output waveform. An external CMOS buffer must be used when driving distances greater than a few inches, to reduce ground bounce within the ADC.

9.2.3 Application Curve

Figure 53 shows the result of a 115-MHz signal sampled at 200 MHz captured by the ADS4128



SNR = 70.13 dBFs SFDR= 83.75 dBFs

THD= 79.72 dBs SINAD= 69.90 dBFs

Figure 53. 115-MHz Signal Captured by ADS4128

10 Power Supply Recommendations

The ADS4128 has two power supplies, one analog (AVDD) and one digital (DRVDD) supply. Both supplies have a nominal voltage of 1.8 V. The AVDD supply is noise sensitive and the digital supply is not.

10.1 Sharing DRVDD and AVDD Supplies

For best performance, the AVDD supply should be driven by a low-noise linear regulator (LDO) and separated from the DRVDD supply. AVDD and DRVDD can share a single supply, but they should be isolated by a ferrite bead and bypass capacitors, in a PI-filter configuration, at a minimum. The digital noise is concentrated at the sampling frequency and harmonics of the sampling frequency, and could contain noise related to the sampled signal. While developing schematics, leave extra placeholders for additional supply filtering.

10.2 Using DC/DC Power Supplies

DC/DC switching power supplies can be used to power DRVDD without issue. AVDD can be powered from a switching regulator. Noise and spurs on the AVDD power supply affect the SNR and SFDR of the ADC, and appear near DC and as a modulated component around the input frequency. If a switching regulator is used, it should have minimal voltage ripple. Supply filtering should be used to limit the amount of spurious noise at the AVDD supply pins. Extra placeholders should be placed on the schematic for additional filtering. Optimize filtering in the final system to achieve the desired performance. The choice of power supply ultimately depends on the system requirements. For instance, if very low phase noise is required, do not use a switching regulator.

10.3 Power Supply Bypassing

Because the ADS4128 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. A 0.1-uF capacitor is recommended near each supply pin. The decoupling capacitors should be placed very close to the converter supply pins.

11 Layout

11.1 Layout Guidelines

11.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS414x, ADS412x EVM User Guide* (SLWU067) for details on layout and grounding.

11.1.2 Supply Decoupling

Because the ADS4128 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

11.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the thermal pad is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271), both available for download at www.ti.com.

11.2 Layout Example

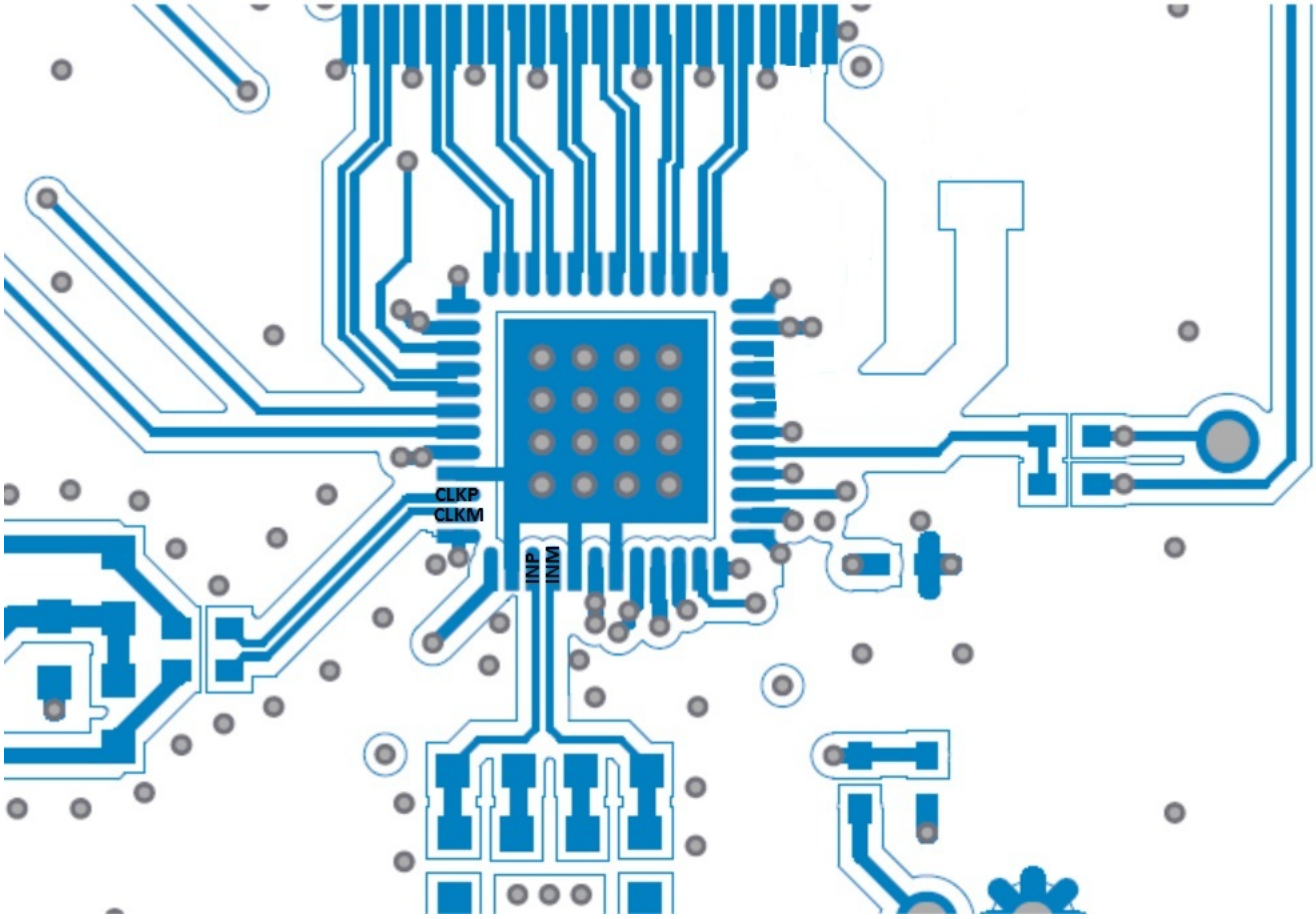


Figure 54. ADS4128EVM PCB Layout

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

模拟带宽 – 基频功率相对低频值下降 3dB 时的模拟输入频率。

孔径延迟 – 从输入采样时钟的上升沿到实际发生采样之间的延迟时间。该延迟在各通道中会有所不同。最大差值被定义为孔径延迟差异（通道间）。

孔径不确定性（抖动） – 采样间的孔径延迟差异。

时钟脉冲宽度/占空比 – 时钟信号的占空比为时钟信号保持逻辑高电平的时间（时钟脉冲宽度）与时钟信号周期的比值。占空比通常以百分比的形式表示。理想差分正弦波时钟的占空比为 50%。

最大转换速率 – 执行指定操作时所采用的最大采样率。除非另外注明，否则所有参数测试均以该采样率执行。

最小转换速率 – ADC 正常工作时的最小采样率。

微分非线性 (DNL) – 理想 ADC 对模拟输入值进行编码转换时以 1 LSB 为步长。DNL 是指任意单个步长与这一理想值之间的偏差（以 LSB 为计量单位）。

积分非线性 (INL) – INL 是 ADC 传递函数与其最小二乘法曲线拟合所确定的最佳拟合曲线的偏差（以 LSB 为计量单位）。

增益误差 – 增益误差是指 ADC 实际输入满量程范围与其理想值的偏差。增益误差以理想输入满量程范围的百分比形式表示。增益误差包括两部分：基准不精确所导致的误差和通道所导致的误差。这两种误差分别定义为 E_{GREF} 和 E_{GCHAN}。

对于一阶近似，总增益误差 $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$。

例如，如果 $E_{TOTAL} = \pm 0.5\%$，则满量程输入范围为 $(1 – 0.5 / 100) \times FS_{ideal}$ 至 $(1 + 0.5 / 100) \times FS_{ideal}$。

偏移误差 – 偏移误差是指 ADC 实际平均空闲通道输出编码与理想平均空闲通道输出编码之间的差值（以 LSB 数表示）。该数量通常转换为毫伏。

温度漂移 – 温度漂移系数（相对于增益误差和偏移误差）指定参数从 T_{MIN} 到 T_{MAX} 每摄氏度的变化量。温度漂移的计算方法是用参数在 T_{MIN} 至 T_{MAX} 范围内的最大变化量除以 $T_{MAX} – T_{MIN}$ 的值。

信噪比 – SNR 是指基频功率 (P_S) 与噪底功率 (P_N) 的比值，不包括直流功率和前 9 个谐波的功率。

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (2)$$

当基频的绝对功率用作基准时，SNR 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SNR 以 dBFS（相对于满量程的分贝数）为单位。

信噪比和失真 (SINAD) – SINAD 是指基频功率 (P_S) 与所有其他频谱成分（包括噪声 (P_N) 和失真 (P_D)，但不包括直流）功率的比值。

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (3)$$

当基频的绝对功率用作基准时，SINAD 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，SINAD 以 dBFS（相对于满量程的分贝数）为单位。

有效位数 (ENOB) – ENOB 测量的是转换器相对于理论限值（基于量化噪声）的性能。

$$ENOB = \frac{SINAD – 1.76}{6.02} \quad (4)$$

总谐波失真 (THD) – THD 是指基频功率 (P_S) 与前 9 个谐波功率 (P_D) 的比值。

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (5)$$

器件支持 **(接下页)**

THD 通常以 dBc 为单位（相对于载波的分贝数）。

无杂散动态范围 (SFDR) – 基频功率与最高的其他频谱成分（毛刺或谐波）功率的比值。SFDR 通常以 dBc 为单位（相对于载波的分贝数）。

双频互调失真 – IMD3 是指基频功率（f_1 和 f_2 频率处）与最差频谱成分（$2f_1 – f_2$ 或 $2f_2 – f_1$ 频率处）功率的比值。当基频的绝对功率用作基准时，IMD3 以 dBc（相对于载波的分贝数）为单位；当基频功率被外推至转换器满量程范围时，IMD3 以 dBFS（相对于满量程的分贝数）为单位。

直流电源抑制比 (DC PSRR) – DC PSSR 是偏移误差变化量与模拟电源电压变化量的比值。DC PSRR 通常以 mV/V 为单位进行表示。

交流电源抑制比 (AC PSRR) – AC PSRR 测量的是 ADC 对电源电压变化的抑制能力。如果 ΔV_{SUP} 表示电源电压的变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (6)$$

电压过载恢复 – 使过载的模拟输入端的误差恢复至 1% 以下所需的时钟数。该技术参数的测试方法是分别施加具有 6dB 正过载和负过载的正弦波信号。然后记录下过载后前几个采样（相对于期望值）的偏差。

共模抑制比 (CMRR) – CMRR 测量的是 ADC 对模拟输入共模变化的抑制能力。如果 ΔV_{CM_IN} 表示输入引脚的共模电压变化，ΔV_{OUT} 表示 ADC 输出编码的相应变化（相对输入而言），则：

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (7)$$

串扰（仅限多通道 ADC）– 串扰测量的是目标通道与其相邻通道之间的内部信号耦合。串扰分两种情况：一种是与紧邻通道（近端通道）之间的耦合，另一种是与跨封装通道（远端通道）之间的耦合。通常采用对邻近通道施加满量程信号的方式来测量串扰。串扰是指耦合信号功率（在目标通道的输出端测得）与邻近通道输入端所施加信号功率的比值。串扰通常以 dBc 为单位进行表示。

12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《QFN 布局指南》*（文献编号：SLOA122）
- *《QFN/SON PCB 连接》*，SLUA271
- *《ADS4226 评估模块》*（文献编号：SLWU067）

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS4128IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4128	Samples
ADS4128IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4128	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

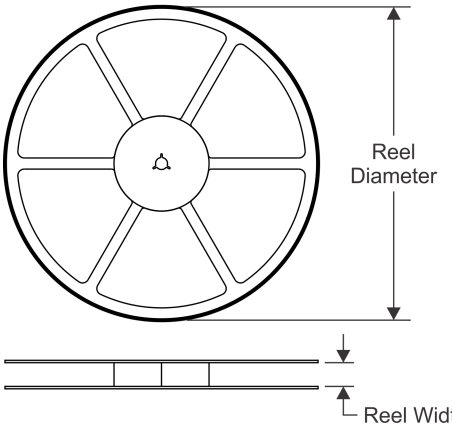
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

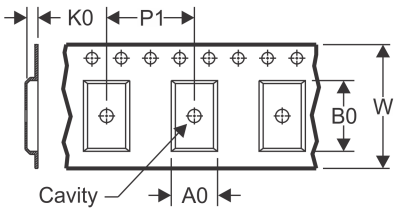
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

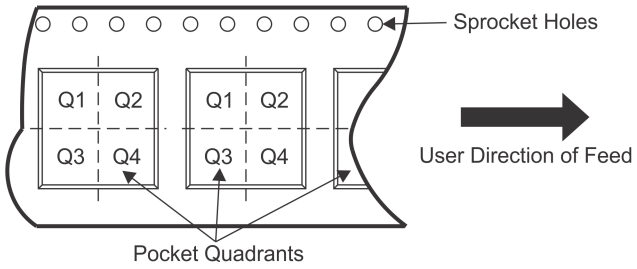


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

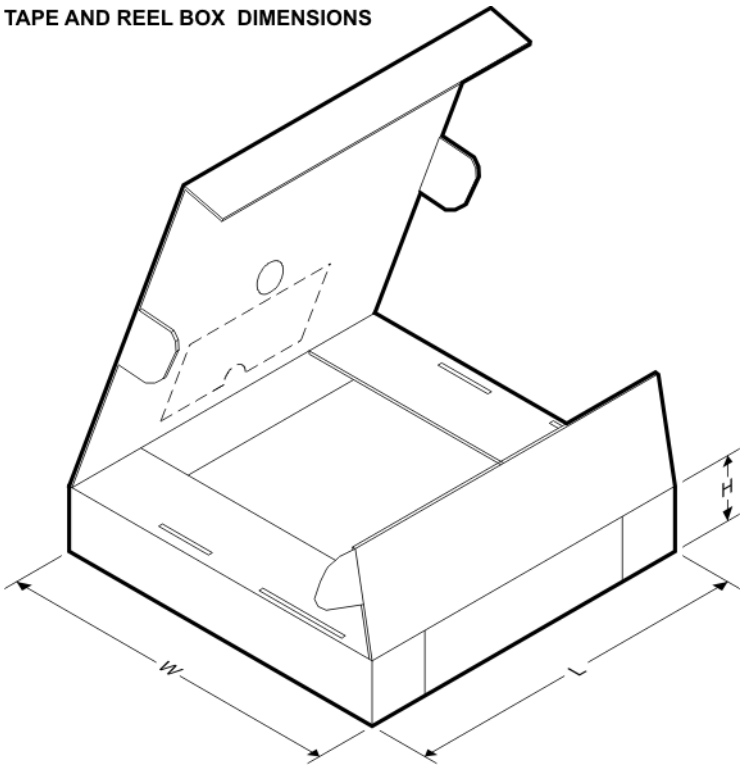
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS4128IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4128IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

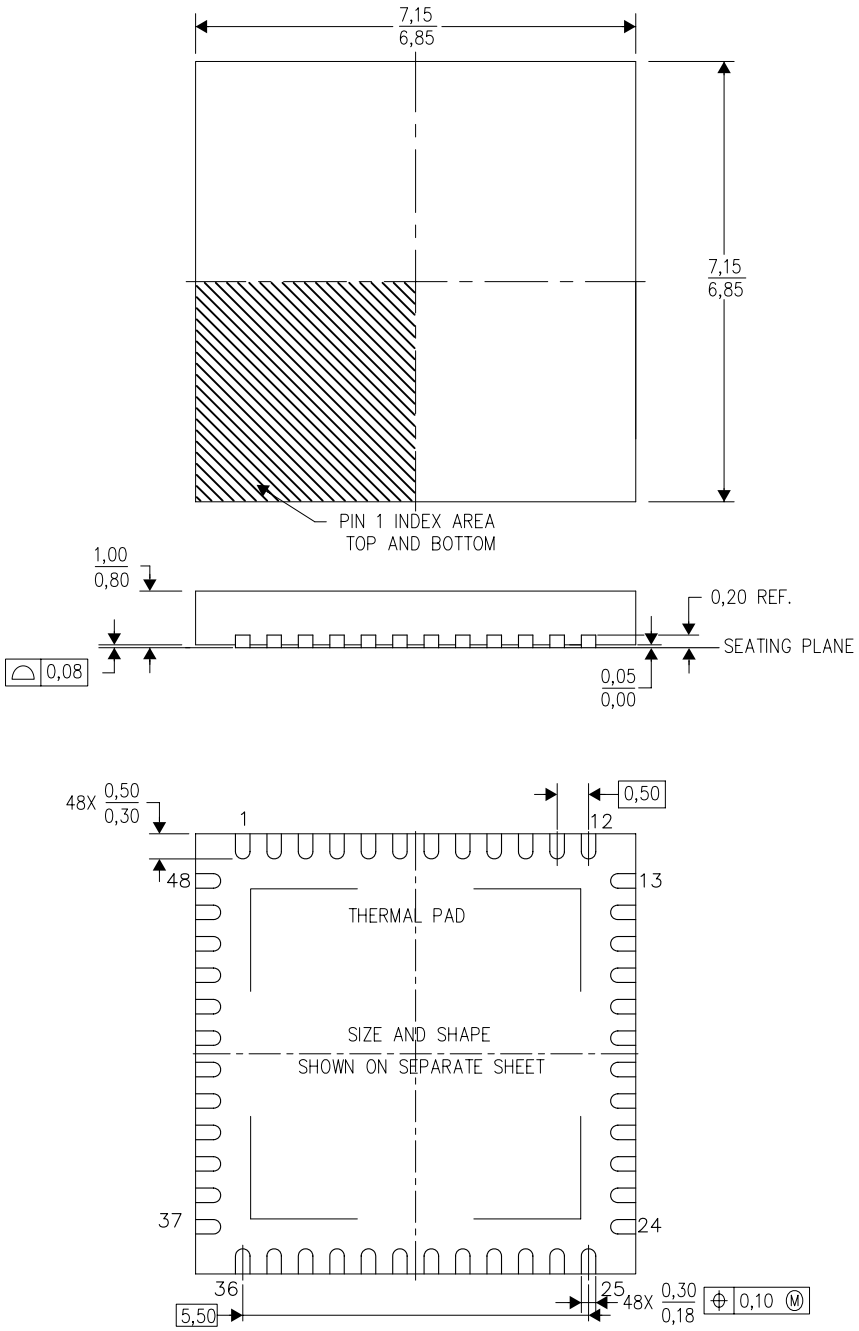
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS4128IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS4128IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

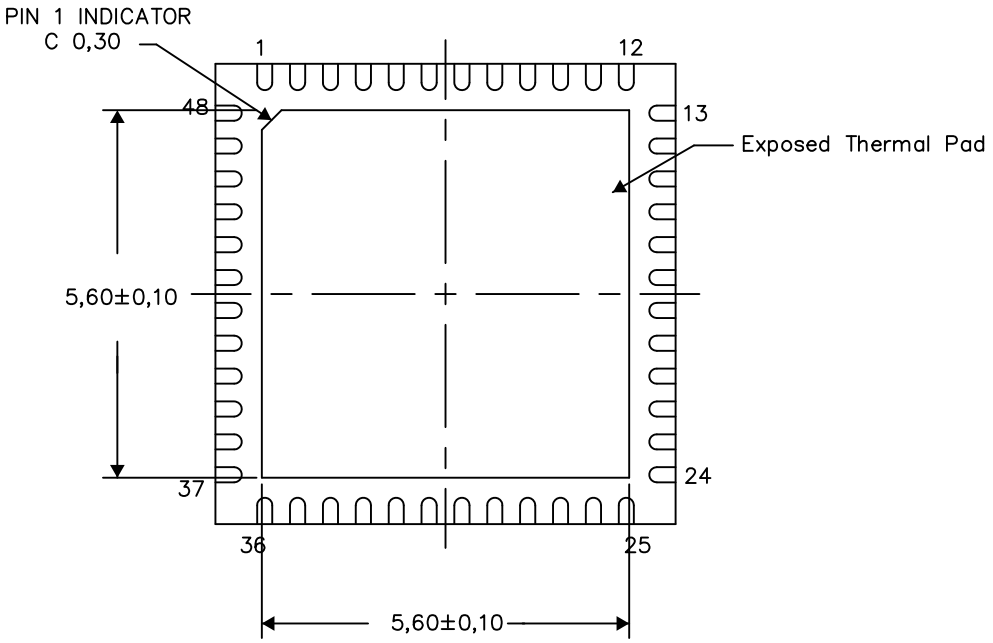
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



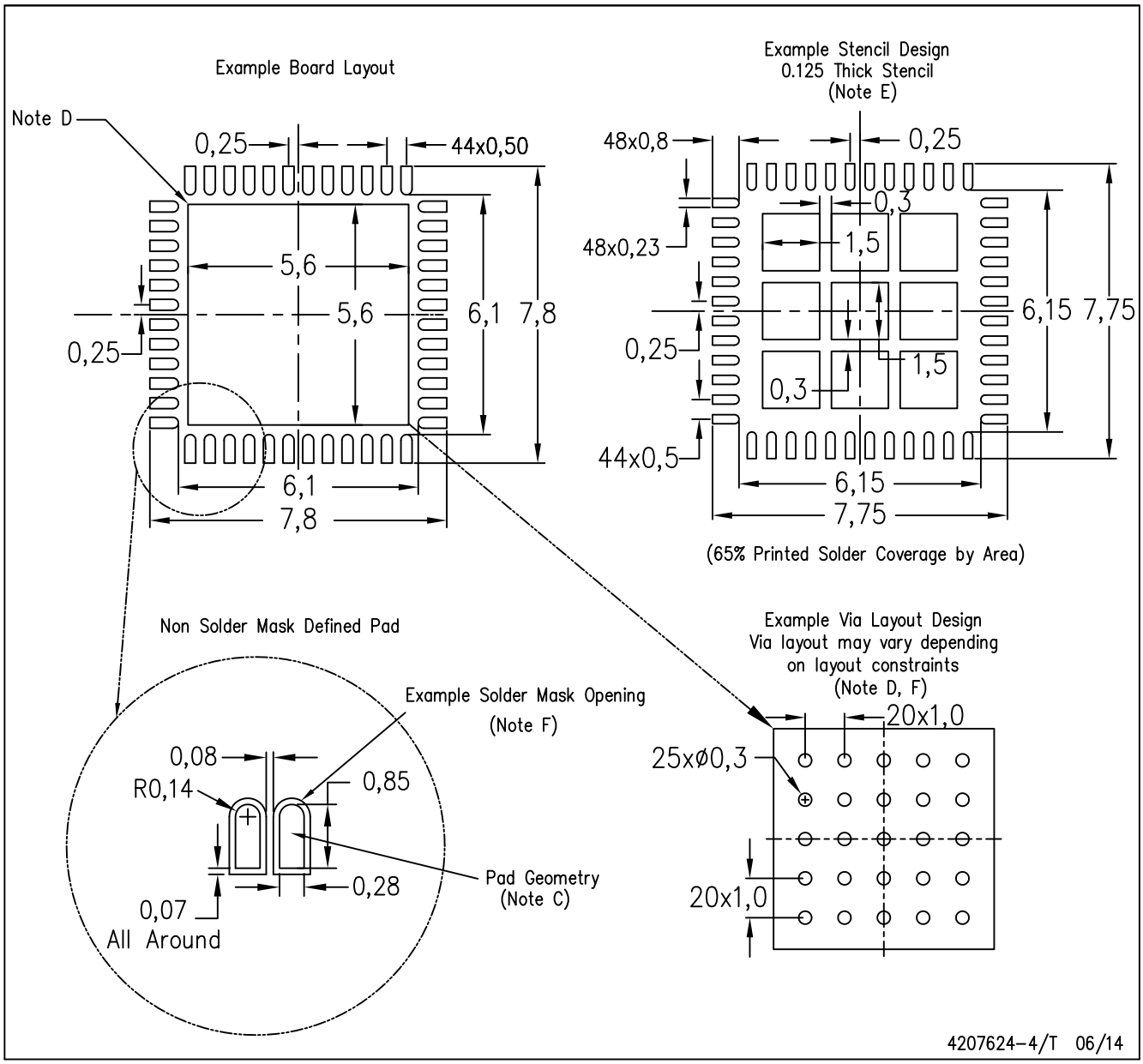
Bottom View

Exposed Thermal Pad Dimensions

4206354–5/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

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只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

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