OVUV_OTUT_CMP

REVISION HISTORY

Revision Number	Date	Description of Change	Author
V0.0	9/21/2022	Draft version	Su Aixue

Table of Contents

OVUV_OTUT_CMP

Introduction

The OVUV_OTUT_CMP is a 31-channel comparator. The comparator can generate fault warning signal when the chip is over-voltage, under-voltage, over-temperature, and under-temperature. Thus, it can be applied to protect the chip from entering into abnormal working state.

The OVUV_OTUT_CMP module has the following features:
• Latch OVUV_OTUT_EN_REG, CELL_OV_THRESH_REG, CELL_UV_THRESH_REG, GPIO_OTUT_THRESH_SEL_REG, GPIO_OT_PACK_THRESH_REG, GPIO_OT_PCB_THRESH_REG, GPIO_UT_PACK_THRESH_REG, GPIO_UT_PCB_THRESH_REG, CB_OT_PACK_THRESH_REG, CB_OT_PCB_THRESH_REG, OVUV_DEGL_REG to OVUV_OTUT_EN, CELL_OV_THRESH, CELL_UV_THRESH, GPIO_OTUT_THRESH_SEL, GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH, OVUV_DEGL once MON_WAKE_GO or ADC_GO_DLY is high; (HWR001_OVUV_OTUT_CMP)
• Compare ADC_DATA_LPF with CELL_OV_THRESH and CELL_UV_THRESH when RR_END is high, and output CELL_OVUV according to OVUV_DEGL when OVUV_OTUT_EN is high; (HWR002_OVUV_OTUT_CMP)
• Compare OTH_ADC_DATA with GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH according to GPIO_OTUT_THRESH_SEL when RR_END is high, and output GPIO_OTUT, GPIO_CBOT when OVUV_OTUT_EN is high; (HWR003_OVUV_OTUT_CMP)
• Reset when OVUV_OTUT_EN is low; (HWR004_OVUV_OTUT_CMP)
• Output CELL_OVUV until counter=OVUV_DEGL; (HWR005_OVUV_OTUT_CMP)
• The counter will +1 when fault is detected; (HWR005_OVUV_OTUT_CMP)
• The max of counter is OVUV_DEGL; (HWR005_OVUV_OTUT_CMP)
• The counter will -1 when fault is not detected; (HWR005_OVUV_OTUT_CMP)
• Update TWARN_THRESH_REG into TWARN_THRESH when ADC_GO_DLY or MON_WAKE_GO is high; (HWSR1_OVUV_OTUT_CMP)
• Compare the gap between OTH_ADC_DATA with TWARN_THRESH when RR_END is high; (Once over range, output TWARN) (HWSR2_OVUV_OTUT_CMP)
• TWARN TWARN_THRESH covers from 110℃ to 145℃, 5℃ step; (HWSR2_OVUV_OTUT_CMP)
• OVUV_OTUT_EN is ignored when TWARN comparison. (HWSR3_OVUV_OTUT_CMP)

Register Definition

Register Map

Table 11 OVUV_OTUT_CMP Register Map

ADDRESS	NAME	DESCRIPTION	RESET VALUE
OVUV_OTUT_CMP			
0x0000	**OVUV_OTUT _CONF1**	OVUV_OTUT_CMP configuration register 1	0x80
0x0001	**OVUV_OTUT _CONF2**	OVUV_OTUT_CMP configuration register 2	0x60

0x0002	**OVUV_OTUT _CONF3**	OVUV_OTUT_CMP configuration register 3	0x60
0x0003	**OVUV_OTUT _CONF4**	OVUV_OTUT_CMP configuration register 4	0x7E
0x0004	**OVUV_OTUT _CONF5**	OVUV_OTUT_CMP configuration register 5	0x7E
0x0005	**OVUV_OTUT _CONF6**	OVUV_OTUT_CMP configuration register 6	0x00
0x0006	**OVUV_OTUT _CONF7**	OVUV_OTUT_CMP configuration register 7	0x00
0x0007	**CB_CONF1**	CB configuration register 1	0x7F
0x0008	**CB_CONF2**	CB configuration register 2	0x78
0x000A	**TWARN_CONF**	TWARN configuration register	0x03
0x1FF6	**ADC_CTRL**	ADC control register	0x00

OVUV_OTUT_CONF1

Register 1. OVUV_OTUT _CONF1 (OVUV_OTUT_CMP configuration register 1, offset 0x0000)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**OVUV_OTUT_EN**	R/W	1'b1	OVUV_OTUT_CMP Enable Bit 0: Disable 1: Enable
6:5	**REV**	R	2'b00	Reserved
4:0	**OVUV_ DEGL**	R/W	5'h00	OVUV_OTUT_CMP Deglitch Number 0 0000:1 0 0001:2 0 0010:3 ... 1 1111:32

OVUV_OTUT_CONF2

Register 2. OVUV_OTUT _CONF2 (OVUV_OTUT_CMP configuration register 2, offset 0x0001)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**REV**	R	1'b0	Reserved
6:0	**OV_THR**	R/W	7'h60	Over-voltage Threshold 000 0000:2V 000 0001:2.025V 000 0010:2.05V ... 111 0111:4.975V 111 1000-111 1111:5V

OVUV_OTUT_CONF3

Register 3. OVUV_OTUT _CONF3 (OVUV_OTUT_CMP configuration register 3, offset 0x0002)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**REV**	R	1'b0	Reserved
6:0	**UV_THR**	R/W	7'h60	Under-voltage Threshold 000 0000:0.7V 000 0001:0.725V 000 0010:0.75V

				... 111 1111:3.875V

OVUV_OTUT_CONF4

Register 4. OVUV_OTUT _CONF4 (OVUV_OTUT_CMP configuration register 4, offset 0x0003)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**OT_ PACK_THR**	R/W	1'h0F	Over-temperature Threshold (PACK) 0 0000:5% 0 0001:6% ... 1 1111:36%
2:0	**UT_ PACK_THR**	R/W	3'h6	Under-temperature Threshold (PACK) 000:76% 001:78% ... 111:90%

OVUV_OTUT_CONF5

Register 5. OVUV_OTUT _CONF5 (OVUV_OTUT_CMP configuration register 5, offset 0x0004)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**OT_ PCB_THR**	R/W	1'h0F	Over-temperature Threshold (PCB) 0 0000:5% 0 0001:6% ... 1 1111:36%
2:0	**UT_ PCB_THR**	R/W	3'h6	Under-temperature Threshold (PCB) 000:76% 001:78% ... 111:90%

OVUV_OTUT_CONF6

Register 6. OVUV_OTUT _CONF6 (OVUV_OTUT_CMP configuration register 6, offset 0x0005)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**GPIO7_THR_SEL**	R/W	1'b0	GPIO7 Threshold Select Bit 0: PACK 1: PCB
6	**GPIO6_THR_SEL**	R/W	1'b0	GPIO6 Threshold Select Bit 0: PACK 1: PCB
5	**GPIO5_THR_SEL**	R/W	1'b0	GPIO5 Threshold Select Bit 0: PACK 1: PCB

4	**GPIO4_THR_SEL**	R/W	1'b0	GPIO4 Threshold Select Bit 0: PACK 1: PCB
3	**GPIO3_THR_SEL**	R/W	1'b0	GPIO3 Threshold Select Bit 0: PACK 1: PCB
2	**GPIO2_THR_SEL**	R/W	1'b0	GPIO2 Threshold Select Bit 0: PACK 1: PCB
1	**GPIO1_THR_SEL**	R/W	1'b0	GPIO1 Threshold Select Bit 0: PACK 1: PCB
0	**GPIO0_THR_SEL**	R/W	1'b0	GPIO0 Threshold Select Bit 0: PACK 1: PCB

OVUV_OTUT_CONF7

Register 7. OVUV_OTUT _CONF7 (OVUV_OTUT_CMP configuration register 7, offset 0x0006)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**REV**	R	4'h0	Reserved
3	**GPIO11_THR_SEL**	R/W	1'b0	GPIO11 Threshold Select Bit 0: PACK 1: PCB
2	**GPIO10_THR_SEL**	R/W	1'b0	GPIO10 Threshold Select Bit 0: PACK 1: PCB
1	**GPIO9_THR_SEL**	R/W	1'b0	GPIO9 Threshold Select Bit 0: PACK 1: PCB
0	**GPIO8_THR_SEL**	R/W	1'b0	GPIO8 Threshold Select Bit 0: PACK 1: PCB

CB_CONF1

Register 8. CB_CONF1 (CB configuration register 1, offset 0x0007)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**CB_ROT_PACK_THR**	R/W	5'h0F	CB Over-temperature Threshold (PACK) 0 0000: 5% 0 0001: 6% ... 1 1111: 36%
2:0	**--**	--	--	--

CB_CONF2

Register 9. CB_CONF2 (CB configuration register 2, offset 0x0008)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**CB_ROT_PCB_THR**	R/W	5'h0F	CB Over-temperature Threshold (PCB) 0 0000: 5% 0 0001: 6% ... 1 1111: 36%
2:0	**--**	--	--	--

TWARN_CONF

Register 10. TWARN_CONF (TWARN configuration register, offset 0x000A)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**REV**	R	5'h00	Reserved
2:0	**TWARN_THR**	R/W	3'h3	TWARN Threshold 000:110℃ 001:115℃ … 111:145℃

ADC_CTRL

Register 11. ADC_CTRL (ADC control register, offset 0x1FF6)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**MON_WAKE_GO**	R/W	1'b0	Mon-wake Starting Bit 0: Ready 1: Execute
6:3	**REV**	R	4'h0	Reserved
2:0	**--**	--	--	--

Function Details

Block Diagram

The main elements of OVUV_OTUT_CMP and their interactions are shown in Fig 1.

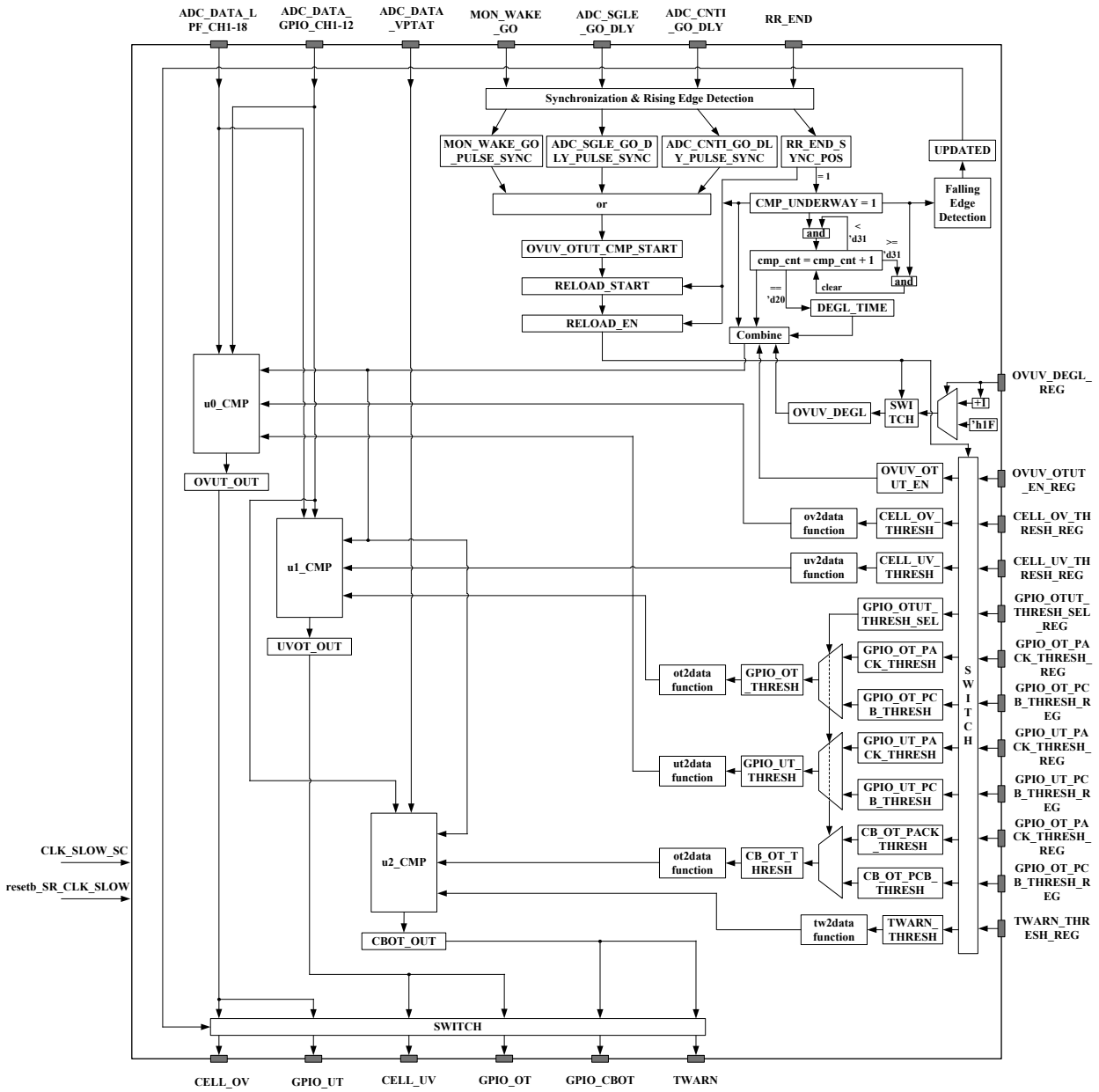

Fig 1. OVUV_OTUT_CMP Block Diagram

OVUV_OTUT_CMP IO Descriptions

This section provides the OVUV_OTUT_CMP IO descriptions.

Table 2 OVUV_OTUT_CMP IO descriptions

Signal	Width	Duration	I/O	Default Value	Register
CLK_SLOW_SC	1	--	I	--	--
resetb_SR_CLK_SLOW	1	--	I	--	--

ADC_SGLE_GO_DLY	1	>1 CLK_SLOW_SC	I	--	--
ADC_CNTI_GO_DLY	1	>1 CLK_SLOW_SC	I	--	--
MON_WAKE_GO	1	>1 CLK_SLOW_SC	I	--	MON_WAKE_GO
OVUV_OTUT_EN_REG	1	--	I	--	OVUV_OTUT_EN
CELL_OV_THRESH_REG	7	--	I	--	OV_THR
CELL_UV_THRESH_REG	7	--	I	--	UV_THR
GPIO_OTUT_THRESH_SEL_REG	12	--	I	--	OVUV_OTUT _CONF6 OVUV_OTUT _CONF7
GPIO_OT_PACK_THRESH_REG	5	--	I	--	OT_ PACK_THR
GPIO_OT_PCB_THRESH_REG	5	--	I	--	OT_ PCB_THR
GPIO_UT_PACK_THRESH_REG	3	--	I	--	UT_ PACK_THR
GPIO_UT_PCB_THRESH_REG	3	--	I	--	UT_ PCB_THR
CB_OT_PACK_THRESH_REG	5	--	I	--	CB_ROT_PACK_THR
CB_OT_PCB _THRESH_REG	5	--	I	--	CB_ROT_PCB_THR
TWARN_THRESH_REG	3	--	I	--	TWARN_THR
OVUV_DEGL_REG	5	--	I	--	OVUV_ DEGL
ADC_DATA_LPF_CH1— ADC_DATA_LPF_CH18	16	--	I	--	--
ADC_DATA_GPIO_CH1— ADC_DATA_GPIO_CH12	16	--	I	--	--
ADC_DATA_VPTAT	16	--	I	--	--
RR_END	1	16 CLK_ADC_SC	I	--	--
TWARN	1	--	O	1'b0	--
CELL_OV	18	--	O	18'h00000	--
CELL_UV	18	--	O	18'h00000	--
GPIO_OT	12	--	O	12'h000	--
GPIO_UT	12	--	O	12'h000	--
GPIO_CBOT	1	--	O	1'b0	--

OVUV_OTUT_CMP Key Signal Descriptions

Table 3 OVUV_OTUT_CMP key signal descriptions

Signal	Width	Duration	Default Value	Description
OVUV_OTUT_CMP_START	1	2 CLK_SLOW_SC	1'b0	It represents starting comparing.
CMP_UNDERWAY	1	--	1'b0	The CMP_UNDERWAY = 1 when the RR_END_SYNC_POS (RR_END after synchronization and rising edge detection) appear. It lasts for 31 clock periods. It represents the comparing is underway. And when CMP_UNDERWAY = 1, the register value can not load in this module.
RELOAD_START	1	1 CLK_SLOW_SC	1'b0	When the rising edge of OVUV_OTUT_CMP_START is detected, the RELOAD_START = 1. And when the comparing is underway, the RELOAD_START is hold, and when the comparing is not underway, the RELOAD_START is cleared at the next clock edge. It is used to record the OVUV_OTUT_CMP_START requirement, and after comparing ends, enable loading register.

RELOAD_EN	1	1 CLK_SLOW_SC	1'b0	It is generated by RELOAD_START except the part of comparing being underway. It is used to enable loading register.
cmp_cnt	5	1 CLK_SLOW_SC	5'b0	It is used to record the number of data compared.
DEGL_TIME	1	1 CLK_SLOW_SC	1'b0	When all the data comparing ends, the DEGL_TIME pulse (1 clock period) is generated. When the DEGL_TIME = 1, the deglitch module is enabled.
UPDATED	1	1 CLK_SLOW_SC	1'b0	When the falling edge of CMP_UNDERWAY is detected, the UPDATED = 1. It is used to enable the road from comparator result to the result register in top module.

OVUV_OTUT_CMP Function Descriptions

The OVUV_OTUT_CMP module has the following functions:
• Latch OVUV_OTUT_EN_REG, CELL_OV_THRESH_REG, CELL_UV_THRESH_REG, GPIO_OTUT_THRESH_SEL_REG, GPIO_OT_PACK_THRESH_REG, GPIO_OT_PCB_THRESH_REG, GPIO_UT_PACK_THRESH_REG, GPIO_UT_PCB_THRESH_REG, CB_OT_PACK_THRESH_REG, CB_OT_PCB_THRESH_REG, OVUV_DEGL_REG to OVUV_OTUT_EN, CELL_OV_THRESH, CELL_UV_THRESH, GPIO_OTUT_THRESH_SEL, GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH, OVUV_DEGL once MON_WAKE_GO or ADC_GO_DLY is high; (Func 1) (HWR001_OVUV_OTUT_CMP)
• Compare ADC_DATA_LPF with CELL_OV_THRESH and CELL_UV_THRESH when RR_END is high, and output CELL_OVUV according to OVUV_DEGL when OVUV_OTUT_EN is high; (Func 2) (HWR002_OVUV_OTUT_CMP)
• Compare OTH_ADC_DATA with GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH according to GPIO_OTUT_THRESH_SEL when RR_END is high, and output GPIO_OTUT, GPIO_CBOT when OVUV_OTUT_EN is high; (Func 3) (HWR003_OVUV_OTUT_CMP)
• Reset when OVUV_OTUT_EN is low; (Func 4) (HWR004_OVUV_OTUT_CMP)
• Output CELL_OVUV until counter=OVUV_DEGL; (Func 5) (HWR005_OVUV_OTUT_CMP)
• The counter will +1 when fault is detected; (Func 6) (HWR005_OVUV_OTUT_CMP)
• The max of counter is OVUV_DEGL; (Func 7) (HWR005_OVUV_OTUT_CMP)
• The counter will -1 when fault is not detected; (Func 8) (HWR005_OVUV_OTUT_CMP)
• Update TWARN_THRESH_REG into TWARN_THRESH when ADC_GO_DLY or MON_WAKE_GO is high; (Func 9) (HWSR1_OVUV_OTUT_CMP)
• Compare the gap between OTH_ADC_DATA with TWARN_THRESH when RR_END is high; (Once over range, output TWARN) (Func 10) (HWSR2_OVUV_OTUT_CMP)
• TWARN TWARN_THRESH covers from 110℃ to 145℃, 5℃ step; (Func 11) (HWSR2_OVUV_OTUT_CMP)
• OVUV_OTUT_EN is ignored when TWARN comparison. (Func 12) (HWSR3_OVUV_OTUT_CMP)

Above functions can be found in the following timing diagrams. Among them, Fig 2 is about data loading from registers, Fig 3 is about "UV" and "OT", Fig 4 is about "OV" and "UT", Fig 5 is about "CBOT" and "TWARN".
Func 1 & Func 9: Sample the value of OVUV_OTUT_CMP_START (its generation can be found in Fig 1) using CLK_SLOW_SC. When the high level of OVUV_OTUT_CMP_START is detected, the value of OVUV_OTUT_EN, CELL_OV_THRESH, CELL_UV_THRESH, GPIO_OTUT_THRESH_SEL,

GPIO_OT_PACK_THRESH, GPIO_OT_PCB_THRESH, GPIO_UT_PACK_THRESH, GPIO_UT_PCB_THRESH, CB_OT_PACK_THRESH, CB_OT_PCB_THRESH, OVUV_DEGL will be set to the value of corresponding registers.

Func 2 & Func 3 & Func 10: Complement it using TDM (Time Division Multiplexer) method. When the posedge of RR_END is detected, CMP_UNDERWAY is set to 1 and the counter starts to count. When the counter value is 31, the CMP_UNDERWAY and the counter is cleared at the next clock posedge. The different counter values are corresponding to different channels. If deglitch is needed, the deglitch will be accomplished when counter value = 20.

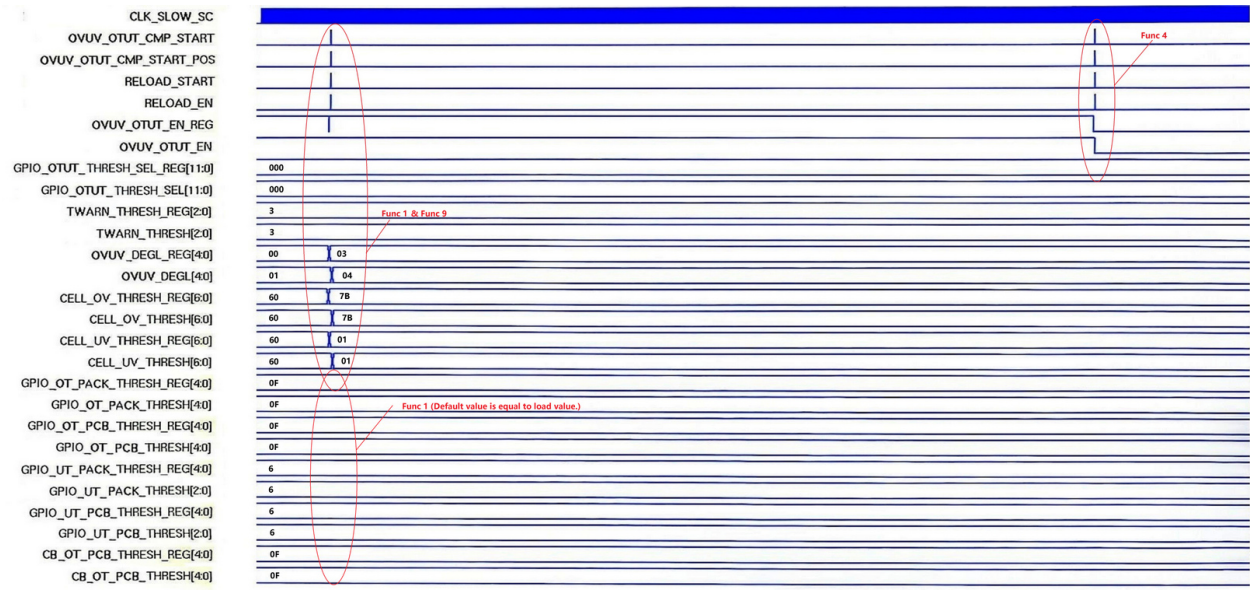

Fig 2. OVUV_OTUT_CMP Timing Diagram 1

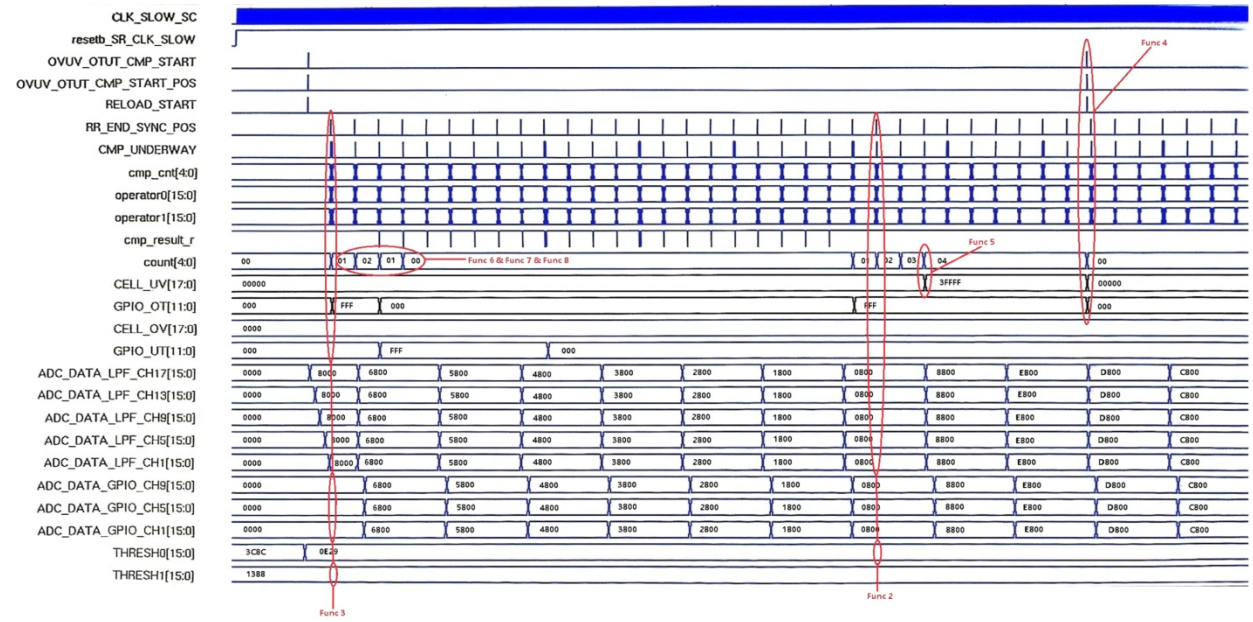

Fig 3. OVUV_OTUT_CMP Timing Diagram 2

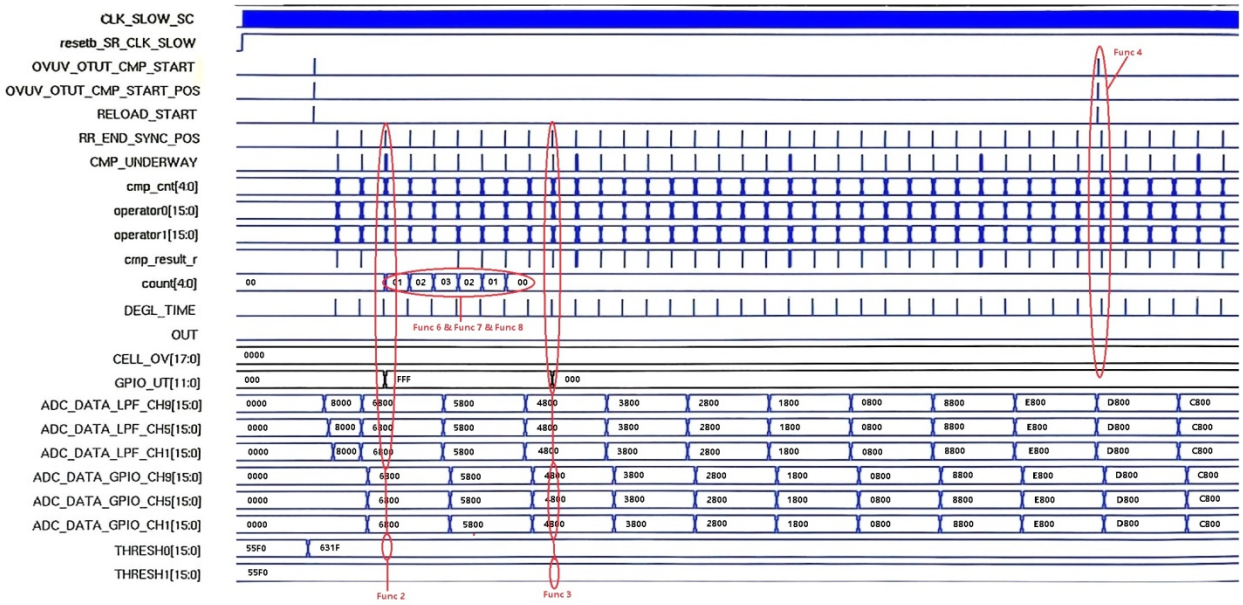

Fig 4. OVUV_OTUT_CMP Timing Diagram 3

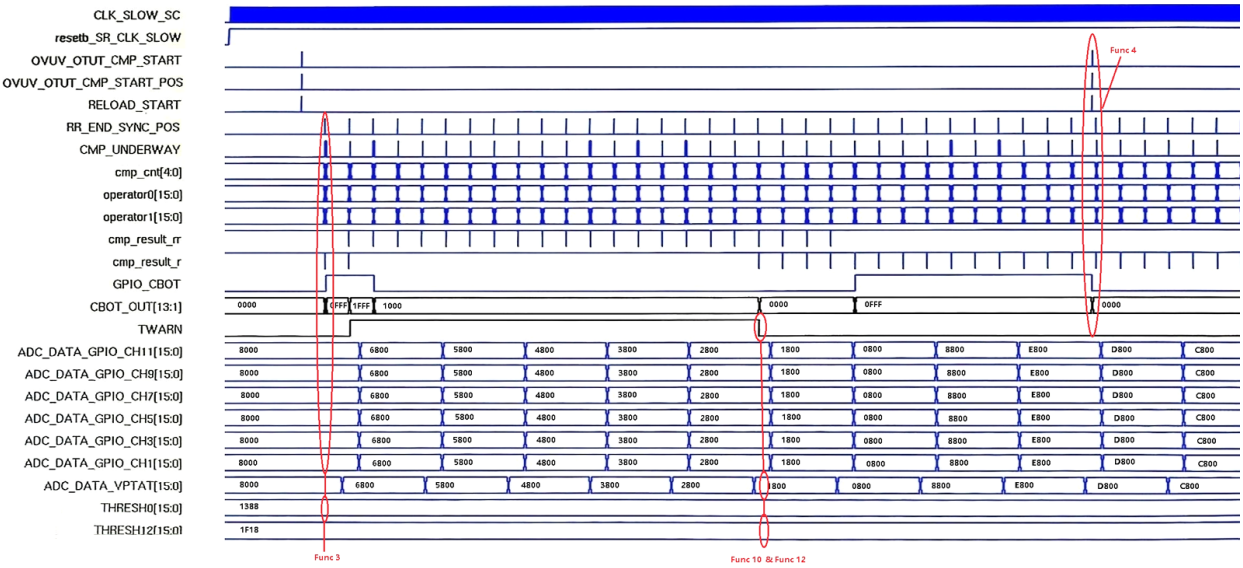

Fig 5. OVUV_OTUT_CMP Timing Diagram 4