

# Agenda

**DAY  
3**

**4**

**Clock Tree Synthesis (Lab continued)**



**5**

**Routing**



**6**

**Chip Finishing**



**CS**

**Customer Support**

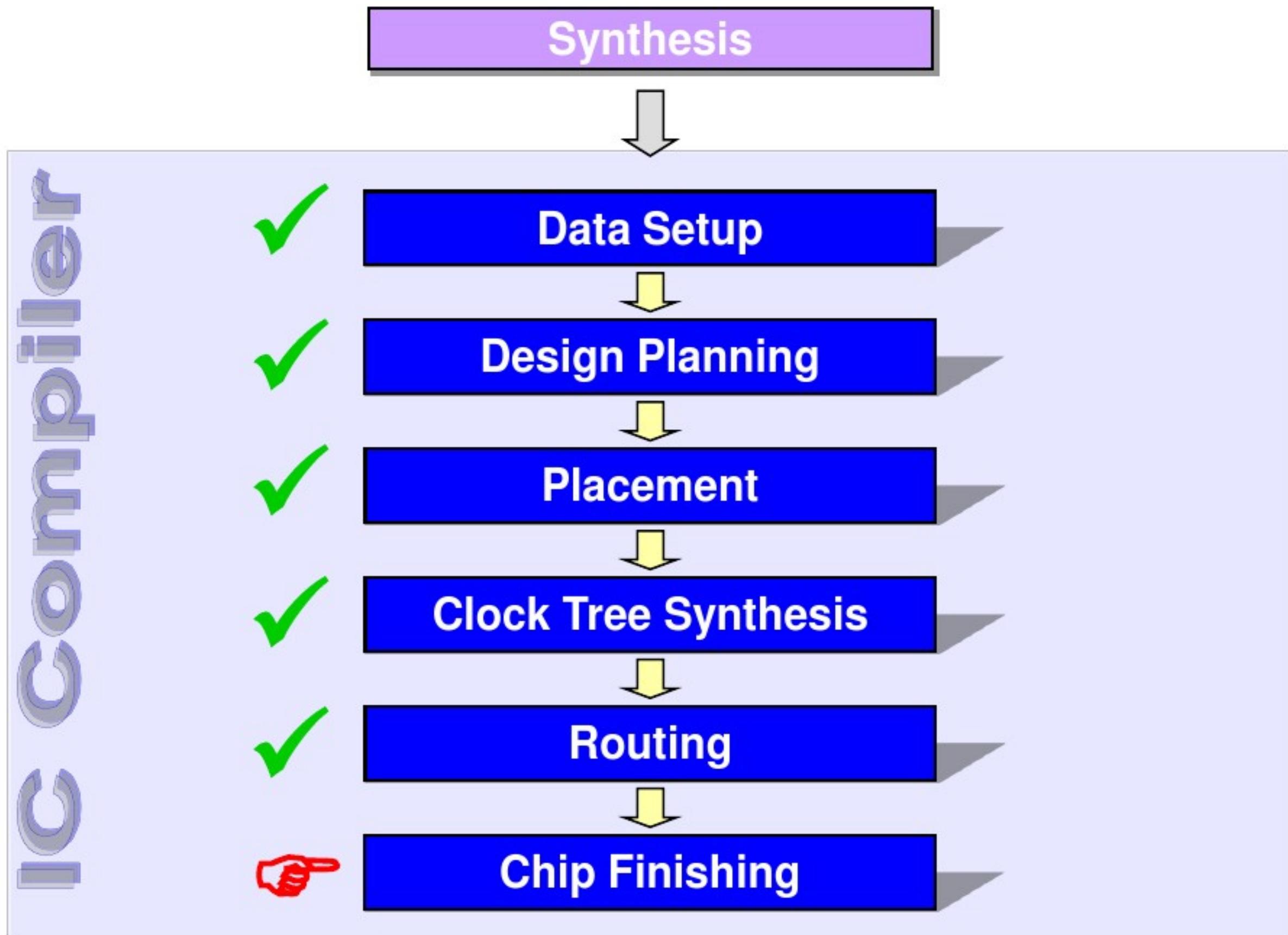
# Unit Objectives



**After completing this unit, you should be able to perform key chip finishing and design for manufacturing steps required after signal routing is complete:**

- Fix antenna violations
- Modify the routing patterns to make them more resistant to defects
- Add redundant contacts
- Perform metal filling
- Insert filler cells

# IC Compiler Flow



# Design Status, Completion of Routing Phase

- Placement – completed
- Clock Tree Synthesis – completed
- Power/Signal/Clock nets – routed
- Setup/Hold timing – Met (positive slack)
- Logical DRC – max cap/transition – no violations
- Physical DRC – no violations

# Chip Finishing Flow

**Post-Route: Timing &  
DRC clean design**

**Reduce critical area**

**Fix antenna violations**

**Insert filler cells**

**Perform incr. timing opt.**

**Insert redundant vias**

**Insert metal fill**

# Random Particle Defects

Critical Area

Antenna

Filler Cells

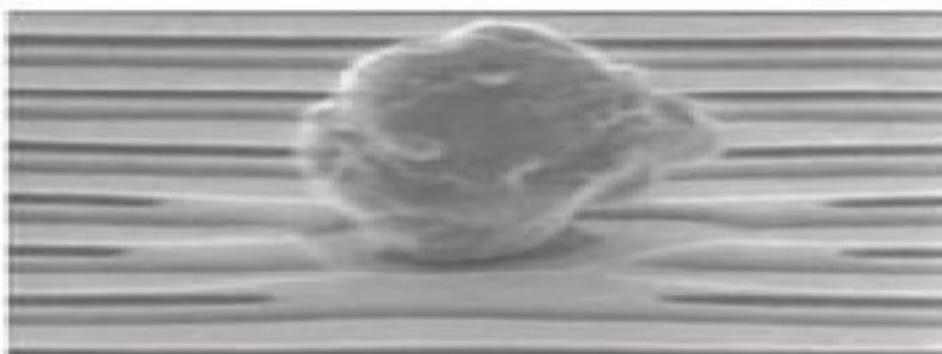
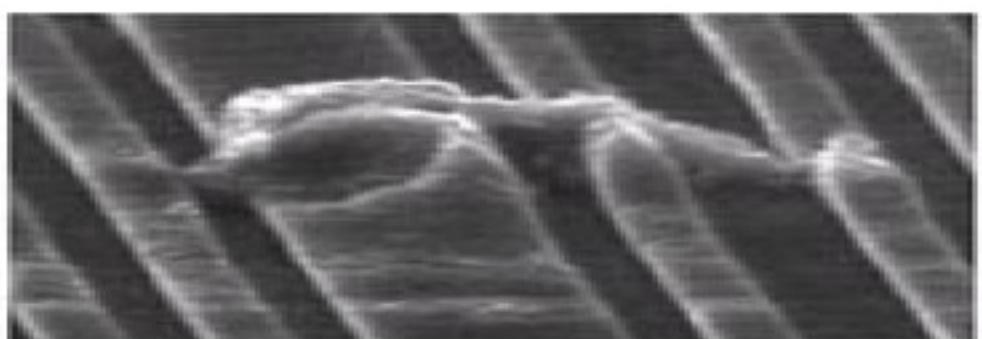
Inc. Timing Opt.

Redundant Vias

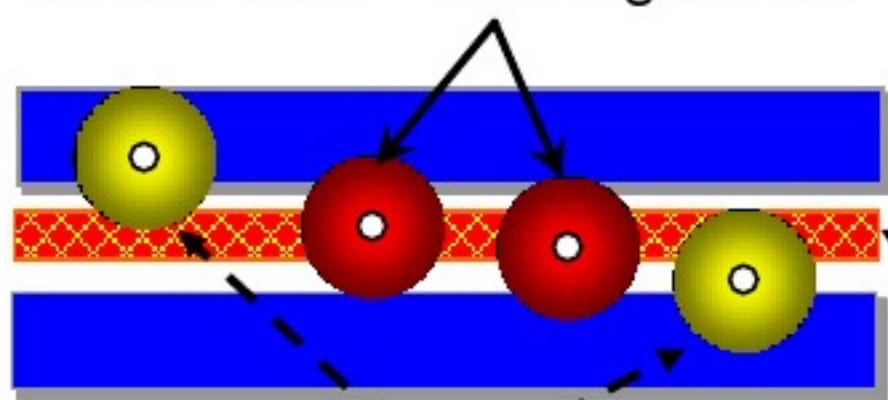
Metal Fill

**Random particle defects during manufacturing may cause *shorts* or *opens* during the fabrication process**

- Wires at minimum spacing are most susceptible to shorts
- Minimum-width wires are most susceptible to opens

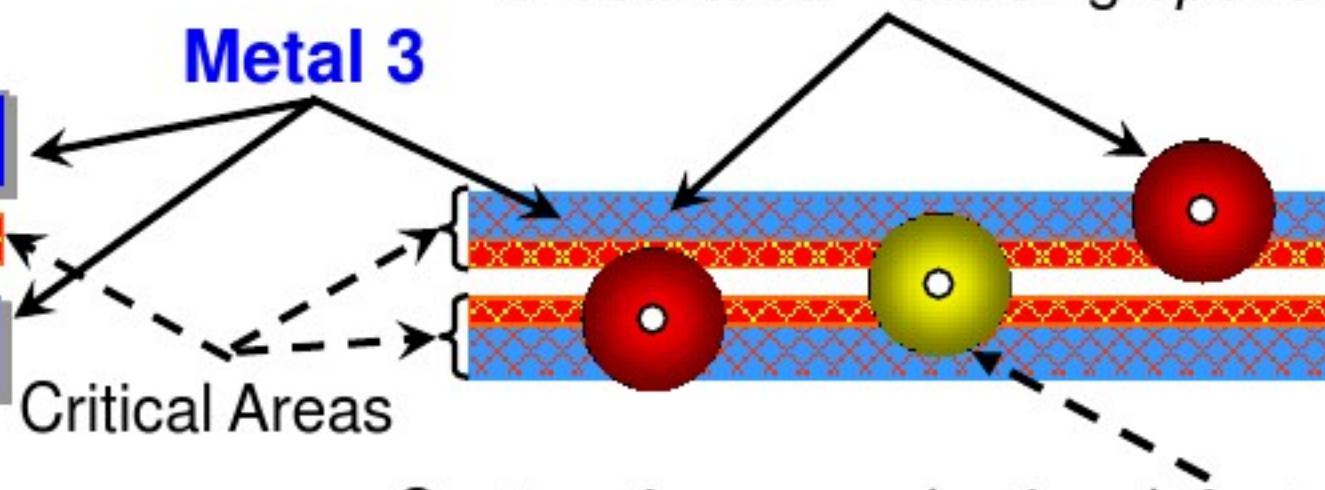


Center of conductive defects within critical area – causing *shorts*



Center of conductive defects outside critical area – no shorts

Center of non-conductive defects within critical area – causing *opens*

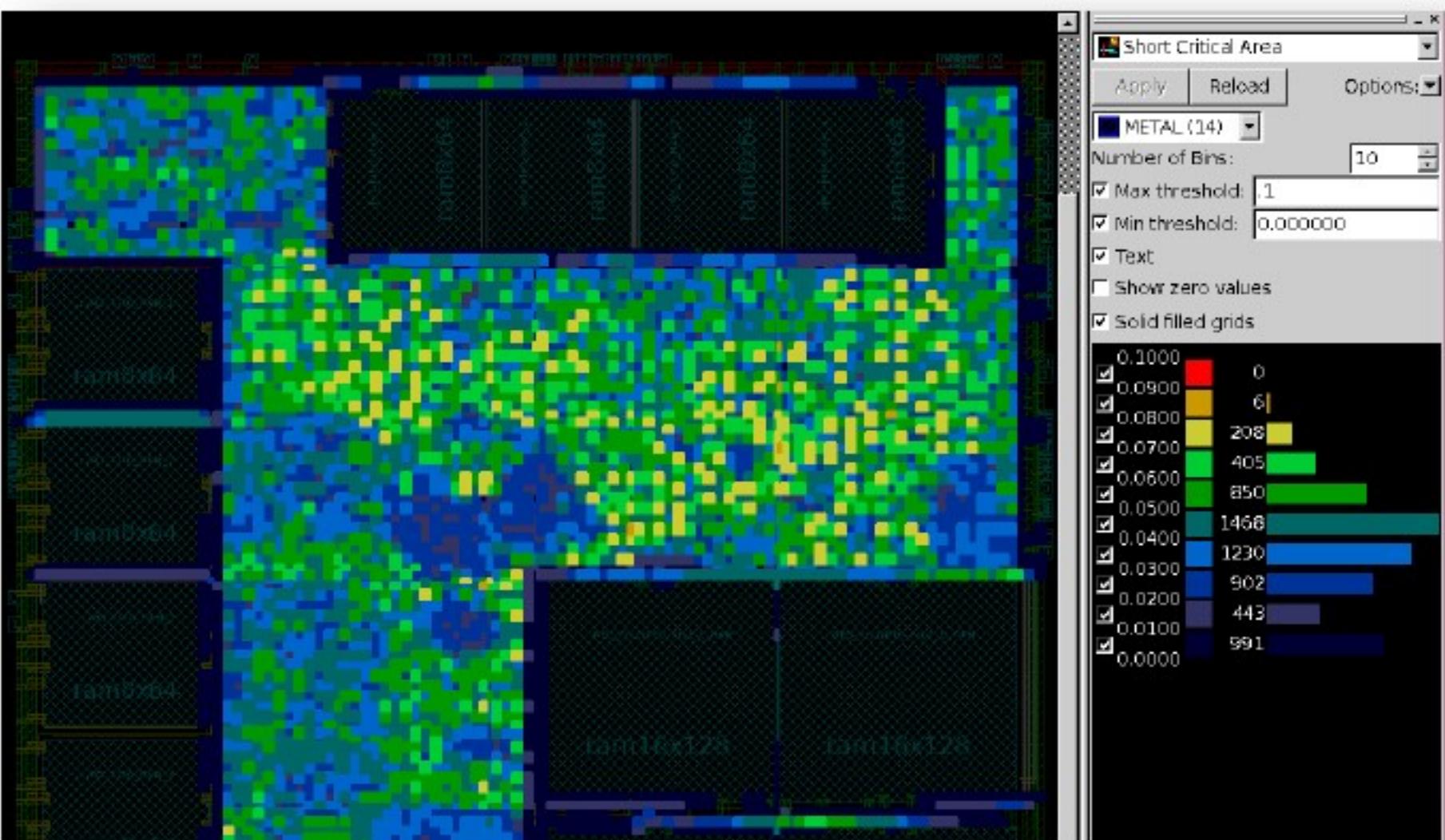


Center of non-conductive defects outside critical area – no opens

# Reporting the Critical Area

```
report_critical_area
  -particle_distr_func_file <file>
  -input_layers {m2 m3 m4}
  -fault_type {short|open}
```

**Generates both textual and graphical output**



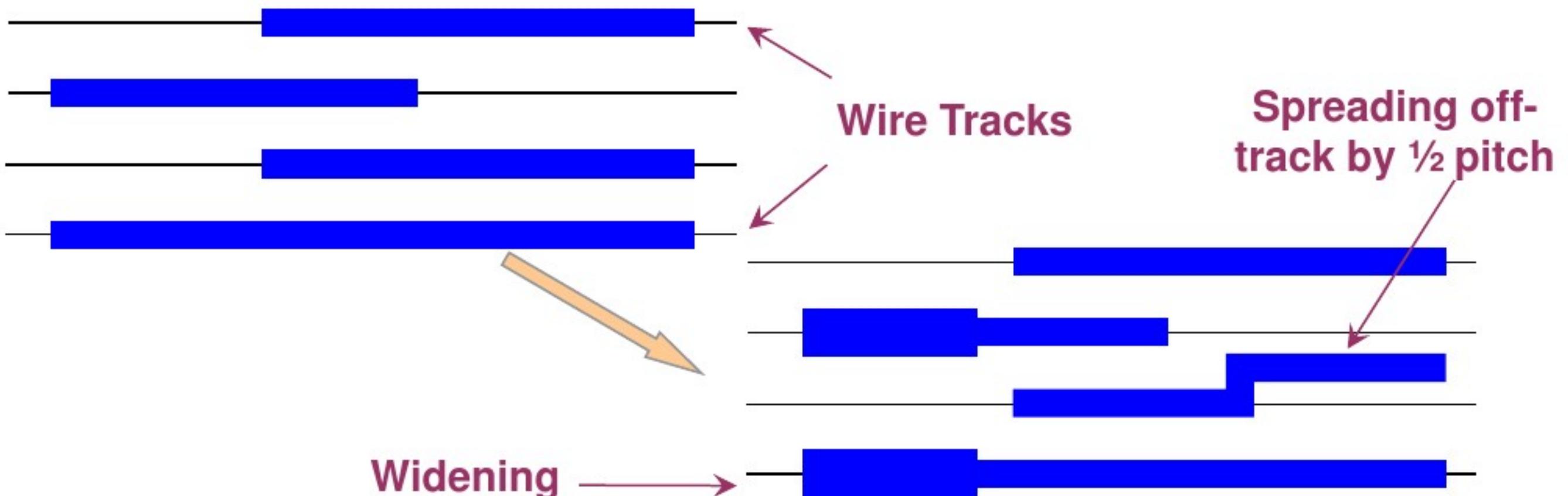
# Discrete Defect Size Distribution

- Defect size distribution function depends on the fabrication process
- IC Compiler accepts discrete defect sizes and their probabilities in a table format
- An example

Defect Size	Probability
0.20	0.002778
0.36	0.000922
0.52	0.000412
0.68	0.000219
0.84	0.000130
...	...

# Solution: Wire Spreading + Wire Widening

```
spread_zrt_wires \
    -timing_preserve_setup_slack_threshold .05 \
    -timing_preserve_hold_slack_threshold .05
widen_zrt_wires \
    -timing_preserve_setup_slack_threshold .05 \
    -timing_preserve_hold_slack_threshold .05
```



# Wire Spreading: spread\_zrt\_wires

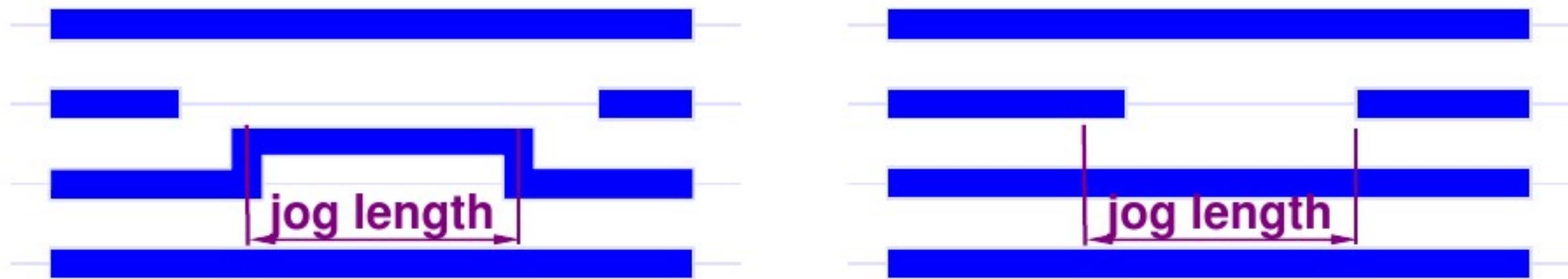
```
spread_zrt_wires
  -pitch real          ;# of pitches to spread,
                       default is 0.5
  -min_jog_length int ;# Minimum jog length in layer
                       unit on preferred direction,
                       default is 2
  -timing_preserve_setup_slack_threshold real
  -timing_preserve_hold_slack_threshold real
```

## Wire spreading

- Postroute function for reducing critical area for shorts
- Spread signal wires by  $\frac{1}{2}$  pitch or user-specified amount
- Only spread in preferred direction
- Automatic search and repair to fix DRCs
- Timing preservation (optional)

# Controlling Minimum Jog Length

- Pushing wires off-track always creates a jog and increases wire length
- Use `-min_jog_length` option to control the minimum jog length (default: 2 pitches)
  - Will not push a wire unless the available space is larger than '`-min_jog_length`'



# Wire Widening: widen\_zrt\_wires

```
widen_zrt_wires
  -timing_preserve_setup_slack_threshold real
  -timing_preserve_hold_slack_threshold real
  -timing_preserve_nets <timing preserve nets>
```

## Wire widening

- Postroute function for reducing critical area for opens
- Will not trigger new fat spacing rules when widening
- Automatic search and repair to fix DRCs
- Timing preservation (optional)

# Fix Remaining Antenna Violations w/ Diodes

Critical Area

Antenna

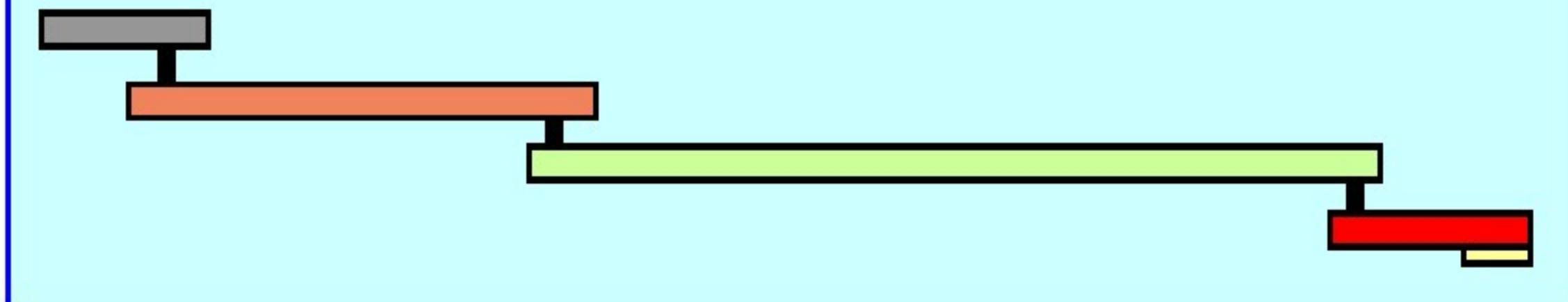
Filler Cells

Inc. Timing Opt.

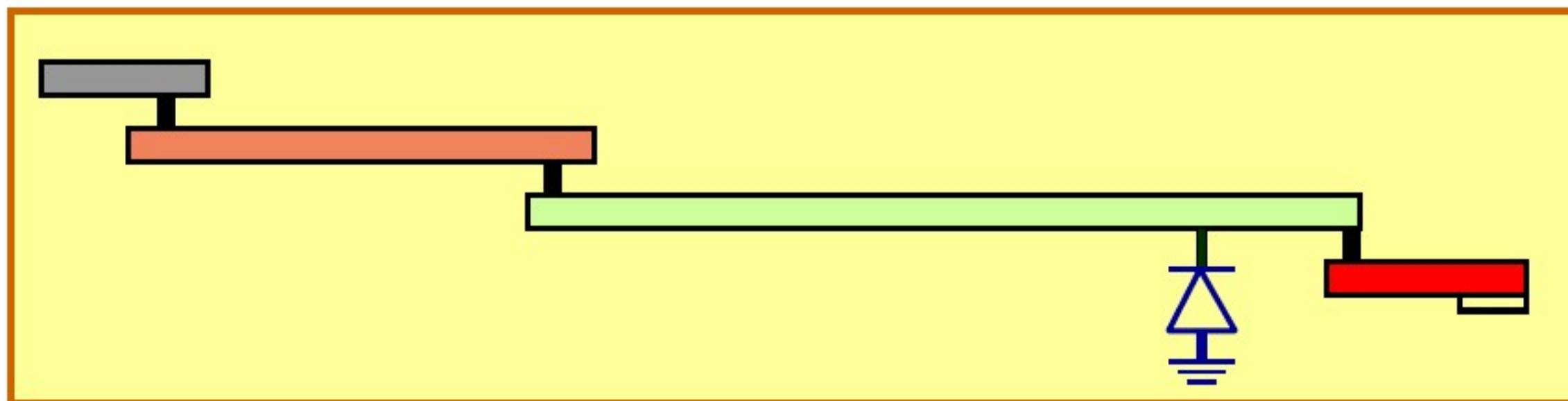
Redundant Vias

Metal Fill

Before inserting diodes



*Diode Inhibits large voltage swings on metal tracks*



During etch phase, the diode clamps the voltage swings.

# Antenna Fixing with Diode Insertion

- **Diode insertion is also concurrent when enabled**
  - It is NOT recommended during detailed route
- **Use diodes to fix antenna violations that are not fixable by layer jumping:**
  - Can specify diode names (automatic if none specified)

```
set_route_zrt_detail_options \
    -antenna true \
    -insert_diodes_during_routing true \
    -diode_libcell_names {adiode1 adiode2}

route_zrt_detail -incremental true
```

# Why Filler Cell Insertion?

Critical Area

Antenna

Filler Cells

Inc. Timing Opt.

Redundant Vias

Metal Fill

- **For better yield, density of the chip needs to be uniform**
- **Some placement sites remain empty on some rows**
  - ICC can fill such empty sites with standard filler cells

# Insert Filler Cells in Unused Placement Sites

## ■ Add filler cells with metal first

- For DRC checking purposes, standard cell PG rails should be complete prior to inserting filler cells with metal

## ■ Then add filler cells without metal

```
insert_stdcell_filler \
    -cell_with_metal "fillCap64 fillCap32" \
    -connect_to_power VDD -connect_to_ground VSS \
    -between_std_cells_only
insert_stdcell_filler \
    -cell_without_metal "fill16 ... Fill1"
    -connect_to_power VDD -connect_to_ground VSS \
    -between_std_cells_only
```

# Is Incremental Timing Optimization Needed?

Critical Area

Antenna

Filler Cells

Inc. Timing Opt.

Redundant Vias

Metal Fill

- Critical area, antenna fixing or filler cell insertion can create small timing violations
- Can perform incremental timing optimization by re-sizing the existing cells

```
route_opt -incremental -size_only
```

# Voids in Vias during Manufacturing

Critical Area

Antenna

Filler Cells

Inc. Timing Opt.

Redundant Vias

Metal Fill

- During routing phase:

```
set_route_zrt_common_options \
    -post_detail_route_redundant_via_insertion medium
set_route_zrt_detail_options \
    -optimize_wire_via_effort_level medium
route_opt ...
```

- During chip finishing phase:

```
insert_zrt_redundant_vias ...
```

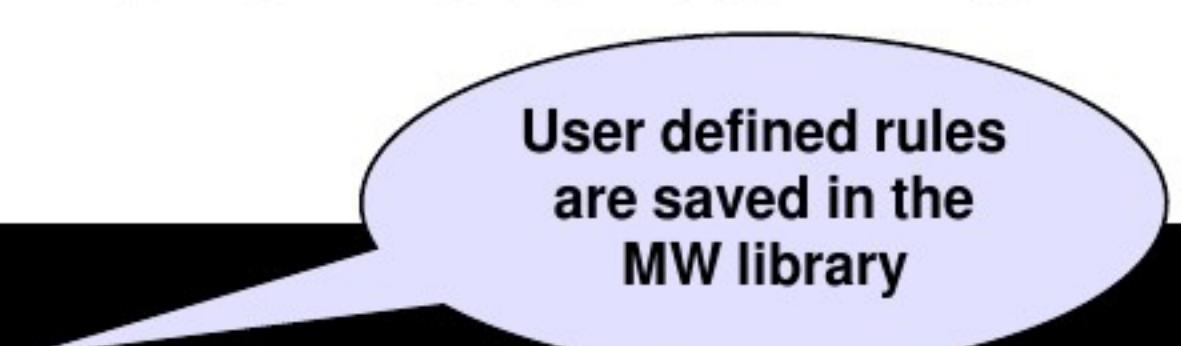
# Redundant Via Insertion: Setup

- Generate via mapping table using all contact codes from the technology file

```
insert_zrt_redundant_vias -list_only
```

- If OK, proceed with redundant via insertion
- If changes are required, define new redundant via rules

```
define_zrt_redundant_vias \
    -from_via {VIA23 VIA34} -to_via {VIA23 VIA34} \
    -to_via_x_size {1 2} -to_via_y_size {2 1}
```



User defined rules  
are saved in the  
MW library

# Redundant Via Insertion: Setup with Priority

- Some vias may be better for DFM, while others are better for routability
- Use `-to_via_weights` option to set a priority
  - Weight is 1 to 10
  - Higher weight via will be tried first
  - With equal weights, prioritization is based on routability

**See example on the next slide**

# Example: Prioritizing for DFM

- For DFM, say: VB > VG > V
  - Best rate of double-vias in that order
  - If single vias remain, optimize in that order
- Example for Via 1 layer... add others as needed

```
define_zrt_redundant_vias \
    -from_via {VB1 VG1 V1 VG1 V1 V1 VG1 V1 V1} \
    -to_via {VB1 VB1 VB1 VG1 VG1 V1 VB1 VB1 VG1} \
    -to_via_x_size {1 1 1 1 1 1 1 1 1} \
    -to_via_y_size {2 2 2 2 2 2 1 1 1} \
    -to_via_weights {5 5 5 4 4 3 2 2 1}
```

- VB1 doubled > VG1 doubled > V1 doubled > VB1 not doubled > VG1 not doubled

# Postroute Redundant Via Insertion

- Use `insert_zrt_redundant_vias` to insert redundant vias
  - `-effort low | med | high`

```
insert_zrt_redundant_vias -effort med
```

- Higher effort level results in better rate (3-5%) but will shift vias more to fit in
  - May be worse for lithography

# Timing Preservation Mode

- **Inserting double vias changes timing**
  - Short nets tend to slow down – increased capacitance
  - Long nets tend to speed up – decreased resistance
- **To maximize double-via rate, perform non-timing-driven via insertion first**
  - `route_opt` deletes double vias only on changed net segments and not on the entire net
- **During chip finishing, enable timing preservation to prevent insertion of double vias on critical nets**

```
insert_zrt_redundant_vias \
    -timing_preserve_setup_slack_threshold slack \
    -timing_preserve_hold_slack_threshold slack \
    -timing_preserve_nets {collection_of_nets}
```

# Reporting Redundant Via Count

## report\_design -physical

Mask Name	Contact Code	Number Of Contacts	Percentage
vial	VIA12A(1)	6578	14.7
vial	VIA12B(2)	26784	59.9
vial	VIA12f(9)	56	0.125
vial_1x2	VIA12A(1)	2982	6.67
vial_2x1	VIA12A(1)	8302	18.6

Default via for layer vial: 74.8%

Yield-optmized via for layer vial: 25.2%

via2	VIA23(3)	14334	25.2
via2_1x2	VIA23(3)	17544	30.8
via2_2x1	VIA23(3)	25039	44

Default via for layer via2: 25.2%

Yield-optmized via for layer via2: 74.8%

.....

Double Via rate for all layers: 58.9%

=====

Total Number of Contacts: 120119

# Reconnect PG and Perform Route Clean-up

```
## Connect Power & Ground
derive_pg_connection -power_net VDD -power_pin VDD \
                      -ground_net VSS -ground_pin VSS
derive_pg_connection -power_net VDD -ground_net VDD -tie

## Final Route clean-up - if needed:
## During minor cleanup, best to turn off ZRoute timing
## options to avoid extraction/timing hits
set_route_zrt_global_options -timing_driven false \
                               -crosstalk_driven false
set_route_zrt_track_options -timing_driven false \
                               -crosstalk_driven false
set_route_zrt_detail_options -timing_driven false

#Catch any opens and try to re-route them
route_zrt_eco
```

# Problem: Metal Over-Etching

Critical Area

Antenna

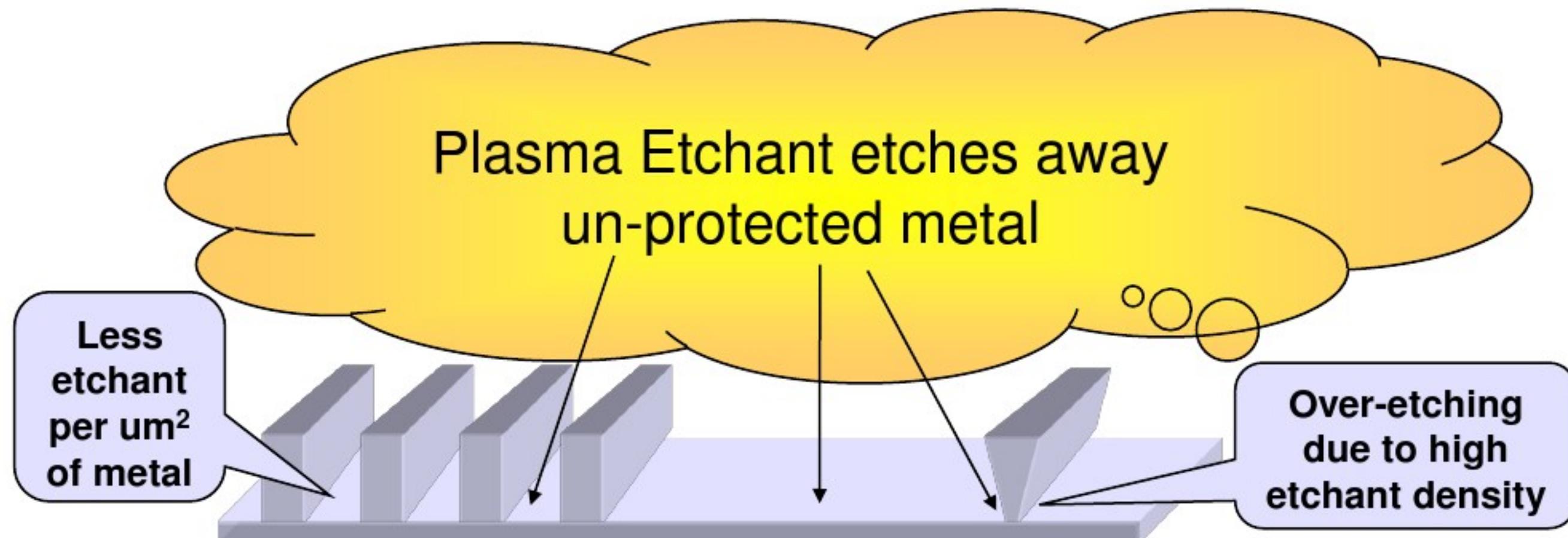
Filler Cells

Inc. Timing Opt.

Redundant Vias

Metal Fill

- A metal wire in a low metal density region receives a higher ratio of etchant and can get over-etched
- Minimum metal density rules are used to control this

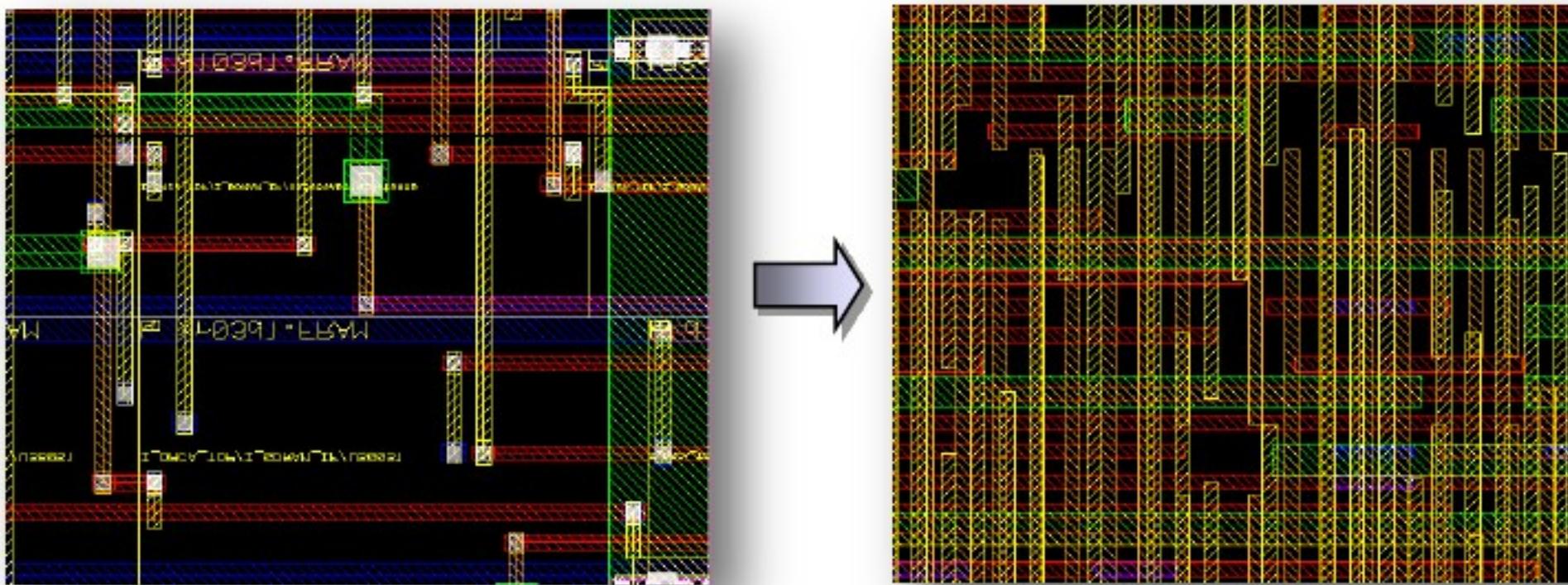


# Insert Metal Fill to Prevent Over-Etching

- Two methods

- IC Compiler: insert\_metal\_filler
- Hercules based inside ICC: signoff\_metal\_fill

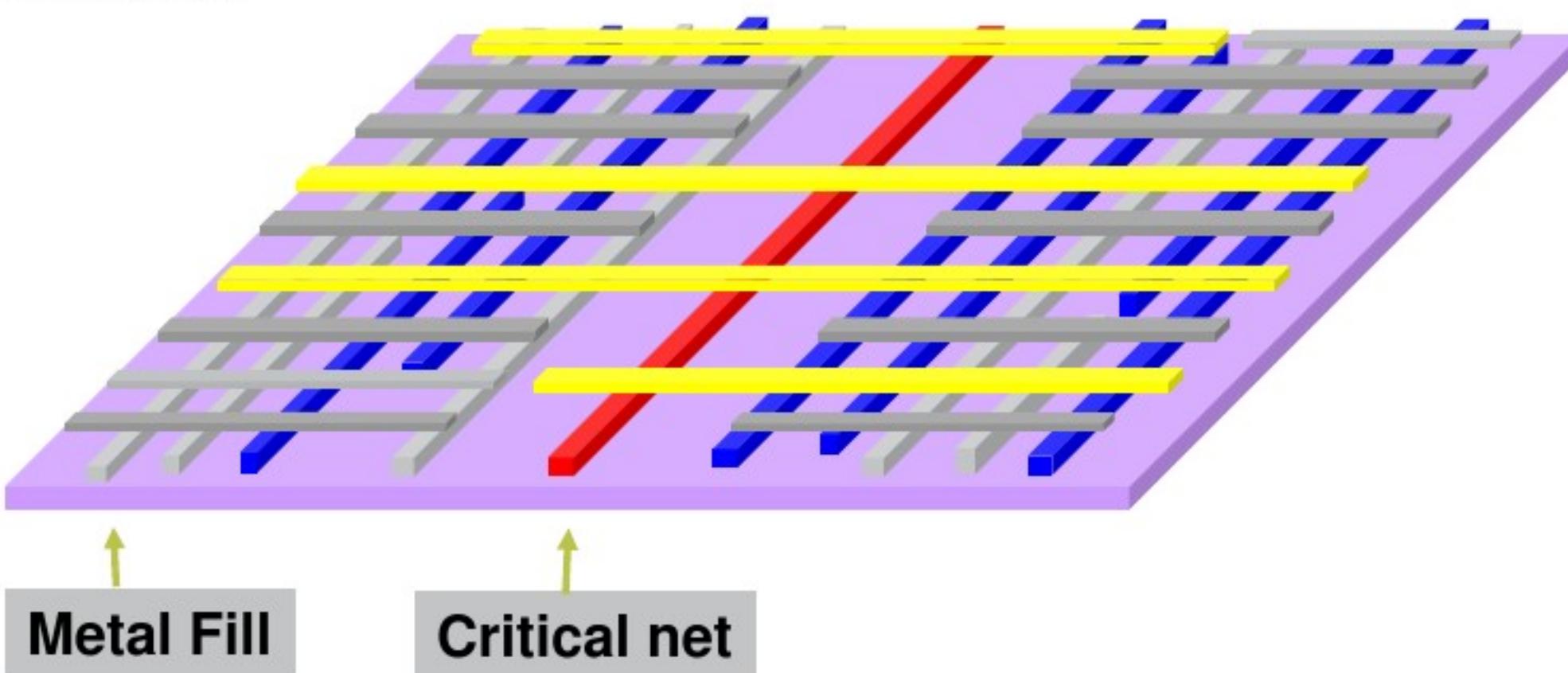
- Hercules is recommended for 65 nm and below



- Fills empty tracks on all layers (default) with metal shapes to meet the minimum metal density rules

# Recommended Metal Fill Options

- **Use `-timing_driven` option to preserve timing on critical nets**
  - Metal fill near critical nets on the same layer, upper layer, and lower layer are removed or trimmed
- **Use `-routing_space 2` option to specify a 2x minSpacing between normal routing wires and the fill metal**



# Summary: Chip Finishing

```
spread_zrt_wires ...
widen_zrt_wires ...

set_route_zrt_detail_options -diode_libcell_names {adiode1 adiode2} \
    -insert_diodes_during_routing true
route_zrt_detail -incremental true

insert_stdcell_filler -cell_with_metal "fillCap64 fillCap32" \
    -connect_to_power VDD -connect_to_ground VSS
insert_stdcell_filler -cell_without_metal "fill64 fill32" \
    -connect_to_power VDD -connect_to_ground VSS

route_opt -incremental -size_only

define_zrt_redundant_vias ...
insert_zrt_redundant_vias -effort medium

set_route_zrt_global_options -timing_driven false -crosstalk_driven false
set_route_zrt_track_options -timing_driven false -crosstalk_driven false
set_route_zrt_detail_options -timing_driven false

route_zrt_eco
insert_metal_filler -routing_space 2 -timing_driven
```

# Final Validation: Parasitics (SPEF or SBPF)

Wire parasitics for PrimeTime are provided via a .SPEF or .SBPF file

```
write_parasitics
  -output <file_name>
  -format <SPEF|SBPF>
  -compress
  -no_name_mapping
```



Use StarRC extraction for signoff

# Final Validation: Netlist Output

- Netlists for STA (Static Timing Analysis) do not require output of “Physical only cells” like:
  - Corner pad cells
  - Pad/core filler cells
  - Unconnected cell instances
- Unconnected cell instances (e.g. spare cells) are needed for LVS

```
change_names -hierarchy -rules verilog  
write_verilog -no_corner_pad_cells ... final.v
```

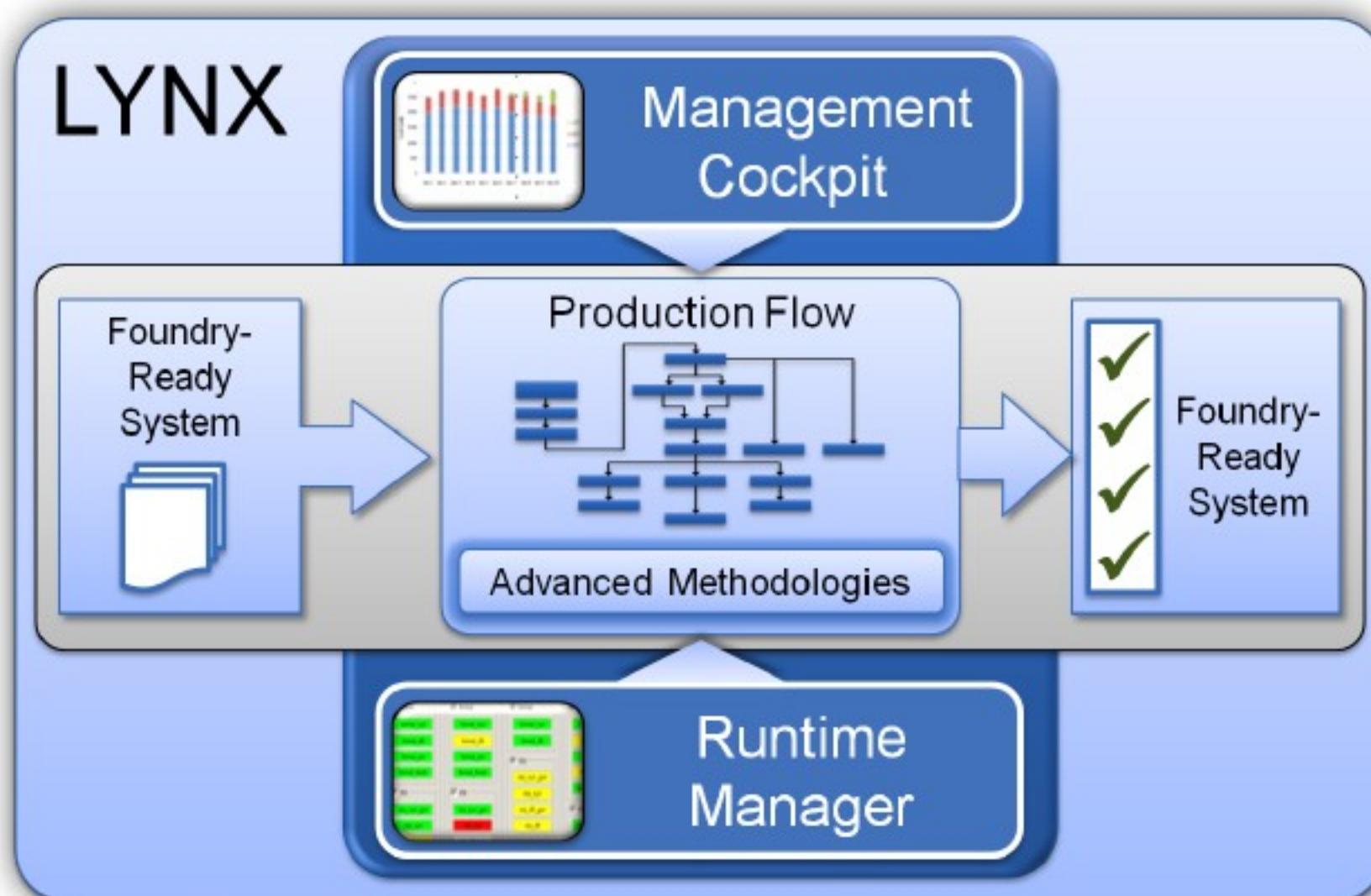
# Final Validation: GDSII Output

```
set_write_stream_options ...  
write_stream -cells DFM_clean orca.gdsii
```

- **GDSII for external physical verification can be generated from IC Compiler**
- **Requires output of “physical only cells” like:**
  - Corner pad cells
  - Pad/core filler cells
  - Unconnected cell instances

# Introducing Lynx Design System

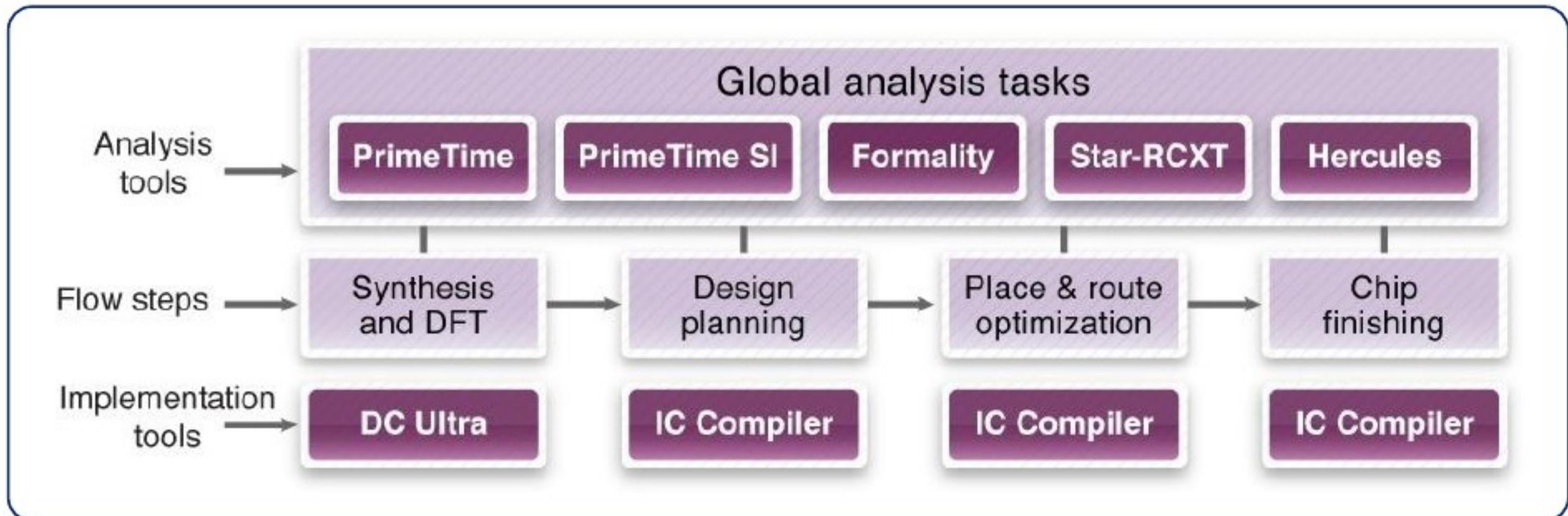
## *Industry's Most Advanced Design Creation System*



Top-down approach to  
reduce total cost of design

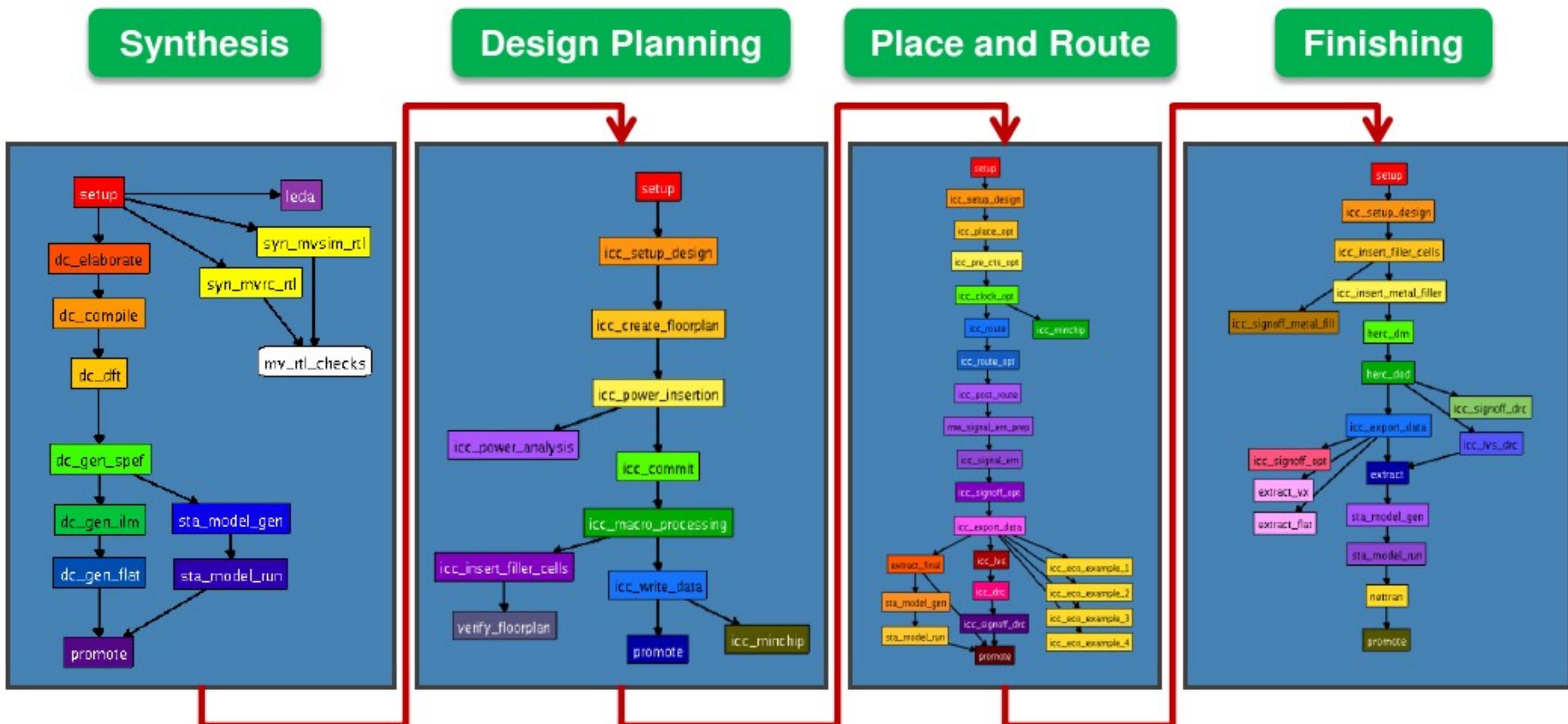
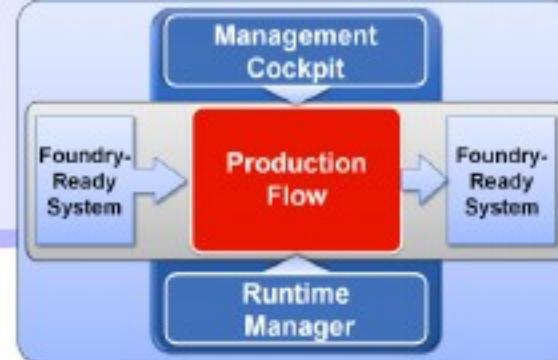
- Open, proven **production** flow in use down to 32nm
- **Support** multiple project teams with divergent needs
- **Easily** configure, monitor and maintain multiple flows from a single environment
- Leverage integrated **low power** methodologies
- Enable **visibility** into key design metrics and design trends
- **Faster** custom flow development with superior end user support

# A Complete RTL-2-GDSII Production Flow



- Proven from 180 to 32nm; over 100 tapeouts
- Incorporates Synopsys RM's for optimal Galaxy tool results
- Advanced Methodologies built in (eg. Low Power, MCMM)
- Fully tested with multiple foundries, libraries, & technology nodes
- Synopsys supported and regularly updated

# Lynx Implementation Flow



Complete RTL-2-GDSII Flow built on ICC and DC

## **For More Information on Lynx**

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**Go to: [www.synopsys.com/Lynx](http://www.synopsys.com/Lynx)**

**Contact your local AC or sales representative**

# Test for Understanding



- 1. What problem are you trying to solve by meeting “metal fill” design rules?**
- 2. What are the two methods for fixing antenna rule violations? Does IC Compiler support both?**
- 3. Placing additional vias in nets may slightly improve timing performance as a side effect. Why does this happen?**

# Summary

You should now be able to perform key design for manufacturing steps required after the signal routing is complete:

- Antenna fixing
- Modifying routing patterns to make them more resistant to short-causing defects
- Adding redundant contacts
- Inserting filler cells
- Metal filling



# Lab 6: Chip Finishing



60 minutes

- Fix antenna violations
- Analyze critical area and use wire spreading/widening to improve manufacturing yield
- Perform via optimization for timing and yield improvement
- Perform standard cell filler insertion, as well as metal filling operations for metal density rule compliance

# **Appendix A**

## **Critical Area Calculations**

# Critical Area Definition

- The region where, if the center of a random defect of a certain size falls on, will cause circuit failure (yield loss)

