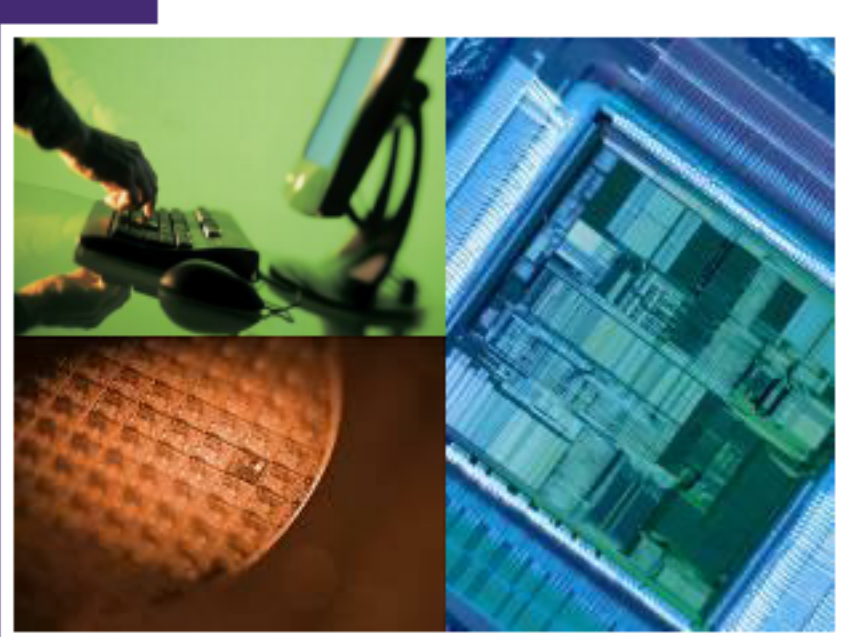
2007.12 IC Compiler Hierarchical Flow Update

Shoukyou Wang



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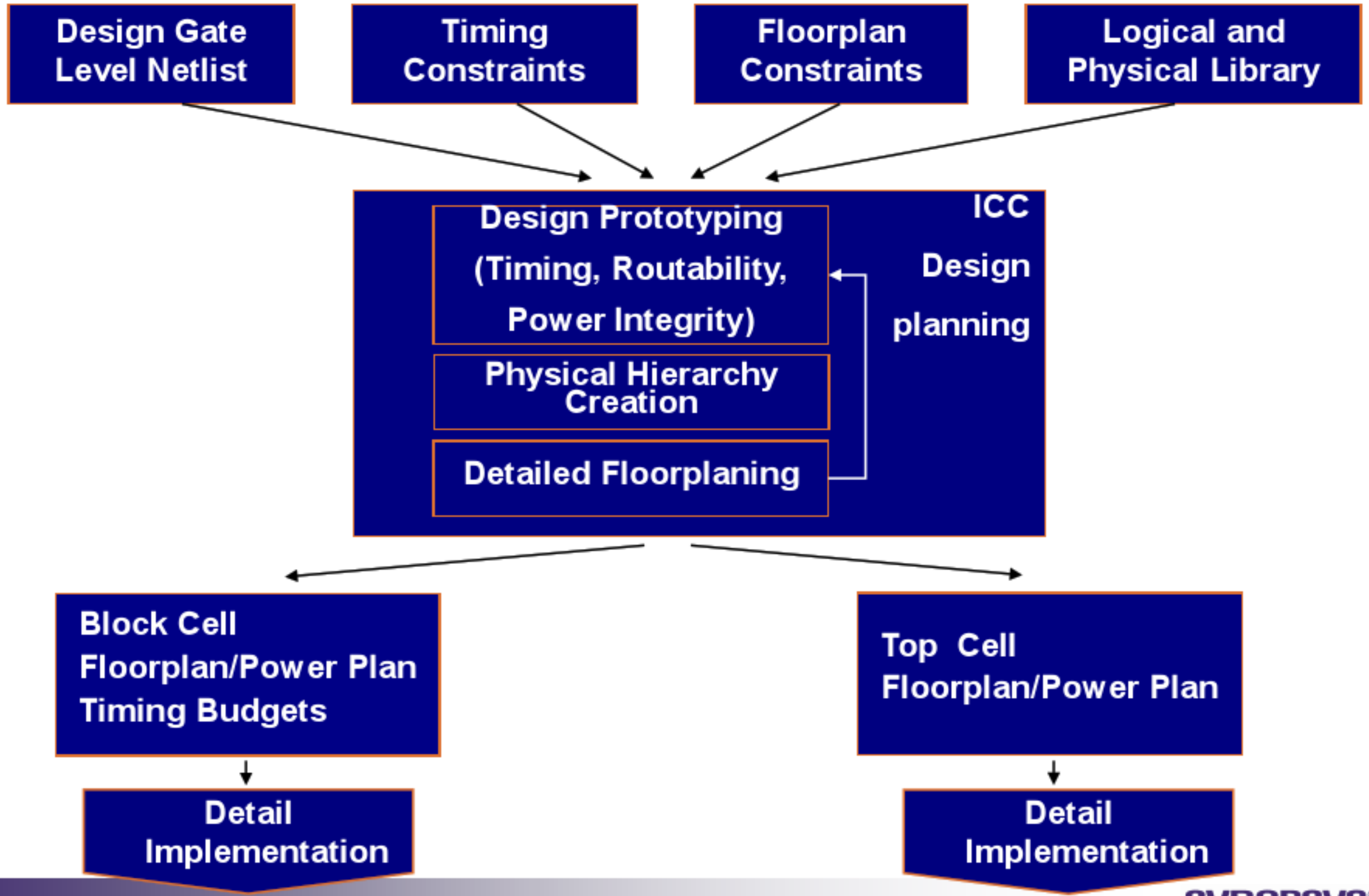
Predictable Success

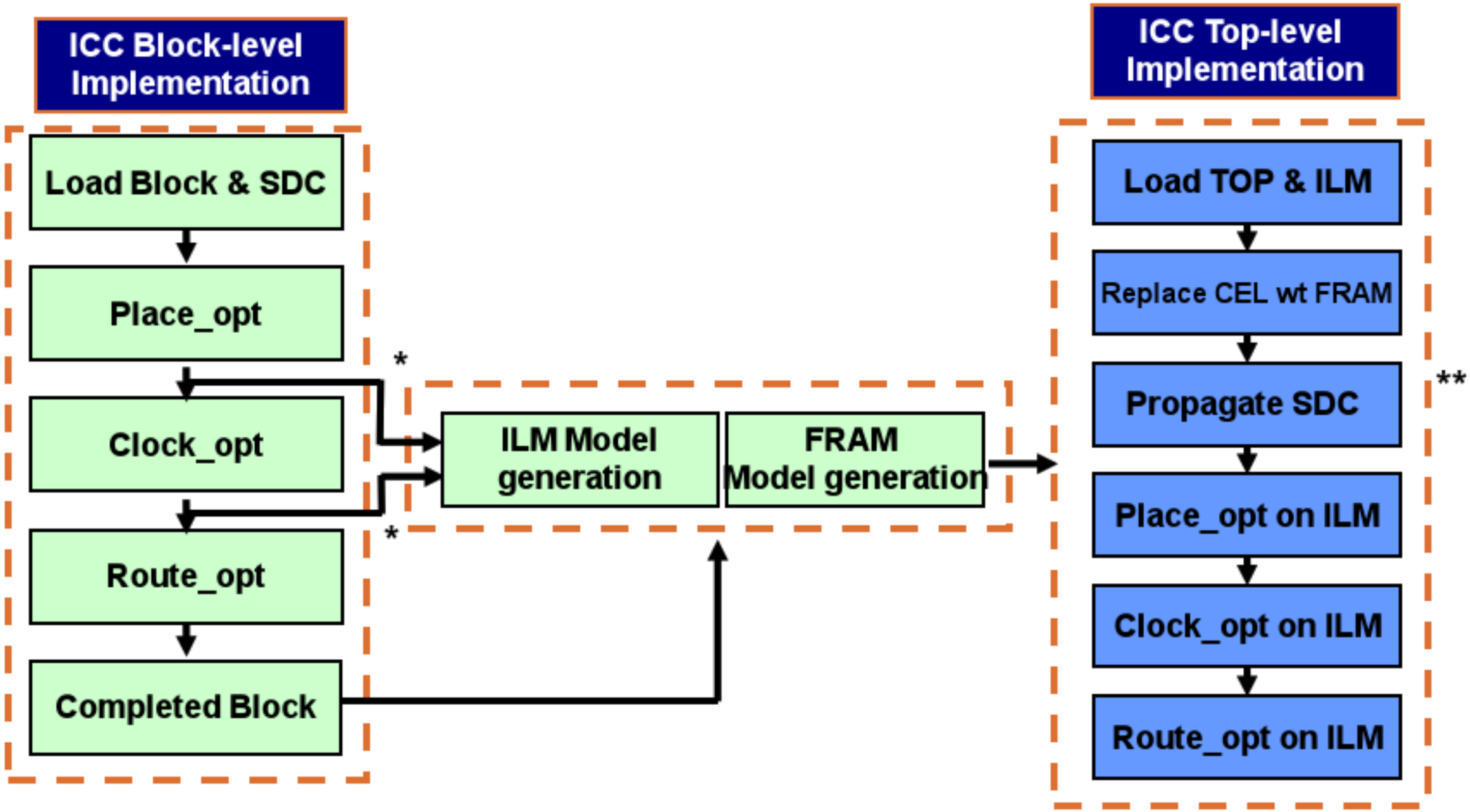
Agenda

- ICC Hierarchical Flow Overview
- Design Planning
- Block Implementation
- Top Level Implementation
- Lab

ICC Hierarchical Methodology



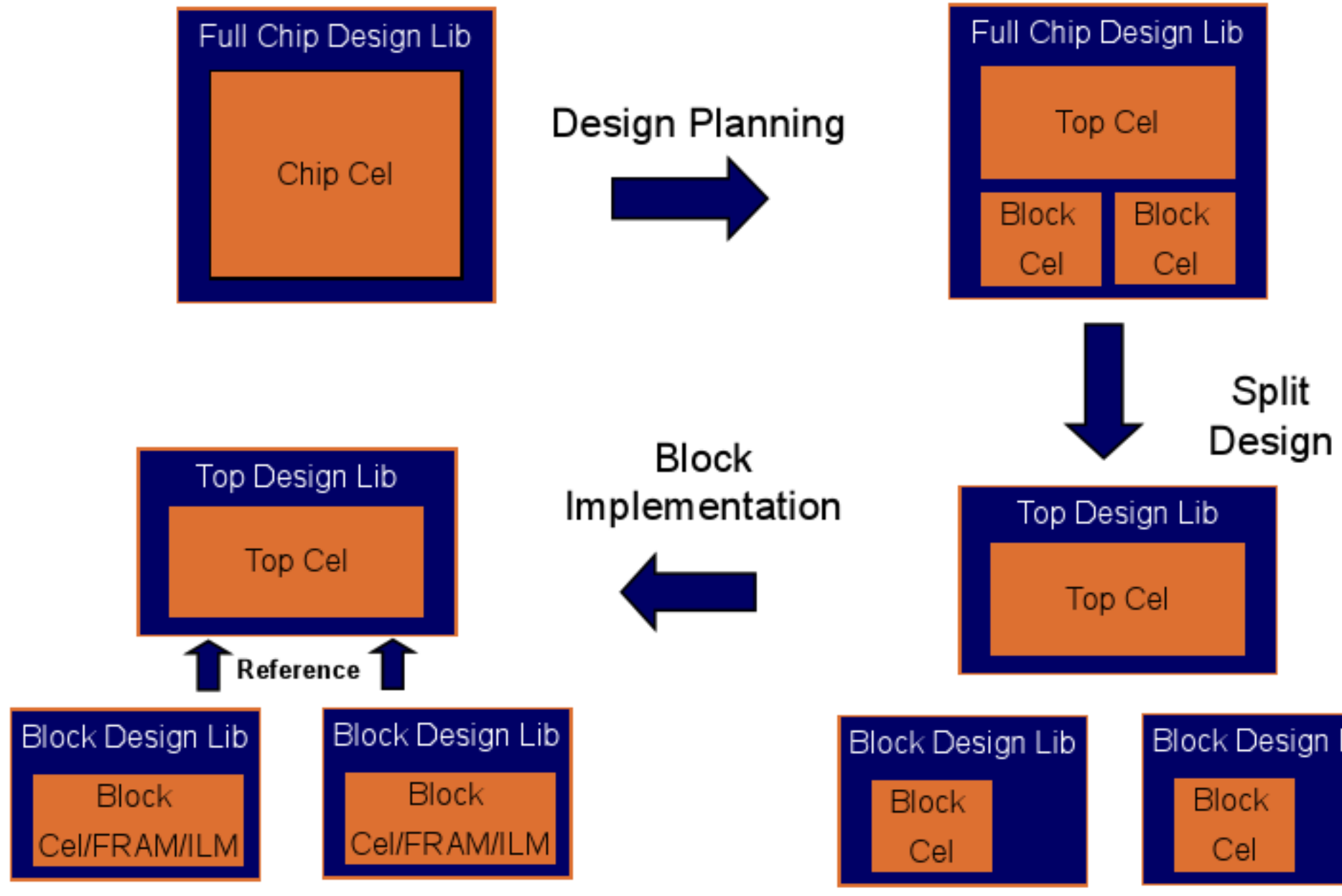
ICC Hierarchical Methodology



* Early Exploration using ILM

** optional

Hierarchical Design Database Management



Agenda

- ICC Hierarchical Flow Overview
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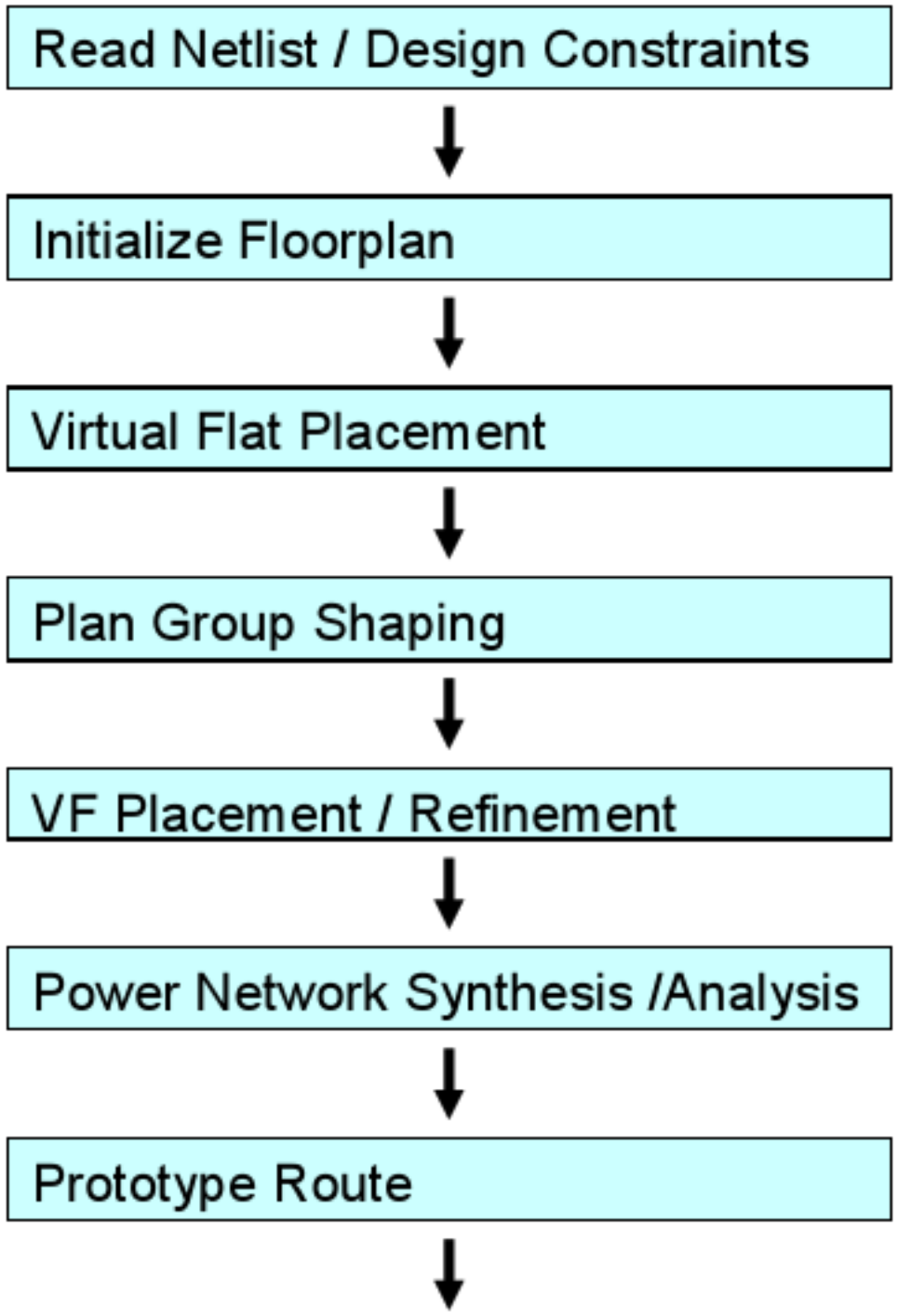
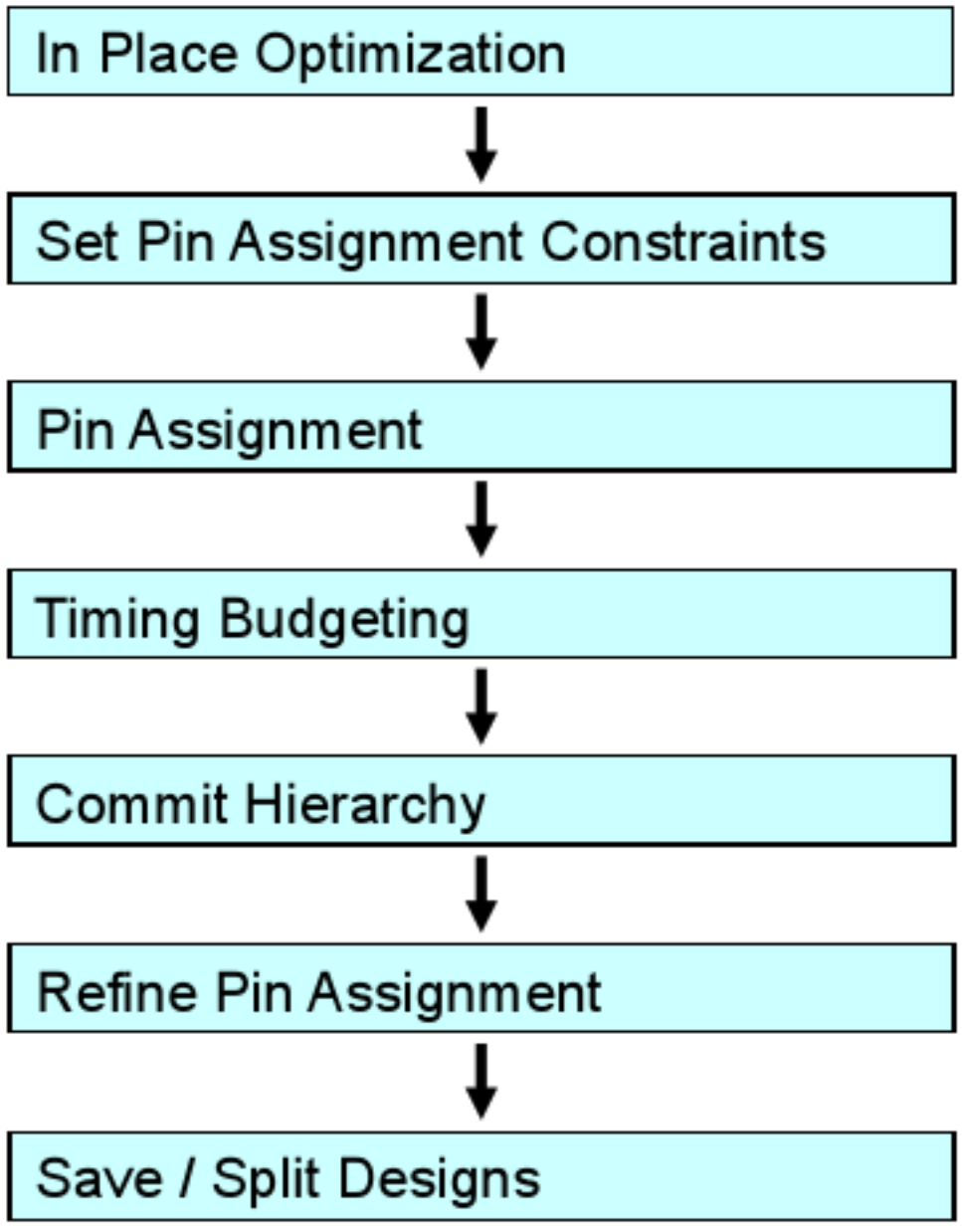
ICC Design Planning



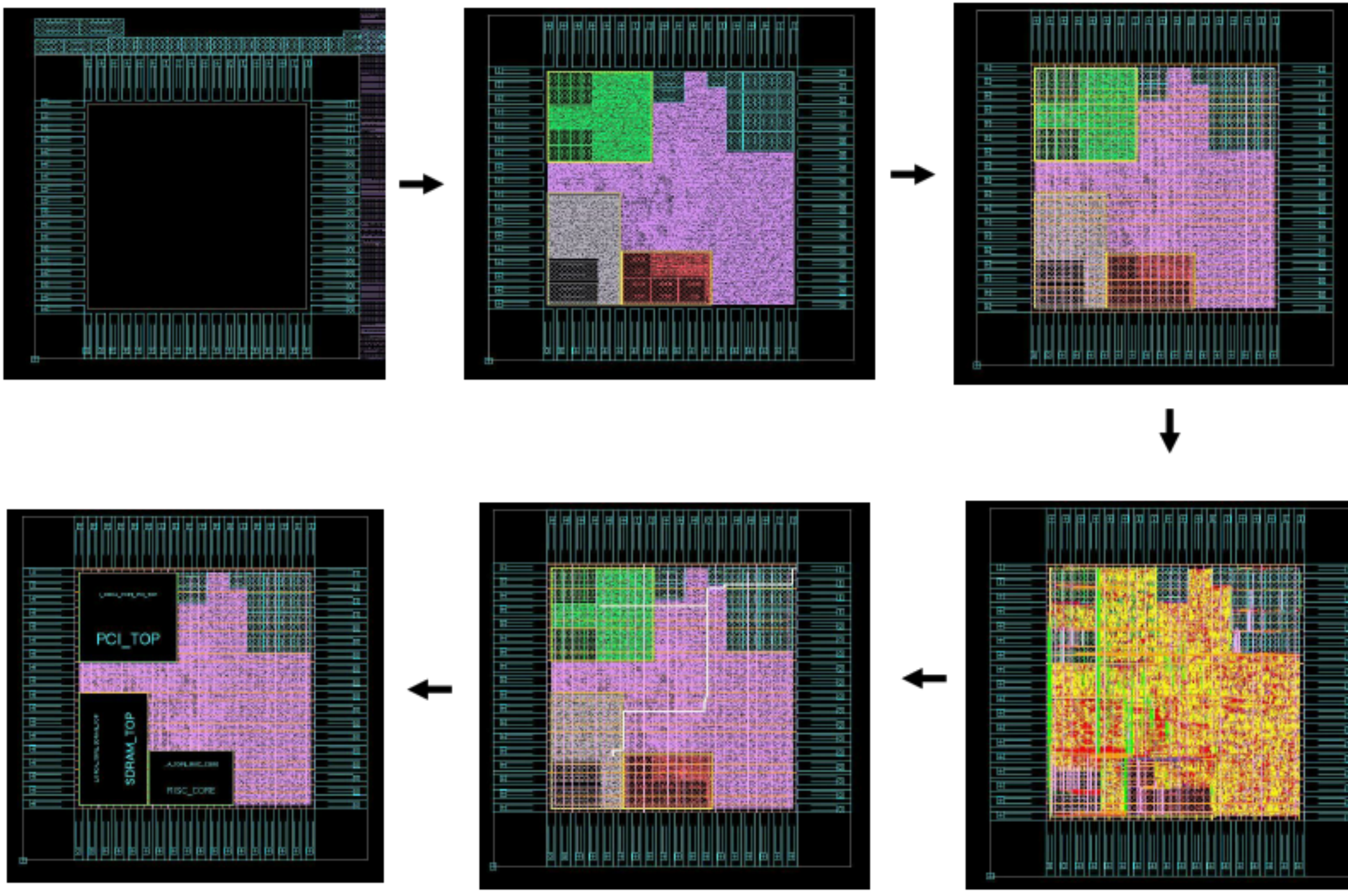

```
create_mw_lib
open_mw_lib
read_verilog_to_cel $netlist_file
set_tlu_plus_files

read_sdc $sdc_file
read_io_constraints io.tdf
initialize_floorplan

set_fp_placement_strategy
report_fp_placement_strategy
create_fp_placement


create_plan_group
shape_fp_blocks
Create_fp_plan_group_padding


create_fp_placement

connect_pg_nets
set_fp_rail_constraints
#set_fp_block_ring_constraints
#set_fp_rail_region_constraints
synthesize_fp_rail
Commit_fp_rail
#preroute_standard_cells

set_parameter -name readPlanGroup -value 1
route_fp_proto

...
```

ICC Design Planning




```
report_timing
set_dont_touch_placement {hard_macro_list }
optimize_fp_timing

set_fp_pin_constraints -allow_feedthroughs [off|on] ...
report_fp_pin_constraints

set_parameter -name readPlanGroup -value 1
route_global

analyze_fp_routing –finalize

extract_rc
report_timing
check_fp_timing_environment
allocate_fp_budgets


commit_fp_plan_groups


check_fp_pin_assignment
check_fp_pin_alignment
place_fp_pins


save_mw_cel –hierarchy
split_mw_lib
```

ICC Design Planning



ICC Design Planning

- Use read_verilog_to_cel to read verilog netlist
  - Use uniquify_fp_mw_cel for non-uniquified netlist
- optimize_fp_timing does virtual route based optimization
- Use plan group aware routing to improve top level congestion analysis

  set_parameter -name readPlanGroup -value 1
- Pin assignment (pin cutting) decides pin location based on intersection of global routes and plan group boundaries (pin cutting)
  - Incremental pin assignment allowed after commit hierarchy
- Do not proceed to pin assignment before solving congestion issues
  - Routing based pin assignment can take long runtime and generate poor result on congested designs
- Use save_mw_cel –hierarchical to save all the open cells

Feedthrough Generation

- Additional steps needed if feedthrough is involved in ICC hierarchical flow
  - Check feedthrough candidates before pin assignment
    - Use analyze_fp_routing
  - Buffer feedthrough nets after pin cutting

```
set fpopt_env_feedthru_buf true
optimize_fp_timing
```

  - Check design for feedthrough connections before ICC implementation
    - Use check_design and search for “LINT-29” “LINT-31” warnings
  - Control optimization commands to insert buffer on feedthrough nets
    - set_fix_multiple_port_nets –all

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- ICC Hierarchical Flow Overview
- Design Planning
- ➢Block Implementation
- Top Level Implementation
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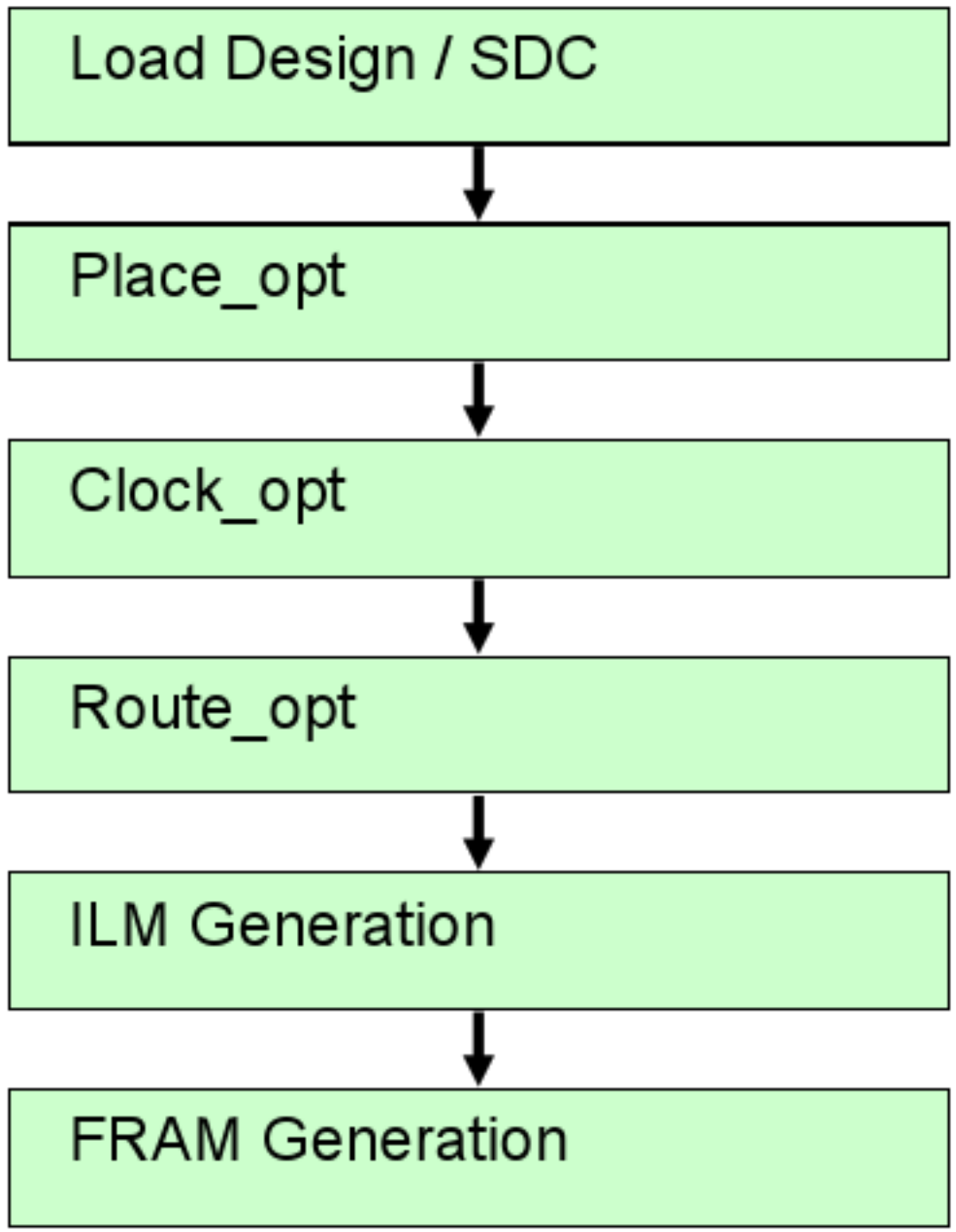
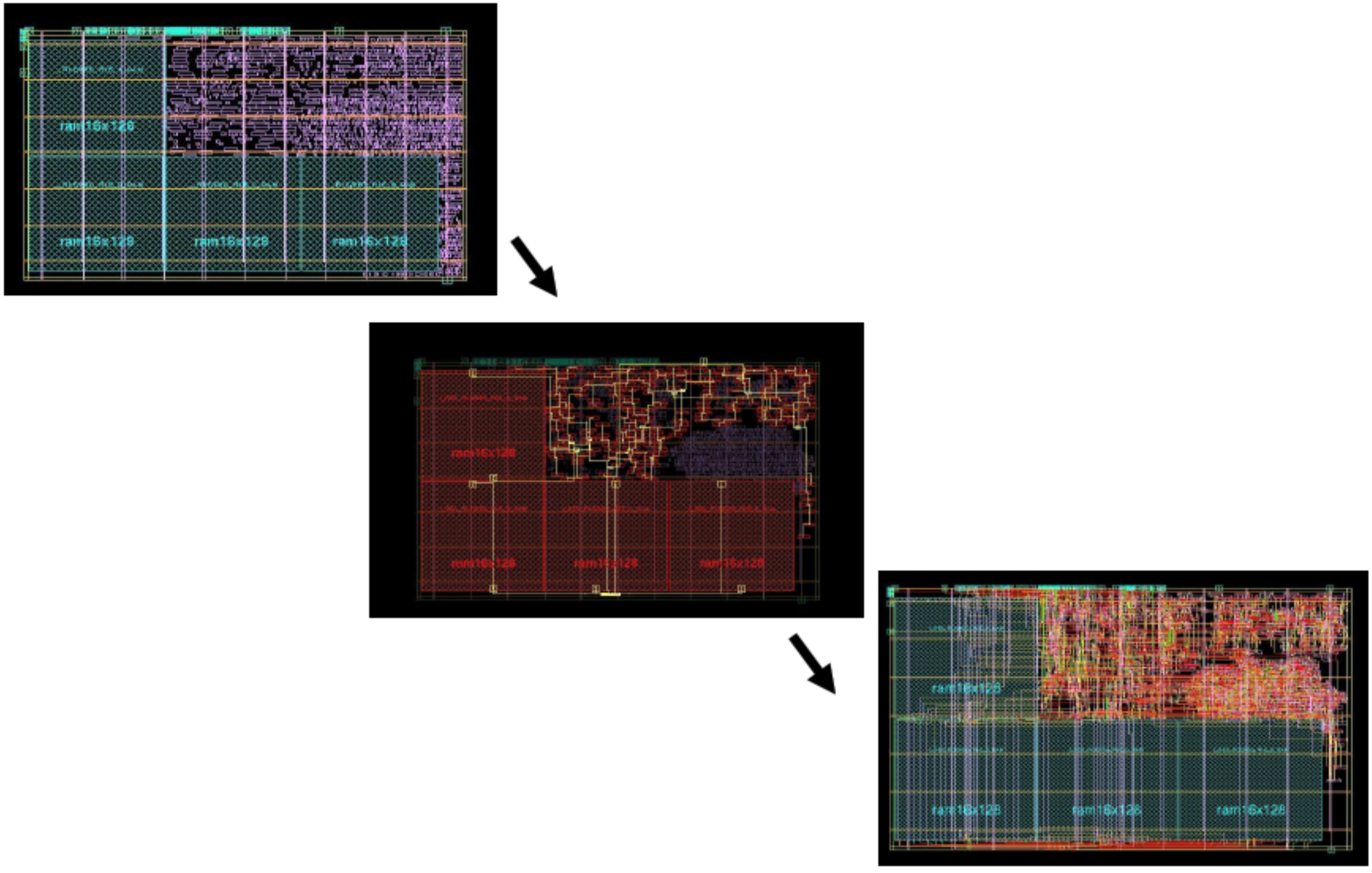
ICC Block Implementation




```
open_mw_cel
set_tlu_plus_file
check_design
set_fix_multiple_port_nets –all

remove_sdc
read_sdc
remove_propagated_clock [all_clocks]

set_dont_touch_placement { hard_macro_list }
set_pnet_options
set_ideal_network [all_fanout -flat -clock_tree ]
place_opt

clock_opt -only_cts -no_clock_route

remove_ideal_network [all_fanout -flat -clock_tree]
set_fix_hold [all_clocks]
clock_opt -only_psyn -no_clock_route

route_group -all_clock_nets

set_si_options
set_route_options
route_opt

save_mw_cel
create_ilm –keep_parasitic –keep_full_clock_tree
create_macro_fram
```

ICC Block Implementation



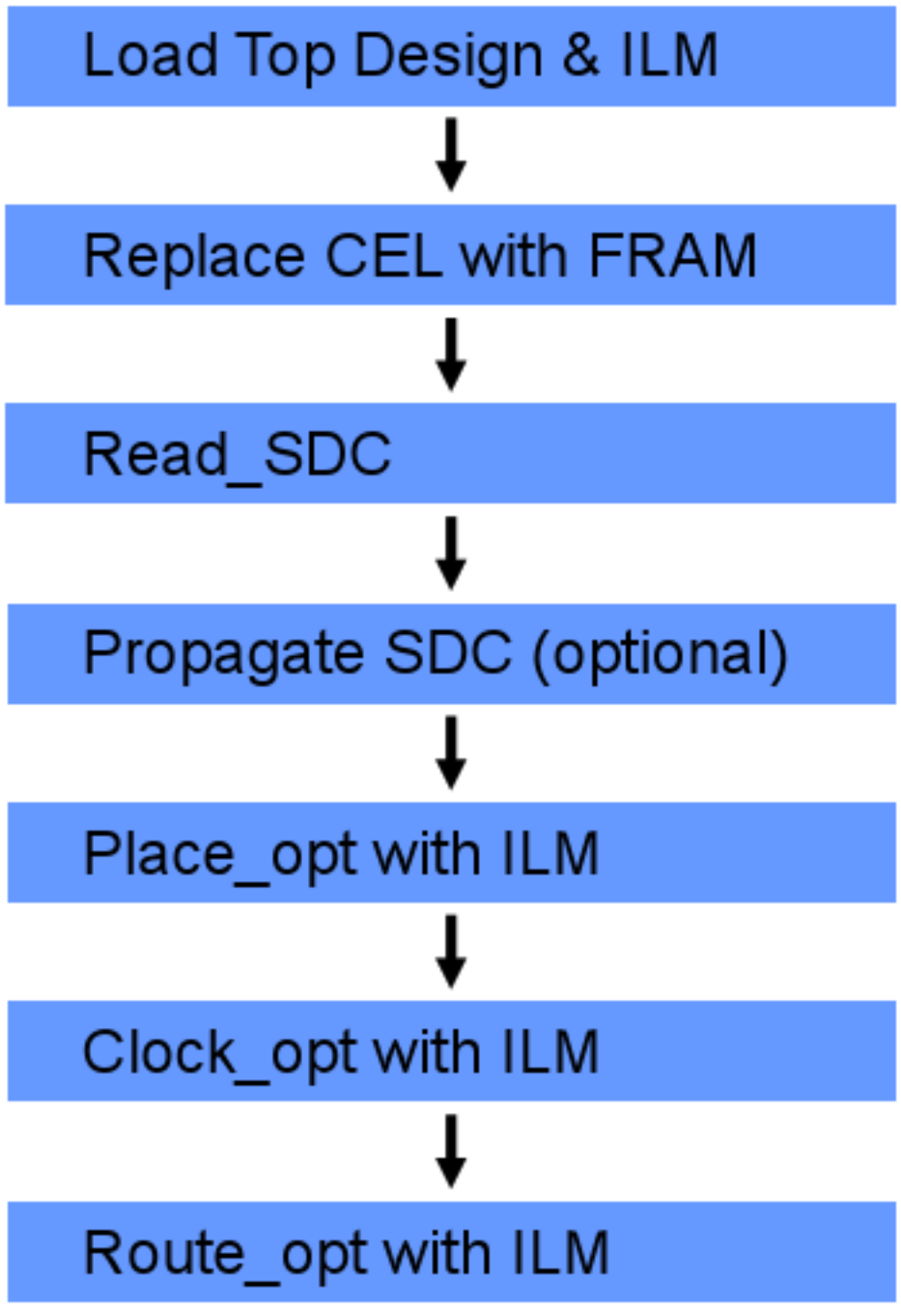
ICC Block Implementation

- Fix hold time violations after CTS
- Use set_si_option to turn on SI options before route_opt
- Use create_ilm –include_xtalk –keep_full_clock_tree to store SI information and local clock tree in ILM
- create_ilm directly saves ILM, no need to use save_mw_cel (since 2007.03)
- Block level flow follows ICC-RM

Agenda

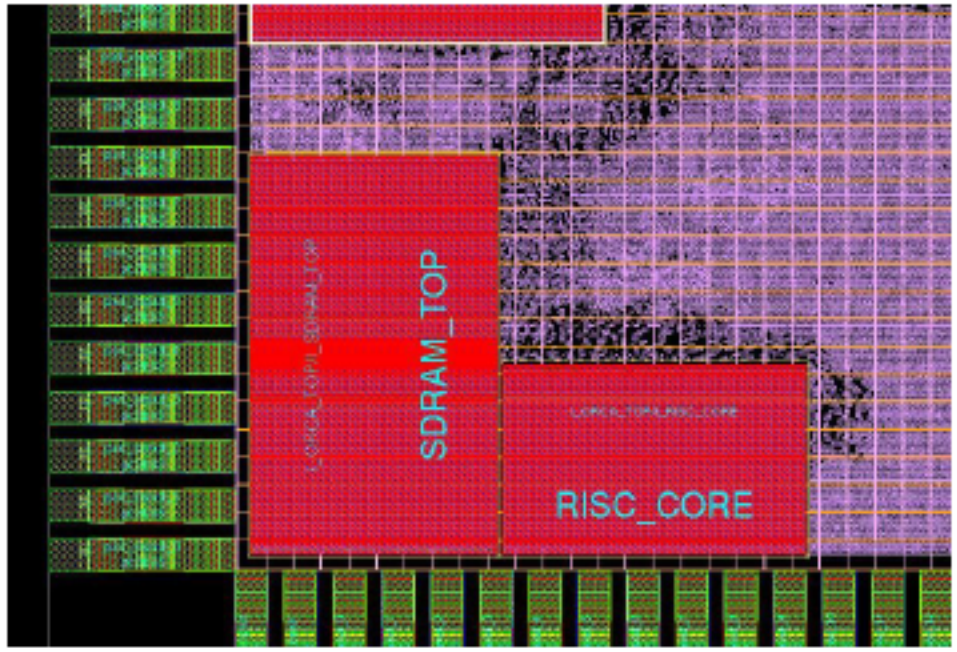
- ICC Hierarchical Flow Overview
- Design Planning
- Block Implementation
- ➢Top Level Implementation
- Lab

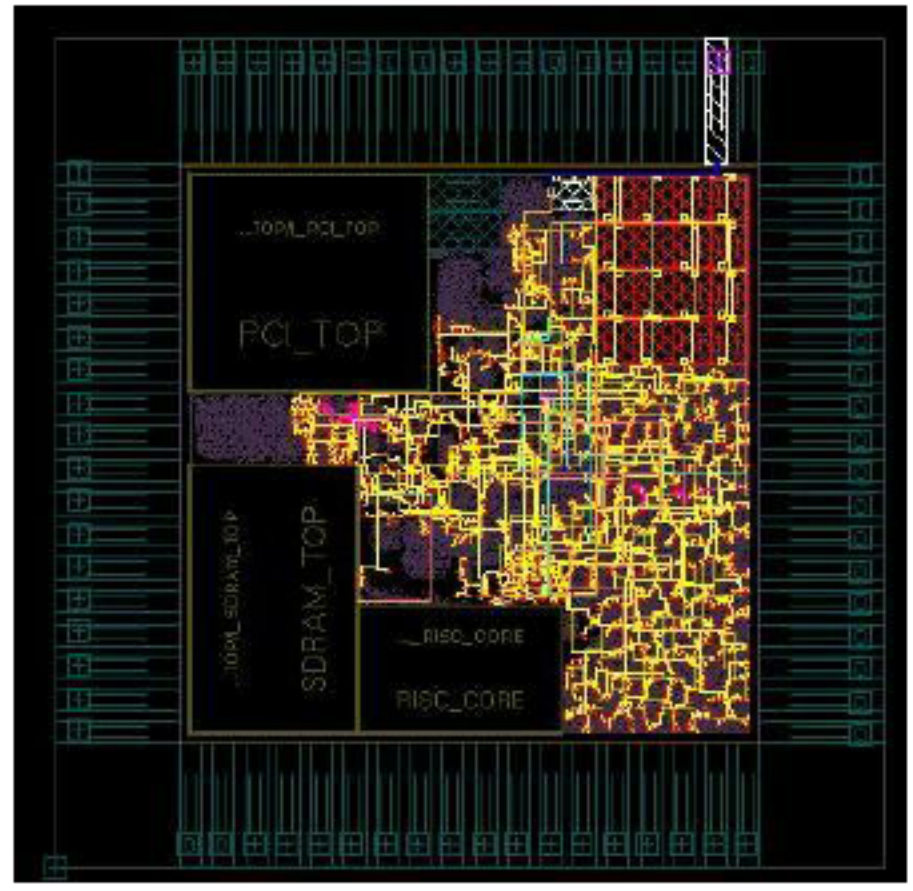
ICC Top Level Implementation

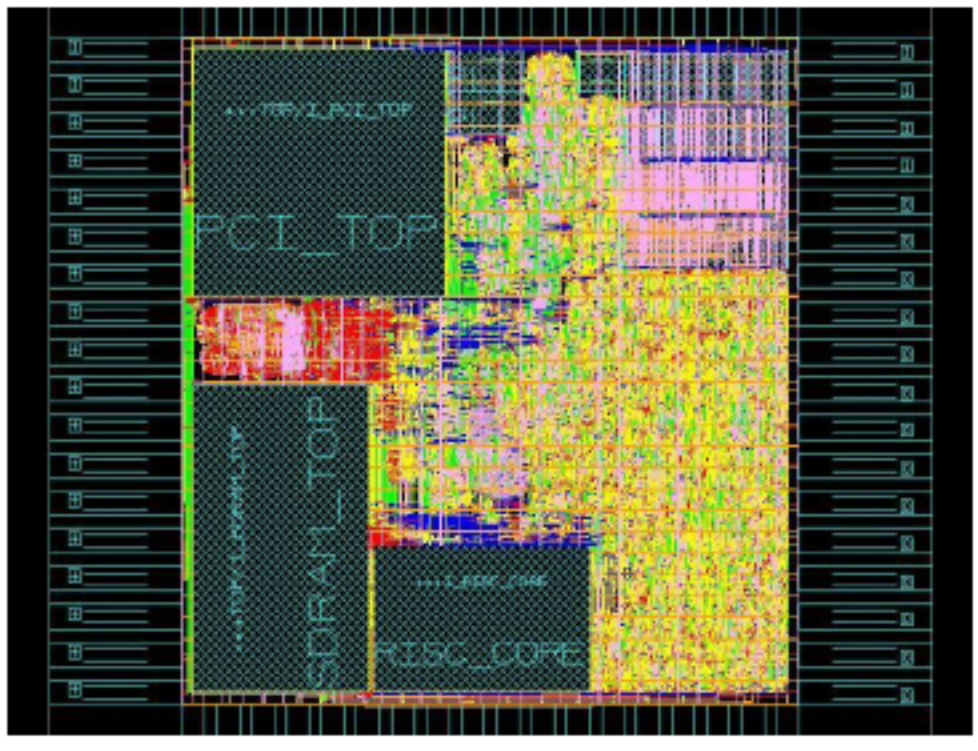



```
set_mw_lib_reference {list block_cel_libs ref_libs}
open_mw_cel

change_macro_view

remove_sdc
read_sdc top.sdc
#propagate_constraints
remove_propagated_clock [all_clocks]

set_dont_touch_placement  {hard_macro_list}
set_pnet_options
set_ideal_network [all_fanout -flat -clock_tree ]
place_opt

set_clock_tree_options -top_mode true
clock_opt -only_cts -no_clock_route

remove_ideal_network [all_fanout -flat -clock_tree]
set_fix_hold [all_clocks]
clock_opt -only_psyn -no_clock_route

route_group -all_clock_nets

set_si_options
set_route_options
route_opt –xtalk_reduction

save_mw_cel
```

ICC Top Level Implementation







ICC Top Level Implementation

- Use ILM/FRAM to represent softmacro in top level
- Top level design loads ILM automatically if ILM is in the reference libraries (since 2007.03)
- No need to do propagate_ilm (since 2007.03)
- Additional SDC constraints can be merged into chip level SDC by using propapate_constraints
- Use “top” mode CTS

Clock Handling

- Clock defined on ILM ports may cause issues in downstream flow steps (Until 2007.03-SP3)
  - Define clock on leaf cell pins
- Fail to propagate up same clock constraints from different ILMs (Until 2007.03-SP3)
  - Create and apply full chip SDC
- CTS does not work on clock nets coming out of ILM (don't touch attribute)
  - Adjust clock tree structure to avoid clock sub tree driven by ILM
  - Disable feedthrough generation for clock pin assignment
- CTS does not support clocks defined inside ILM
  - Do not include PLL module in soft macro

2007.12 Hierarchical Flow Projects

- CTS
  - A-2007.12-cts-005 Support ILM clock definition and CTS exceptions Production
  - A-2007.12-cts-007 Hierarchical Clock Planning Production
  - A-2007.12-cts-024 Mark Clock Tree (Phase I) Production
- ILM
  - A-2007.12-hierarchy-001 Feed-thru support for ILM Production
  - A-2007.12-hierarchy-002 Support Nested ILM Production
  - A-2007.12-hierarchy-003 Support ILM for non place and route blocks Beta
  - A-2007.12-hierarchy-005 Compact ILM Production

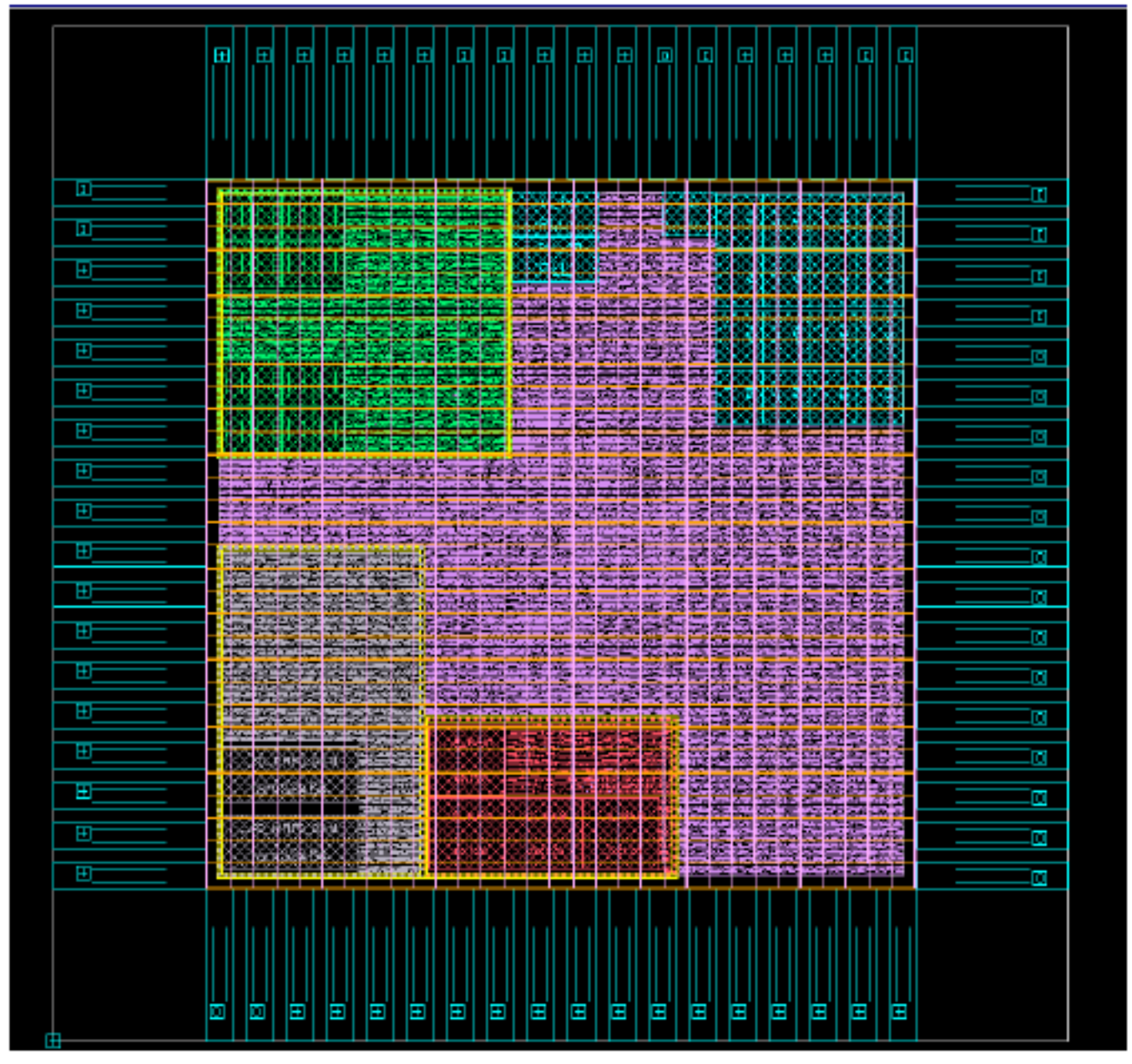
Agenda

- ICC Hierarchical Flow Overview
- Design Planning
- Block Implementation
- Top Level Implementation

➢Lab

Lab

- Testcase: ORCA
  - 54k Inst
  - 41 Hard Macros
  - 3 Soft Macros
    - PCI_TOP
    - RISC_CORE
    - SDRAM_TOP
  - 6 routing layers



Lab Flow

- Hier flow automation based on ICC-RM/ICC-DP-RM
  - Chip Level Design Planning
    - ICC-DP-RM plus Hierarchical DP features
  - Block Implementation
    - ICC-RM plus ILM/FRAM generation
  - Top Level Impelmentation
    - ICC-RM with ILM/FRAM setting
- Data
  - /remote/cae791/hier_flow_lab/ICC_Hier_Lab_2007.03_SP2.tar

Lab Flow

- Phase 1: ICC DP at Top level
  - cd phase_1
  - make dp
- Phase 2: ICC Block Implementation
  - cd phase_2
  - cd PCI_TOP/RISC_CORE/SDRAM_TOP
  - make ic
- Phase 3: ICC Top Level Implementation
  - cd phase_3
  - make ic

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