

Leon (Xuanang) Li

Ph.D. Student - Computer Engineering, University of California, San Diego

@ xul065@ucsd.edu

+1 (858) 666-7695

San Diego, US

Education

University of California, San Diego

Ph.D. in Computer Engineering

Sep 2019-Current, Advisor: Professor Alex Orailoglu

B.S. in Computer Science, *Magna Cum Laude*

Sep 2015-Jun 2019, Advisor: Professor Alex Orailoglu

Work Experience

Cadence Design Systems

Software Engineer Intern

2021 Summer

- Developing Cadence Genus DFT and Modus ATPG produces to improve parallelism and reduce memory usage.
- Developing TCL scripts to verify Cadence tool-flow.
- Incorporating Cadence EDA and testing tools for evaluating the attack resilience of logic obfuscation.

Research Experience

Graduate & Undergraduate Researcher at UCSD

2018-Current

My research interest lies in novel attack strategies on logic locking by exploiting design and test principles, as well as in developing provably-trustworthy hardware systems. The redundancy attack I have proposed [VTS'19, DATE'19] has constituted a critical part in the latest security evaluation framework of logic locking. My current research projects include:

- Developing RTL sequential logic obfuscation methods to achieve multi-dimensional attack resilience.
- Integrating industrial ATPG engines (e.g. TetraMAX) in the oracle-less redundancy attack tool.

Publication

- L. Li, S. Ni, and A. Orailoglu, "JANUS: Boosting Logic Obfuscation Scope Through Reconfigurable FSM Synthesis," in review at *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 2021.
- L. Li and A. Orailoglu, "Redundancy Attack: Breaking Logic Locking through Oracle-less Rationality Analysis," in review at *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2021.
- B.Tan, [et al, including L.Li], "A Community Review of Logic Locking: Reflections, Benchmarking, and Outlook," in review at *IEEE Transactions on Computers (TCOMP)*, 2021.
- L. Li and A. Orailoglu, "Shielding logic locking from redundancy attacks," in *IEEE VLSI Test Symposium (VTS)*, pp.1-6, April 2019.
- L. Li and A. Orailoglu, "Piercing logic locking keys through redundancy identification," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pp. 540-545, March 2019.

Awards

- Third Place in CSAW Logic Locking Conquest, Nov 2019
 - Competed with 10+ university teams in attacking latest locking methods and achieved leading oracle-less efficacy.
- UCSD CSE Research Open House First Place Research Prize, Jan 2019
 - As an undergrad, won the departmental top research prize for graduate students.
- Powell Fellowship Recipient, 2019-2020
- Jacobs School of Engineering Fellowship Recipient, 2019-2021
- UCSD CSE Honorable Mention for Undergraduate Award for Excellence in Research, Jun 2019
- A. Richard Newton Young Student Fellow at DAC 2018, 2019, and 2020

Instruction Experience

Teaching Assistant and Tutor

2016 – Current

- VLSI Testing**
- Synthesis Methodologies in VLSI CAD**
- Design Techniques for Digital Systems*
- Digital Systems Lab*
- Computer Architecture*
- Programming in Java*

** graduate level; * undergraduate level

Skills and Tools

- Proficient in Java, C/C++, and Verilog
- Intermediate in Python and VHDL
- Familiarity with Atalanta ATPG, Design Compiler, Innovus, and ICC2