BK7231U Datasheet

802.11n + BLE 4.2 Comb SoC

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Contents

Revision History

Version	Description	Date	Author
v0.1	Preliminary draft	Mar/12/2018	WF
v0.2	Update package with GPIO28	Mar/20/2018	WF
v0.3	Update with more detail and measurement data	Apr/3/2018	WF
v0.4	Update TX power and current	Apr/12/2018	WF

Figure 1 Revision History

1. Introduction

BK7231U is a 2.4 GHz 802.11n and BLE 4.2 comb chip with multi-media feature. It integrates hardware and software component to finish a complete 802.11b/g/n application, which supports AP and STA role simultaneously, and integrates Bluetooth Low Energy 4.2 transceiver and protocol stack. The 120 MHz ARM9E MCU and embedded 256 KB RAM make it able to support multiple cloud links and also suitable for audio and image application。

BK7231U has flexible peripheral such as PWM, I2S, I2C, UART, SPI, SDIO, USB and IrDA. Up to six channel 32-bit PWM outputs make it suitable for precise LED control.

BK7231U has microphone signal amplify circuit and high performance ADC that it can get 16 bit speech signal with 16 kHz sample rate.

BK7231U has I2S interface, which can work as either master and slave. The sample rate could be from 8 kHz to 48 kHz, and MCLK could be provided to external audio CODEC.

BK7231U has 8-bit DVP to get image data from CMOS sensor, which can be encoded by internal VGA grade motion JPEG codec. The integrated QSPI interface supports FLASH and RAM extension at the same time.

BK7231U provides complete interface to work with external Bluetooth chip, such as co-existence interface, 26 MHz clock and 32.768 kHz low power clock. BK7231U is able to provide transmit active and receive active indicators through two independent ports, to support external PA and external LNA.

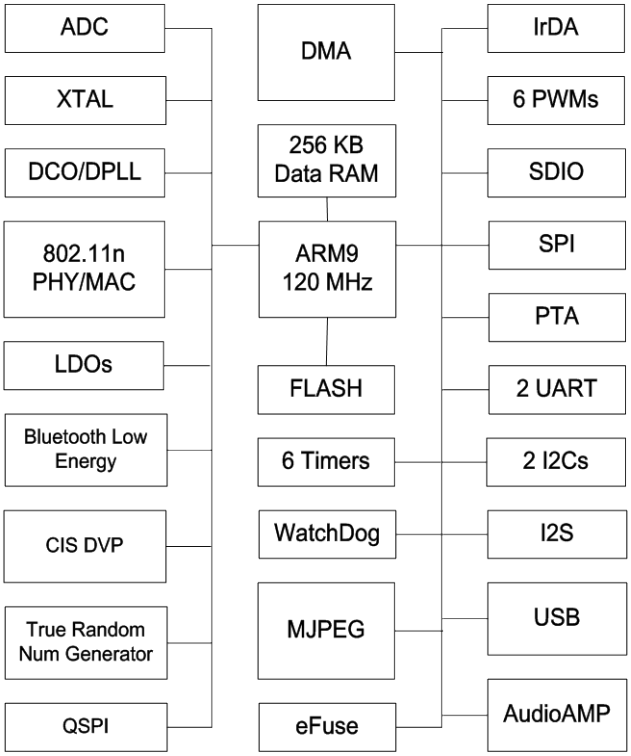
BK7231U has 32 bytes eFUSE for unique ID, code encryption and debug interface disable. The true random number generator supports security communication.

At connected status with Wi-Fi power saving mode, the MCU can enter stand-by mode with a few tens micro-amp current.

There is a deep sleep mode with a few micro-amp current, and could be wake up by either GPIO activation or 32-bit RTC time.

2. Features

- 802.11 b/g/n 1x1 compliant
- Up to 17 dBm output power at 54 Mbps mode
- Wide-band and narrow-band interference detection and alleviation
- 20/40 MHz bandwidth and STBC
- Working mode STA, AP, Direct
- AP and STA role simultaneously
- Bluetooth low energy 4.2 with -90 dBm sensitivity and 20 dBm output power
- Classic Bluetooth co-existence
- Six 32-bit timer and one always on timer
- Six 32-bit PWM with either high speed clock or low power clock
- Microphone signal amplify
- Multi-channel ADC with high speed 10-bits or low speed 16-bit with internal decimation filter
- CMOS sensor 8-bit DVP
- VGA Motion JPEG hardware encoder and dedicate DMA
- 32 bytes eFUSE and true random number generator
- 26 MHz and 32 KHz clock signal output
- ARM9E MCU up to 120 MHz
- 256 KB internal data RAM
- QSPI for RAM and FLASH extension
- QSPI RAM direct mapping to data RAM space
- Multiplexing program download and JTAG interface
- Full speed USB host and device
- 50 MHz SDIO interface and SPI
- Dual I2C interface
- Dual high speed UART with flow control capability



3. Pin Description

BK7231U has QFN5x5 32pin package, with major function for IoT application. Advanced audio and image function will be provided in larger package.

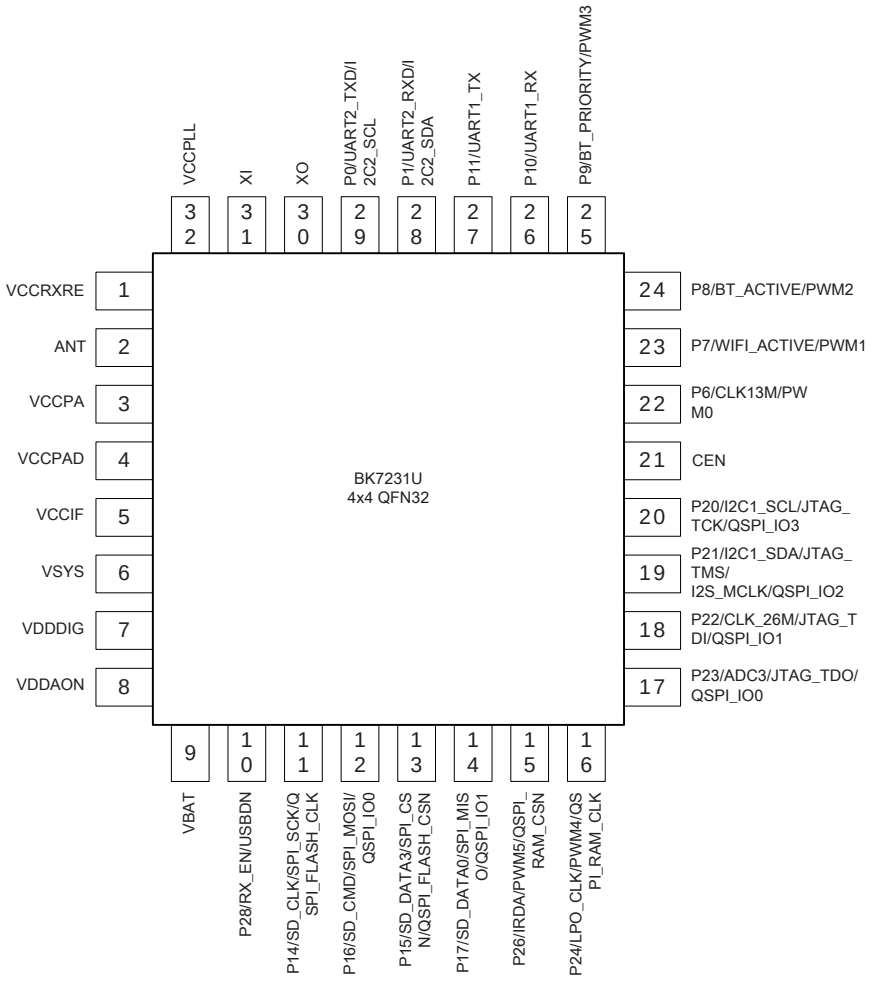


Figure 2 BK7231U 32PIN Definition

Figure 3 BK7231U 32PIN Description

32PIN	Name	Pin Type	Description
1	VCCRXFE	I	RF receiver power supply. Supplied by VSYS
2	ANT	IO	2.4 GHz RF signal port
3	VCCPA	I	RF PA power supply. Supplied by VSYS
4	VCCTX	I	RF transmitter power supply. Supplied by VSYS
5	VCCIF	I	IF power supply. Supplied by VSYS
6	VSYS	O	System LDO output, ~3.0 V
7	VDDDIG	O	Digital LDO output, ~1.2 V
8	VDDAON	O	Always on LDO output, ~1.2 V
9	VBAT	I	Chip power supply, 3.0~3.6V
10	P28/RX_EN/USBDN	IO	GPIO or RX enable or USB DN
11	P14/SD_CLK/SPI_SCK/QSPI_FLASH_CLK	IO	GPIO or SD Card Clock or SPI Clock or QSPI FLASH clock
12	P16/SD_D0/SPI_MOSI/QSPI_IO0	IO	GPIO or SD Card DATA0 or SPI MOSI or QSPI IO0
13	P15/SD_CMD/SPI_CSN/QSPI_FLASH_CSN	IO	GPIO, SD_CMD or SPI CSN or QSPI FLASH CSN
14	P17/SD_D1/SPI_MISO/QSPI_IO1	IO	GPIO or SD Card DATA1 or SPI MISO or QSPI IO1
15	P26/IRDA/PWM5/QSPI_RAM_CSN	IO	GPIO or IrDA input or PWM 5 or QSPI RAM CSN
16	P24/ LPO_CLK/PWM4/QSPI_RAM_CLK	IO	GPIO or low power clock output or PWM 4 or QSPI RAM clock
17	P23/ADC3/TDO/QPIO_IO0	IO	GPIO or ADC or JTAG TDO, or QSPI IO0 FLASH download data output at download mode
18	P22/XHOUT/TDI/QSPI_IO1	IO	GPIO or Crystal clock output, or JTAG TDI or QSPI IO1

			FLASH download data input at download mode
19	P21/I2C1_SDA/TMS/QSPI_IO2	IO	GPIO or I2C1 TMS, or JTAG TMS or QSPI IO2 Flash download chip enable signal at download mode
20	P20/I2C1_SCL/TCK/QSPI_IO3	IO	GPIO or I2C1 SCL, or JTAG TCK or QSPI IO3 Flash download port clock signal at download mode
21	CEN	I	Chip enable, active high
22	P6/CLK13M/PWM0	IO	GPIO or 13 MHz clock output or PWM 0
23	P7/WIFI_ACTIVE/PWM1	IO	GPIO or Wi-Fi active output or PWM 0
24	P8/BT_ACTIVE/PWM2	IO	GPIO or Bluetooth active input or PWM 2
25	P9/BT_PRIORITY/PWM3	IO	GPIO or Bluetooth priority input or PWM 3
26	P10/UART1_RXD	IO	GPIO or UART1 RXD
27	P11/UART1_TXD	IO	GPIO or UART1 TXD
28	P1/UART2_RXD/I2C2_SDA	IO	GPIO or UART2 RXD or I2C2 SDA
29	P0/UART2_TXD/I2C2_SCL	IO	GPIO or UART2 TXD or I2C2 SCL
30	XO	O	26/40 MHz Crystal output
31	XI	I	26/40 MHz Crystal input
32	VCCPLL	I	RF PLL power supply. Supplied by VSYS after RC filter

4. Wi-Fi and Bluetooth

The BK7231U supports full features of 802.11b/g/n Wi-Fi system, with both HT20 and HT40 capability. There are transmitter active indicator (GPIO25) and receiver active indication (GPIO28) for external LNA and PA to reach longer range.

The integrated Bluetooth low energy 4.2 shares the single antenna port with Wi-Fi transceiver, and both Wi-Fi and Bluetooth could work simultaneously with precise time multiplexing.

5. Clock

There are seven root clock signals in the system.

- X26M: The high speed crystal oscillator, typical frequency is 26 MHz, which is also the reference clock signal for digital PLL (DPLL) and audio PLL (I2SPLL); There is tunable load capacitance from 6 to 18 pF (both side have this capacitance) with 64 steps to tune the crystal frequency, that no external capacitance is needed; This clock signal has about one milliseconds startup time
- DCO: Internal high speed digital controlled oscillator, with frequency from 26 MHz to 120 MHz, and about +/-2 frequency variation after calibration; This clock signal has a few microsecond startup times
- X32K: The high speed crystal oscillator, typical frequency is 32.768 kHz
- D32K: 32 kHz clock signal divided from X26M
- ROSC: Internal low speed ring oscillator with ±2% variation after calibration
- DPLL: High speed 480 MHz PLL clock
- I2SPLL: PLL for audio signal, typical frequency is 1024*FS and typical FS is 44.1 kHz or 48 kHz

Low power clock (LPO_CLK) is selected from X32K, D32K or ROSC.

The MCU and peripheral clock selection option is list as follows.

	X26M	**DCO**	**DPLL**	**LPO_CLK**	**I2SPLL**
MCU	√	√	√	√	
ADC	√	√			√
SDIO	√	√			
PWM	√	√		√	

SPI	√	√			
I2C2	√	√			
IrDA	√	√			
I2C1	√	√			
UART2	√	√			
UART1	√	√			
QSPI	√	√	√		
Timer 1	√				
Timer 2				√	
I2S					√
CIS/MJPEG			√		
Watch Dog				√	
Always on timer				√	

There is also clock output capability to output clock signal for external components.

- The LPO_CLK and X26M clock could be output to GPIO for general purpose.
- 13 MHz clock divided from X26M: It is aimed to provide clock for FM receiver
- I2S MCLK: It is divided from I2SPLL and the divider number could be 1, 2, 4, 8, 16
- PCLK for CIS Sensor: It is divided from DPLL and the typical frequency is 24 MHz, 48 MHz or 96 MHz

6. Reset

System power on, digital power on and watch dog reset have the same reset effect for major blocks except always on logic, that any reset will reset the BK7231U whole chip to initial status. The always on logic has one 32 bit timer and 16 bit retention register, which could be only reset to initial value by system power on reset.

Waking up from either shut down mode or deep sleep mode will power on digital from power down mode, that trigger the whole system reset procedure.

7. Power management

To reduce power, the BK7231U can be put in three low power modes as follows.

Shutdown – In this mode all circuits are powered down when CEN = 0, and the system will power on only after CEN back and keep to high for a few milliseconds.

Deep sleep mode – In this mode all circuits are powered down except the GPIO and always on logic, that any GPIO edge transition or always on timer time out event can power up the system again. The retention register could keep it contents at this mode.

Normal Standby – In this mode the MCU stop running and all peripheral interrupt can resume MCU.

Low voltage Standby – In this mode the MCU and all digital logic stop their clock, and the power supply of them decrease to a much lower retention voltage, that the current could be much lower. In this mode, only GPIO and RTC timer could resume the system to run mode with normal voltage.

8. Peripheral

8.1. UART

BK7231U has two sets of UART. The maximum baud rate can be up to 6 Mbps. It supports 5, 6, 7 and 8 bits data mode, and supports even, odd or none parity check. The stop bit can be either 1 or 2 bits.

The UART1 supports hardware and software flow control with RTS and CTS signal.

At MCU low voltage stand-by mode, the continuously low level applied on TXD or RTD could wake up the MCU that the UART and MCU can resume to active mode.

8.2. SPI

BK7231U supports one high speed SPI interface with maximum 50 MHz clock speed, with only slave mode. This high speed SPI has dedicated DMA channel that could work on high speed without MCU load.

It also supports low speed SPI interface with up to 8 MHz, with both master and slave mode. The receive data could be latched on either rising edge or falling edge of clock signal. The transmit data could be set by MSB or LSB first.

8.3. SDIO

BK7231U SDIO has both master and slave mode, and one bit to four bits mode with maximum 50 MHz clock speed. SDIO could be used as master mode to read external SD card or used by external host to communicate with chip as slave mode.

SDIO has dedicated DMA channel that could work on high speed without MCU load.

8.4. I2C

BK7231U supports two sets of I2C with normal 400 kHz clock speed, with 7 bit addressing. If low level on SCL or bus idle duration is greater than a programmable threshold, it will generate interrupt to MCU.

8.5. USB

BK7231U has full speed USB 2.0, with both host and device mode. The host or device mode is selected by software register.

USB has dedicated DMA channel that could work on high speed without MCU load.

8.6. ADC

BK7231U has multi-channel ADC and supports 10-16 bits output with internal decimation filter. Single, continuously and software read mode are supported.

Besides GPIO, the system power VSYS, temperature sensor and internal calibration circuit could be also the ADC source.

8.7. PWM

BK7231U has six 32-bit PWM outputs. The PWM running clock can be either high speed clock or low power clock. Each PWM runs independently with its own duty cycle.

The PWM has capture mode that can count the cycle between two rising edges or two falling edges.

8.8. Timer

BK7231U has two group peripheral timers; each group has three 32-bit timers. The first group three timers run with crystal clock with 4-bit prescaler. The second group three timers run with low power clock with another 4-bit prescaler.

The watch dog time is used to reset system as long as the software runs out of order, and it stops as long as MCU stops or power off.

The always on timer works under always on power domain, that it can keep running even MCU is power off.

8.9. GPIO

BK7231U has total 40 GPIOs and anyone could be set an interrupt source to interrupt system at active mode or wake up system from sleep mode.

The GPIO has peripheral function as table below.

GPIO	Peripheral Function
GPIO0	UART2_TXD/I2C2_SCL
GPIO1	UART2_RXD/I2C2_SDA
GPIO2	I2S_CLK/ADC5
GPIO3	I2S_SYNC/ADC4
GPIO4	I2S_DIN/ADC1
GPIO5	I2S_DOUT/ADC2

GPIO6	CLK13M/PWM0
GPIO7	WIFI_ACTIVE/PWM1
GPIO8	BT_ACTIVE/PWM2
GPIO9	BT_PRIORITY/PWM3
GPIO10	UART1_RX
GPIO11	UART1_TX
GPIO12	UART1_CTS/ADC6/PGA_INP
GPIO13	UART1_RTS/ADC7/PGA_INN
GPIO14	SD_CLK/SPI_SCK/QSPI_FLASH_CLK
GPIO15	SD_CMD/SPI_CSN/QSPI_FLASH_CSN
GPIO16	SD_DATA0/SPI_MOSI/QSPI_IO0
GPIO17	SD_DATA1/SPI_MISO/QSPI_IO1
GPIO18	SD_DATA2/QSPI_IO2
GPIO19	SD_DATA3/QSPI_IO3
GPIO20	I2C1_SCL/JTAG_TCK/QSPI_IO3
GPIO21	I2C1_SDAJTAG_TMS/ I2S_MCLK/QSPIO_IO2
GPIO22	CLK_26M/JTAG_TDI/QSPI_IO1
GPIO23	ADC3/JTAG_TDO/ QSPI_IO0
GPIO24	LPO_CLK/PWM4/QSPI_RAM_CLK
GPIO25	TXEN/USBDP/
GPIO26	IRDA/PWM5/QSPI_RAM_CSN
GPIO27	CIS_MCLK
GPIO28	RX_EN/USBDN/
GPIO29	PCLK
GPIO30	HSYNC/SPI_SCK
GPIO31	VSYNC/SPI_CSN
GPIO32	PXD0/SPI_MOSI
GPIO33	PXD1/SPI_MISO
GPIO34	PXD2/SD_CLK
GPIO35	PXD3/SD_CMD
GPIO36	PXD4/SD_DATA0
GPIO37	PXD5/SD_DATA1
GPIO38	PXD6/SD_DATA2
GPIO39	PXD7/SD_DATA3

Figure 4 GPIO Peripheral Functions

8.10. FLASH Download

Any time the digital logic resets to active, within a few hundred milliseconds the GPIO20~GPIO23 will act as mode selection port and then back to normal GPIO mode. If there is FLASH download command, these four ports will change to FLASH download port that FLASH could be programming.

8.11. CMOS Sensor Interface and MJPEG Encoder

The CMOS sensor interface provides 8-bit parallel port interface (GPIO32~GPIO39) to VGA sensor, together with main clock (GPIO27), pixel clock (GPIO29), HSYNC (GPIO30) and VSYNC (GPIO31) signal. Supported sensor could be but not limited to be OV7676, OV7670, GC0308, GC0309, GC0329 and PAS6329.

The interface and MJPEG work with 96 MHz clock divided from DPLL, and the main clock to the sensor is integer divided from 96 MHz.

The sensor YUV input will be directly fed to hardware MJPEG encoder, and the MJPEG encoder output will be write to data memory directly by dedicate DMA.

The YUV signal format could be YUYV, UYVY, YYUV and UVYY. HSYNC and VSYNC edge could be set independently.

8.12. IrDA interface

There is a hardware IrDA decoder interface to decode the signal. Also the interface has the capture timer capability to allow software decoding the input signal.

8.13. I2S interface

The I2S interface supports both master and slave mode, with sample rate from 7.35 kHz to 96 kHz. The master clock can be output by GPIO21.

8.14. Microphone amplify

GPIO12 and GPIO13 could be set as differential microphone input, and the input signal could be amplified by internal audio amplifier. Amplified audio signal could be converted to digital signal and decimate to standard 16 kHz 16 bit PCM data by ADC.

8.15. QSPI Interface

The QSPI is designed for FLASH and RAM extension. The data IO are time shared by FLASH and RAM, while dedicate clock and select signal are separately used by FLASH and RAM. The QSPI can work up to 120 MHz, and FLASH clock and RAM clock can be set different.

8.16. Security

There are a true random number generator and eFUSE for system and communication security.

The 32 byte eFUSE could be written through download port GPIO20~GPIO23 at download mode. The eFUSE has defined function mapping as follows. All bytes could be read by MCU and download port except low 16 bytes could not be read out by download port.

Byte 31	Byte 30:16	Byte 15:0
JTAG Interface Disable	User Defined such as MAC address	Code Encryption

8.17. Temperature Sensor

The temperature sensor has +/-3 degree precision and could detect temperature from -40 to +125 degree, and digital result could be read out from ADC.

9. Characteristics

9.1. Absolute maximum ratings

Item	Pin Name	Min.	Max.	Unit

Battery and Power Supply IO	VCCRXFE, VCCPA, VCCTX, VCCIF, VSYS, VBAT, CEN, VCCPLL	-0.3	3.9	V
Core Power Supply	VDDDIG, VDDAON			
Digital Input Pin		-0.3	3.9	V
Analog Pin	XO, XO	-0.3	1.5	
RF Pin	ANT	-0.3	1.5	V
Storage Temperature		-55	125	℃

9.2. ESD Ratings

Item	Detail	Value	Unit
ESD_HBM	Electrostatic Discharge Tolerance under Human Body Model	+/-2000	V
ESD_MM	Electrostatic Discharge Tolerance under Man Machine Model	+/-200	V
ESD_CDM	Electrostatic Discharge Tolerance under Charged Device Model	+/-250	V

9.3. Recommended operating conditions

Parameters	Condition	Min.	Typ.	Max.	Unit
Operation Voltage	VBAT-pin	3.0	3.3	3.6	V
Operation Temperature		-20		85	℃

9.4. Current Consumption

Parameters	Condition	Min.	Typ.	Max.	Unit
Transmit current	17 dBm, 802.11b 11Mbps		230		mA
Transmit current	14 dBm, 802.11g 54Mbps		200		mA
Receiver current	-10 dBm input, 802.11g 54Mbps		104		mA
Receiver current	-10 dBm input, 802.11n HT40 MCS7		124		mA
Normal Stand-By	MCU stop, Modem power Off, could be woke up by internal timer		68		uA
Low Voltage Stand-By	MCU stop with low voltage, could be only woke up by GPIO or RTC timer		24		uA

Deep-sleep current	All power off, could be only woke up by GPIO or RTC timer		7		uA
Shut-down current	CEN=0		1		uA
Note: The measurement above is at 25 degree and 3.3 V battery voltage					

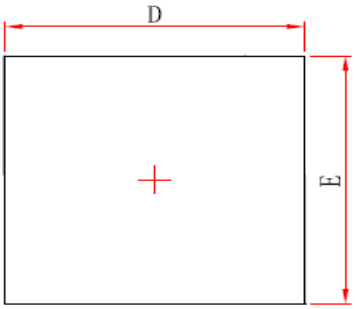
9.5. WLAN Receiver Characteristics

Parameters	Condition	Min.	Typ.	Max.	Unit
Sensitivity	HT40 MCS7		-69		dBm
	HT20 MCS7		-71		dBm
	54 Mbps OFDM		-75		dBm
	6 Mbps OFDM		-92		dBm
	11 Mbps DSSS		-90		dBm
	2 Mbps DSSS		-94		dBm
ACS (25 MHz away)	54 Mbps OFDM		21		dB
	11 Mbps DSSS		31		dB

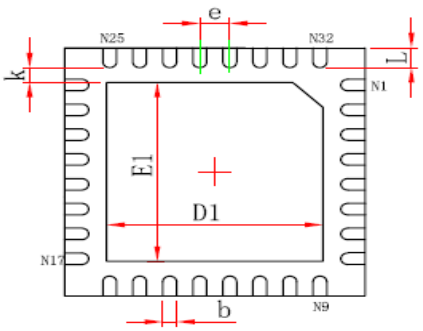
9.6. WLAN Transmitter Characteristics

Parameters	Condition	Min.	Typ.	Max.	Unit
Transmit Power EVM and MASK Compliant	54 Mbps OFDM		14		dBm
	11 Mbps DSSS		17		dBm

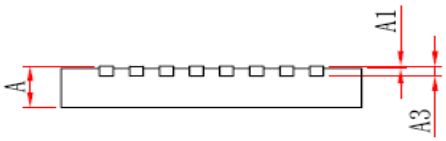
10. Package



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.300	3.500	0.130	0.138
E1	3.300	3.500	0.130	0.138
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

11. Order Information

Part number	Package	Packing	MPQ(ea)
BK7231UQN32	QFN32_5X5	Tape Reel	3K