Total time: 100min

Description : This circuit is designed to count, incrementing itself every 2 seconds. It then displays the number of “1” bits. It can also store the counter value in a RAM memory for later use.

Implement the above described circuit using the diagram below, where:

Counter = counter circuit with enable input. Reset is active low. One counter is on 30b, the other on 4b. (you can write 2 separate counters or use parameters). The first counter will be able to count up to 2 seconds. Replace the “?” with the correct value as to achieve this requirement.

Comparator a>b circuit = outputs “1” if input a is greater than input b. “0” otherwise.

Mux = multiplexer circuit.

ROM = Read Only Memory used as a lookup table to fast calculate how many “1” bits the input has.

Transcoder-7seg = Transcoder module that outputs data in the specific 7seg display format.

Ram = Ram memory used for storing data from the second counter’s output.

Simulation waveforms:

clock : changes every 2 time units

reset : initial value 1; after 100 time units becomes 0; after 25 clock cycles becomes 1;

mux select : initially 1. Changes after 300 time units.

ram addr : initially 0. After 300 time units becomes 5.

Simulation stops after 10.000.000 time units.

In order for the simulation to complete in a reasonable time, please set “?” at 500_000. After simulations have ended please remember to set the proper value back.

Constrangeri:

clock = 50 Mhz

rst_n = button 1. Buttons work on negative logic.

sel (from mux) = button 0

7seg0 and 7seg1 = 7segment displays

Ram addr input = switches 2:0

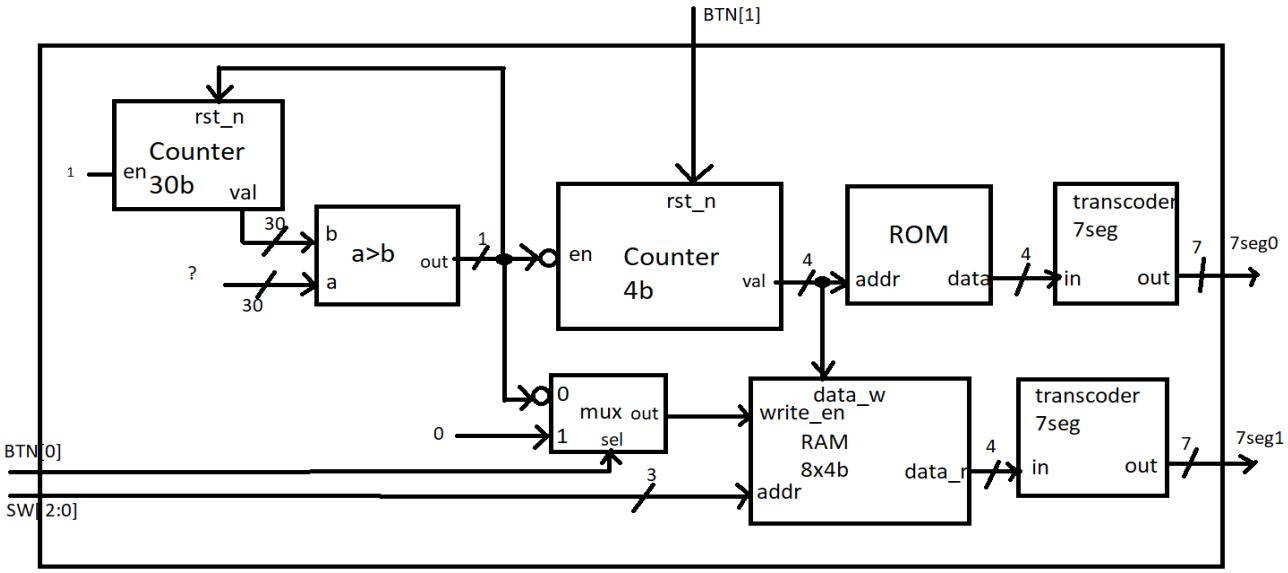
Important :

Replace the “?” with the proper value in order to make the first counter count up to 2 seconds .

Interfaces must be identical the those used in the schematic below.

Give proper names to all your files, modules, wire.

Take note that some inputs are negated. You can use additional not gates (not represented on the schematic for clarity reasons) if that is the way you choose to implement this functionality.



Points distribution: (total 30)

Top : 5

Counter1 : 2

Counter2 : 2

(If parametrized approach is chosen: Counter_parametrized : 6)

Comparator : 1

Multiplexer : 1

ROM : 3

RAM : 4

Transcoder : 0 (is given)

Testbench : 4

Simulation : 3

Constraints : 3

Final functionality, FPGA demonstration : 2