CPE 301 - MICROPROCESSOR SYSTEM DESIGN
Fall 2013

HOMEWORK No. 03 - DUE (beginning of class) September 17

NOTE: These problems are adapted from chapter 12 of *Digital Logic and Computer Design* by Morris Mano (Mano **Book2** Chapter 12 on WebCampus). There is also an additional memory design reference (Mano **Book1** Chapter 7 on WebCampus) which is from an earlier version of your CPE 201 textbook.

1. (a) How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(b) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?
(c) How many lines must be decoded for chip select? Specify the size of the decoders.

2. A microprocessor uses RAM chips of 1024 X 1 capacity.

(a) How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?
(b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

3. A ROM chip of 1024 X 8 bits has four select inputs and operates from a 5-volt power supply. How many pins are needed for the IC package? Draw a block diagram and label all input and output terminals in the ROM.

4. Extend the memory system of Fig. 12-13 to 4096 bytes of RAM and 4096 bytes of ROM. List the memory-address map and indicate what size decoders are needed.

5. A microprocessor employs RAM chips of 256 X 8 and ROM chips of 1024 X 8. The microcomputer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped 1/0 configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

(a) How many RAM and ROM chips are needed?
(b) Draw a memory-address map for the system.
(c) Give the address range in hexadecimal for RAM, ROM, and interface.

6. An 8-bit microprocessor has a 16-bit address bus. The first 15 lines of the address are used to select a bank of 32K bytes of memory. The high-order bit of the address is used to select a register which receives the contents of the data bus. Explain how this configuration can be used to extend the memory capacity of the system to 8 banks of 32K bytes each, for a total of 256K bytes of memory.