CPE 301

Microprocessor System Design Lab
Fall 2013

LAB #11

Objective:

To become familiar with Verilog and the Xilinx FPGA compiler.

Procedure:

1. Read the support documents in this folder

2. Because the support documents use a different tool chain than we do there are several differences in procedure. The Gates2 example is provided for both tool chains. Please read and compare (FPGA_Design_Gates2.pdf) and (XilinxTutoriaScreenshotsl.pdf).

3. Using the Xilinx tool chain:

    a. Implement and test the Gates4 example in (FPGA_Design_Gates4.pdf)

    b. Implement and test Problem 3.1 in (FPGA_Design_Gates4.pdf)

    c. Implement and test Problem 3.2 in (FPGA_Design_Gates4.pdf) - NOTE: a 3 to 8 decoder example is attached as the last page of (FPGA_Design_Gates4.pdf).

Use the XilinxTutorialScreenshots1.pdf file as a guide to compile and simulate these examples. You will generate the simulations as described beginning at step 12 in the tutorial. You will then complete the steps beginning with step 24 of the tutorial and program and test the Spartan 3E FPGA on the Digilent Nexsys-2 development board.

NOTES:

You can download and install the required software on your own computer or use the computers in the lab which already have the software installed. The Xilinx download is quite large and may require a long time to download.