**Lab 10: Counters**

Terence Henriod

CPE 201

April 22, 2013

**Design a sequential circuit that counts from 0 to 7 indefinitely.**

1. **State Diagram**

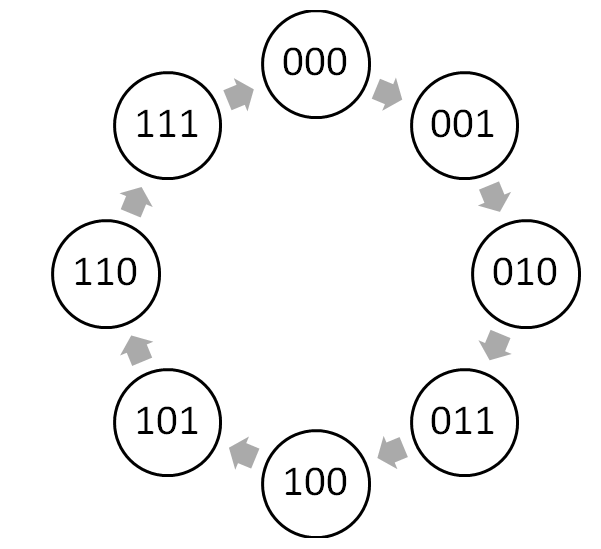


Figure 1: The state diagram for the enable-high synchronous counter. Its input is not displayed, because the only input is the clock. The state changes with every tick.

1. **State Transition Table**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Inputs | | | Next States | | | Outputs | | | |
| mi | A | B | C | A(t+1) | B(t+1) | C(t+1) | O2 | O1 | O0 | 7-Seg  Disp |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 2 |
| 3 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 3 |
| 4 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 4 |
| 5 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 5 |
| 6 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 6 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 7 |

Table 1: The state table for the synchronous counter. The state changes with every clock tick.

1. **K-maps**

\*Note: The K-maps are ordered differently to accommodate for the alternative placement of the ‘E’ values in the truth table.

* 1. **A(t+1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A \ BC | 00 | 01 | 11 | 10 |
| 0 |  |  | 1 |  |
| 1 | 1 | 1 |  | 1 |

Table 2: The K-map for the activity of A(t+1).

* 1. **B(t+1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A \ BC | 00 | 01 | 11 | 10 |
| 0 |  | 1 |  | 1 |
| 1 |  | 1 |  | 1 |

Table 3: The K-map for the activity of B(t+1).

* 1. **C(t+1)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A \ BC | 00 | 01 | 11 | 10 |
| 0 | 1 |  |  | 1 |
| 1 | 1 |  |  | 1 |

Table 4: The K-map for the activity of C(t+1).

1. **Simplified logical expressions for inputs**

Note: Some of the expressions were re-evaluated so that an XOR gate could be used for convenience.

1. **Design in Logisim**

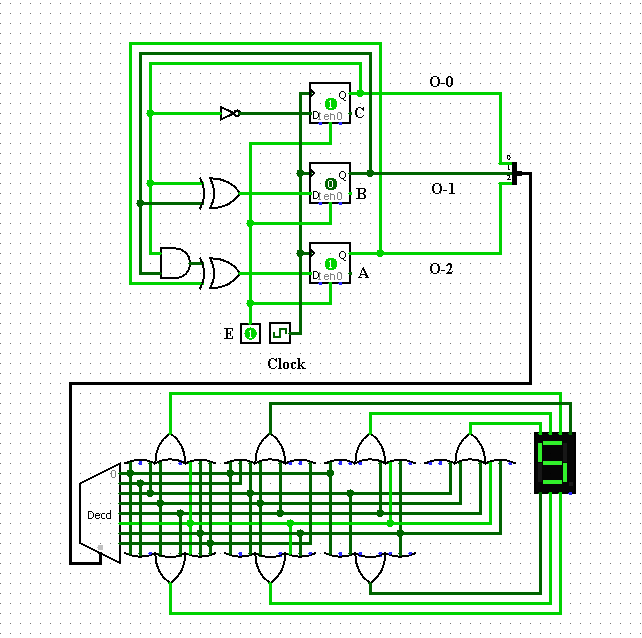


Figure 2: The Logisim implementation of the enable-high synchronous binary counter, along with a 7-segment display and driver. The counter implementation is in the top half, with the 7-segment display below.

1. **Breadboard Implementation using 74174 (6xD flip-flop), 7408 (AND), 7486 (XOR).**

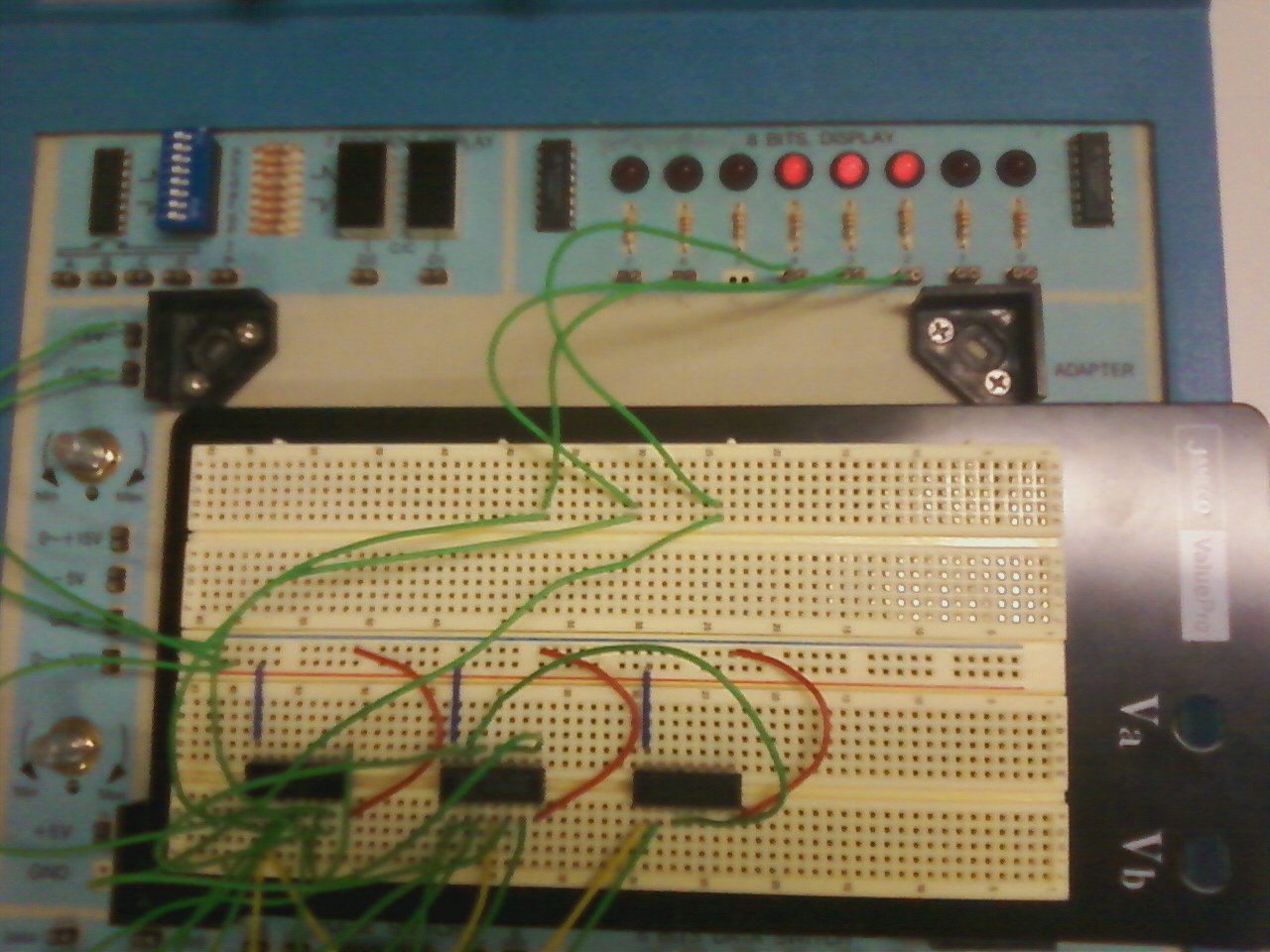


Image 1: A picture of the breadboard implementation of the synchronous counter circuit, using XOR instead of some other logical operations.