**Lab 5: Full-Adders**

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**Full-Adder Design**

1. Truth Table

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Inputs | | | Outputs | |
| Input 1 (X) | Input 2 (Y) | Input 3 (Z) | S | C |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

1. K-Map

For S:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Z**\**XY | 00 | 01 | 11 | 10 |
| 0 |  | 1 |  | 1 |
| 1 | 1 |  | 1 |  |

For C:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Z**\**XY | 00 | 01 | 11 | 10 |
| 0 |  |  | 1 |  |
| 1 |  | 1 | 1 | 1 |

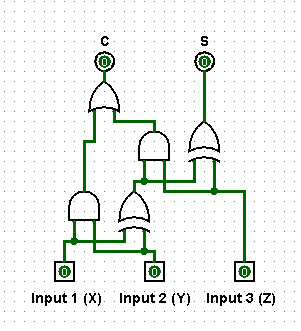
1. Simplified Logical Expressions

S(X, Y, Z) = (X Y) Z X Y Z (with odd number of 1s 🡪 1)

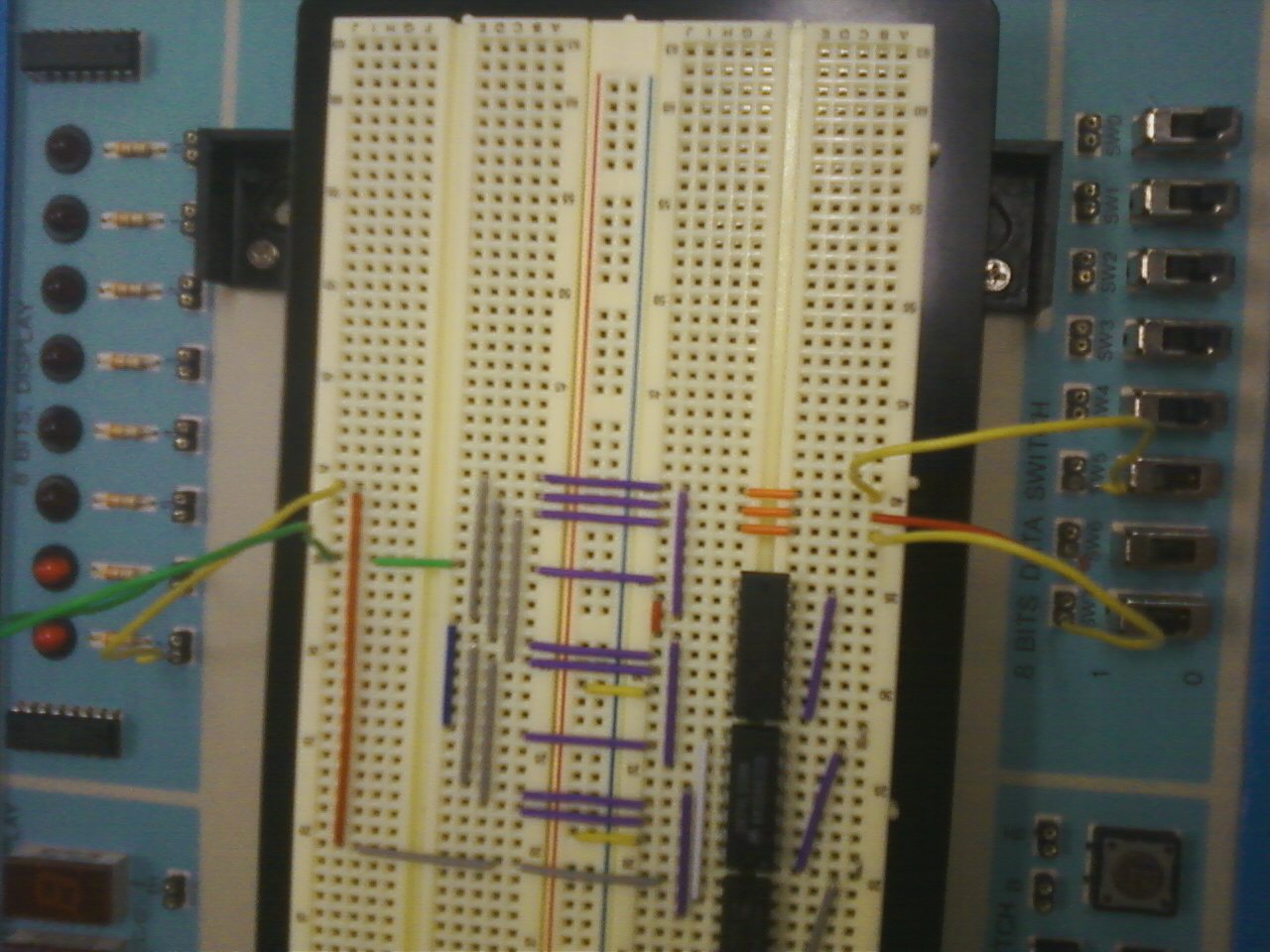
C(X, Y, Z) = XY + (X Y) \* Z XY + XZ + YZ

**Full-Adder Implementation**

1. Design in Logisim



1. Breadboard implementation using the 7486 (XOR), 7432 (OR), and 7408 (AND) chips.



As can be seen in the picture, all three switches are set to the on (1) position, producing the binary equivalent of 3 (11), as indicated by the LEDs.