**Lab 6: Decoders**

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CPE 201

March 25, 2013

**Part 1: 2-to-4 Decoder (Active High)**

Design a 2-to-4 (2 Inputs and 4 Outputs) decoder. (Enable bit will be active high. Output will be active high)

1. Truth Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| E  (Active High) | i0 | i1 | d0 | d1 | d2 | d3 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Table 1: The truth table of an Active-High 2 to 4 decoder.

1. Logical Expressions
2. Logisim Circuit using 7408 (AND) and 7404 (INVERTER)

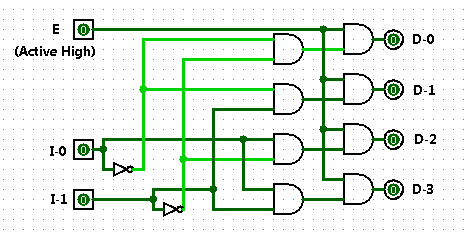


Figure 1: The Logisim implementation of an Active-High 2 to 4 decoder in AND implementation.

**Part 2: 2-to-4 Decoder (Active Low)**

Design a 2-to-4 (2 Inputs and 4 Outputs) decoder. (Enable bit will be active low. Output will be active low)

1. Truth Table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| E  (Active High) | i0 | i1 | d0 | d1 | d2 | d3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 2: The truth table of an Active-Low 2 to 4 decoder.

1. Logical Expressions
2. Logisim Circuit using 7410 (3 Input NAND) and 7404 (INVERTER)

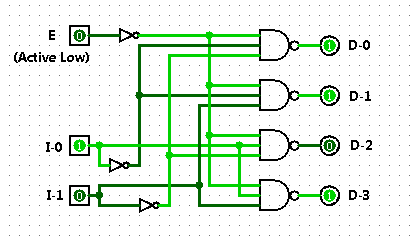


Figure 2: The Logisim implementation of an Active-Low 2 to 4 decoder in NAND implementation.

1. Breadboard Implementation Using 7410 (3 Input NAND) and 7404 (INVERTER)

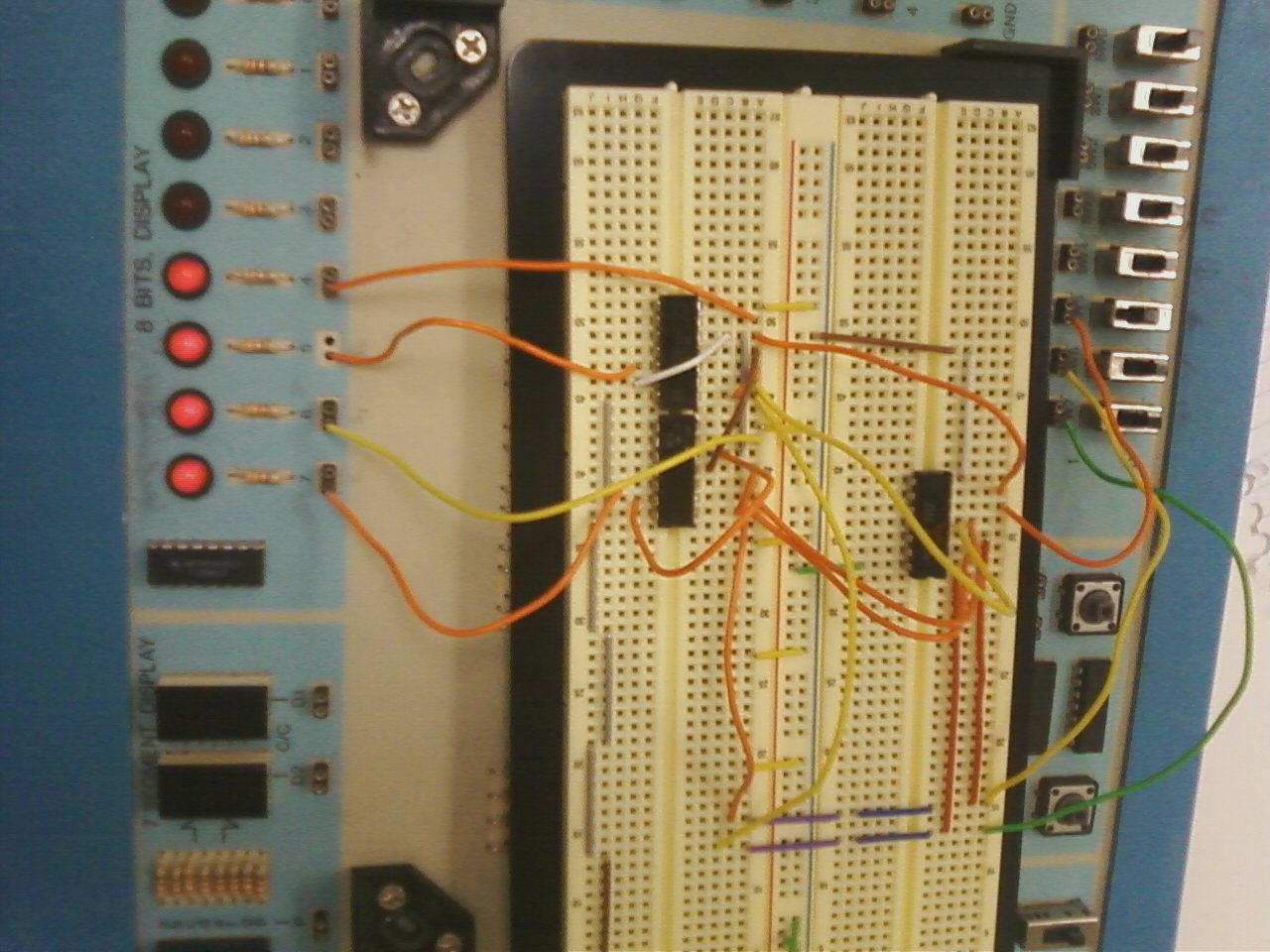


Figure 3: The breadboard implementation of an Active-Low 2 to 4 decoder using 3 input NAND implementation.