Embedded Systems

GPIO Devices

Lesson 06

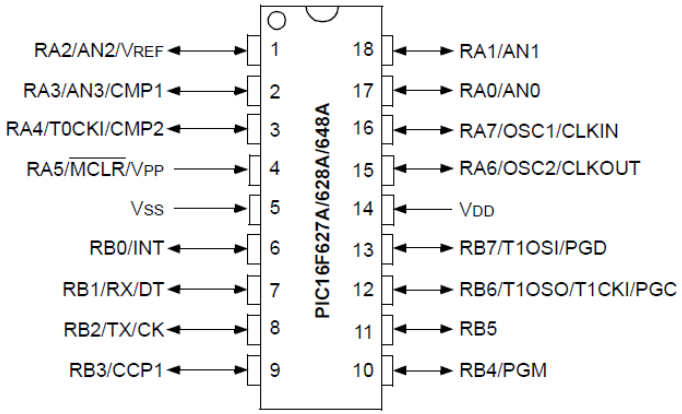
Francesco Menichelli

francesco.menichelli@uniroma1.it

GPIO basic

GPIO (General Purpose Input Output)

- Can drive to logical 0 or 1 a specific pin or group of pins
- Can be used for protocol emulation
  - Requires software emulation, i.e. significant CPU load
  - Examples: serial protocol, I2C, pulse generation, etc.
- What logical 0/1 means?
- How software can drive the pin?
  - We need the detailed peripheral description (reference manual datasheet)
- What kind of loads can be connected?
  - We need the electrical specifications (hardware datasheet)

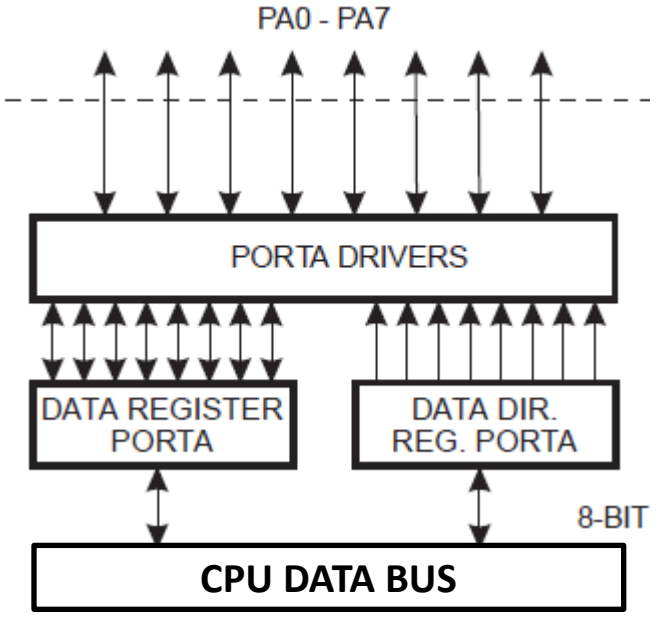


Example: GPIO on PIC16F1648

- RA0-RA7
- RB0-RB7

GPIO basic

- Bidirectional ports require at least two registers
  - Data direction register
    - Specify the direction of the port at bit level (e.g. 0=input ; 1=output
  - Data register
    - If configured as output - Write: output data to external pin ; Read: read data from register
    - If configured as input – Write: discarded ; Read: read data from external pin

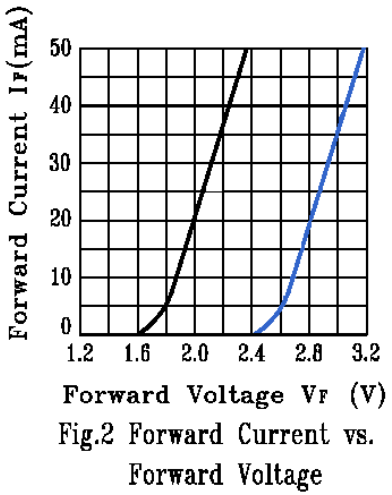


Example: Internal GPIO structure in Atmega family

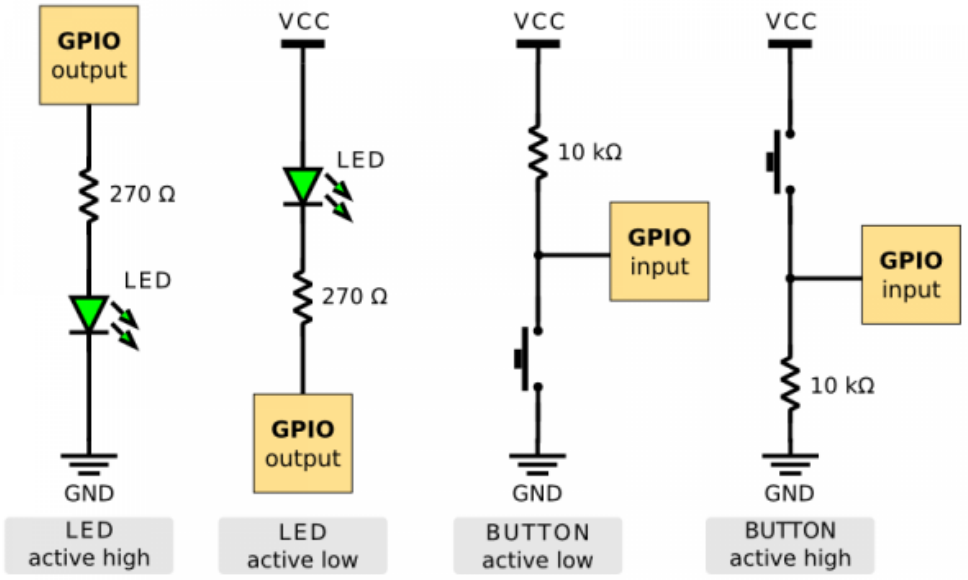
- PA0-PA7
- Drivers, data register, data direction register

GPIO basic

- GPIO example
  - Output: led drive
  - Input: button press
- How LED resistor is calculated?
- How BUTTON resistor is calculated?

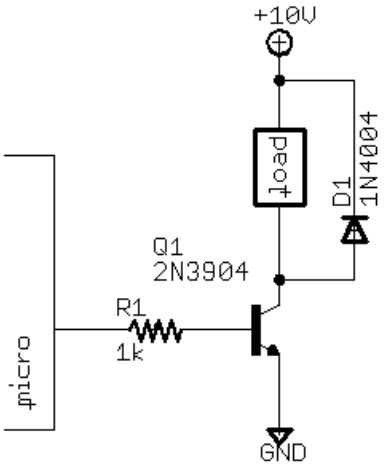


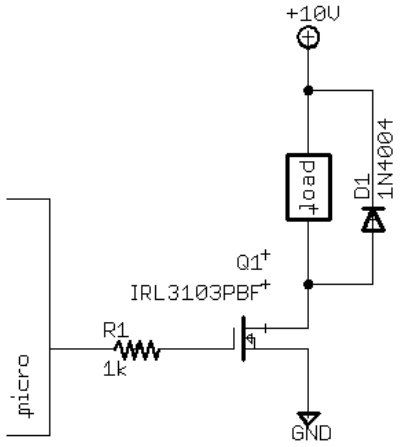
Typical LED forward Current vs. Voltage for two different LED colors



GPIO driving current

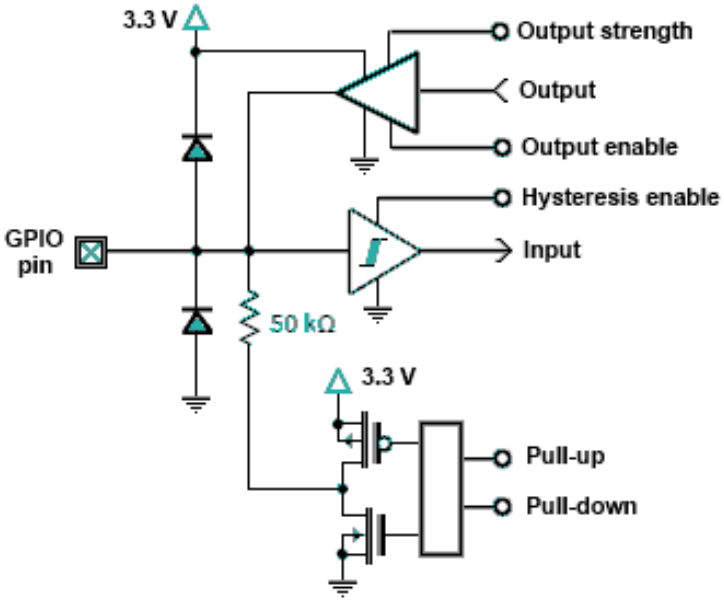
- Maximum direct drive current can be derived from hardware datasheet
  - Generally in the order of 10-20 mA
- If more current is needed, a transistor used as switch is a common solution
  - BJT switch
    - Rbase dimensioning (R1)
  - MOSFET switch
    - Rgate dimensioning (R1)





GPIO general circuit example

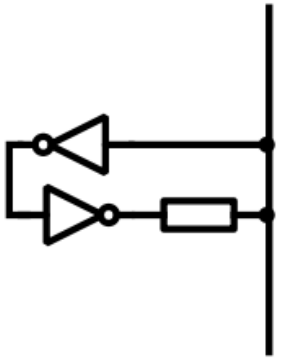
- The input gate detects whether the input voltage level is low or high by comparing it to a threshold voltage.
- To provide noise immunity and prevent chatter on transitions, the input gate can be configured to act as a Schmitt trigger, with input hysteresis. With hysteresis there are different threshold voltages for rising and falling transitions.
- The output drives to either 3.3V (high) or 0V (low). Drivers are buffering transistors with (relatively) high current driving capability.
- A pull-up/down resistor can be inserted via software configuration bits. The transistors that enable the pull-up/down resistor contribute their appreciable nonlinear resistance to it, so the effective resistance is not constant over the input pin voltage range



GPIO electrical characteristics

GPIO input/output pin electrical characteristics	
Output low voltage V_{OL}	< 0.40 V [1] < 0.66 V [2] < 0.40 V [3]
Output high voltage V_{OH}	> 2.40 V [4] > 2.64 V [5] > 2.90 V [6]
Input low voltage V_{IL}	< 0.80 V [7] < 0.54 V [8] < 1.15 V [9]
Input high voltage V_{IH}	> 2.00 V [10] > 2.31 V [11] > 2.15 V [12]
Hystereses	> 0.25 V [13] 0.66 – 2.08 V [14]
Schmitt trigger input low threshold V_{T-}	1.09 - 1.16 V [15] 0.9 [16]
Schmitt trigger input high threshold V_{T+}	2.24 - 2.74 V [17] 0.90 V [18]
Pull-up/down resistance	40 – 65 KΩ [19] 100 KΩ [20]
Pull-up/down current	< 50 uA [21] < 28 uA [22]
Pin capacitance	5 pF [23]
Bus hold resistance	5-11 KΩ [24]

- Bus-holders are used to prevent CMOS gate inputs from getting floating values when they are connected to tri-stated nets. Otherwise both transistors in the gate could get turned on, thus shorting the power supply and ground, which would destroy the CMOS gate.



GPIO example PIC16F628

FIGURE 5-1: BLOCK DIAGRAM OF RA0/AN0:RA1/AN1 PINS

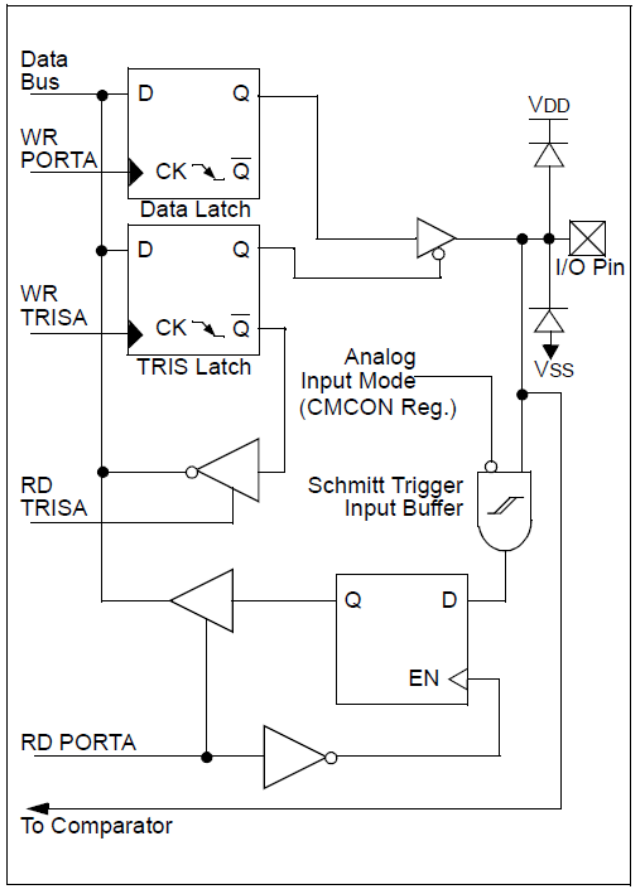
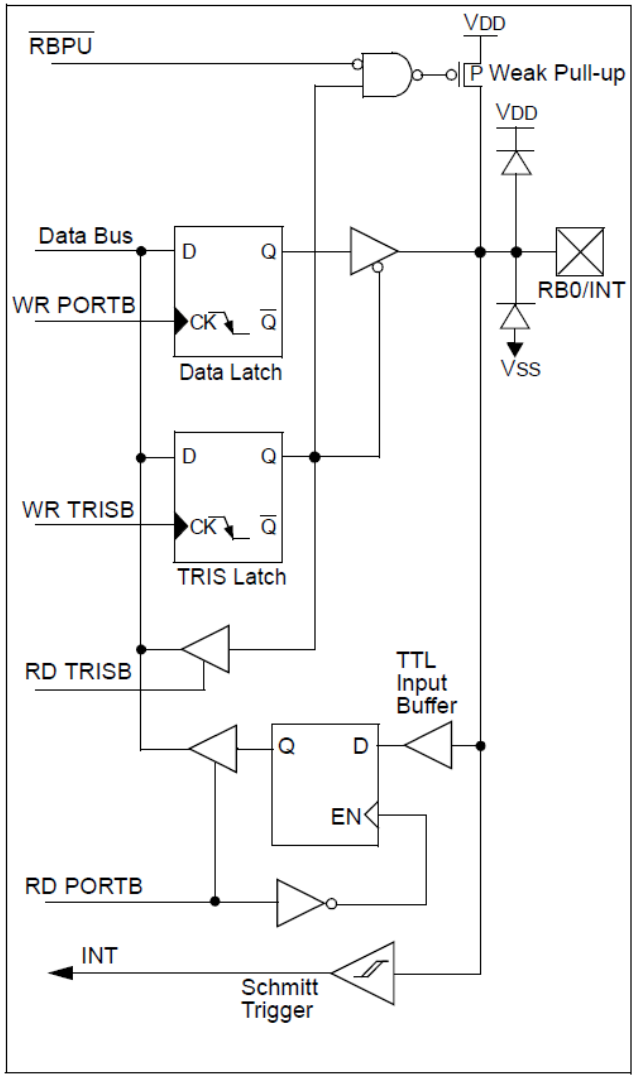


FIGURE 5-8: BLOCK DIAGRAM OF RB0/INT PIN



GPIO example PIC16F628

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial and -40°C ≤ TA ≤ +125°C for extended Operating voltage VDD range as described in DC specification Table 17-2 and Table 17-3				
Param. No.	**Sym**	**Characteristic/Device**	**Min**	**Typ†**	**Max**	**Unit**	**Conditions**
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	—	0.8	V	VDD = 4.5V to 5.5V
			VSS	—	0.15 VDD	V	otherwise
D031		with Schmitt Trigger input(4)	VSS	—	0.2 VDD	V	
D032		MCLR, RA4/T0CKI,OSC1 (in RC mode)	VSS	—	0.2 VDD	V	**(Note1)**
D033		OSC1 (in HS)	VSS	—	0.3 VDD	V	
		OSC1 (in LP and XT)	VSS	—	0.6	V	
	VIH	**Input High Voltage**					
		I/O ports					
D040		with TTL buffer	2.0V	—	VDD	V	VDD = 4.5V to 5.5V
			.25 VDD + 0.8V	—	VDD	V	otherwise
D041		with Schmitt Trigger input(4)	0.8 VDD	—	VDD	V	
D042		MCLR RA4/T0CKI	0.8 VDD	—	VDD	V	
D043		OSC1 (XT and LP)	1.3	—	VDD	V	
D043A		OSC1 (in RC mode)	0.9 VDD	—	VDD	V	**(Note1)**
D043B		OSC1 (in HS mode)	0.7 VDD		VDD	V	
D070	IPURB	**PORTB weak pull-up current**	50	200	400	µA	VDD = 5.0V, VPIN = VSS
	IIL	**Input Leakage Current(2), (3)**					
		I/O ports (Except PORTA)	—	—	±1.0	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
D060		PORTA(4)	—	—	±0.5	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
D061		RA4/T0CKI	—	—	±1.0	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1, MCLR	—	—	±5.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP oscillator configuration
	VOL	**Output Low Voltage**					
D080			—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5 V, -40° to +85°C
		I/O ports(4)	—	—	0.6	V	IOL = 7.0 mA, VDD = 4.5 V, +85° to +125°C
	VOH	**Output High Voltage(3)**					
D090		I/O ports (Except RA4(4))	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5 V, -40° to +85°C
			VDD – 0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5 V, +85° to +125°C
D150	VOD	**Open-Drain High Voltage**	—	—	8.5*	V	RA4 pin PIC16F627A/628A/648A, PIC16LF627A/628A/648A

GPIO example PIC registers

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
05h	PORTA	RA7	RA6	RA5(1)	RA4	RA3	RA2	RA1	RA0	xxxx 0000	qqqu 0000
85h	TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111
1Fh	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
9Fh	VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	000- 0000	000- 0000

Legend: - = Unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition. Shaded cells are not used for PORTA.

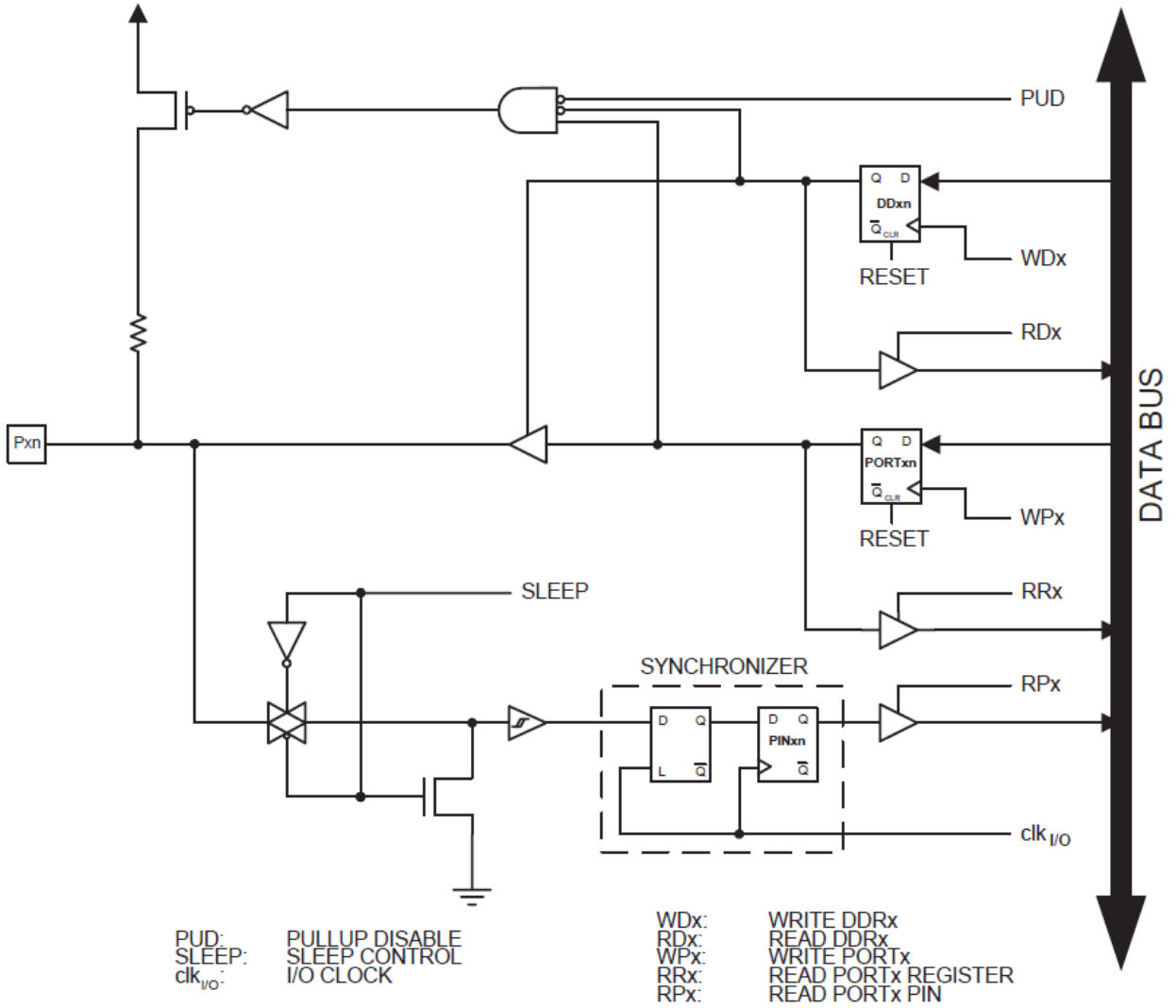
TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4(1)	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111
81h, 181h	OPTION	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: u = unchanged, x = unknown. Shaded cells are not used for PORTB.

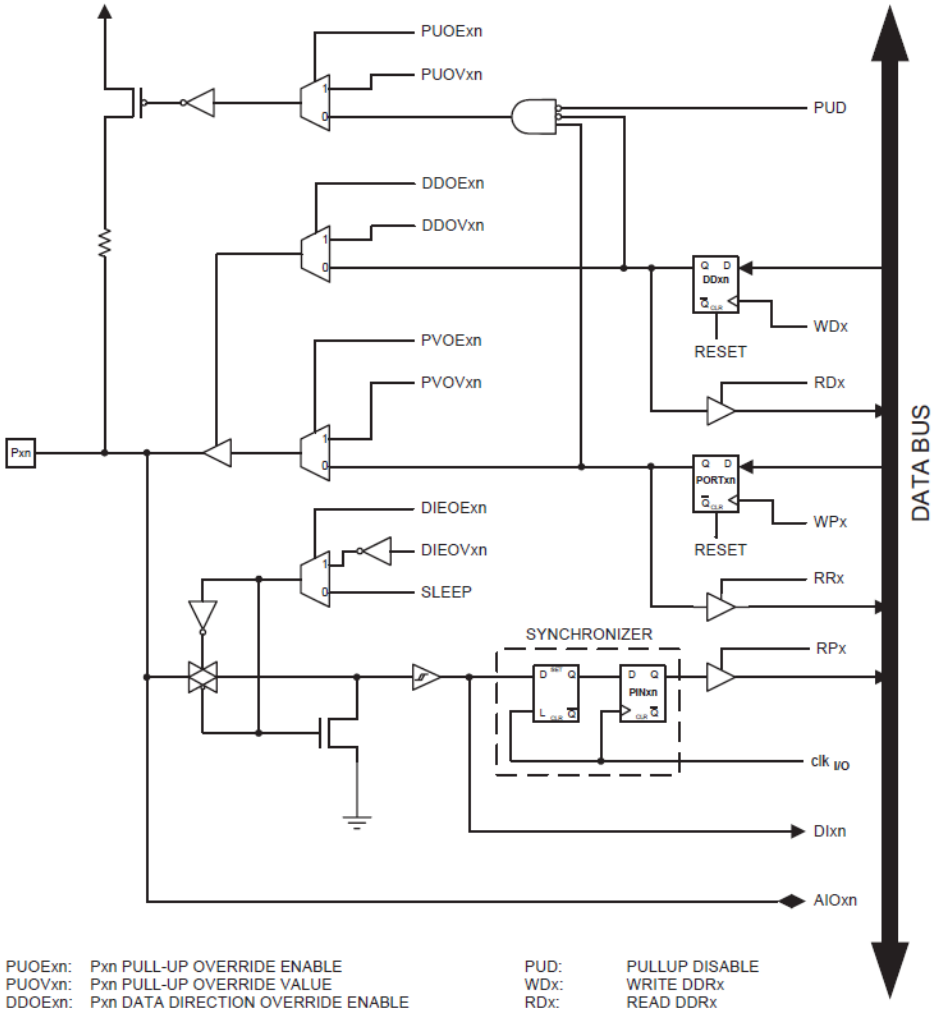
GPIO example ATmega

Figure 30. General Digital I/O(1)



GPIO example ATmega

Figure 33. Alternate Port Functions(1)



PUOExn:	Pxn PULL-UP OVERRIDE ENABLE	PUD:	PULLUP DISABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE	WDx:	WRITE DDRx
DDOExn:	Pxn DATA DIRECTION OVERRIDE ENABLE	RDx:	READ DDRx
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE	RRx:	READ PORTx REGISTER
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE	WPx:	WRITE PORTx
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE	RPx:	READ PORTx PIN
DIEOExn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE ENABLE	$clk_{I/O}$:	I/O CLOCK
DIEOVxn:	Pxn DIGITAL INPUT-ENABLE OVERRIDE VALUE	DIxn:	DIGITAL INPUT PIN n ON PORTx
SLEEP:	SLEEP CONTROL	AIOxn:	ANALOG INPUT/OUTPUT PIN n ON PORTx

GPIO example ATmega - registers

Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Port B Input Pins Address – PINB

Bit	7	6	5	4	3	2	1	0	
	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

GPIO example ATmega - registers

- Each port pin consists of three Register bits: DDxn, PORTxn, and PINxn.
- The DDxn bit in the DDRx Register selects the direction of this pin. If DDxn is written logic one, Pxn is configured as an output pin. If DDxn is written logic zero, Pxn is configured as an input pin.
- If PORTxn is written logic one when the pin is configured as an input pin, the pull-up resistor is activated. To switch the pull-up resistor off, PORTxn has to be written logic zero or the pin has to be configured as an output pin.
- If PORTxn is written logic one when the pin is configured as an output pin, the port pin is driven high (one). If PORTxn is written logic zero when the pin is configured as an output pin, the port pin is driven low (zero).
- Independent of the setting of Data Direction bit DDxn, the port pin can be read through the PINxn Register bit.
- PINxn Register bit and the preceding latch constitute a synchronizer. This is needed to avoid metastability if the physical pinchanges value near the edge of the internal clock.

GPIO example ATmega - code

- Set PORT B pins 0 and 1 high, 2 and 3 low, and define the port pins from 4 to 7 as input with pull-ups assigned to port pins 6 and 7.
- Set PORT B pins 0 to 3 as outputs and pins from 4 to 7 as inputs
- The resulting pin values are read back again
- A *nop* instruction is included to be able to read back the value recently assigned to some of the pins

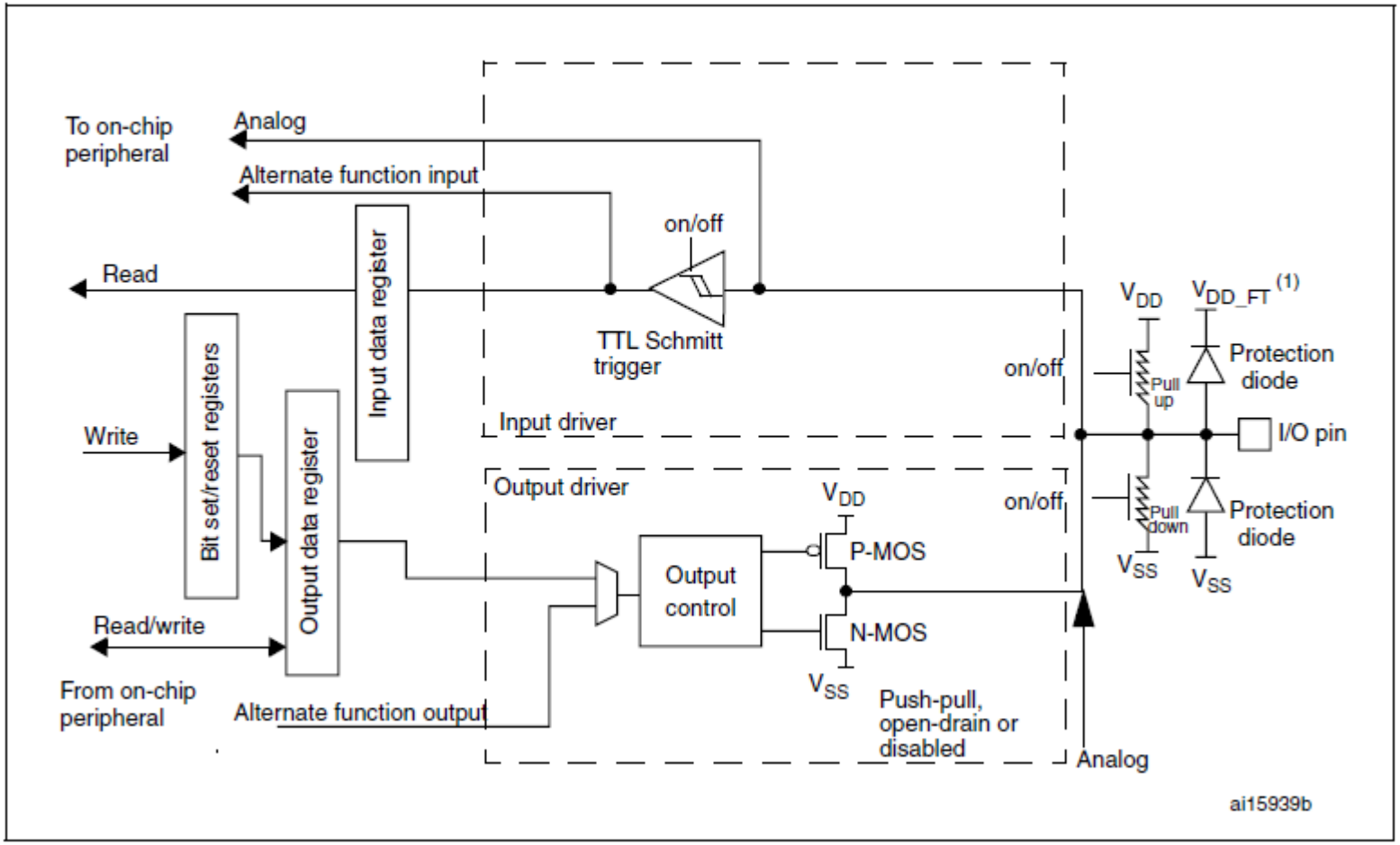
```
unsigned char i;
...
/* Define pull-ups and set outputs high */
/* Define directions for port pins */
PORTB = 0xC3;
DDRB = 0x0F;
/* Insert nop for synchronization*/
_NOP();
/* Read port pins */
i = PINB;
...
```

GPIO example ST32F

- **GPIO main features**
  - Up to 16 I/Os under control
  - Output states: push-pull or open drain + pull-up/down
  - Output data from output data register (GPIOx_ODR) or peripheral (alternate function output)
  - Input states: floating, pull-up/down, analog
  - Input data to input data register (GPIOx_IDR) or peripheral (alternate function input)
  - Bit set and reset register (GPIOx_BSRR) for bitwise write access to GPIOx_ODR
  - Locking mechanism (GPIOx_LCKR) provided to freeze the I/O configuration
  - Analog function

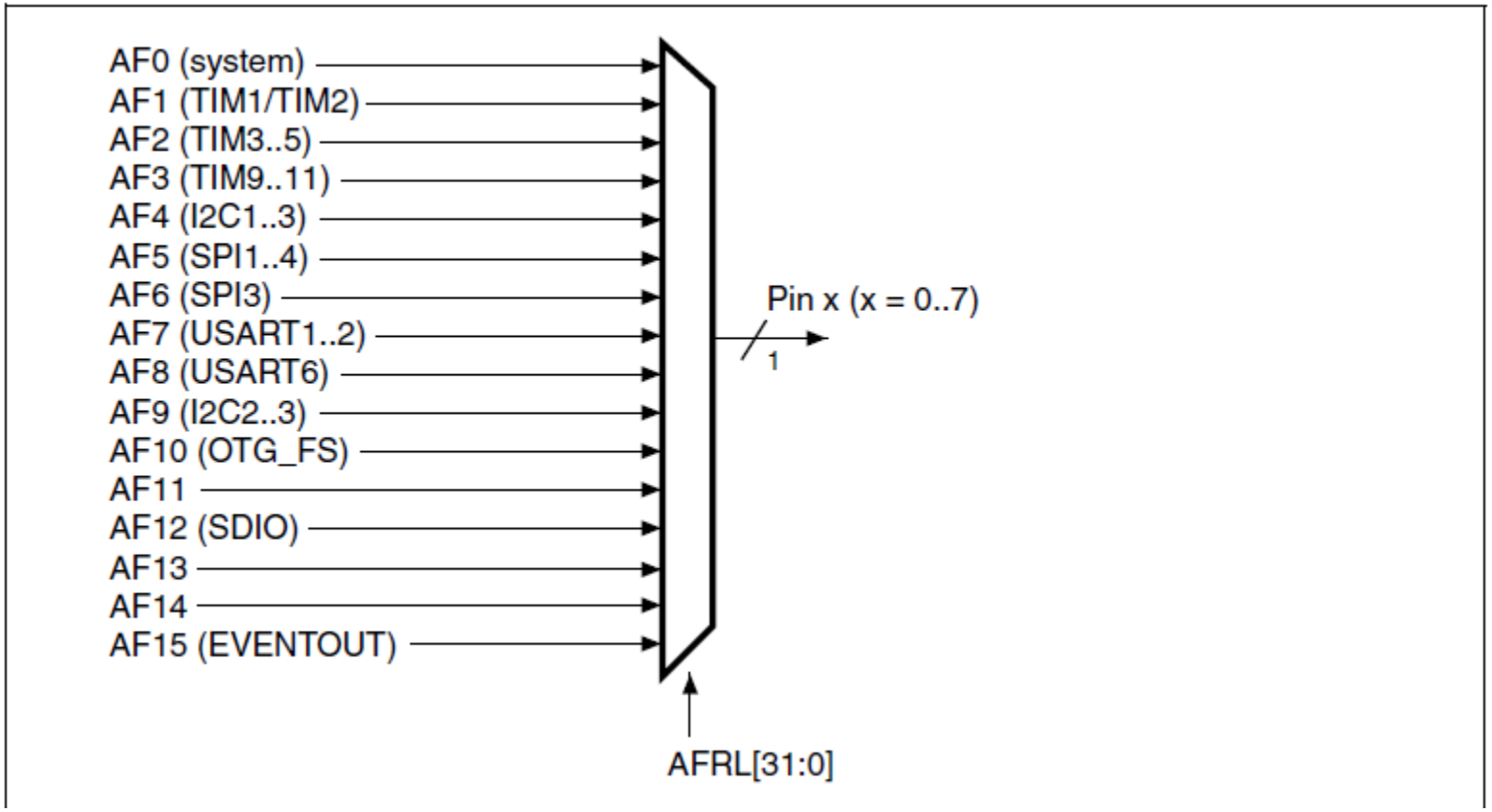
GPIO example ST32F

Figure 16. Basic structure of a five-volt tolerant I/O port bit



GPIO example ST32F

Figure 17. Selecting an alternate function on STM32F401xB/C and STM32F401xD/E



GPIO example ST32F - Registers

I/O port control registers

- Each of the GPIOs has four 32-bit memory-mapped control registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR) to configure up to 16 I/Os.
  - GPIOx_MODER register is used to select the I/O direction (input, output, AF, analog).
  - GPIOx_OTYPER and GPIOx_OSPEEDR registers are used to select the output type (pushpull or open-drain) and speed
  - GPIOx_PUPDR register is used to select the pull-up/pull-down whatever the I/O direction.

GPIO example ST32F - Registers

- **GPIO port mode register (GPIOx_MODER)**

Address offset: 0x00

Reset values:

- 0x0C00 0000 for port A
- 0x0000 0280 for port B
- 0x0000 0000 for other ports

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 2y:2y+1 **MODERy[1:0]:** Port x configuration bits (y = 0..15)

These bits are written by software to configure the I/O direction mode.

00: Input (reset state)

01: General purpose output mode

10: Alternate function mode

11: Analog mode

GPIO example ST32F - Registers

I/O port data registers

- Each GPIO has two 16-bit memory-mapped data registers: input and output data registers (GPIOx_IDR and GPIOx_ODR).
- GPIOx_ODR stores the data to be output, it is read/write accessible.
- The data input through the I/O are stored into the input data register (GPIOx_IDR), a read-only register.

8.4.6 GPIO port output data register (GPIOx_ODR) (x = A..E and H)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **ODRy**: Port output data (y = 0..15)

These bits can be read and written by software.

Note: For atomic bit set/reset, the ODR bits can be individually set and reset by writing to the GPIOx_BSRR register (x = A..E and H).

GPIO example ST32F - Registers

I/O data bitwise handling

- The bit set reset register (GPIOx_BSRR) is a 32-bit register which allows the application to set and reset each individual bit in the output data register (GPIOx_ODR). The bit set reset register has twice the size of GPIOx_ODR.
- To each bit in GPIOx_ODR, correspond two control bits in GPIOx_BSRR: BSRR(i) and BSRR(i+SIZE).
- When written to 1, bit BSRR(i) sets the corresponding ODR(i) bit. When written to 1, bit BSRR(i+SIZE) resets the ODR(i) corresponding bit.
- Writing any bit to 0 in GPIOx_BSRR does not have any effect on the corresponding bit in GPIOx_ODR. If there is an attempt to both set and reset a bit in GPIOx_BSRR, the set action takes priority.
- The GPIOx_BSRR register provides a way of performing atomic bitwise handling.

GPIO example ST32F - Registers

8.4.7 GPIO port bit set/reset register (GPIOx_BSRR) (x = A..E and H)

Address offset: 0x18

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BS15	BS14	BS13	BS12	BS11	BS10	BS9	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bits 31:16 **BRy:** Port x reset bit y (y = 0..15)

These bits are write-only and can be accessed in word, half-word or byte mode. A read to these bits returns the value 0x0000.

0: No action on the corresponding ODRx bit

1: Resets the corresponding ODRx bit

Note: If both BSx and BRx are set, BSx has priority.

Bits 15:0 **BSy:** Port x set bit y (y= 0..15)

These bits are write-only and can be accessed in word, half-word or byte mode. A read to these bits returns the value 0x0000.

0: No action on the corresponding ODRx bit

1: Sets the corresponding ODRx bit

GPIO example ST32F - Registers

GPIO locking mechanism

- It is possible to freeze the GPIO control registers by applying a specific write sequence to the GPIOx_LCKR register.
- The frozen registers are GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR, GPIOx_AFRL and GPIOx_AFRH.
- When the LOCK sequence has been applied to a port bit, the value of the port bit can no longer be modified until the next reset.
- Each GPIOx_LCKR bit freezes the corresponding bit in the control registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, GPIOx_PUPDR, GPIOx_AFRL and GPIOx_AFRH).

GPIO example ST32F - Registers

I/O alternate function input/output

- Two registers are provided to select one out of the sixteen alternate function inputs/outputs available for each I/O.
- With these registers, it is possible to connect an alternate function to some other pin as required by the application.
- This means that a number of possible peripheral functions are multiplexed on each GPIO using the GPIOx_AFRL and GPIOx_AFRH alternate function registers.

External interrupt/wakeup lines

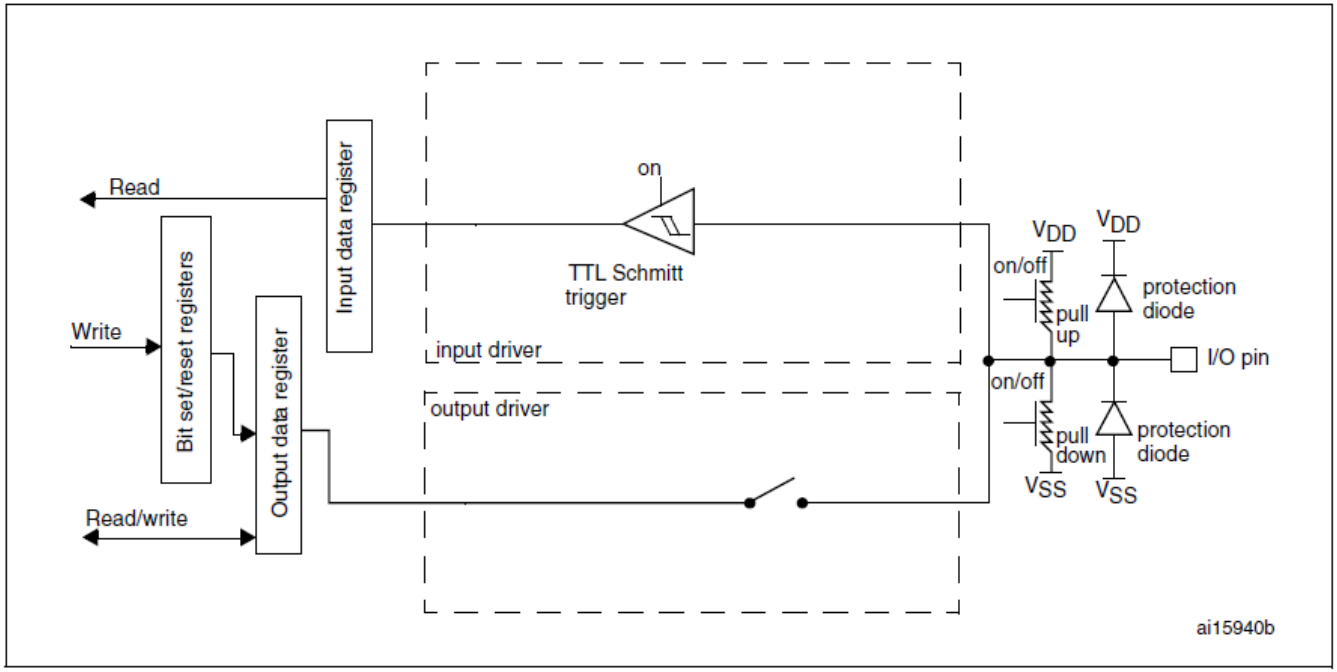
- All ports have external interrupt capability. To use external interrupt lines, the port must be configured in input mode.

GPIO example ST32F - Circuit

Input configuration

- The output buffer is disabled
- The Schmitt trigger input is activated
- The pull-up and pull-down resistors are activated depending on the value in the GPIOx_PUPDR register
- The data present on the I/O pin are sampled into the input data register every AHB clock cycle
- A read access to the input data register provides the I/O State

Figure 18. Input floating/pull up/pull down configurations

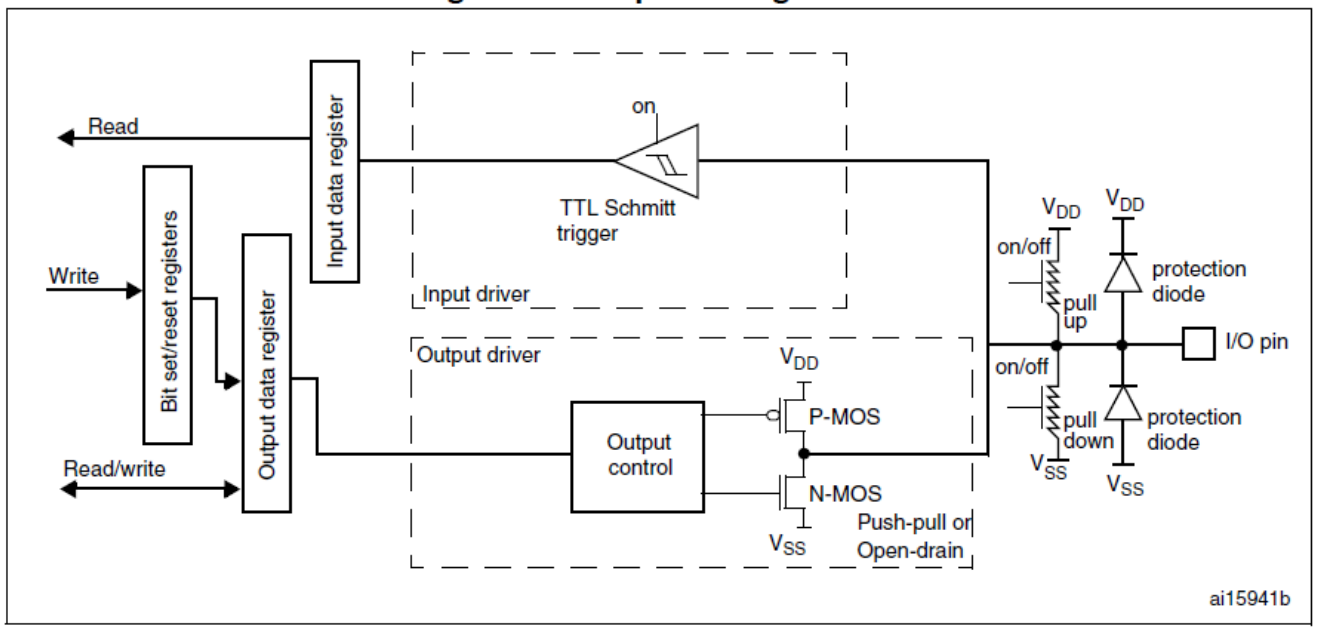


GPIO example ST32F - Circuit

Output configuration

- The output buffer is enabled:
  - Open drain mode: A “0” in the Output register activates the N-MOS whereas a “1” in the Output register leaves the port in Hi-Z (the P-MOS is never activated).
  - Push-pull mode: A “0” in the Output register activates the N-MOS whereas a “1” in the Output register activates the P-MOS
- The Schmitt trigger input is activated
- The weak pull-up and pull-down resistors are activated or not depending on the value in the GPIOx_PUPDR register
- The data present on the I/O pin are sampled into the input data register every AHB clock cycle
- A read access to the input data register gets the I/O state
- A read access to the output data register gets the last written value

Figure 19. Output configuration



GPIO example ST32F - Circuit

Analog configuration

- The output buffer is disabled
- The Schmitt trigger input is deactivated, providing zero consumption for every analog value of the I/O pin. The output of the Schmitt trigger is forced to a constant value (0).
- The weak pull-up and pull-down resistors are disabled
- Read access to the input data register gets the value “0”

Figure 21. High impedance-analog configuration