Embedded Systems

Acquisition devices, ADC, DAC

Lesson 10

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Digital signals

- Discretization of time
  - Nyquist theorem
  - Non ideal low pass filters
- Quantization of input
  - Introduce error
  - Depend on the number of bits used for representation

Analog to Digital Converters

- Defined by
  - bandwidth (the range of frequencies it can measure)
  - signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces).
- Bandwidth depends
  - sampling rate
  - how it handles aliasing errors
- Dynamic range is influenced by
  - resolution (the number of quantization levels)
  - linearity and accuracy (how well the quantization levels match the true analog signal)
  - jitter (timing errors).
- The dynamic range can be summarized in terms of effective number of bits (ENOB)
  - the number of bits of each measure that are on average not noise.
  - An ideal ADC has an ENOB equal to its resolution.

ADC Charaterization

- Resolution
  - the number of discrete values it can produce
  - It is usually expressed in bits
    - One effective bit of resolution changes the signal-to-noise ratio of the digitized signal by 6 dB ($\log_{10} 2 \approx 0.301$)
  - can be defined electrically, and expressed in volts
    - LSB voltage: the minimum change in voltage required to guarantee a change in the output code level

$$Q = \frac{E_{full\ scale\ range}}{2^M}$$

Where M is the resolution in bits and

$$E_{full\ scale\ range} = V_{RefHi} - V_{RefLow}$$

Example:

- Full scale measurement range: -5 to 5 volts
- ADC resolution is 8 bits: 256 quantization levels
- ADC voltage resolution: Q = (10 V − 0 V) / 256 = 10 V / 256 ≈ 0.039 V ≈ 39 mV.

ADC Charaterization

- Quantization error
  - Noise introduced by quantization in an ideal ADC.
  - It is a rounding error between the analog input voltage and the digitized value.
  - In an ideal analog-to-digital converter, the quantization error is uniformly distributed between −1/2 LSB and +1/2 LSB, the Signal-to-quantization-noise ratio (SQNR) can be calculated as

$$SNQR = 20\log_{10}(2^Q) \approx 6.02 \cdot Q \text{ dB}$$

Where Q is the number of quantization bits.

Example: 16-bit ADC has a maximum signal-to-noise ratio of 6.02 × 16 = 96.3 dB

- Quantization error is distributed from DC to the Nyquist frequency
  - Oversampling and digital filtering can effectively improve the SQNR.

ADC Charaterization

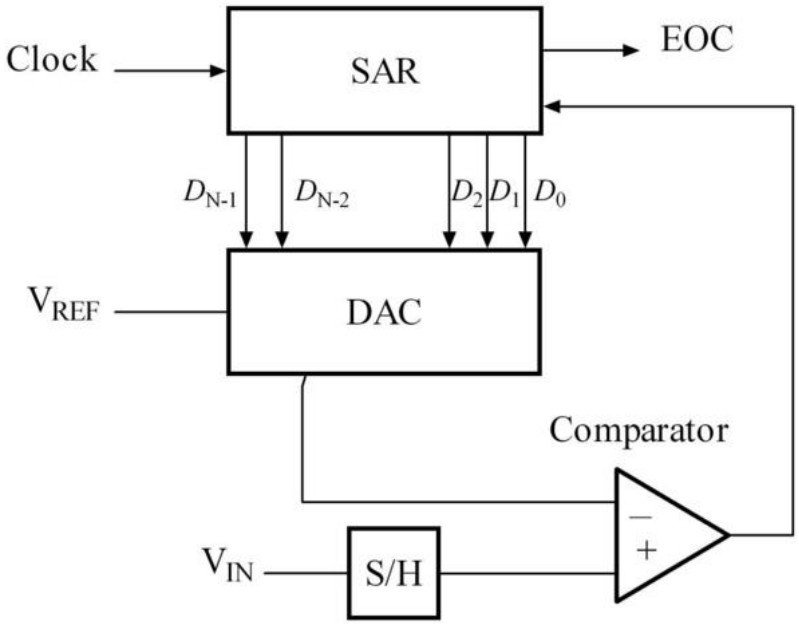
- Non-linearity
  - Integral non-linearity (INL) and differential non-linearity (DNL)
- Jitter
  - non-ideal sampling clock (phase noise) results in some uncertainty when samples are recorded
  - additional noise that reduces the effective number of bits (ENOB) below that predicted by quantization error
  - The error is zero for DC, small at low frequencies, but significant when high frequencies have high amplitudes

ADC architectures

- Direct-conversion ADC or flash ADC
- Successive-approximation ADC
- Integrating ADC or dual-slope ADC
- Pipeline ADC (or also called subranging quantizer)
- Sigma-delta ADC or delta-sigma ADC

Successive-approximation ADC

- Uses a comparator to successively narrow a range that contains the input voltage.
- At each step, the converter compares the input voltage to the output of an internal DAC and the approximation is stored in a successive approximation register (SAR).
- The conversion takes at least N cycles, where N is the number of bits of the ADC



S/H: Sample and hold circuit to acquire the input voltage (Vin).
Comparator: Analog voltage comparator, compares Vin to the output of the internal DAC and outputs the result SAR.
SAR: A successive approximation register, supply an approximate digital code of Vin to the internal DAC.
DAC: Supplies the comparator with an analog voltage equal to the digital code output of the SARin

Successive-approximation ADC

- Conversion sequence
  - The SAR is initialized with the most significant bit (MSB) set to 1.
  - The SAR value is fed into the DAC, which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage.
  - If this analog voltage exceeds Vin the comparator causes the SAR to reset this bit, otherwise the bit is left to 1.
  - Then the next bit is set to 1 and the same test is done, continuing this binary search until every bit in the SAR has been tested.
  - The resulting code is the digital approximation of the sampled input voltage and is finally output by the SAR at the end of the conversion (EOC).

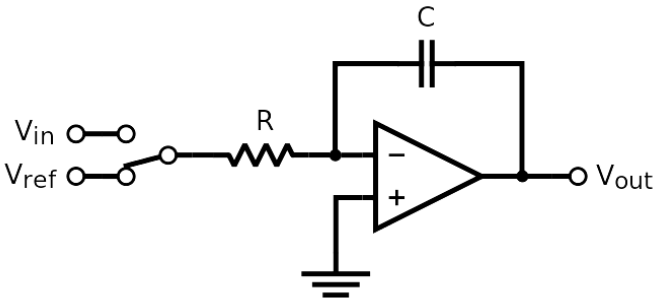
Example:

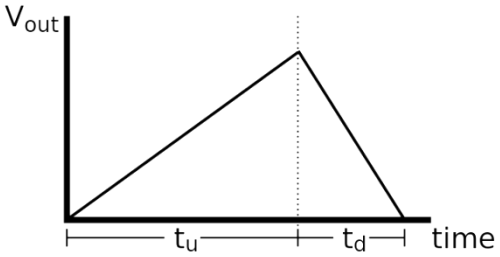
Consider an input voltage of 6.3 V and the initial range is 0 to 16 V.

- The input 6.3 V is compared to 8 V (midpoint of the 0–16 V range)
- The comparator reports that the input voltage is less than 8 V, so the SAR is updated resetting the MSB.
- For the second step, the input voltage is compared to 4 V (midpoint of 0–8V).
- The comparator reports the input voltage is above 4 V, so the SAR the present bit is left to 1
- For the third step, the input voltage is compared with 6 V (halfway between 4 V and 8 V)
- The comparator reports the input voltage is greater than 6 volts, and search range becomes 6–8 V.
- The steps are continued until the desired resolution is reached.

Integrating ADC or dual-slope ADC

- Applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (run-up period).
- A known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (run-down period).
- The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period.
- The run-down time measurement is made in units of the converter's clock (longer integration times allow for higher resolutions).





$$V_{out-rise} = -\frac{V_{in}}{RC} t_u$$

$$V_{out-fall} = -\frac{V_{ref}}{RC} t_d + V_{out-rise} = 0$$

$$V_{in} = -V_{ref} \frac{t_d}{t_u}$$

The value is independent from RC constant

Integrating ADC or dual-slope ADC

- The resolution of the ADC is determined primarily by the length of the run-down period and by the time measurement resolution
- The required resolution (in number of bits) dictates the minimum length of the run-down period for a full-scale input ($V_{in} = -V_{ref}$, $t_u = t_d$):

$$t_d = \frac{2^n}{f_{clk}}$$

$$t_{conversion} = t_u + t_d = 2\frac{2^n}{f_{clk}}$$

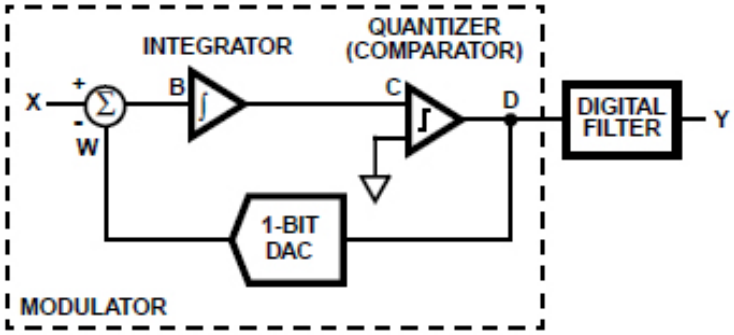
Example:

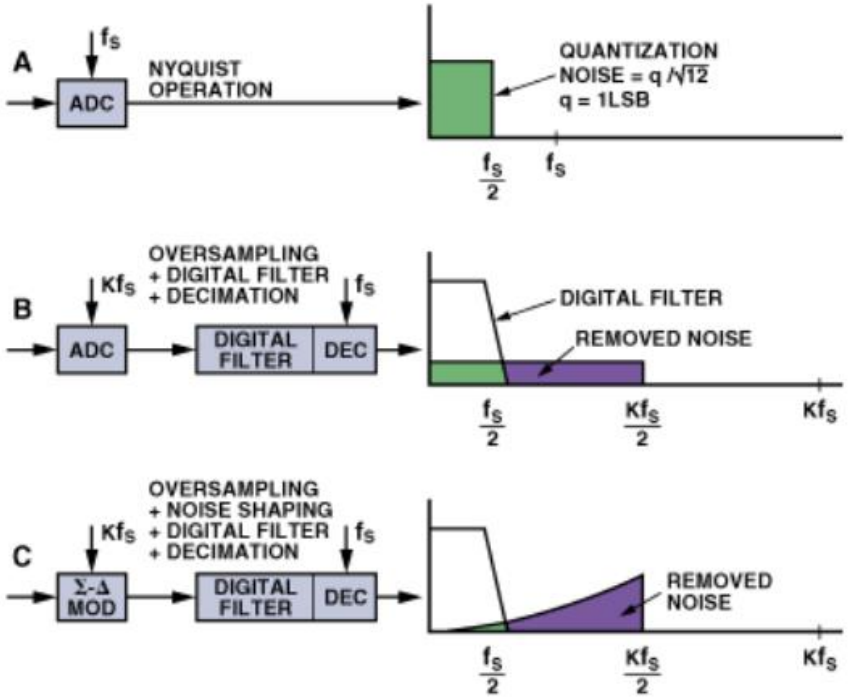
- 16 bit resolution, fclock 8 MHz
- tconversion = 16.4ms (61 samples per second).

- Converters of this type are used in most digital voltmeters for their linearity and flexibility.

Sigma-delta ADC

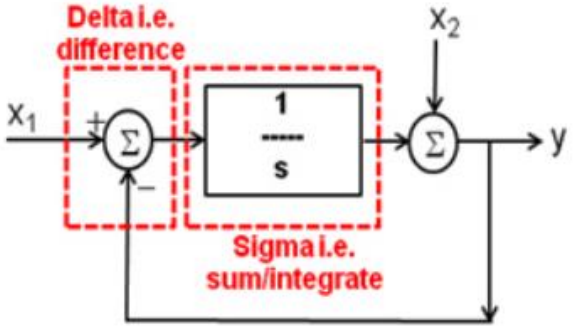
- A ΣΔ-ADC has a modulator and a digital filter (also known as decimation filter)
- The modulator converts the input analog signal into 1-bit digital signal at frequency $f_{oversample}$
- The low pass digital filter average the samples and provide an n-bit digital signal

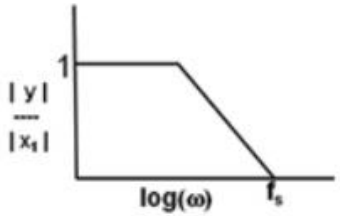




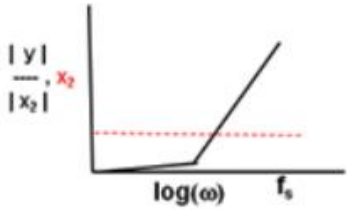
Sigma-delta ADC

- Noise shaping
  - ΣΔ is a low pass filter for input signal
  - ΣΔ is a high pass filter for quantization noise





STF = (Signal transfer function) $\frac{y}{x_1} = \frac{1/s}{(1+1/s)} = \frac{1}{1+s} \sim 1$ @DC



NTF = (Noise transfer function) $\frac{y}{x_2} = \frac{1}{(1+1/s)} = \frac{s}{1+s} \sim 0$ @DC

Sigma-delta ADC

Conversion example

- The input X is a DC input of 3/8. The resultant signal at each point in the signal path for each signal sample is shown in Table 1.
- A repetitive pattern develops every sixteen samples, and the average of the signal W over samples 1 to 16 is 3/8, thus showing that the feedback loop forces the average of the feedback signal W to be equals to the input X.

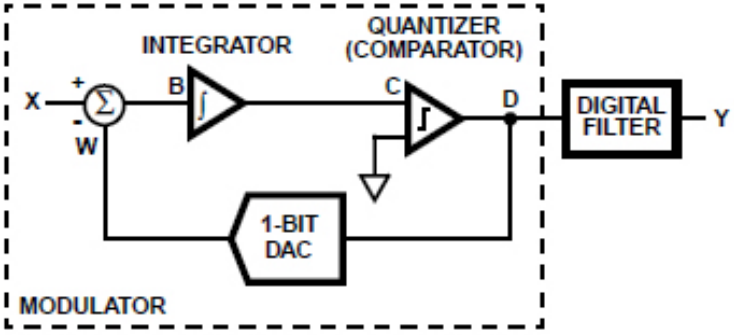


TABLE 1. CONVERSION EXAMPLE

SAMPLE (n)	X (INPUT)	B ($A-W_{n-1}$)	C ($B+C_{n-1}$)	D (0 or 1)	W (-1 or +1)
0	3/8	0	0	0	0
1	3/8	3/8	3/8	1	+1
2	3/8	-5/8	-2/8	0	-1
3	3/8	11/8	9/8	1	+1
4	3/8	-5/8	4/8	1	+1
5	3/8	-5/8	-1/8	0	-1
6	3/8	11/8	10/8	1	+1
7	3/8	-5/8	5/8	1	+1
8	3/8	-5/8	0/8	0	-1
9	3/8	11/8	11/8	1	+1
10	3/8	-5/8	6/8	1	+1
11	3/8	-5/8	1/8	1	+1
12	3/8	-5/8	-4/8	0	-1
13	3/8	11/8	7/8	1	+1
14	3/8	-5/8	2/8	1	+1
15	3/8	-5/8	-3/8	0	-1
16	3/8	11/8	8/8	1	+1
17	3/8	-5/8	3/8	1	+1
18	3/8	-5/8	-2/8	0	-1

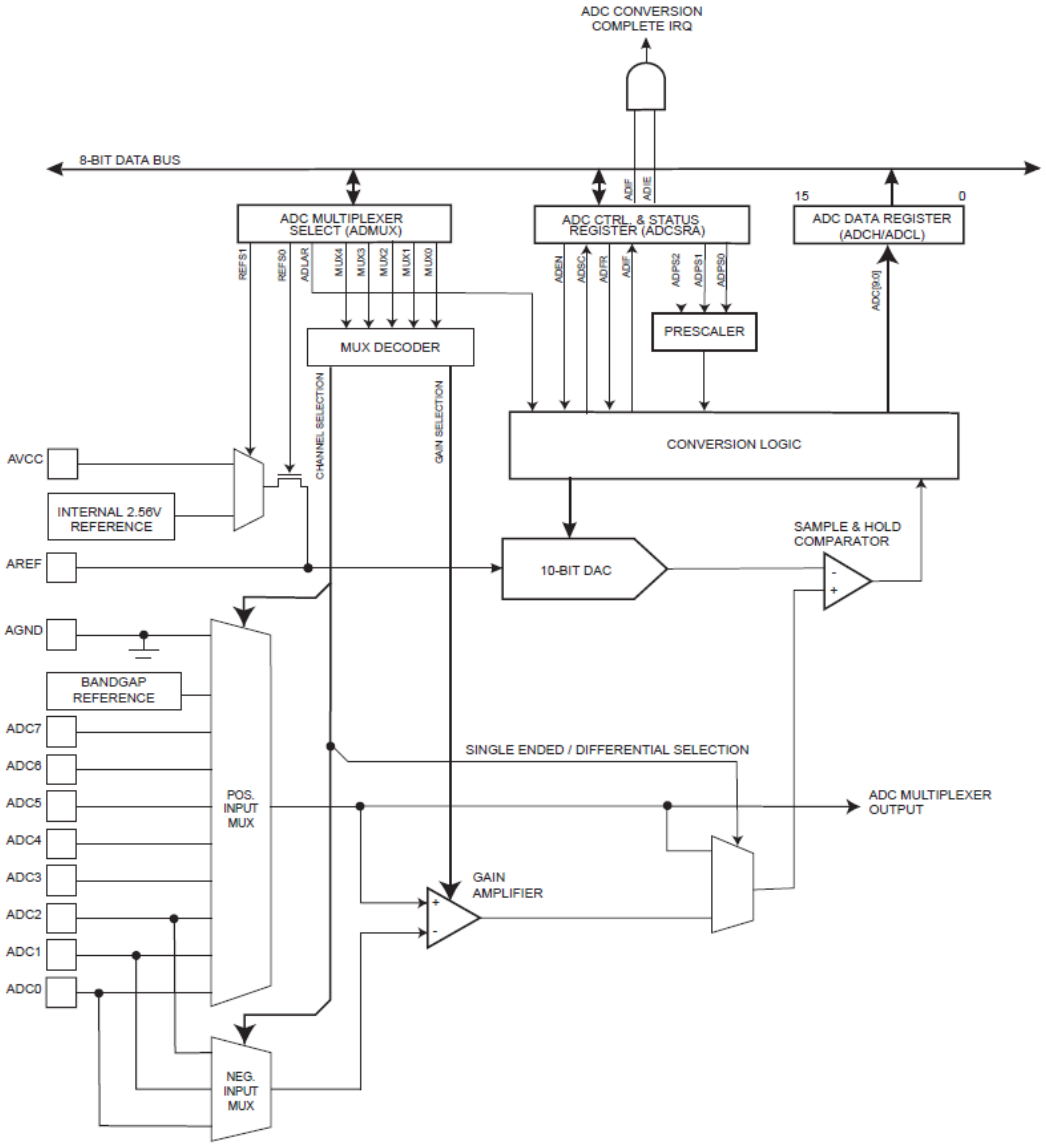
Atmega ADC

- 10-bit Resolution (SAR)
- 8-channel Analog Multiplexer which allows 8 single-ended voltage inputs
- constructed from the pins of Port F. The single-ended voltage inputs refer to 0V (GND).
- 65 - 260 µs Conversion Time (15 kSPS at Maximum Resolution)
- 0 - VCC ADC Input Voltage Range
- Free Running or Single Conversion Mode
- Interrupt on ADC Conversion Complete
- Sleep Mode Noise Canceler
- 0.5 LSB Integral Non-linearity
- ±2 LSB Absolute Accuracy

Atmega ADC

- Programmable gain stage, providing amplification steps of 0 dB (1x), 20 dB (10x), or 46 dB (200x) on the differential input voltage before the A/D conversion.
- If 1x or 10x gain is used, 8-bit resolution can be expected. If 200x gain is used, 7-bit resolution can be expected.
- The ADC has a separate analog supply voltage pin, AVCC. AVCC must not differ more than ± 0.3V from VCC.
- Internal reference voltages of nominally 2.56V or AVCC are provided On-chip.

Atmega ADC block diagram



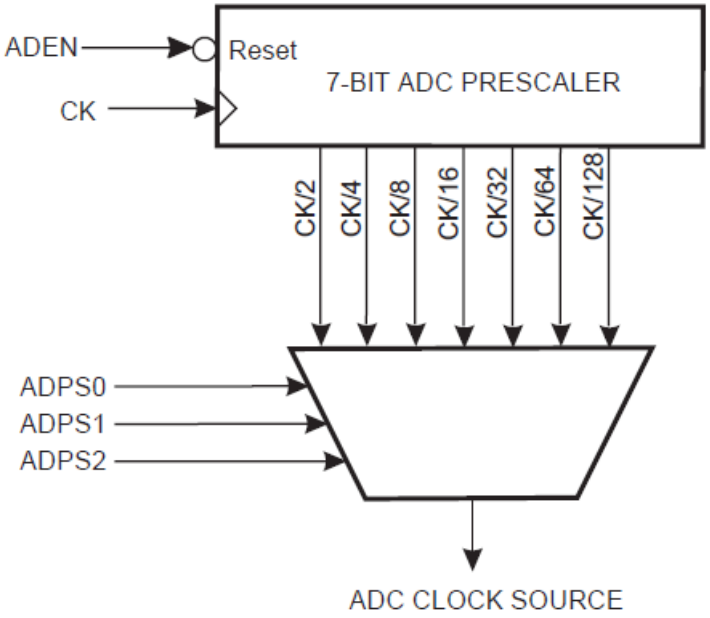
Atmega ADC

- The ADC converts an analog input voltage to a 10-bit digital value through successive approximation.
- The minimum value represents GND and the maximum value represents the voltage on the AREF pin minus 1 LSB.
- Optionally, AVCC or an internal 2.56V reference voltage may be connected to the AREF pin.
- Any of the ADC input pins, as well as GND and a fixed bandgap voltage reference, can be selected as single ended inputs to the ADC.
- If differential channels are selected, the differential gain stage amplifies the voltage difference between the selected input channel pair by the selected gain factor.
- If single ended channels are used, the gain amplifier is bypassed altogether.

Atmega ADC clock generator

- By default, the successive approximation circuitry requires an input clock frequency between 50 kHz and 200 kHz to get maximum resolution.
- If a lower resolution than 10 bits is needed, the input clock frequency to the ADC can be higher than 200 kHz to get a higher sample rate.

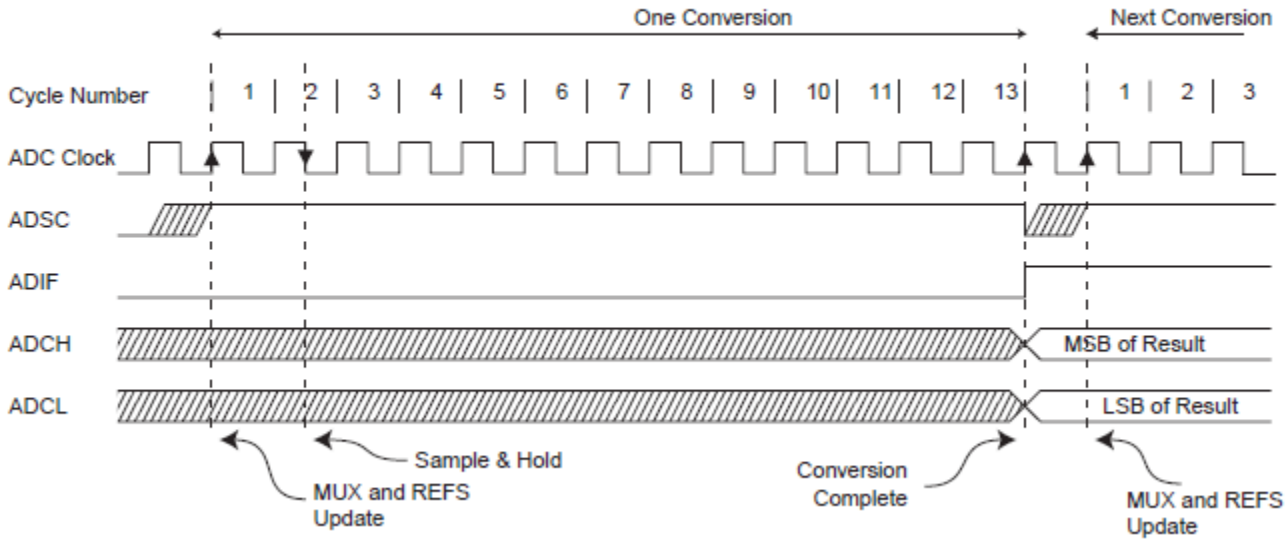
Figure 109. ADC Prescaler



Atmega ADC timing

- A normal conversion takes 13 ADC clock cycles. The first conversion after the ADC is switched on (ADEN in ADCSRA is set) takes 25 ADC clock cycles in order to initialize the analog circuitry.
- The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an first conversion.

Figure 111. ADC Timing Diagram, Single Conversion



Atmega ADC reference voltage

- The reference voltage for the ADC (VREF) indicates the conversion range for the ADC.
- Single ended channels that exceed VREF will result in codes close to 0x3FF.
- VREF can be selected as
  - AVCC (voltage coming from power supply regulator, low accuracy, low temperature stability)
  - internal 2.56V reference (generated from the internal bandgap reference , high accuracy, high temperature stability)
  - external AREF pin.
- If the user has a fixed voltage source connected to the AREF pin, the user may not use the other reference voltage options in the application, as they will be shorted to the external voltage.

$$ADC = \frac{V_{IN} \cdot 1024}{V_{REF}}$$

Single-ended channel

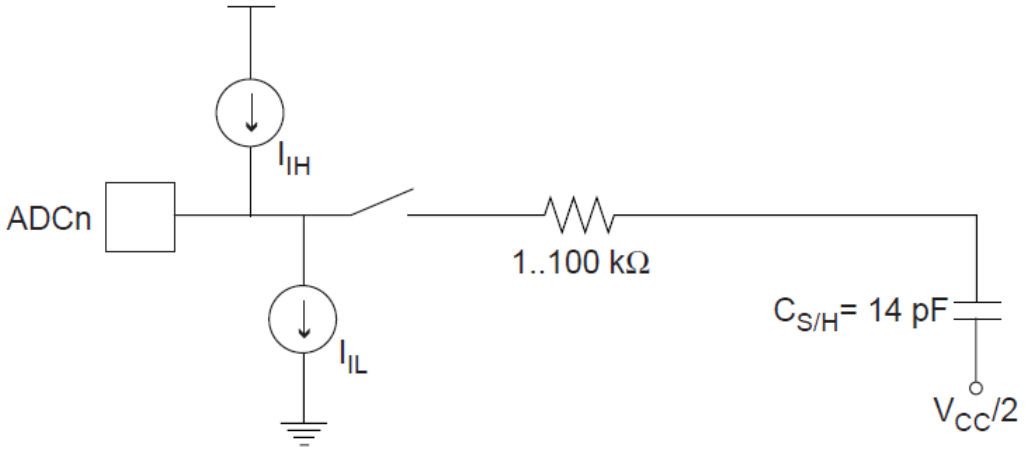
$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot GAIN \cdot 512}{V_{REF}}$$

Differential channel

Atmega ADC Analog Input Circuitry

- An analog source applied to ADCn is subjected to the pin capacitance and input leakage of that pin
- When the channel is selected, the source must drive the S/H capacitor through the series resistance (combined resistance in the input path).
- The ADC is optimized for analog signals with an output impedance of approximately 10 kΩ or less.
- If a source with higher impedance is used, the sampling time will depend on how long time the source needs to charge the S/H capacitor.

Figure 113. Analog Input Circuitry

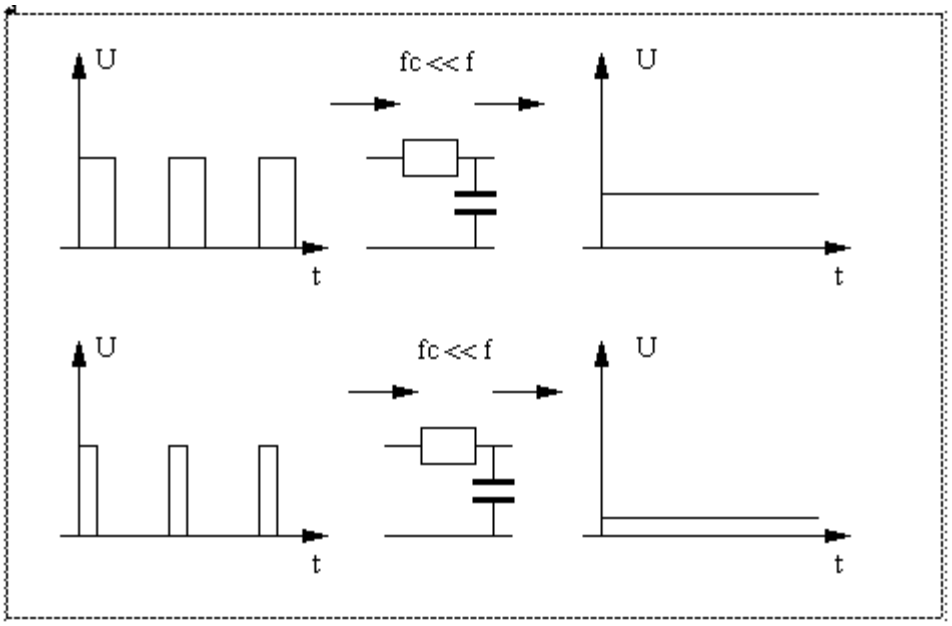


Digital to Analog converters

- Less crytical than ADC
- Architectures
  - PWM DAC
  - Binary-weighted DAC
  - Delta-sigma DAC

PWM DAC

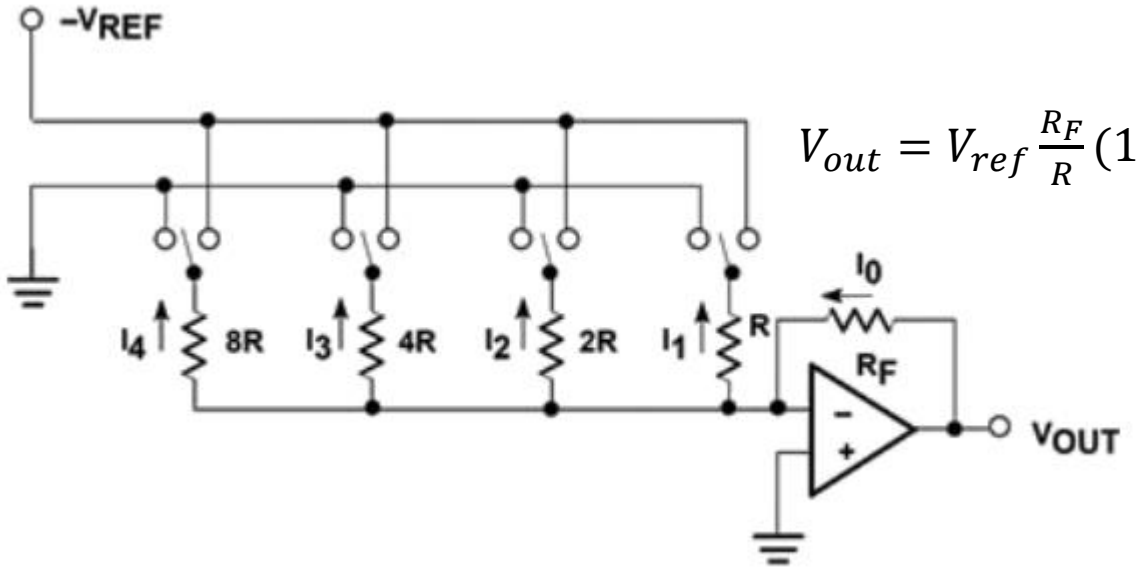
- A stable current or voltage is switched into a low-pass analog filter with a duration determined by the digital input code.



$$V_{out} = V_{ref} \cdot duty\_cycle$$

Binary-weighted DAC

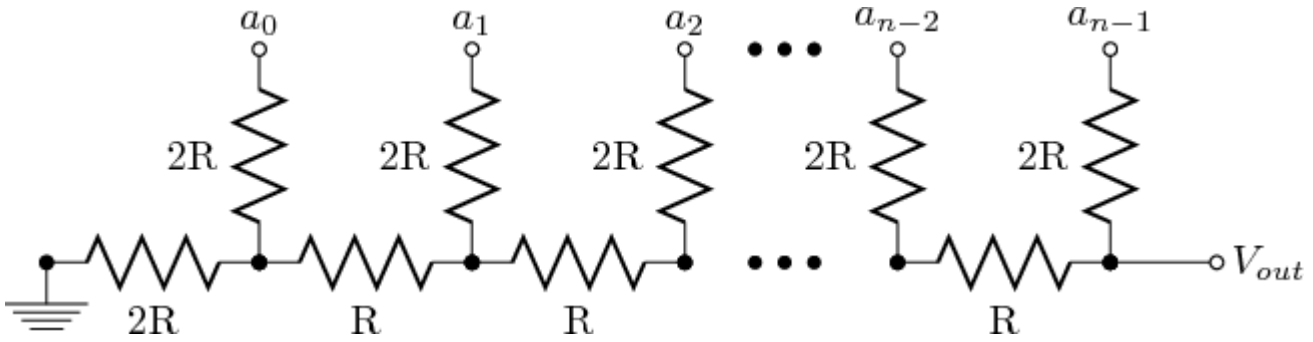
- Individual electrical components for each bit of the DAC connected to a summing point.
- These voltages or currents sum to the correct output value.
- Fast but suffers from poor accuracy because of the high precision required for each individual voltage or current.
- Usually limited to 8-bit resolution or less.



$$V_{out} = V_{ref}\frac{R_F}{R}(1 \cdot b_0 + 2 \cdot b_1 + 4 \cdot b_3 + 8 \cdot b_4)$$

Binary-weighted DAC

- R-2R Ladder
  - Cascaded structure of resistor values R and 2R.
  - Improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources).
  - Wide converters perform slowly due to large RC constants for each added R-2R link.



Delta-sigma DAC

- The digital delta-sigma