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# A Review of Solid-State Circuit Breakers

Rostan Rodrigues , Senior Member, IEEE, Yu Du, Member, IEEE, Antonello Antoniazzi, Member, IEEE, and Pietro Cairoli , Member, IEEE

**Abstract**—Although conventional electromechanical circuit breakers have a proven record as effective and reliable devices for circuit protection, emerging power distribution technologies and architectures, such as dc microgrids, require improved interruption performance characteristics (e.g., faster switching speed). The need for faster switching operation, in combination with the latest developments of advanced power semiconductor technologies, has spurred an increase in the research and development in the area of solid-state circuit breakers. This article provides a comprehensive review of various solid-state circuit breaker technologies that have been reported in the literature during recent years. First, we categorize solid-state circuit breakers based on key features and subsystems, including power semiconductor devices, main circuit topologies, voltage clamping methods, gate drivers, fault detection methods, and commutation methods for power semiconductor devices. Second, we discuss the various challenges associated with the design of solid-state circuit breakers from the perspective of generic applications and provide a comparison of several solid-state breaker technologies based on key metrics. Finally, we provide a useful framework and point of reference for future development of solid-state circuit breakers for many emerging power distribution applications.

**Index Terms**—Breaker topology, current sensing, fault protection, gate driver, power semiconductor devices, solid-state circuit breaker, trip electronics, voltage clamping.

## I. INTRODUCTION

SOLID-STATE circuit breakers (SSCBs) are power semiconductor-based protection apparatuses, with no moving parts for fault current interruption, renowned for their excellent operational and system level benefits. First and foremost, the response time of semiconductor devices is several orders of magnitude shorter than that of the electromechanical mechanisms typical of conventional circuit breakers. Second, unlike electromechanical circuit breakers, which rely on contact separation for current interruption, semiconductor devices can interrupt the flow of electrical charges without arcing. Moreover, thanks to the extremely quick current interruption capability, semiconductor-based circuit breakers can limit the let-through energy and arc

hazard exposure in the event of a fault by multiple orders of magnitude. Furthermore, because of the absence of moving parts, power semiconductor devices can execute a much higher number of operations. This translates into a greatly increased lifetime for circuit breakers. Finally, because semiconductor devices have no moving parts, they operate without making any noise. On top of the aforementioned benefits that are true for most power distribution applications, semiconductor-based circuit breakers offer several additional benefits that may be application-specific.

In recent years, many power system applications have emerged, such as marine power distribution systems [1], data centers [2], aviation power distribution [3], battery protection [4], photovoltaic systems [5], power converter protection [6], railway power systems [7], defense power systems [8], and electric vehicle (EV) charging infrastructure [9]. Most of these applications use low voltage (48–1500 V) and lower range of medium voltage (5–10-kV) dc power distribution for superior system-level benefits. Some of the most cited benefits are as follows: higher efficiency power generation on electric ship and marine platforms [10], reduction of power conversion stages and hence increased efficiency in data centers, renewable integration, and flexible EV charging infrastructure [11]. Despite the clear benefits in operation, emerging dc distribution systems require higher performance protection devices than state-of-the-art electromechanical circuit breakers. The existing electromechanical protection solutions have limited capability to protect dc systems due to the very high magnitude and rise rate ( $di/dt$ ) of fault currents and the inherently slow response time of mechanical systems. Moreover, because of the absence of natural zero current crossing in dc, mechanical circuit breakers require additional arc extinguishing mechanisms to drive the fault current to zero. To overcome these challenges, many researchers are looking into alternative solutions such as SSCBs.

As a point of comparison, electromechanical breakers have two tripping mechanisms, an electromagnetic action for short-circuit protection, and a bimetallic action for overload current protection. Short-circuit detection and interruption are based on electro-magnetic action that consists of contacts and a series-connected solenoid which involves several moving parts. Due to this mechanical nature, the electromechanical breakers have a short-circuit protection response time ranging from a few milliseconds to hundreds of milliseconds depending on their voltage, current rating, and tripping technology [12]. Even the most advanced current limiting electromechanical breakers start limiting the fault current in few milliseconds. Instead, SSCBs have much faster response time, thanks to the extremely fast

Manuscript received September 29, 2019; revised February 7, 2020 and April 21, 2020; accepted June 2, 2020. Date of publication June 17, 2020; date of current version September 4, 2020. Recommended for publication by Associate Editor J. Clare. (Corresponding author: Rostan Rodrigues.)

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Digital Object Identifier 10.1109/TPEL.2020.3003358

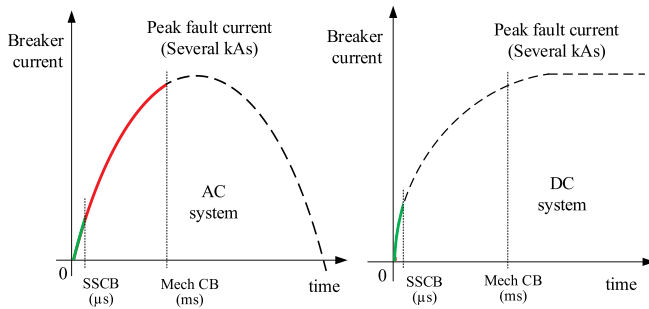


Fig. 1. Representative response time of SSCB vs. state-of-the-art electromechanical breaker during a short-circuit event.

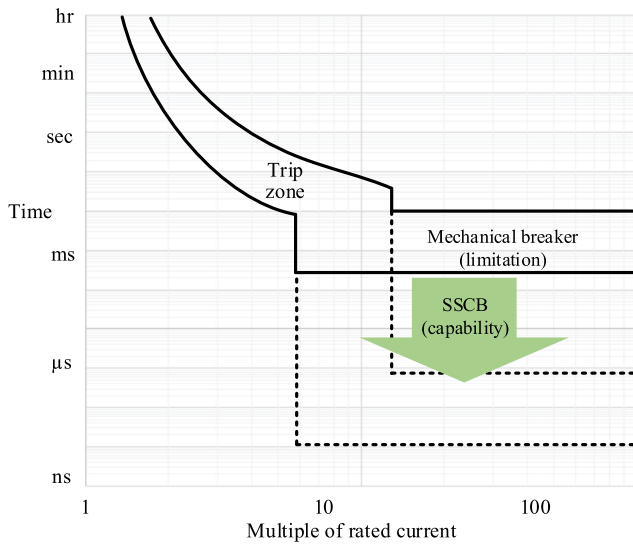


Fig. 2. Tripping capabilities of electromechanical breakers and SSCBs.

reaction speed of power semiconductor devices. Since the turn-OFF of semiconductor devices is controlled by a relatively low power electrical signal, initiation of the SSCB turn-OFF and current-limiting action can happen in microseconds or even in tens of nanoseconds. Fig. 1 aims to illustrate the pronounced difference in response time and current limitation capability of an SSCB versus state-of-the-art current-limiting electromechanical breakers.

The interruption time of an SSCB is several orders of magnitude shorter than that of an electromechanical counterpart. Interruption time is mainly limited by the speed and accuracy of the fault detection circuit and the turn-OFF speed of the power semiconductor devices, which is usually within tens of nanoseconds to tens of microseconds, depending on the semiconductor technology of choice. Fig. 2 depicts the capability of SSCBs in terms of instantaneous trip time on a typical current–time circuit breaker tripping curve.

During the past decade, an increase in research activity on SSCBs has been noted. Renewed interest in SSCB technologies mainly stems from researchers reaching manufacturing maturity of low loss, high efficiency, and fast switching wide bandgap (WBG) power semiconductors supporting a wide range of system applications [13]–[20].

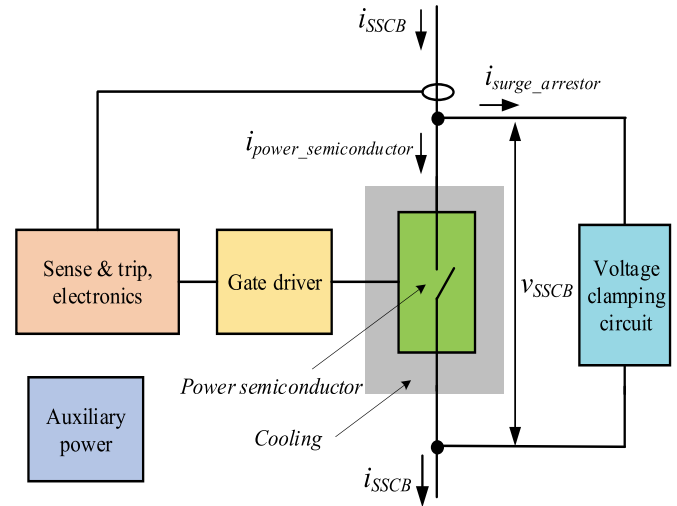


Fig. 3. Key components of SSCB.

Overall, many different types of SSCB technologies have been proposed in the literature and various aspects of SSCB subsystems and key components have been addressed. Nevertheless, the recent renewed interest in high performance protection in emerging applications has been the main motivation behind this work.

We provide an extensive review of SSCB technologies that apply to many of the aforementioned emerging applications, especially in the low-voltage (LV) and lower range of medium-voltage (MV) distribution systems. Section II explains the basic building blocks and operating principle of an SSCB. Section III analyzes several key components of SSCB designs such as power semiconductor devices, main power circuit topology, voltage clamping circuits, gate driver unit, fault sense, and trip electronics. Section IV presents a discussion which primarily focuses on addressing challenges in the design of SSCBs, and comparison of various technologies with some key metrics. Finally, we provide recommendations on potential improvements to the state-of-the-art technology with the intention to meet the application requirements for SSCBs.

## II. PRINCIPLES OF SOLID-STATE CIRCUIT BREAKERS

The key components of a generic SSCB are power semiconductor device, gate driver, cooling system, voltage clamping circuit, fault sensing system, sense and trip electronics, and auxiliary power supply. Fig. 3 shows a conceptual block diagram of a generic SSCB. The number of power semiconductors depends on the voltage and current rating of the application, power semiconductor technology, and topology of the breaker. It is worth mentioning that there are a few topologies that assume slightly different architecture than Fig. 3; for example, the Z-source SSCB [21], silicon carbide junction field effect transistor (SiC JFET)-based self-powered SSCB [22], and few others.

A representative waveform of the switching operation for a semiconductor-based circuit breaker is also shown in Fig. 4. During normal operation, the power semiconductor device stays

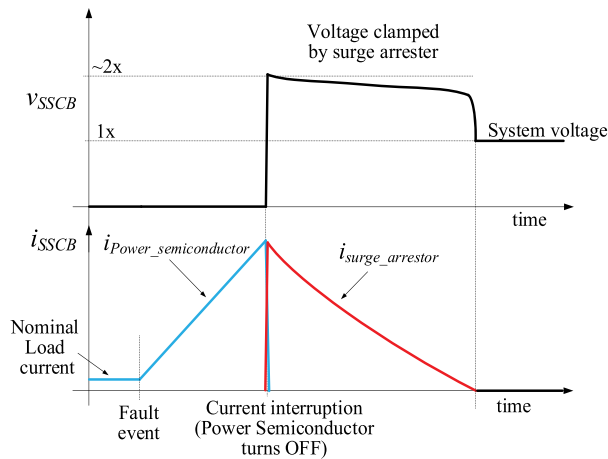


Fig. 4. Typical switching (turn-OFF) waveform of SSCB.

in ON-state. The gate driver unit applies appropriate bias voltage or current to the power semiconductor gate terminal to keep it in a stable and low-resistance ON-state.

The sensing and trip electronics continuously monitors the breaker current. If any fault or overload condition is detected, the sense and trip electronics turn OFF the power semiconductor through a gate driver or a commutation circuit. When the power semiconductor is turned OFF, the residual energy in the system inductance builds up voltage on the power semiconductor. When this voltage reaches a certain value, the voltage clamping circuit gets activated and the voltage is clamped to a safe level for the power semiconductor. Once the voltage clamping circuit absorbs all the residual system energy and the system current is driven to zero, both power semiconductor and voltage clamping circuit are in a high impedance state, and the voltage across the circuit breaker settles on the system voltage.

### III. REVIEW OF SOLID-STATE CIRCUIT BREAKER TECHNOLOGIES

This section provides a review of different elements of SSCBs in the literature, including the power semiconductor technologies, the power circuit topologies, voltage clamping circuits, gate drivers, fault sensing methods, and trip electronic solutions. Each major topic area will be presented with a categorization tree to summarize major trends as well as descriptive figures for key concepts.

#### A. Power Semiconductor Technologies for Solid-State Circuit Breakers

While there are many ways to design an SSCB, the technology of the power semiconductor devices drives the design based on what is available in the market or custom-designed for this particular application. In fact, different power semiconductor technologies are characterized by different properties and these properties will determine how a specific device can be used in combination with others. For example, some devices can conduct current in only one direction or are able to block voltage only in one direction. This will influence what topology

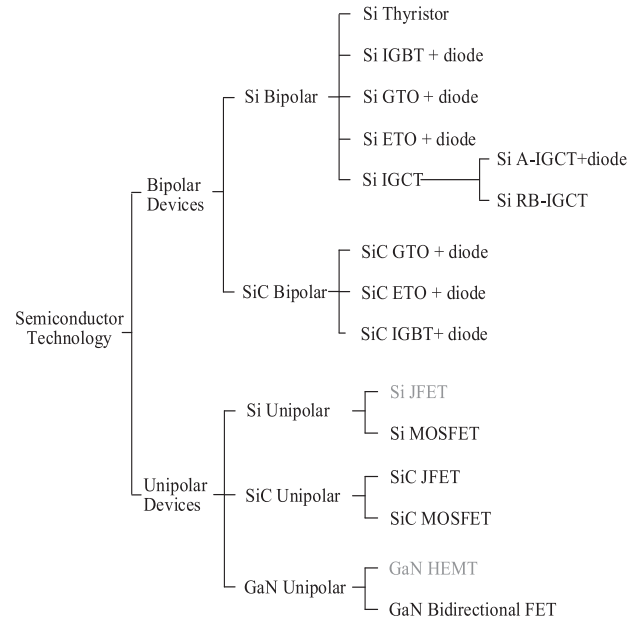


Fig. 5. Analysis tree of power semiconductor technology used for SSCBs.

and what other devices are needed to be used in combination with it. Another example is how well a technology performs with overcurrent, or currents much higher than the nominal conduction current. A further example is the passive state of a device, determining whether it is normally ON or normally OFF when no control energy or gate voltage is applied. In this section, we explore a cross section of the different semiconductor technologies analyzed by the literature for low-voltage and lower range of medium-voltage SSCB applications. Moreover, we investigate how the unique characteristics of the semiconductor technologies influence the way devices are used, their advantages, and their limitations.

We start by organizing power semiconductor devices with similar properties into categories. Fig. 5 summarizes the categorization of the power semiconductor technologies that are used in the power circuit of SSCBs or similar applications into an analysis tree.

As illustrated in Fig. 5, the first significant distinction among semiconductor technologies is between bipolar and unipolar devices. This distinction has very important implications in terms of both allowed direction of current flow, power loss profile, overcurrent capability, and dependency of the conduction characteristic on operating temperature.

The second significant distinction is between devices where the predominant material is silicon (Si) and devices where the predominant material is a WBG material [such as silicon carbide (SiC) and gallium nitride (GaN)]. Si devices exhibit a high maturity level and are commercially available with an extended range of voltage and current ratings. WBG semiconductors show superior material properties enabling power devices operation at higher temperatures, voltages, and switching speeds [15].

The third significant distinction can be identified in terms of device structure within each category. For example, within the



Si bipolar category, there are many fundamental device structures, such as silicon-controlled rectifier (SCR), insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), gate turn-OFF thyristor (GTO), and emitter turn-OFF thyristor (ETO). Within the identified fundamental device structures, there are a large number of different implementations and manufacturing processes that vary across manufacturers. For the sake of this review, we will only be discussing at the level of the fundamental structures summarized in Fig. 5.

Silicon bipolar devices, such as thyristors, IGBTs, GTOs, ETOs, and IGCTs can block voltages up to 6.5–8.5 kV and nominal currents up to 3–6 kA. Moreover, they have very good reliability proven by long-term operation in the field. Furthermore, they are characterized by very good overcurrent and short-circuit capability, especially for the thyristor family (i.e., SCRs, GTOs, ETOs, and IGCTs).

These are some of the reasons why Si bipolar devices are proposed by some researchers for SSCBs for medium-voltage distribution systems. Implementation of MV circuit breakers based on Si IGBT, gate-commutated thyristor (GCT) and GTO have been proposed for MVAC distribution systems up to 4.5 kV and 4 kA [23].

IGBTs with a blocking voltage of 4.5 kV are used in the application of medium voltage dc (MVdc) bus tie SSCBs for electric ships. An SSCB was demonstrated in experimental results with a system voltage up to 10 kVdc and 1000 A, with an 800 ns opening time [24]. IGBTs are also proposed as a valuable option for circuit breakers based on hybrid circuit topologies, as in the case of a Super-GTO (SGTO) + IGBT topology with the ON-state efficiency of thyristors and the maximum controllable current of IGBTs [25].

The reverse-blocking IGCT (RB-IGCT) is mainly accomplished by the integration of a blocking diode and IGCT on the same die [26]. A substantial reduction in power losses results from this integration. Anode engineering also contributes to the reduced ON-state losses. With an anode-to-cathode voltage drop of only 0.9 V at 1000 A (much lower than IGBT and standard IGCT, GTO, etc.), the RB-IGCT was proposed as a valuable device for SSCBs for dc distribution systems. A solid-state dc circuit breaker based on two 2.5 kV RB-IGCTs was demonstrated with experimental validation up to a voltage of 1 kV and a turn-OFF current of 7 kA [17], [27]. A two-pole solid-state dc circuit breaker with nominal current rating of 1.5 kA and nominal voltage rating of 1 kV was demonstrated in a compact solution with two-phase cooling based on pulsating heat pipes [28], [29]. IGCTs with blocking voltage up to 10 kV were also demonstrated for MV applications [17], [30].

An SSCB design based on the series connection of two 4.5 kV self-powered emitter turn-OFF thyristors and one 10-kV diode was demonstrated for a 4.16-kV system and tested up to 2.5 kV and a turn-OFF current of 3.3 kA [31].

Silicon unipolar devices find some applications in the low-voltage, low-power space. For example, silicon metal oxide semiconductor field effect transistors (Si MOSFETs) are proposed as a power semiconductor device in SSCBs for aircraft power distribution system applications. A topology based on a 650-V, 143-A MOSFETs is proposed for a 270-V, 200-A circuit breaker

with overload capability of 2000 A and 400 A<sup>2</sup>s [32]. An Si MOSFET is also proposed for 380 V, 15 A unidirectional circuit breaker applications [33]. Low-voltage silicon dual-MOSFETs (p-mos and n-mos) can also be used as trip activation switches for a higher voltage 1.2-kV SiC JFET cascode [34]. This new concept is based on a high-voltage SiC JFET in cascode with low-voltage dual-MOSFET switch. In this dual-MOSFET concept, during short-circuit, the voltage across series-connected Si MOSFETs and their gate driver circuit generate positive chain reaction to establish  $-15$  V at the gate of the SiC JFET, which then turns OFF. This concept was demonstrated and tested with up to 400 V and a turn-OFF current of 25 A.

As mentioned earlier, WBG semiconductors show superior material properties enabling power device operation at higher temperatures, voltages, switching speeds, as well as very low conduction losses per specific die area. For this reason, a substantial amount of research has applied these emerging power semiconductor devices to SSCBs and similar applications.

SiC unipolar devices, such as JFETs and MOSFETs, are the technologies that have reached maturity earlier than other WBG devices and they exhibit specific ON-resistance as low as 0.9 m $\Omega$  cm<sup>2</sup> for a blocking voltage of 650 V, 2.5 m $\Omega$  cm<sup>2</sup> for a blocking voltage of 1.2 kV, with projections of halving specific on-resistance with design and process improvements [16].

SiC normally ON JFETs have been discussed as a potentially good fit for SSCB applications based around two main reasons. First, SiC JFETs have been demonstrated with very low specific ON-resistance, which leads to high current density and low conduction losses per die area. Second, the normally ON nature of these devices requires no energy to maintain the device in ON state. Implementations of SSCBs for dc applications have been demonstrated for systems with up to 400 V, nominal currents up to 5 A, with a turn-OFF current up to 200 A, and with a current interruption time shorter than 0.8  $\mu$ s [22], [35], [36]. Special implementations of SiC JFETs also enable optically triggered fault detection, thanks to light emission at high current [36].

The SiC MOSFET has also been presented as a valuable power semiconductor device for SSCBs. Low conduction losses, high temperature operation, and the market availability from a large number of semiconductor manufacturers are among the main reasons for using SiC MOSFETs. Circuits for SSCBs have been evaluated for dc distribution systems for datacenters, aircraft distribution systems, and electric vehicle charging stations. Multiple different implementations of SiC MOSFET-based breakers have been demonstrated and tested for system voltages of 270, 380, and 850 V, turn-OFF currents up to 450 A, nominal current ratings up to 5, 15, and 100 A with air cooling and up to 375 A with liquid cooling [33], [37]–[39].

Among WBG unipolar devices, vertical GaN power semiconductor devices have the lowest theoretical ON-state specific resistance and they can deliver very low conduction losses. However, lateral GaN devices with higher resistance are more mature, e.g., GaN-on-Si devices. As one type of unique lateral GaN devices, monolithic bidirectional GaN field effect transistors (FETs) with blocking voltage of 650 V and a room temperature ON-resistance of 200 m $\Omega$  were evaluated as a power switch for

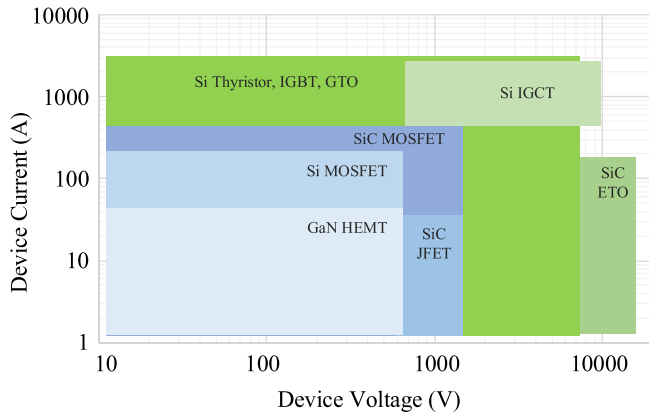


Fig. 6.  $I$ - $V$  map of major power semiconductor devices in SSCB literature.

SSCB applications. This dual-gate, bidirectional, normally ON, GaN-on-Si high electron mobility transistor (HEMT) device is able to conduct current in both directions and block both positive and negative voltage. For these reasons, it is interesting for bidirectional dc and ac circuit breaker applications [40]. An implementation of an SSCB based on bidirectional GaN devices has been developed and tested for a system voltage of 300 Vdc, and a turn-OFF current of 45 A.

Bipolar structures based on WBG semiconductor materials are mostly suited for high-voltage applications, because of the inherent high knee voltage penalty that causes high specific conduction losses in the low-voltage application category. A 4.5-kV MVdc SSCB based on 15-kV SiC ETO was evaluated for a unidirectional circuit breaker for MVdc power distribution. Three 15-kV SiC ETOs were connected in parallel and tested with a system voltage up to 4.5 kVdc, and a turn-OFF current up to 200 A [41].

Fig. 6 summarizes the  $I$ - $V$  map of power semiconductors used in SSCBs in the literature. Moreover, power semiconductor devices with higher voltage and current ratings than mentioned in the literature are also commercially available and can be used for the design of SSCBs depending on the design needs and requirements.

### B. Circuit Topology for Implementing SSCB

Circuit topologies supporting SSCBs are highly dependent on the characteristics of the power semiconductor switches and the application requirements. Power semiconductor characteristics of interest include power loss, cost, size, interruption speed, and other attributes. In this section, we discuss different topologies proposed in the SSCB literature. Fig. 7 summarizes major SSCB topologies reported in the literature.

The first category of SSCB topologies is based on the fully controlled power semiconductor switches, such as GTO, IGCT, ETO, bipolar junction transistor, IGBT, MOSFET, JFET, and HEMT. Typically, the breaker is required to conduct bidirectional current and block bipolar voltage as an expected functionality. The anti-parallel placement of reverse-blocking switches may provide the lowest power loss, since in this configuration, there is only one switch conducting the current. As an

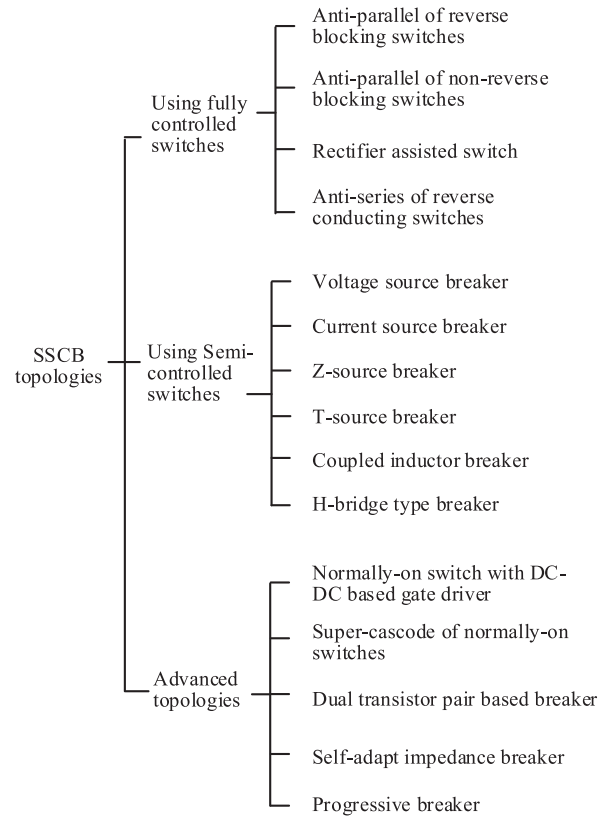


Fig. 7. SSCB topologies in literature organized in categorization tree.

example, RB-IGCTs can be used in anti-parallel configuration [27]. Moreover, the RB-IGCT switch is specially optimized to obtain minimal conduction loss, where the 2.5-kV device provides less than 1 V drop at nominal current. However, most reverse-blocking switches are designed for current source inverter applications. In these cases, the devices are optimized for high switching speed and their conduction loss is sacrificed. Alternatively, an anti-parallel topology can be made from two asymmetrical IGCTs or GTOs, but in this case, since the device cannot block negative voltage, a diode is needed in series with each IGCT. This choice would lead to higher conduction losses compared to a topology based on RB-IGCTs. An example of anti-parallel topology with GTO and IGCT is discussed in [23].

Supported by a full-bridge rectifier consisting of four diodes, it is possible to use only one fully controllable power semiconductor switch (e.g., IGBT). The switch could be symmetrical, asymmetrical, or a reverse-conducting type. The total cost of semiconductor switches is low with the penalty of high conduction loss as three devices are always in the current path [42].

In the lower current range, unipolar FETs have lower conduction loss than bipolar devices because they do not have the PN junction knee voltage in forward conduction. However, FET devices are typically reverse conducting because they have integral body diodes. Therefore, anti-series topology is suited for them. They are more efficient in a synchronous rectification mode where the reverse current is conducted through the channel instead of body diodes. This allows the power loss to be kept small in bidirectional conduction [36]. Bipolar devices could

also employ the anti-series topology. In many cases, a diode is co-packaged with IGBT or IGCT devices to make the switch reverse conducting as shown in [24] and [43].

The second category of the SSCB topologies is based on semi-controlled power semiconductor switches, more specifically thyristors or SCRs. These SCRs have low conduction loss, low cost, and are suitable for high current applications. An SCR is a reverse blocking switch, and anti-parallel configuration of SCRs can be used as a low-loss SSCB. However, one major challenge for thyristors is that their gate terminal cannot turn OFF the device. To build an SCR-based SSCB, an additional circuit is required to help the SCR interrupt the current. If a voltage source, such as a capacitor, is used to reverse-bias the SCR and interrupt the current from the SCR, these topologies can be considered as voltage source breakers [23], [44], [45]. In contrast, if a controlled current is injected to the SCR to create the zero-current crossing for current interruption, these topologies can be considered as current source circuit breakers [46], [47].

In addition to voltage and current source breakers, Z-source breakers are reported in [21]. This topology utilizes the Z-source LC circuit to automatically switch OFF the SCR in response to a short-circuit fault in the dc system. Z-source breakers feature fast turn-OFF and simple control, and the system power source does not experience the fault current. An improved Z-source breaker is introduced in [48]. To achieve similar objectives of automatic fast current interruption and simple control, a T-source breaker is reported in [49], [50], which consists of a two-winding transformer and a capacitor formed in a T-shape. The current gain can be adjusted by the transformer turns ratio. Similarly, coupled-inductor breakers [51] decrease the system power source current when fault current increases. They can also respond to faults rapidly and automatically. An H-bridge-type breaker is presented in [52]. Passive inductance and capacitance elements are configured in an H-bridge structure that enables the SCR (or other switch element) within the bridge to open and achieve dc circuit breaker action.

In the third category of SSCB topologies, more advanced power semiconductor devices or auxiliary circuits are employed. In recent years, normally ON type power semiconductors are available, such as GaN HEMT and SiC JFET. Their specific ON-resistance is low, and they are potentially an attractive solution for low current SSCBs. For example, a dc–dc converter-based fast turn-OFF gate driver is presented for SiC JFET switches in [22]. In normal operation, gate drive voltage is not required since the device is normally ON. When a fault occurs, the dc–dc converter will convert the increased ON-state voltage to a negatively biased gate voltage to turn the switch OFF. A super-cascode topology of normally ON switches can be used for higher voltage applications [53], [54]. It makes series connection of switches easy and only one gate driver is needed for the series of switches. An SSCB without the need of additional sensing circuitry by using dual transistor pair topology is presented in [34]. The topology consists of standard n-type and p-type Si-MOSFETs and the cascoded SiC-JFETs for increased blocking capability. A self-adapted fault current-limiting breaker is proposed in [55], in which the topology bypasses the dc reactor in normal operation and connects it to the fault circuit quickly to limit the fault

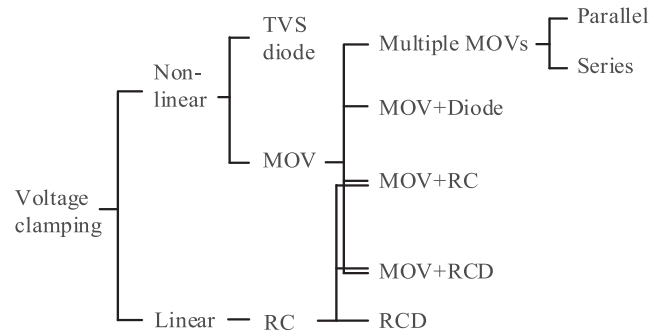


Fig. 8 Categorization of voltage clamping solutions in literature.

current. The topology potentially allows use of both SSCB and mechanical breakers in a multiterminal dc distribution network. A progressive switching scheme for SSCB is presented in [56], to suppress the fault surge while reducing component size and cost. It facilitates the use of smaller, less expensive components, such as low-voltage MOSFETs, to build a higher voltage SSCB.

The hybrid use of the fundamental SSCB topologies is also possible. For example, coupled-inductor-assisted thyristors are in parallel with IGCT switches to reduce the overall loss and size [23]. The combination of SGTO in parallel with IGBTs allows steady-state currents to flow through the low loss SGTOs, and IGBTs offer a much higher maximum turn-OFF current density [25].

### C. Voltage Clamping Circuit

SSCB is a series device and, in most applications, has to withstand unclamped inductive switching whenever the breaker turns OFF the current. Such turn-OFF event can easily create severe overvoltage on the power semiconductor device causing it to fail permanently. This is avoided by a snubber or voltage clamping circuit. The clamping can be realized by single or combination of multiple energy-absorbing components. The design of clamping circuit is usually driven by acceptable clamping voltage, energy-absorbing capability, peak fault current, leakage current at nominal voltage, etc. This section explores different voltage-clamping solutions presented in the literature, briefly discusses their operating principles, and presents a qualitative comparison among them.

Traditional snubber design methods for converters cannot be directly applied to SSCBs. Converter snubbers focus on loss minimization and quick voltage suppression; however, in SSCBs, the design focus is on overvoltage suppression with much larger energy absorption and high fault current withstanding. Many converters use nondissipative snubber so as to store energy during switching and then return back to main circuit at appropriate time, hence improving system efficiency. However, since the breaker switches very rarely, the turn-OFF loss reduction and efficiency improvement through nondissipative snubber is ineffective in SSCBs [57].

There are different types of voltage-clamping solutions as summarized in Fig. 8. At high level, the clamping solution can be either linear or nonlinear according to the type of voltage clamping component used. A simple linear solution, C type, is

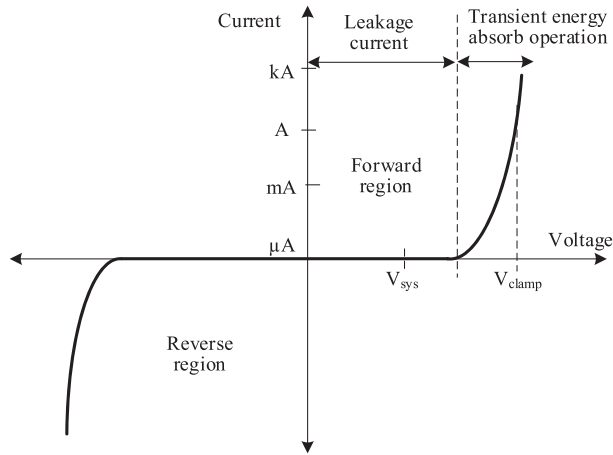


Fig. 9. Typical  $I$ - $V$  characteristics of MOV.

by using a snubber capacitor across the power semiconductor. The charging of snubber capacitor slows down the voltage rise rate as well as the peak voltage across the power device. In this process, the capacitor absorbs some of the energy stored in system inductance. However, the C-type snubber may oscillate with system inductance during the turn-OFF event as well as it can cause high discharge current through power semiconductor when the device is turned ON. To solve these issues, a resistor can be added in series with the capacitor to form resistor-capacitor (RC) snubber.

The resistor would damp the oscillations and limit the turn-ON discharge current into power semiconductor. However, during turn-OFF, the voltage drop across this resistor is also reflected on power semiconductor. This additional drop can increase the peak turn-OFF voltage requirement of the power semiconductor. These demerits make RC snubber solution quite challenging for SSCB applications [57].

An improved version of RC snubber is a resistor-capacitor-diode (RCD) snubber, where a diode is added in parallel to the resistor. This combination eliminates the additional drop of voltage across the resistor as well as significantly reduces the voltage oscillations during the turn-OFF [4], [8], [57], [58]. Design methodology and experimental performance comparison of three different circuit configurations of RCD snubber for low-voltage dc microgrid application is presented by [57].

Another type of clamping solution is by using metal oxide varistor (MOV). The MOVs are made from different materials such as silicon oxide (SiO), zinc oxide (ZnO), and silicon carbide. [59]. The fundamental operating principle of the MOV is the change of resistance as a function of applied voltage, as highlighted in Fig. 9. The change in resistance is negatively proportional to voltage, i.e., when zero voltage is applied, it has very high resistance, and when the applied voltage reaches clamping voltage, it has the lowest resistance.

The key characteristics of MOVs is that the change of resistance is a highly nonlinear function of the applied voltage. During the circuit breaker turn-OFF process, once the clamping voltage is reached, the voltage across the MOV remains fairly constant, with a progressive decrease in voltage as the energy

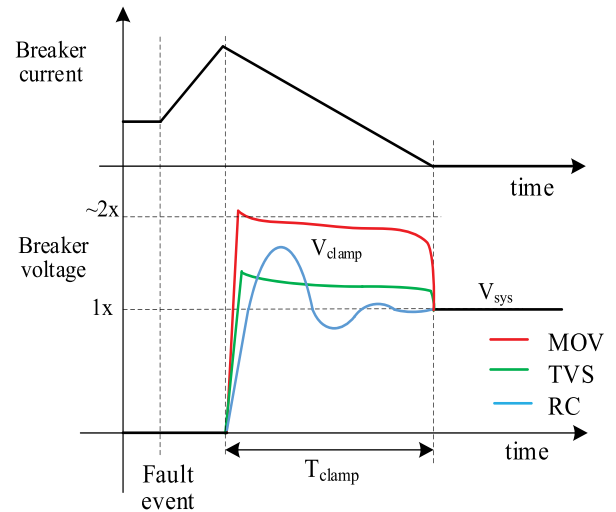


Fig. 10. Representative waveform of voltage clamping event for different clamping solutions mainly highlighting the difference in clamping voltage level and waveforms.

stored in system inductance is dissipated in the MOV. This magnetic energy stored in the circuit is greatly influenced by the system current as well as the system inductance. With appropriate selection of MOV, a safe clamping voltage can be assured for power semiconductors [2], [28], [34], [60]. For example, Martin *et al.* [2] discussed a four-step selection process, for choosing the MOV, that considers several key design parameters such as voltage margin, surge current capability, and leakage current. Some researchers have proposed a method to separate two functions of the MOV, voltage clamping and energy absorption, by using two different MOVs at strategic location in the circuit [59], [61]. However, the MOVs have limited lifetime due to its degradation during the process of energy absorption. This limits the number of turn-OFF operations that can be accomplished by using MOVs [38].

A more exotic solution for clamping the turn-OFF voltage is use of transient voltage suppression (TVS) diode. TVS diodes are a solid-state solution and operate under avalanche mode to clamp the voltage while absorbing the residual energy of system inductance [38]. The TVS diodes and MOVs both have fast response time; however, the TVS diodes are much more expensive than the MOVs for similar power and clamping voltage requirements. Some researchers are also exploring hybrid solutions that consist of combinations of MOV and RCD circuits, multiple MOVs in series, or parallel, etc. [9], [62], [63]. An optimized structure of parallel combination of MOV and RCD circuit is presented by [62] that reduces voltage stress of power semiconductor in uninterruptible power supply (UPS) application. Fig. 10 shows a representative waveform comparing performance of RC snubber, MOV, and TVS diode during a turn-OFF process of SSCB.

Table I shows a qualitative comparison of few different voltage clamping methods discussed in the literature.

The main requirement to drive the system current to zero is by establishing clamping voltage higher than system voltage. In case of MOVs and TVS diodes, increasing clamping voltage



TABLE I  
QUALITATIVE COMPARISON OF VOLTAGE CLAMPING SOLUTIONS

Clamping type	Pros	Cons
C	Simple; lower $V_{\text{clamp}}$ & $dv/dt$	Oscillations; High discharge current
RC	lower oscillations	Higher $V_{\text{clamp}}$ and $dv/dt$
RCD	Lower oscillations; Lower $V_{\text{clamp}}$ & $dv/dt$	More components
MOV	Better clamping than RCD	Limited lifetime; No $dv/dt$ control,
MOV+RCD	Advantages of MOV and RCD	More components and cost
Multiple MOVs	Scalability	Voltage and current balancing
TVS diode	Better clamping than MOV	Higher cost

will reduce the voltage clamping duration. On the one hand, the higher clamping voltage brings system current to zero faster but also puts more voltage stress on the power semiconductor. A higher clamping voltage could also generate undesired overvoltages across sensitive equipment upstream. On the other hand, clamping voltage closer to the system voltage would need longer time to bring the system current to zero and hence clamping device would need to dissipate more energy. Therefore, a trade-off between the fault current extinguishing time and the safe clamping voltage needs to be established for cost-effective and optimum performance of the SSCBs [38], [64]. Based on the selected ratings of voltage clamping devices in the literature, a generally accepted peak clamping voltage range can be given by [57]

$$1.5 \text{ p.u.} < V_{\text{clamp}} < 2.5 \text{ p.u.} \quad (1)$$

where, 1 p.u. is the nominal voltage of breaker.

#### D. Gate Driver

The main function of the gate driver is to control the conduction, blocking, and switching states of the power semiconductor. Depending on the type of the power semiconductor device, the gate driver could be voltage-driven (FETs and IGBTs) or current-driven (thyristors) configuration. Moreover, depending on the breaker topology, there could be single or multiple gate drivers. A more advanced gate driver can also have additional features such as fault sensing and active control of switching process. In this section, we explore various gate driver configurations presented in the literature.

The gate drivers for SSCBs have slightly different requirements and functionalities as compared to power converter gate drivers. In power converters, the gate driver needs auxiliary power which is proportional to the switching frequency. Instead, in SSCBs, turn-ON and turn-OFF are rare occurrences. Therefore, the auxiliary power demand is mainly defined by the ON-state and the OFF-state power requirements of the power semiconductor.

In WBG converter gate drivers, the high  $dv/dt$  during switching can induce common mode currents through auxiliary power supply and signal interconnections, and therefore, high  $dv/dt$  isolation is required in the interconnections. However, in SSCBs, the switching  $dv/dt$  could be reasonably lower, and therefore, the demand on  $dv/dt$  isolation can be low as well. Gate drivers for converter also need to consider other system-level constraints

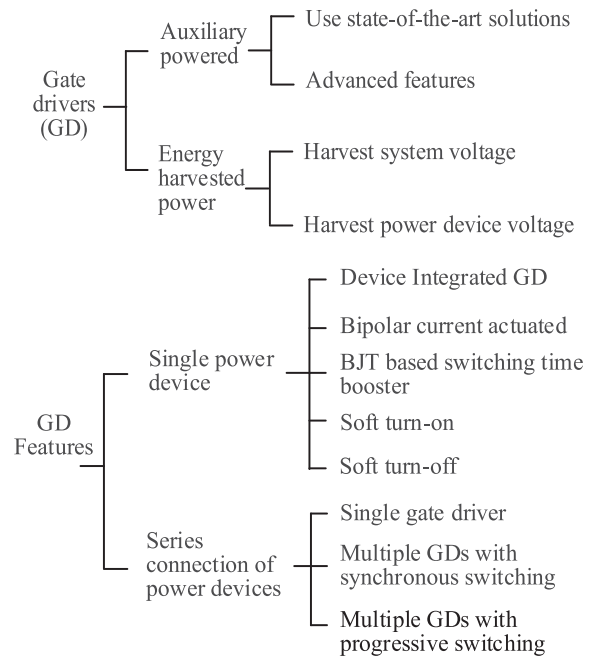


Fig. 11. Categorization of gate driver solutions in literature.

such as deadtime and cross-talk in phase legs. Such requirements do not exist in the breaker applications.

However, in SSCBs, the gate driver needs to supply continuous gate bias both for ON and OFF states of power semiconductor. This bias could be positive, negative, or zero voltage depending on the power semiconductor. This usually is not a big challenge since most power semiconductors used in SSCB literature are voltage-driven or pulse current-driven devices and require very low power to keep them ON or OFF.

Based on the available literature, the gate drivers for SSCBs can be categorized, as shown in Fig. 11. The majority of the gate drivers for low-voltage SSCBs are auxiliary powered by a power supply from ground level for their operation. Although the gate drivers using auxiliary power supply are already commercially available, many researchers are looking into implementing advanced features in the gate driver to enable high-performance SSCBs and combining multiple functionalities in one place. Some of these advanced features include monitoring power semiconductor parameters (voltage, current, temperature) to extract the fault current information, soft turn-ON [35], soft turn-OFF [65], onboard digital control for high-speed pulsewidth modulation-mode operation under certain operating conditions [39], etc.

For circuit breakers based on normally ON power semiconductors such as SiC JFETs, some researchers have explored fault energy-harvesting techniques to turn-OFF the power semiconductors during overcurrent faults [22], [66]. Such SSCBs, which do not need or use continuous auxiliary power supply for their normal operation, need some energy to keep the SiC JFET in OFF-state. Fig. 12 shows several different ways how gate drivers are designed for single as well as series-connected power semiconductors in the literature.

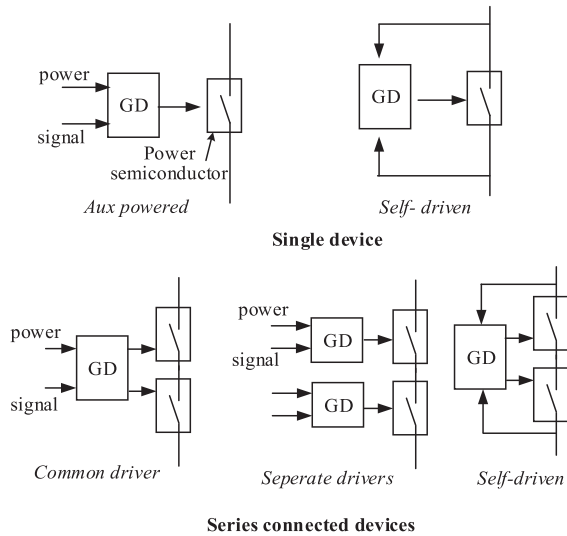


Fig. 12. Different types of gate drivers discussed in the SSCB literature (for single and series-connected power semiconductors).

The gate driver design also varies based on the power semiconductor. The available SSCB literature shows that researchers have attempted to design gate drivers for many different types of power semiconductors. The normally-OFF devices such as Si/SiC MOSFETs and IGBTs require positive voltage to keep them in the ON-state and zero or negative bias is needed to keep them in OFF-state. Typically, this positive voltage is about +20 V and negative voltage is between  $-5$  and  $-20$  V depending on the type of device [6], [62]. For JFET, on the other hand, being normally ON, a zero voltage is enough to keep it in ON-state, whereas negative voltage is needed to keep it OFF. The negative voltage is about  $-15$  to  $-20$  V [22], [66]. For some other high-power semiconductors such as thyristors, IGCT, ETO, and GTO, a custom gate driver is designed to achieve the best performance out of those devices, [27], [31], [67]; for example, the RB-IGCT is designed by integrating GCT power module and the gate driver PCB with very low inductance gate-cathode loop connection for high-performance switching operation [27].

Moreover, the literature shows that there is a trend to exploit the power semiconductor properties to detect the presence of fault current. In topologies with two SiC JFETs connected in anti-series, the reverse-conducting JFET develops a detectable voltage across gate-source terminals during overcurrent events [8]. Another example is a cascode topology that can be used to leverage the ON-state voltage drop across low-voltage n-type and p-type MOSFETs in the gate-source path of SiC JFET to turn the JFET OFF during overcurrent events [34].

In recent literature, Ren *et al.* [63] proposed a single gate driver configuration for series connection of two SiC MOSFETs, whereas Mackey *et al.* [56] proposed multiple gate drivers for series connection of SiC MOSFETs with progressive switching during turn-OFF.

### E. Fault Sense and Trip Electronic Circuit

The primary function of a breaker is to stop or limit the flow of current during overload or fault current event. This is usually

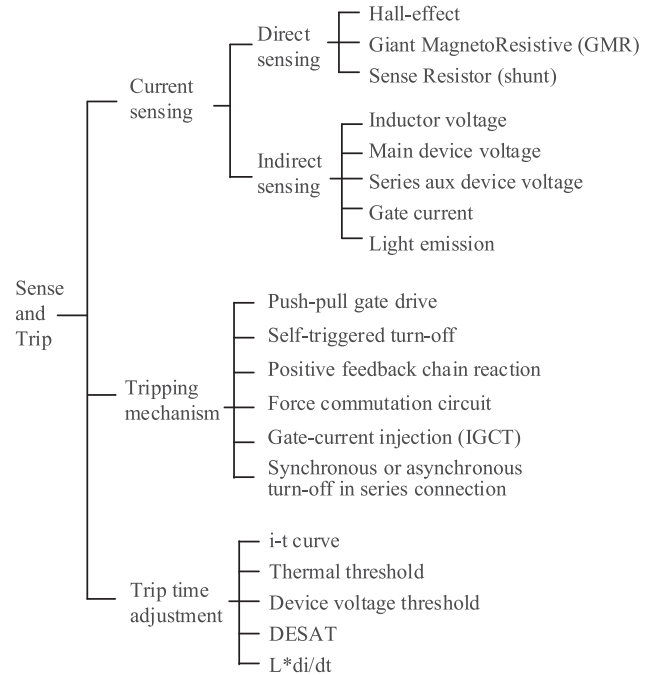


Fig. 13. Categorization of fault sense and trip electronic solutions in SSCB literature.

done by sensing fault current in a direct or indirect method. The main requirements of fault current sensors are high bandwidth for fast response, low losses, and compact and suitable interface with control circuitry. This section analyzes different methods of current sensing and tripping used in the literature as well as methods for adjusting the tripping characteristics of the breaker.

Depending on application, the system inductance could vary within wide range of values (few  $\mu\text{H}$  to several mH). This means the rate of change of current during short-circuit fault would also vary in a wide range. Therefore, it is important to have an adequate sensor design that performs well within wide range of  $di/dt$  and current values. Apart from high bandwidth and fast response times, the sensor should also have lower losses than main power semiconductor to keep the breaker efficiency as high as possible; this is particularly important in the case of self-supplied SSCBs where the power is harvested. Fig. 13 shows different types of current sensing and tripping mechanism explored by researchers in the literature.

1) *Current Sensing:* The existence of fault can be detected directly or indirectly by sensing the load current. The direct sensing of current means using a dedicated current sensor to continuously measure and monitor the current. The current measurement can be done by different types of current sensors such as Hall-effect current sensor [5], [19], giant magneto-resistive (GMR) current sensor [35], and current sense resistor [59], [69]. On the other hand, the indirect current sensing uses system parameters that are dependent on instantaneous or root mean square (RMS) value of current and rate of change of current. For example, the voltage across main power semiconductor device can be used to sense the fault [54], [66].

During normal load operation, the current flowing through a normally ON power device (SiC JFET or GaN MOSFET) induces

a small voltage across its drain–source terminals. However, during fault current condition, a large current flows through the power device inducing sufficient voltage across it, which then triggers fault sensing and tripping circuit. A similar approach is proposed by [34]; however, instead of sensing voltage on main power semiconductor (SiC JFET), the method senses voltages across two low-voltage Si MOSFETs in series with main power semiconductor.

A fault detection method by sensing voltage across an inductor is proposed by [70]. The high  $di/dt$  during fault causes a certain voltage to be established on the inductor. This voltage is used to activate protection circuit. Urciuoli *et al.* [8] use gate current of reverse-conducting SiC JFET during high current conditions as an indication of fault event, whereas Victor *et al.* [36] use the light emitted by SiC JFET die during high current conditions. The intensity of light is proportional to magnitude of current and therefore can be monitored for detecting the fault.

2) *Tripping Mechanism*: The tripping mechanism in SSCBs varies with type of power semiconductor and main power circuit topology used. For devices like MOSFETs, JFETs, and IGBTs, a traditional push–pull type of gate driver can do the job provided that the auxiliary power supply is available. For some energy-harvested SSCBs, the tripping mechanism can be slightly different.

Some researchers proposed desaturation (DESAT) sensing and protection for IGBTs [6], [62]. This can be accomplished by commercially available gate driver chips with DESAT feature. For power devices like thyristors (SCR), the turn-OFF is usually done by force commutation circuits [44], [45], [71]. The commutation circuit consists of additional passive and active components. The commutation circuit may or may not need to have prestored energy depending on the topology.

For advanced thyristors (IGCT, GTO, etc.), the turn-OFF is done by diverting the device's internal channel current through gate driver and essentially turning it OFF. Since these devices are designed for high-power applications, their turn-OFF currents can be very high (several kAs), which means their gate drivers should also be able to carry such a high current for short duration during turn-OFF transition [25], [27], [31].

3) *Tripping Time Adjustment*: The tripping characteristics are used as a timing reference during fault protection. Depending on the magnitude of fault current, the trip time can vary as defined by the  $i^2t$  requirements for the application. The tripping characteristics for SSCBs are not yet fully developed in industry, and therefore, many researchers and designers follow traditional tripping characteristics designed for electromechanical breakers. Also, it is important to note that, since the semiconductor devices have limited overloading capability, the tripping curve also serves for SSCB's self-protection.

A typical tripping characteristic is shown in the Fig. 2. When the current increases slightly above the nominal value, the system can handle the excess heating for longer duration of time (minutes to hours), whereas current many times larger than its nominal value can cause large heating in very short duration (milliseconds to seconds). In order to accomplish the variable tripping time as a function of fault current, different methods have been implemented by researchers. Some commonly used methods are discussed in this section.

A relatively precise method to implement trip curve is to have dedicated current sensors and store the fault current and time information in the digital processing units such as DSP, microcontroller, and field programmable gate array (FPGA). The intelligent unit can have lookup table of trip-curve or can have mathematical model to keep track of fault energy. The intelligent unit can then make a tripping decision when appropriate amount of  $i^2t$  has occurred [3], [72]. Such intelligence also allows tuning of trip-curve depending on the application requirements. Some lower precision methods are also explored by the researchers. These methods may allow tuning of the tripping curve during the design phase or maintenance cycle of the breaker but not tunable during runtime. In case of [70], by varying the value of voltage sense inductor, the tripping time can be adjusted. A similar approach can be made for [65], [73], where, by changing a timing resistor or capacitor, the trip time can be adjusted.

#### IV. DISCUSSION

This section discusses SSCB design trends in the literature, and highlights several challenges associated with the breaker design and important considerations from applications perspective.

The literature has addressed SSCBs for a wide range of nominal voltage (few hundred volts to tens of kV) and nominal current ratings (few amps to few kAs). Table II shows a comparison of few selected SSCB technologies for various system metrics that were experimentally validated. In this table,  $V_n$  and  $I_n$  are nominal voltage and current, respectively, and  $I_{\text{interrupt}}$  is the maximum current that can be interrupted by the SSCBs.

For applications in LV and lower range of MV, the use of a single power semiconductor is normally enough to block the nominal voltage and system overvoltage. This is mainly due to the availability of many different types of devices with voltage rating in this voltage space. SSCBs with higher nominal currents can be obtained by parallel connection of discrete devices or by using power modules with a large number of dies in parallel. SSCBs in the high MV space are not part of this study and they require different circuit topologies that most likely involve series connection of power semiconductor devices since devices above 10–15 kV are not commonly available or have not reached manufacturing maturity.

As part of its operation, a circuit breaker needs to support a wide range of currents, usually up to 5–10 $\times$  of the nominal current for a time duration in the order of milliseconds to seconds. This type of short-duration high current, also known as overcurrent or surge current, can be quite challenging for an SSCB. During these surge events, the conduction losses, and hence the temperature of the semiconductor die, increase very rapidly. This can lead to the overheating, damage, or early aging of the semiconductor devices. Moreover, emerging low ON-resistance WBG devices have smaller dies and higher current density compared to silicon counterparts for the same ON-state resistance or forward voltage drop. A small die area has lower thermal mass and may result in a reduced surge current capability. In recent years, some research has been carried out to understand the challenges associated with surge currents in power semiconductors [77]–[82]. From here, we can

TABLE II  
COMPARISON OF A FEW SELECTED SSCB TECHNOLOGIES IN LITERATURE WITH EXPERIMENTAL VALIDATIONS

Power device technology	$V_n$ (V)	$I_n$ (A)	$I_{\text{interrupt}}$ (A)	Power Topology	Voltage clamping method	Fault sensing	Intended Application
Si IGBT [24]	10k	800	1k	Series devices	N/A	Current sensor	Shipboard MVDC
SiC ETO [41]	4.5k	200	200	Parallel device	MOV	Current sensor	MVDC
Si RB-IGCT [28]	1k	1.5k	6.5k	Anti-parallel devices	MOV	Sense resistor	LVDC
Si IGBT [74]	1k	1k	2k	Anti-series devices	N/A	di/dt reactor	Marine LVDC
SiC MOSFET [37]	850	100	240	Single device	Avalanche Breakdown Diode	Device voltage	Mobile platforms
Si IGBT [75]	800	N/A	10k	Parallel devices	N/A	Current sensor	Shipboard MVDC
SiC JFET [8]	600	60	234	Anti-series devices	RCD	Gate current	Bidirectional LVDC
SiC SIT [76]	400	12.5	N/A	Single device	Not used	Sense resistor	Data center LVDC
SiC JFET [35]	400	5	80	Anti-series devices	MOV	GMR sensor	LVAC
GaN MOSFET [40]	300	N/A	45	Monolithic bidirectional switch	MOV	Device voltage	LVDC
Si SCR [44]	220	13.1	50	Force commutation, anti-parallel devices	MOV+RCD	Current sensor	AC grid
Si CoolMOS [72]	220	1	10	Single device	Not used	Current sensor	DC home distribution
Si MOSFET [70]	190	N/A	14	Single device	Free-wheeling diode	Inductor voltage	DC microgrid

conclude that more innovation in packaging and cooling system integration is needed to improve the surge current capability of SSCBs to meet the robustness needs in many traditional as well as emerging applications [83].

The device voltage utilization factor in the SSCB applications is another area that has room for improvement. In most cases, the ratio between the power semiconductor blocking voltage rating and the system nominal voltage rating is 1.5 to 2.5. This overrating in voltage of the power semiconductor devices is needed to accommodate the overvoltages that are required to effectively drive the current to zero during a current interruption and inductive overvoltages generated at turn-OFF. This voltage overrating directly reflects in an increased cost of the semiconductor devices and thus the SSCB. Therefore, a voltage clamping solution that provides low leakage at nominal voltage and limits peak voltage close to nominal voltage would help improve the device utilization and help to reduce the cost of the circuit breaker. However, this will come with the drawback of longer times for reducing the current to zero [28], [33].

Apart from delivering best performance at component level, SSCBs need to be able to coordinate at system level. This is becoming more of a need than a feature, especially in the increasing complexity of power distribution network in many applications [84]–[88]. One of the key challenges at system level is the coordination with other breakers to correctly isolate fault-affected area as quickly as possible while maintaining high power quality and availability to other system components. Such coordination can become quite a challenge when the system

has different types of protection technologies with different response speeds. This would be the case where a system has a mix of electromechanical breakers, fuses, hybrid, and solid-state breakers.

Another challenge is the higher leakage current from the OFF-state power semiconductors and the high impedance state of the voltage clamping circuit when the circuit breaker is in open position. The leakage current of solid-state breakers can be orders of magnitude higher than breakers that rely on contact separation. This is true particularly during overvoltages and at high operational temperature. In this condition, high leakage current could lead to device overheating. The leakage current can be reduced by choosing semiconductor devices with low leakage current or by external means, such as by use of a galvanic isolation switch in series with the semiconductor devices [56], [74]. Another important necessity for a galvanic isolation switch may arise when the OFF-state voltage of the circuit breaker exceeds the semiconductor device breakdown voltage due to system-wide surge voltage transients. This is mainly because power semiconductor devices are less robust against intense overvoltage transients and can fail abruptly during such overvoltage events. On the other hand, the addition of galvanic switch can increase complexity and form factor of SSCBs.

## V. CONCLUSION

This article presents a review of SSCB technologies that can address the growing demand for high-performance protection



devices in many emerging power systems applications in the LV and lower range of MV.

Various power semiconductor devices and circuit topologies have been proposed in the literature to support different types of SSCBs at different nominal voltages and nominal current ratings. Some deliver cost-effective solutions (e.g., Si IGBT and IGCT), and others show a lot of potential in terms of efficiency and power density (e.g., WBG semiconductors). It is also important to notice that power devices which would be excellent fit for converter applications may not necessarily be suitable for SSCBs. This is mainly due to different types of requirements for circuit breaker applications, such as low conduction loss, continuous gate bias, and high thermal transient capability.

Surge current withstanding is also one of the main challenges for SSCBs. Although the power semiconductor die is a main bottleneck in surge conditions, more innovation in packaging and cooling system integration can help to achieve the full potential of the power semiconductor devices in SSCBs.

Several different voltage-clamping solutions have also been validated by researchers. Some of these voltage-clamping circuits enable high device utilization (e.g., TVS diode), and others deliver fast current interruption in a cost-effective way (e.g., MOV).

A few different types of gate driving strategies have been discussed in the literature. Some researchers have also capitalized on specific properties of power semiconductors, such as device voltage, gate loop currents, and light emitted by power semiconductor dies to detect fault currents and turn-OFF the circuit breaker. We can conclude that it has been proven that the SSCBs can interrupt the short-circuit fault within few microseconds or less, limit the let-through fault energy, and reduce the arc flash hazard for maintenance personnel. However, more work is needed to address some remaining challenges, such as minimizing ON-state losses, maximizing power device voltage utilization, improving surge current capability, decreasing OFF-state leakage current, and increasing power density.

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