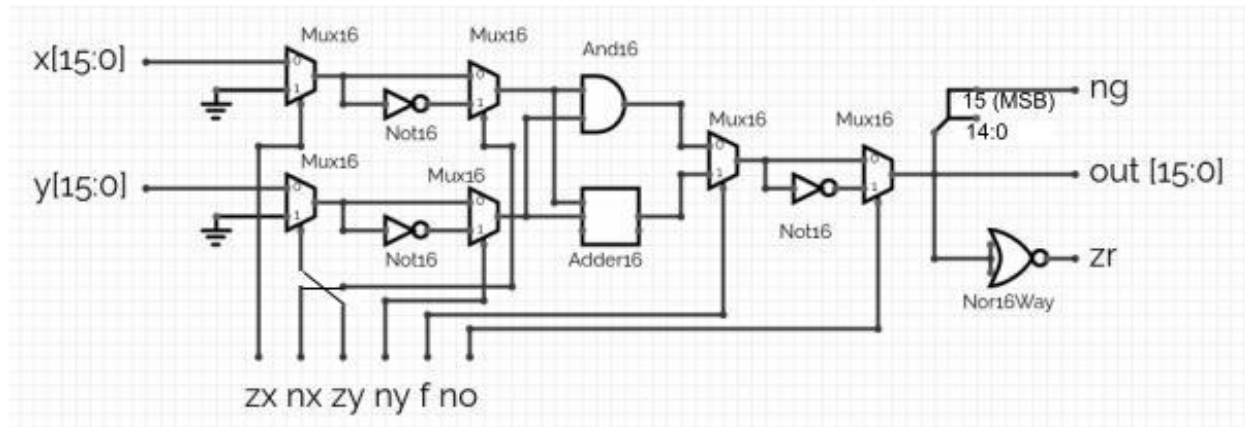


Entrega de arquivos em verilog

• Unidade Lógica Aritmética (ALU)

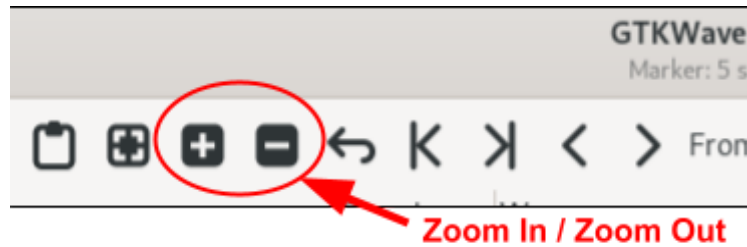


zx	nx	zy	ny	f	no	out
if zx then x=0	if nx then x=!x	if zy then y=0	if ny then y=!y	if f then out=x+y else out=x&y	if no then out=!out	out(x,y)=
1	0	1	0	1	0	0
1	1	1	1	1	1	1
1	1	1	0	1	0	-1
0	0	1	1	0	0	x
1	1	0	0	0	0	y
0	0	1	1	0	1	!x
1	1	0	0	0	1	!y
0	0	1	1	1	1	-x
1	1	0	0	1	1	-y
0	1	1	1	1	1	x+1
1	1	0	1	1	1	y+1
0	0	1	1	1	0	x-1
1	1	0	0	1	0	y-1
0	0	0	0	1	0	x+y
0	1	0	0	1	1	x-y
0	0	0	1	1	1	y-x
0	0	0	0	0	0	x&y
0	1	0	1	0	1	x y

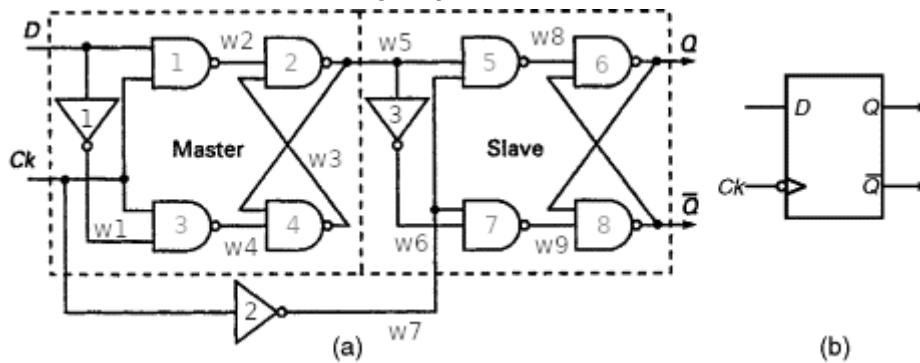
Lógica Sequencial

Dica:

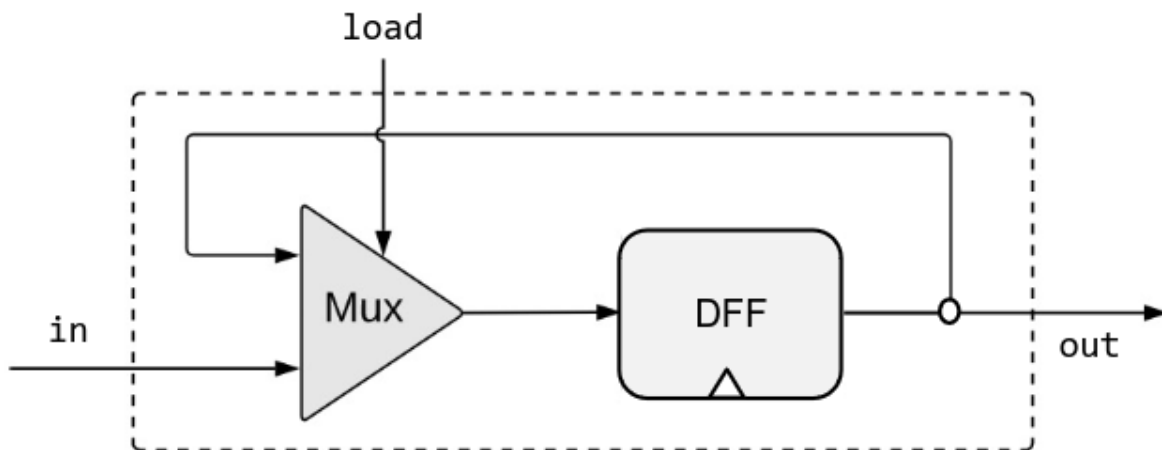
Se precisar aproximar ou afastar as formas de onda no gtkwave, basta utilizar os botões de zoom in/out



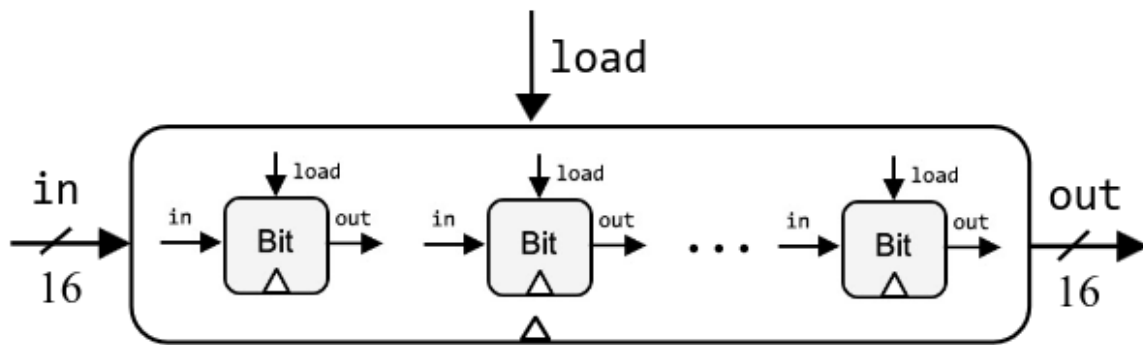
- **DLatch**, flip-flop tipo D em configuração de sensibilidade à descida de clock



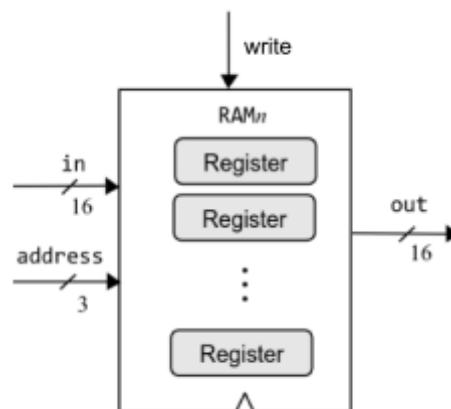
- **Bit**, o registrador de 1-Bit



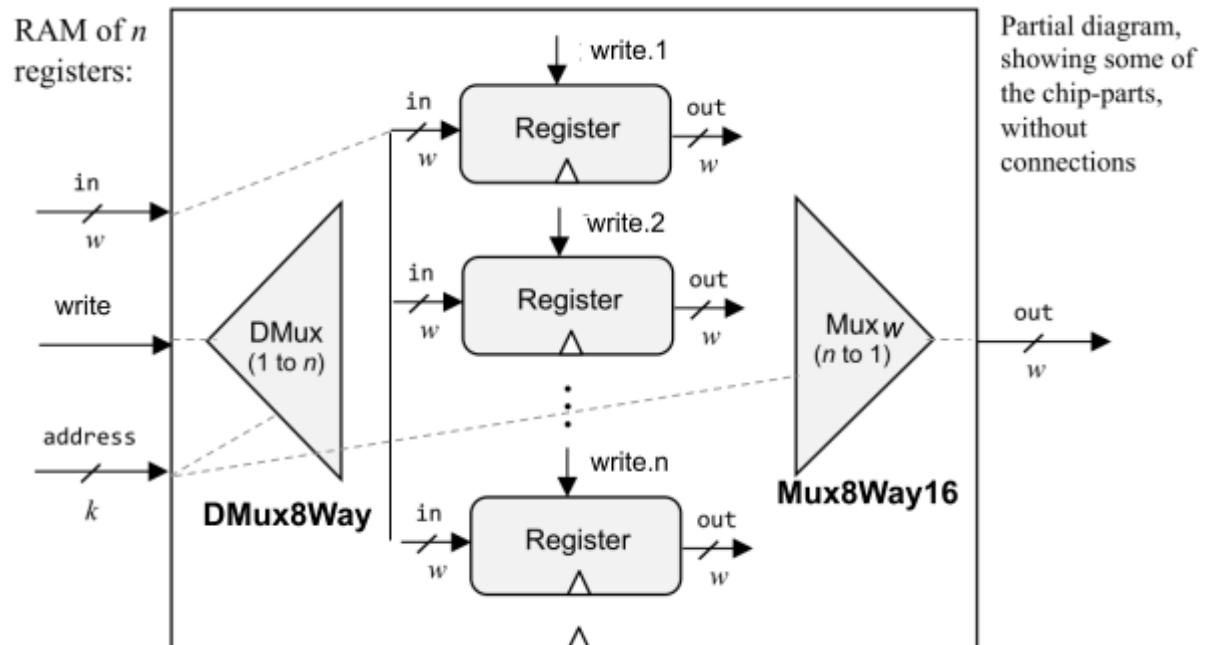
- **Register16**, o registrador de 16-Bits



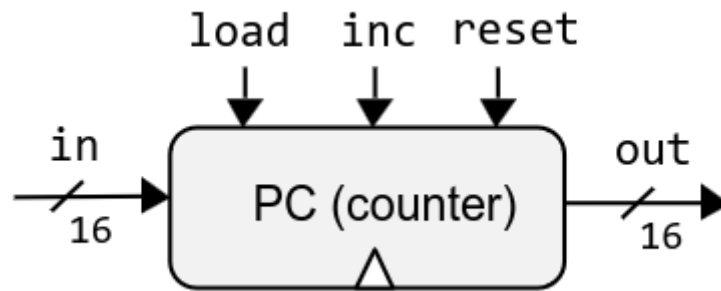
- **RAM8**, a memória de 8 registradores



Dica:



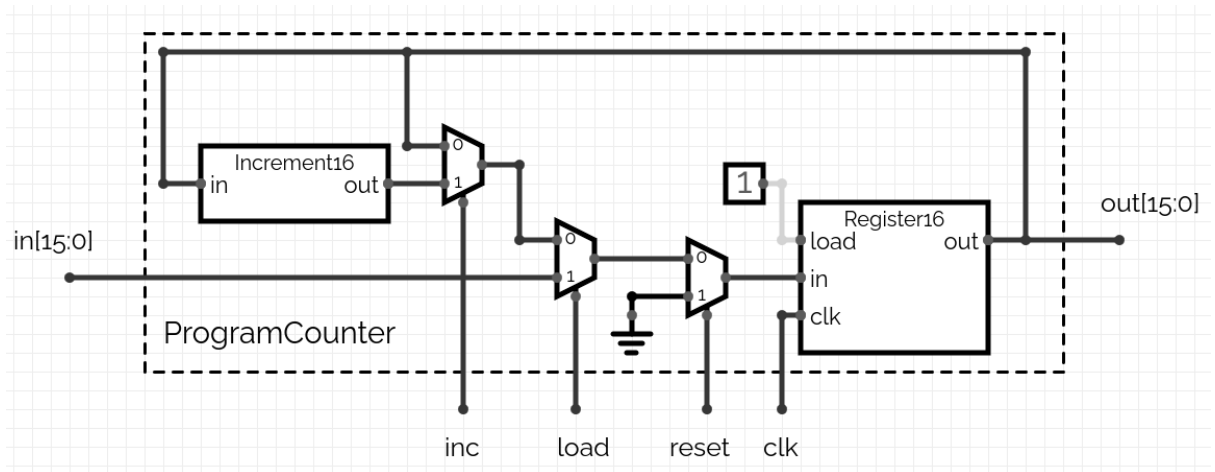
- **ProgramCounter**, o contador de programa



```

if      reset(t - 1) out(t) = 0           // resetting
else if load(t - 1)  out(t) = in(t - 1)  // setting
else if inc(t - 1)   out(t) = out(t - 1) + 1 // incrementing
else                out(t) = out(t - 1)  // maintaining

```



**Para a ordem de entradas e saídas nas declarações de seus módulos,
favor consultar os respectivos arquivos de *testbench***