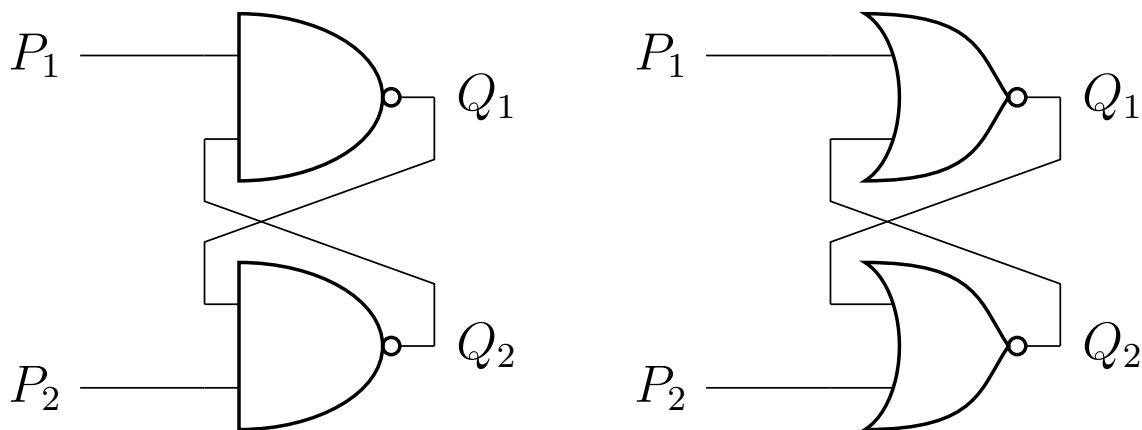


GATE QUESTION ECE 2009 Q38

Question

Q38) Refer to the NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made $(0,1)$ and then, after a few seconds, made $(1,1)$. The corresponding stable outputs (Q_1, Q_2) are:



Options:

- (A) NAND: first $(0,1)$ then $(0,1)$, NOR: first $(1,0)$ then $(0,0)$
- (B) NAND: first $(1,0)$ then $(1,0)$, NOR: first $(1,0)$ then $(1,0)$
- (C) NAND: first $(1,0)$ then $(1,0)$, NOR: first $(1,0)$ then $(0,0)$
- (D) NAND: first $(1,0)$ then $(1,1)$, NOR: first $(0,1)$ then $(0,1)$

Solution

1. NAND Latch Analysis

The NAND latch consists of two cross-coupled NAND gates, with outputs given by:

$$Q_1 = \overline{P_1 \cdot Q_2}, \quad Q_2 = \overline{P_2 \cdot Q_1}$$

Step 1: Inputs $(0,1)$

$$Q_1 = \overline{0 \cdot Q_2} = \overline{0} = 1$$

$$Q_2 = \overline{1 \cdot Q_1} = \overline{1} = 0$$

Output: $(Q_1, Q_2) = (1, 0)$

Step 2: Inputs $(1,1)$

$$Q_1 = \overline{1 \cdot Q_2} = \overline{1 \cdot 0} = \overline{0} = 1$$

$$Q_2 = \overline{1 \cdot Q_1} = \overline{1 \cdot 1} = \overline{1} = 0$$

Output: $(Q_1, Q_2) = (1, 0)$

P_1	P_2	NAND Output (Q)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1: NAND Gate Truth Table

2. NOR Latch Analysis

The NOR latch consists of two cross-coupled NOR gates, with outputs given by:

$$Q_1 = \overline{P_1 + Q_2}, \quad Q_2 = \overline{P_2 + Q_1}$$

Step 1: Inputs (0,1)

$$Q_1 = \overline{0 + Q_2} = \overline{0} = 1$$

$$Q_2 = \overline{1 + Q_1} = \overline{1} = 0$$

Output: $(Q_1, Q_2) = (1, 0)$

Step 2: Inputs (1,1)

$$Q_1 = \overline{1 + Q_2} = \overline{1} = 0$$

$$Q_2 = \overline{1 + Q_1} = \overline{1} = 0$$

Output: $(Q_1, Q_2) = (0, 0)$

P_1	P_2	NOR Output (Q)
0	0	1
0	1	0
1	0	0
1	1	0

Table 2: NOR Gate Truth Table

Final Answer

- **NAND latch:** First (1,0), then (1,0) - **NOR latch:** First (1,0), then (0,0)

Correct Option: (C)